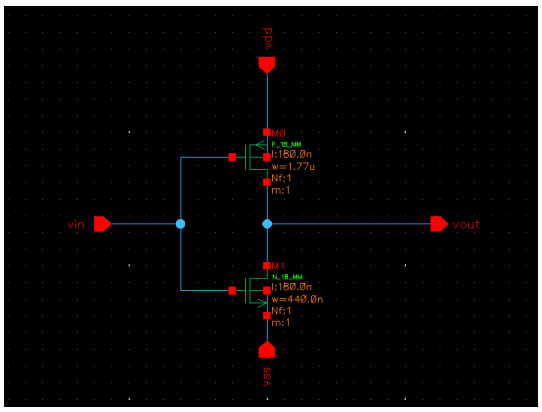
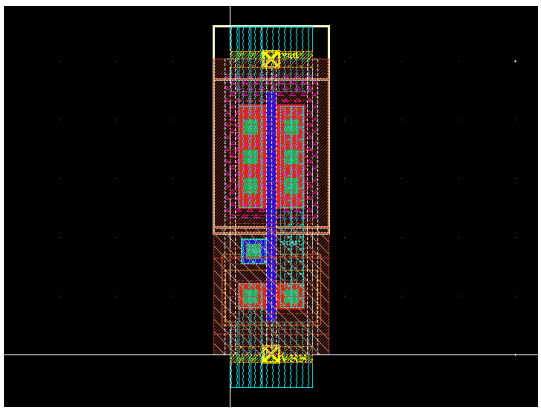
Standard Cell Layout Design Portfolio

Designed & Verified: INV, NAND, XOR, MUX, D-Latch

INV Standard Cell

The CMOS Inverter is the simplest and most fundamental logic cell, performing signal inversion.

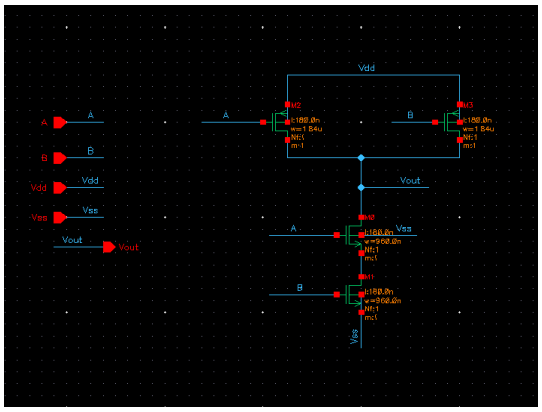


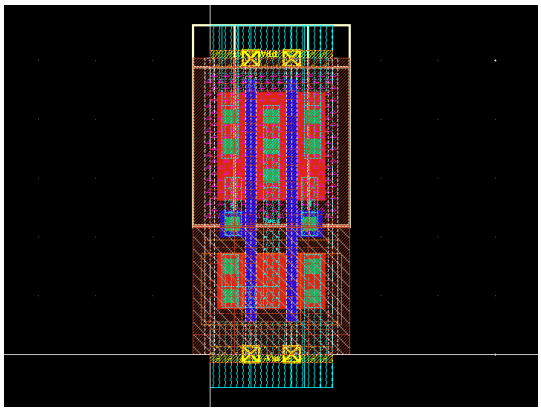


A	Y
0	1
1	0

NAND Standard Cell

A 2-input NAND gate is a universal logic gate, forming the foundation for all combinational logic circuits.



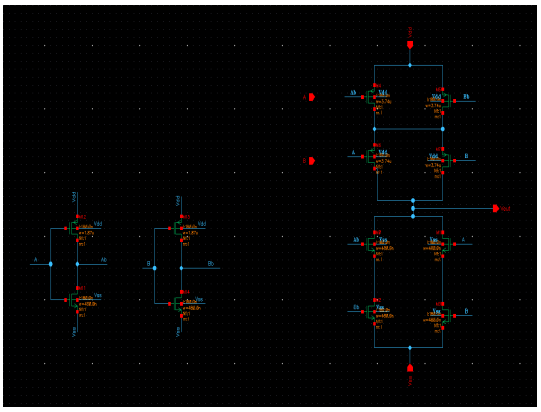


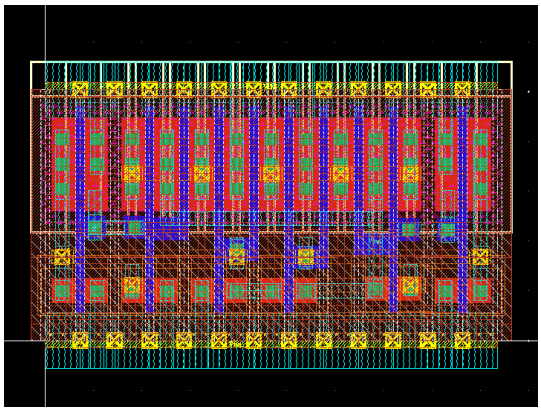
A	B	Y
0	0	1
0	1	1

1	0	1
1	1	0

XOR Standard Cell

The XOR gate outputs high only when the inputs differ, widely used in arithmetic and parity logic.

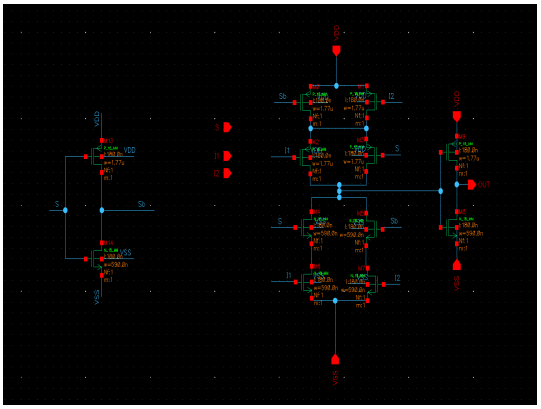


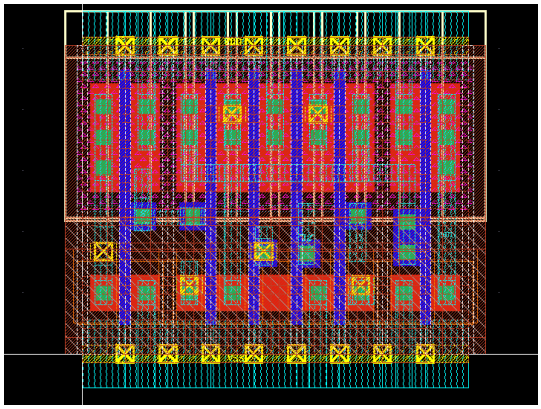


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

MUX Standard Cell

The 2:1 Multiplexer selects one of two input signals based on the select signal, key in datapath control.

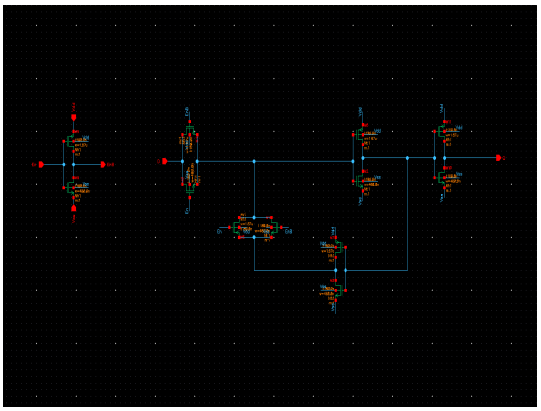


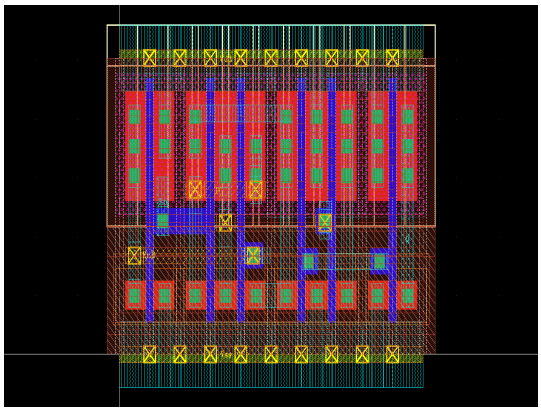


S	D0	D1	Y
0	D0	D1	D0
1	D0	D1	D1

D-Latch Standard Cell

A D-Latch is a level-sensitive storage element, fundamental to sequential logic and flip-flop design.





Enable	D	Q(next)
0	X	Q(prev)
1	0	0
1	1	1