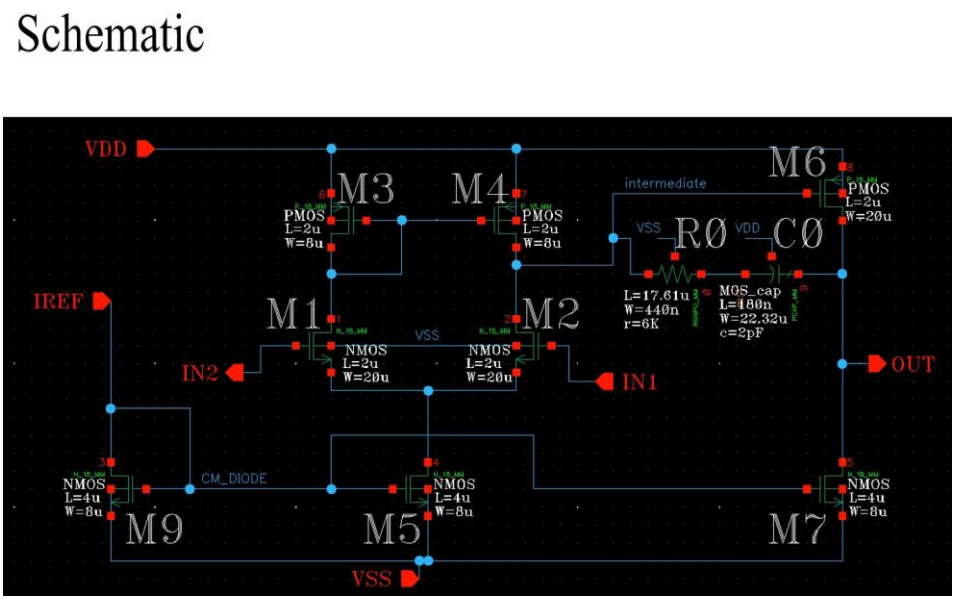
Two-Stage CMOS Operational Amplifier Design Portfolio

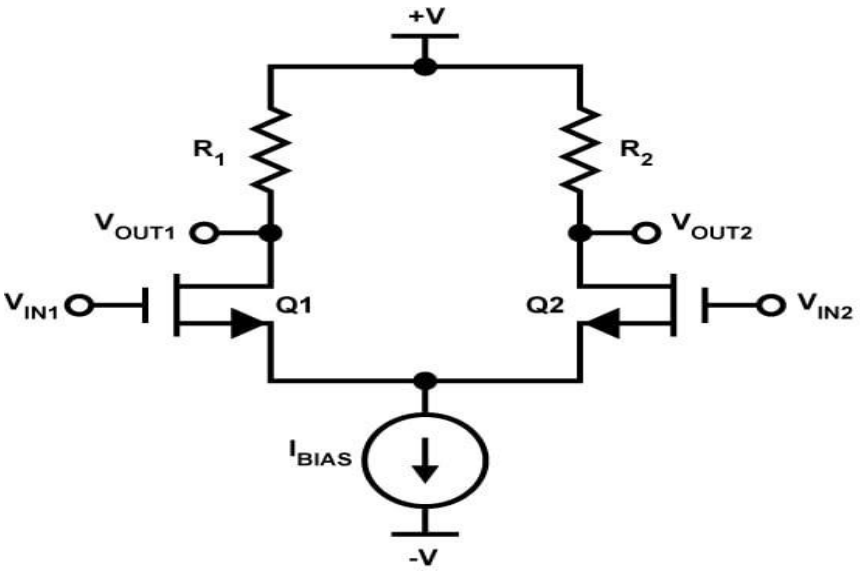
This portfolio showcases the complete design and layout of a Two-Stage CMOS Operational Amplifier, highlighting differential pairs, current mirrors, floorplanning, placement, routing, and verification stages. Matching techniques such as **Common Centroid** and **Interdigitation** have been applied to ensure high precision and symmetry in analog layout.

Schematic of the Two-Stage Op-Amp



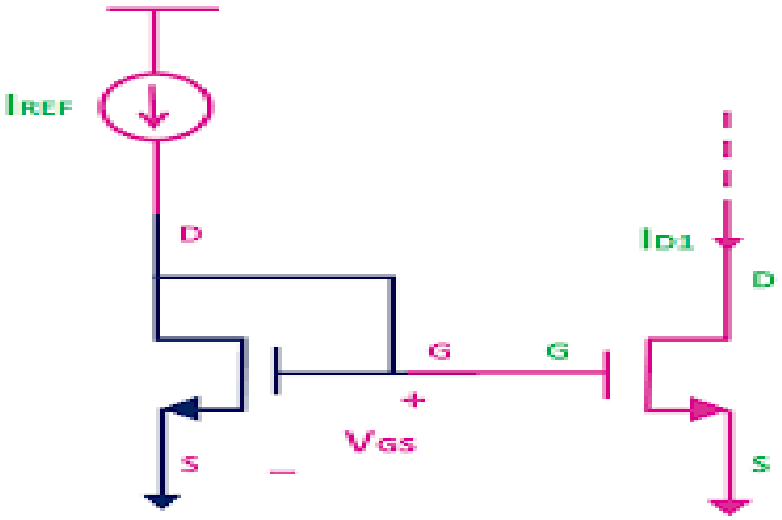
The schematic illustrates the design of a two-stage CMOS operational amplifier, showing transistor-level connections and biasing setup.

Differential Pair Layout



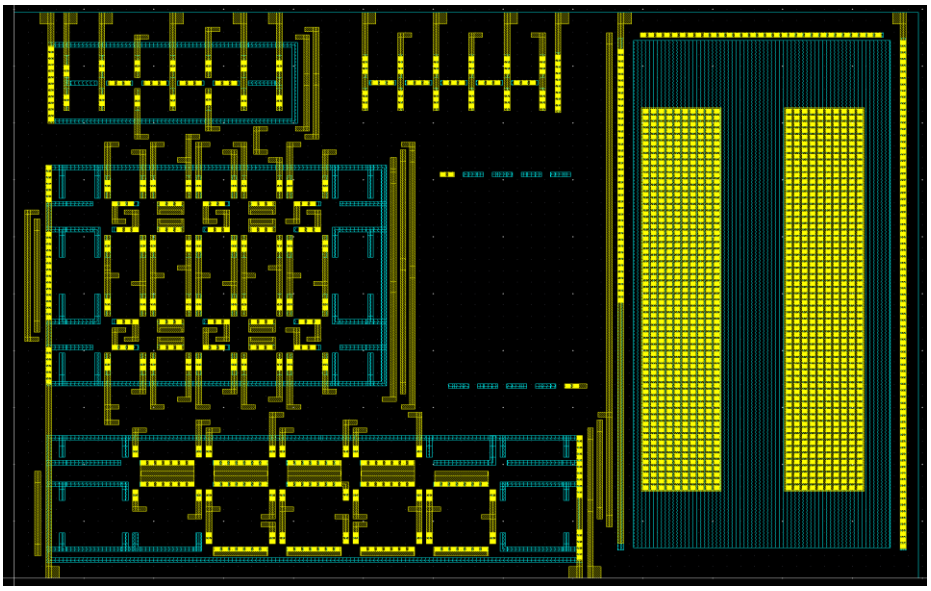
The differential pair ensures input stage linearity and common-mode noise rejection. Matching is achieved using common centroid arrangement for balanced parasitics.

Current Mirror Layout



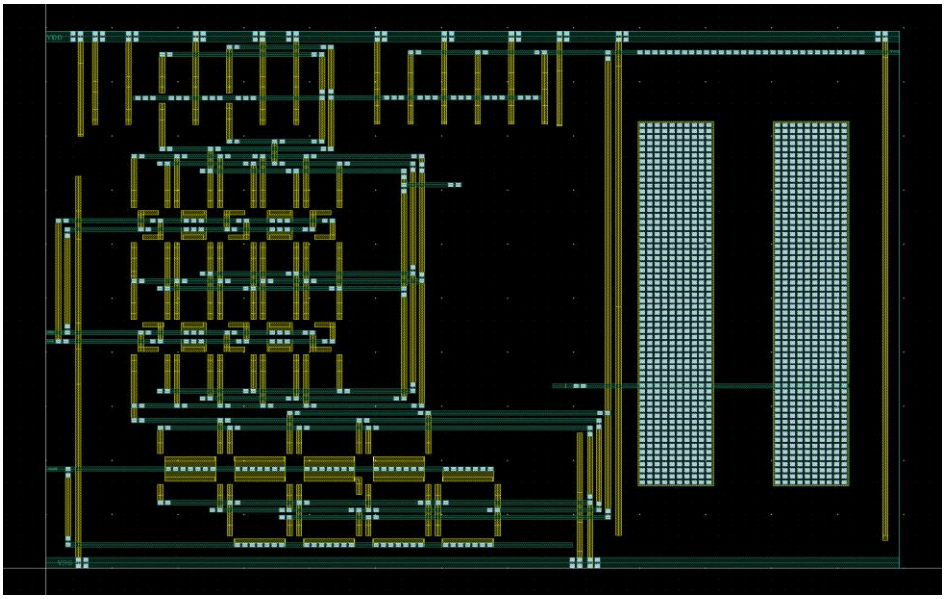
Current mirrors provide biasing and gain control. Interdigitation and symmetry techniques are used for precise current replication.

Routing for M1, M2



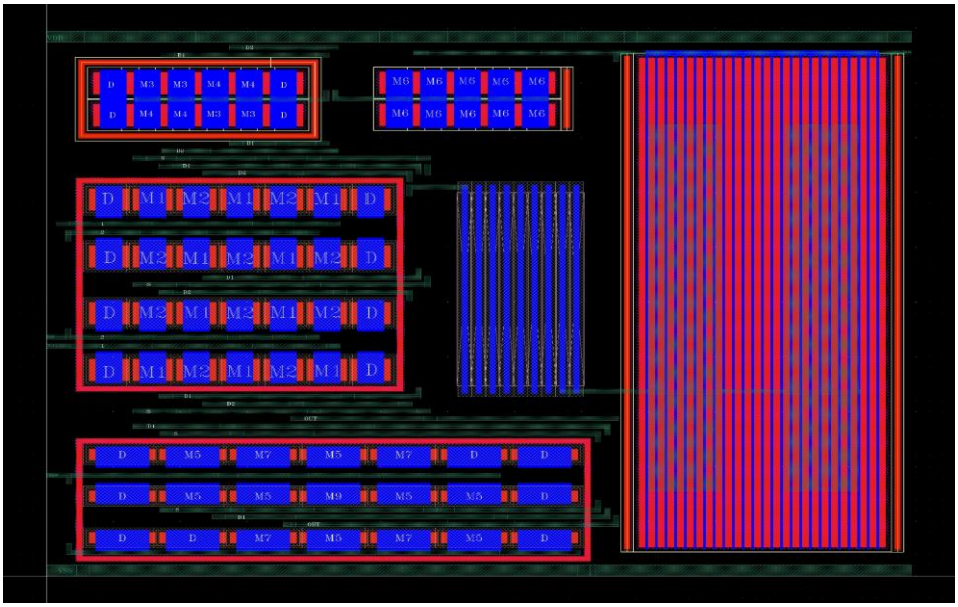
Metal interconnections for transistors M1 and M2 are carefully routed to maintain symmetry and reduce mismatch.

Routing for M2, M3



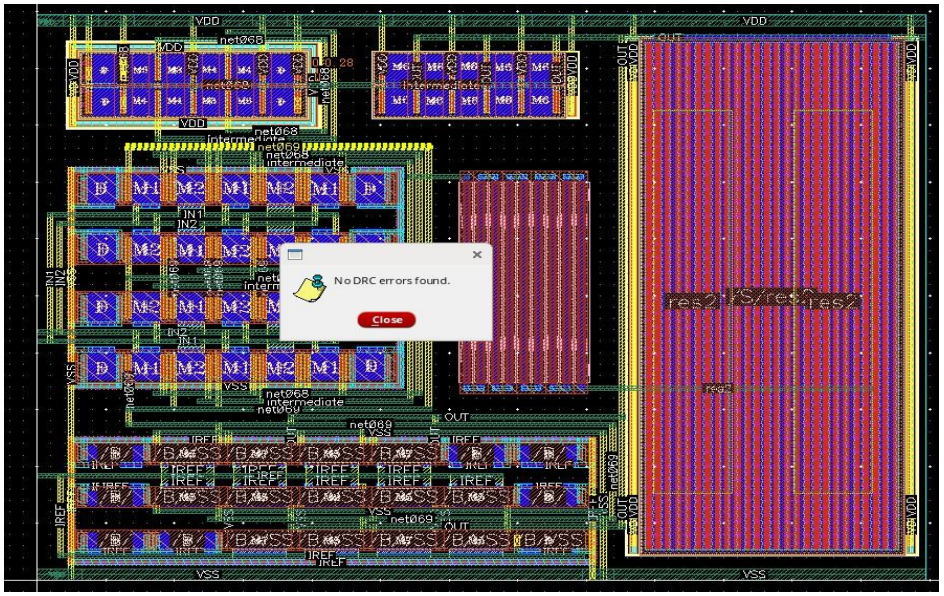
This stage connects M2 and M3 with matched path lengths and balanced parasitic capacitances for uniform current flow.

Routing for M3 and Differential Pair



The routing integrates the differential pair and current mirror stages, maintaining matched geometries and minimal offset potential.

DRC Verification

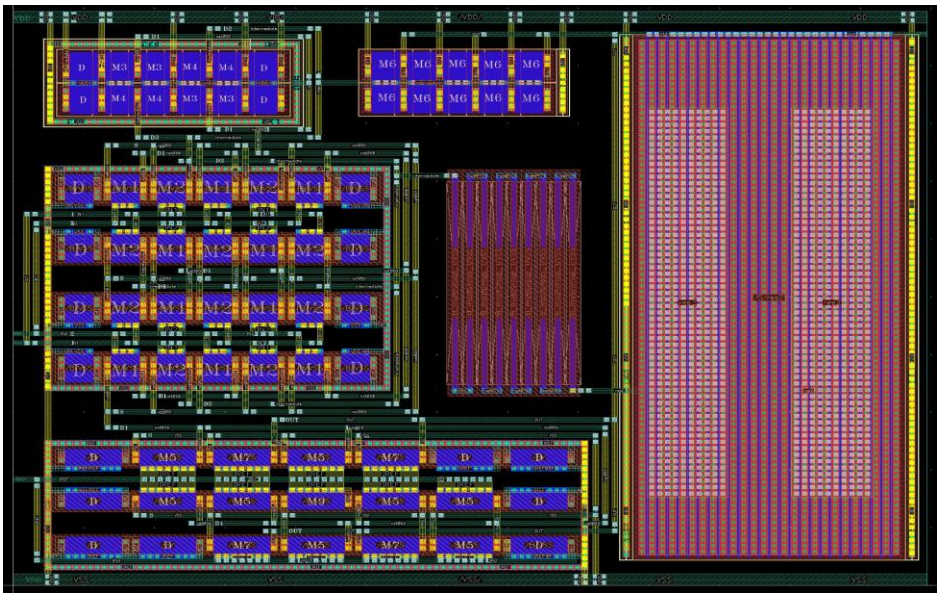


Design Rule Check (DRC) confirms there are no violations and the layout adheres to fabrication constraints.

LVS Verification

Layout Versus Schematic (LVS) ensures that the physical layout corresponds exactly to the intended schematic connections.

Final Op-Amp Layout



The complete layout demonstrates a clean, symmetrical design with proper device matching and routing integrity.

Conclusion:

The Two-Stage CMOS Op-Amp design integrates differential amplification, current mirror biasing, and precise layout strategies. By employing **Common Centroid** and **Interdigitation** matching techniques, the design achieves high accuracy, minimized offset, and robust performance—ideal for analog signal processing applications.