Experiment No. 6

Aim: To study Half and Full adder circuits.

Apparatus: Digital trainer kit, IC 7486, IC 7408, IC 7432, single strand wires.

Theory:

1.Half Adder:

Half adder is a combinational circuit that performs simple addition of two binary numbers. If we assume A and B as the two bits whose addition is to be performed,the block diagram and a truth table for half adder with A, B as inputs and Sum, Carry as outputs can be tabulated as follows.

The logical expression for sum & carry can be obtained from the truth table and using K map is given as :

$$S = AB + BA = A + B$$
$$C = AB$$

Truth Table:

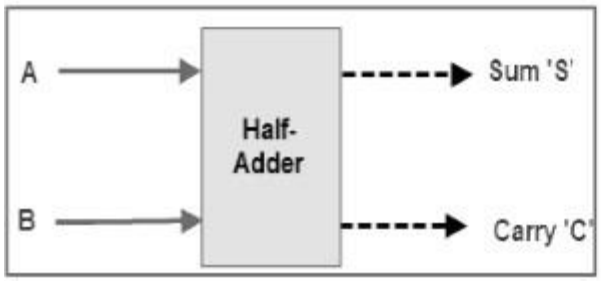


Figure - Full Adder Logic Diagram and

Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure - Full Adder Truth Table

If A and B are binary inputs to the half adder, then the logic function to calculate sum S is Ex – OR of A and B and logic function to calculate carry C is AND of A and B. Combining these two, the logical circuit to implement the combinational circuit of half adder is shown below -

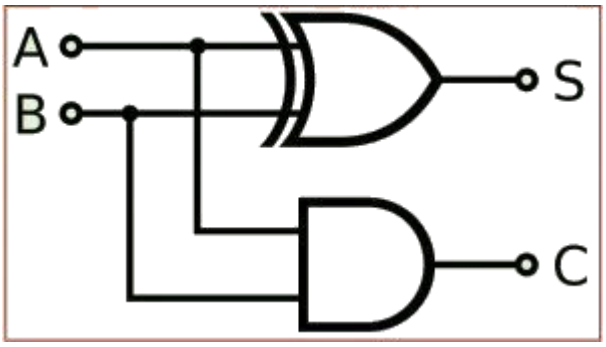


Figure : Half Adder Logic Diagram

1.2) Half Adder using NOR gates -

Five NOR gates are required in order to design a half adder. The circuit to realize half adder using NOR gates is shown below.

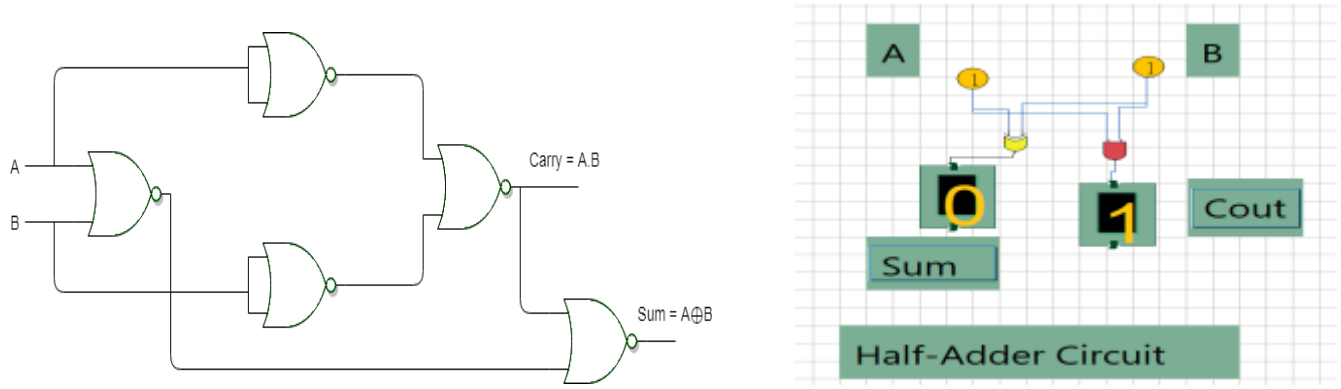


Figure - Realization of half adder using NOR Gates

2) Full Adder:

An half adder has only two inputs and there is no provision to and carry from adder bit. When multibit addition is performed for this purpose third input terminal is added and this circuit is used to add An, Bn & Cn-1 where An, Bn and nth order bit of numbers A & B respectively. And Cn-1 is carry generated from addition of (n-1)th order bits. This circuit is referred as Full adder. Let A,B,C are two bit no. & c is carry generated in previous addition of two 1 bit numbers.

Full adder is a digital circuit used to calculate the sum of three binary bits.Two of the three bits are same as before which are A, the augend bit and B, the addend bit. The additional third bit is carry bit from the previous stage and is called 'Carry' – in generally represented by CIN. It calculates the sum of three bits along with the carry. The output carry is called Carry – out and is represented by Carry OUT.

The block diagram of a full adder with A, B and CIN as inputs and S, Carry OUT as outputs is shown below.

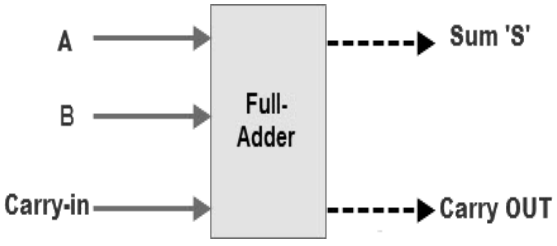


Figure - Full Adder Block Diagram

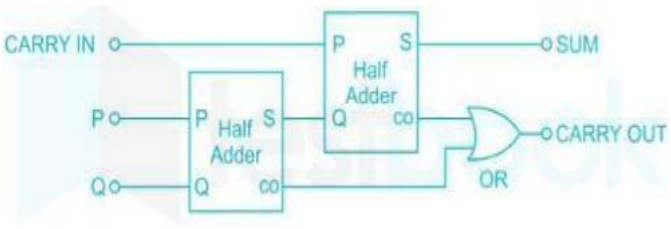


Figure - Full Adder can be Realized using two half adders

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure - Full Adder Truth Table and

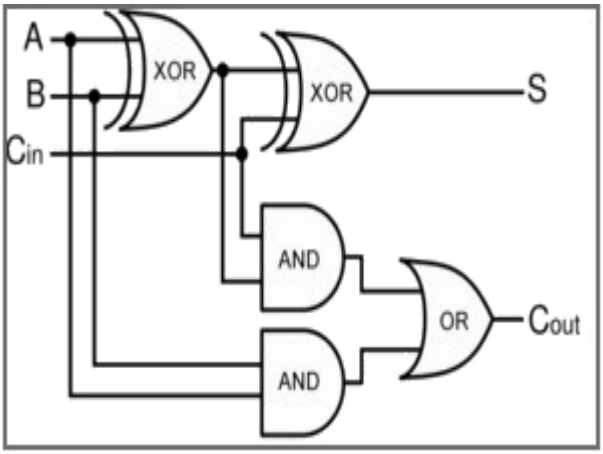


Figure - Full Adder Logic Diagram

2.2)Full Adder using NOR gates -

As mentioned earlier, a NOR gate is one of the universal gates and can be used to implement any logic design. The circuit of full adder using only NOR gates is shown below.

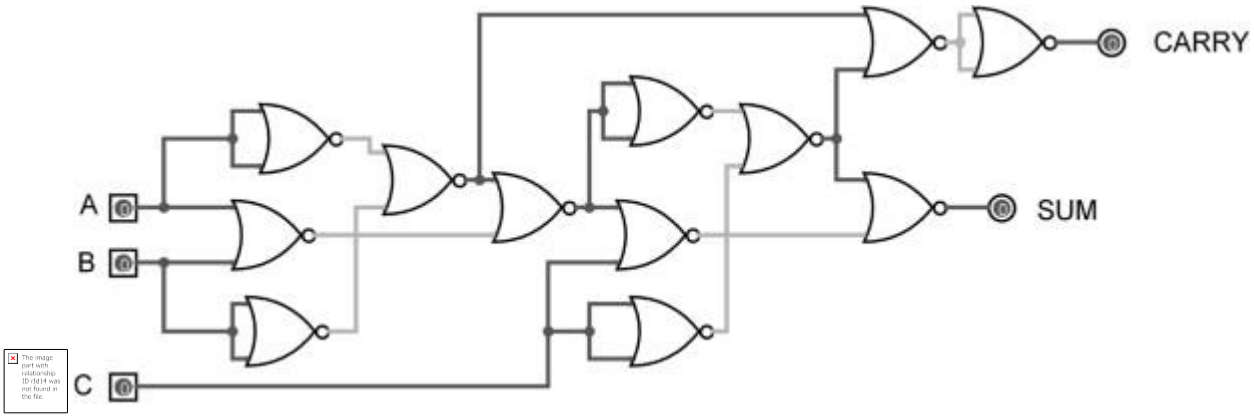
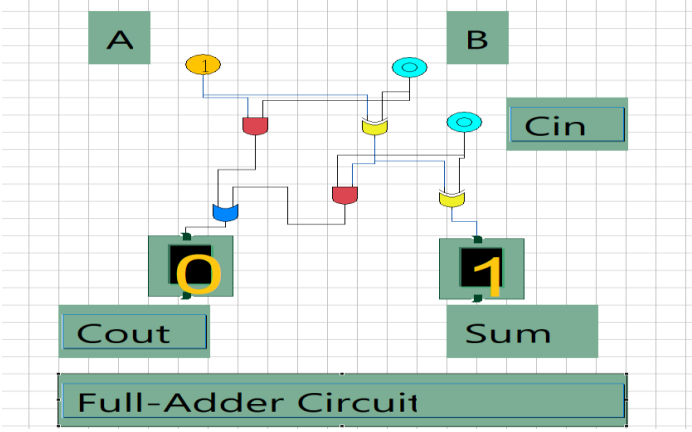


Figure - Full Adder using NOR gates

Let A,B,C are two bit no. & c is carry generated in previous addition of two 1 bit numbers.

From the k map expression for Full Adder is given as: For Sum s=A + B + C
For carry C0 = AB + BC + CA



Procedure:

Connect the circuit as shown in the circuit diagram. Make sure that circuit is connected properly as per IC pin diagram of respective IC's as shown in Logic Diagram

Observe and verify sum and carry output by connecting it to 2 bit displays.

Conclusion:

Half adder circuits adds two 1 bit numbers in which no provision for adding carry generated in lower order bit addition where as in full adder we can add carry generated from previous addition.

QUESTIONS:

1. What is a combinational circuit

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2. What is a sequential circuit?

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3. If A and B are the inputs of a half adder, the sum is given by _____
a: A AND B b: A OR B **c**: A Ex-OR B d: A EX-NOR B

4. If A and B are the inputs of a half adder, the carry is given by _____
a: A AND B b: A OR B c: A Ex-OR B d: A Ex-NOR B

5. If A, B and C are the inputs of a full adder then the sum is given by _____
Options
A : A AND B AND C B : A OR B AND C
C : A XOR B XOR C D : A OR B OR C

6. Half-adders have a major limitation in that they cannot _____
   a) Accept a carry bit from a present stage
   b) Accept a carry bit from a next stage
   c) Accept a carry bit from a previous stage
   d) Accept a carry bit from the following stages

7. How many AND, OR and EXOR gates are required for the configuration of full adder?
   a) 1, 2, 2 **b**) 2, 1, 2 c) 3, 1, 2 d) 4, 0, 1