Experiment No. : 03

Aim: To implement 4-bit carry look ahead adder.

Objective:

1. To reducing computation time with respect of ripple carry adder by using carry generate and propagate functions.

2. The adder will add two 4 bit numbers.

Theory:

A **carry-lookahead adder** (CLA) or fast **adder** is a type of **adder** used in digital logic. A **carry-lookahead adder** improves speed by reducing the amount of time required to determine **carry** bits. It can be contrasted with the simpler, but usually slower, *ripple carry adder* for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry bit have been calculated to begin calculating its own result and carry bits (see adder for detail on ripple carry adders). The carry-lookahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits of the adder. To reduce the computation time, there are faster ways to add two binary numbers by using carry lookahead adders. They work by creating two signals P and G known to be **Carry Propagator** and **Carry Generator**. The carry propagator is propagated to the next level whereas the carry generator is used to generate the output carry ,regardless of input carry. The block diagram of a 4-bit Carry Lookahead Adder is shown here below

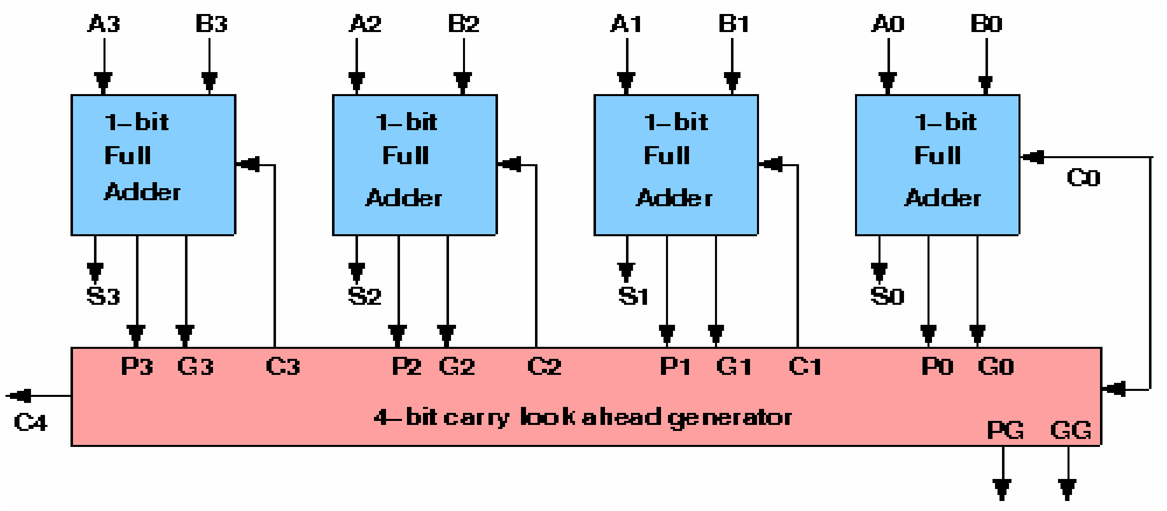
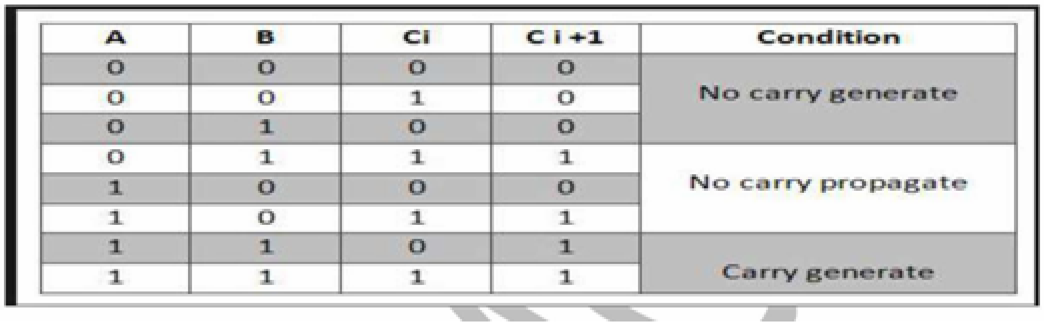


Fig1: 4-bit carry lookahead adder.

The number of gate levels for the carry propagation can be found from the circuit of full adder. The signal from input carry Cin to output carry Cout requires an AND gate and an OR gate, which constitutes two gate levels. So if there are four full adders in the parallel adder, the output carry C5 would have 2 X 4 = 8 gate levels from C1 to C5. For an n-bit parallel adder, there are 2n gate levels to propagate through.



A	B	Ci	C i+1	Condition
0	0	0	0	No carry generate
0	0	1	0	
0	1	0	0	
0	1	1	1	No carry propagate
1	0	0	0	
1	0	1	1	
1	1	0	1	Carry generate
1	1	1	1	

Fig 2: carry lookahead adder truth table

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Design Issues:

The corresponding boolean expressions are given here to construct a carry lookahead adder. In the carry-lookahead circuit we ned to generate the two signals carry propagator(P) and carry generator(G),

Pi = Ai $\oplus$ Bi

Gi = Ai · Bi

The output sum and carry can be expressed as

Sumi = Pi $\oplus$ Ci

Ci+1 = Gi + (Pi · Ci)

Having these we could design the circuit. We can now write the Boolean function for the carry output of each stage and substitute for each Ci its value from the previous equations:

C1 = G0 + P0 · C0

C2 = G1 + P1 · C1 = G1 + P1 · G0 + P1 · P0 · C0

C3 = G2 + P2 · C2 = G2 P2 · G1 + P2 · P1 · G0 + P2 · P1 · P0 · C0

C4 = G3 + P3 · C3 = G3 P3 · G2 P3 · P2 · G1 + P3 · P2 · P1 · G0 + P3 · P2 · P1 · P0 · C0

Procedure:

1. Start the simulator as directed. This simulator supports 5-valued logic.

2. To design the circuit we need 7 half adder, 3 OR gate, 1 V+(to give 1 as input), 3 Digital display(2 for seeing input and 1 for seeing output sum), 1 Bit display(to see the carry output), wires.

3. The pin configuration of a component is shown whenever the mouse is hovered on any canned component of the palette or press the 'show pinconfig' button. Pin numbering starts from 1 and from the bottom left corner(indicating with the circle) and increases anticlockwise.

4. For half adder input is in pin-5,8 output sum is in pin-4 and carry is pin-1.

6. Click on the half adder component(in the Adder drawer in the pallet) and then click on the position of the editor window where you want to add the component(no drag and drop, simple click will serve the purpose), likewise add 6 more full adders(from the Adder drawer in the pallet), 3 OR gates(from Logic Gates drawer in the pallete), 1 V+, 3 digital display and 1 bit Displays(from Display and Input drawer of the pallete,if it is not seen scroll down in the drawer).

7. To connect any two components select the Connection menu of Palette, and then click on the Source terminal and click on the target terminal. According to the circuit diagram connect all the components, connect V+ to the upper input terminals of 2 digital displays according to you input. connect the OR gates according to the diagram shown in the screenshot connect the pin-1 of the half adder which will give the final carry output. connect the sum(pin-4) of those adders to the terminals of the third digital display which will give output sum. After the connection is over click the selection tool in the pallete.

8. See the output, in the screenshot diagram we have given the value 0011(3) and 0111(7) so get 10 as sum and 0 as carry.you can also use many bit switches instead of V+ to give input and by double clicking those bit switches can give different values and check the result.

Circuit diagram of Carry Look ahead Adder:

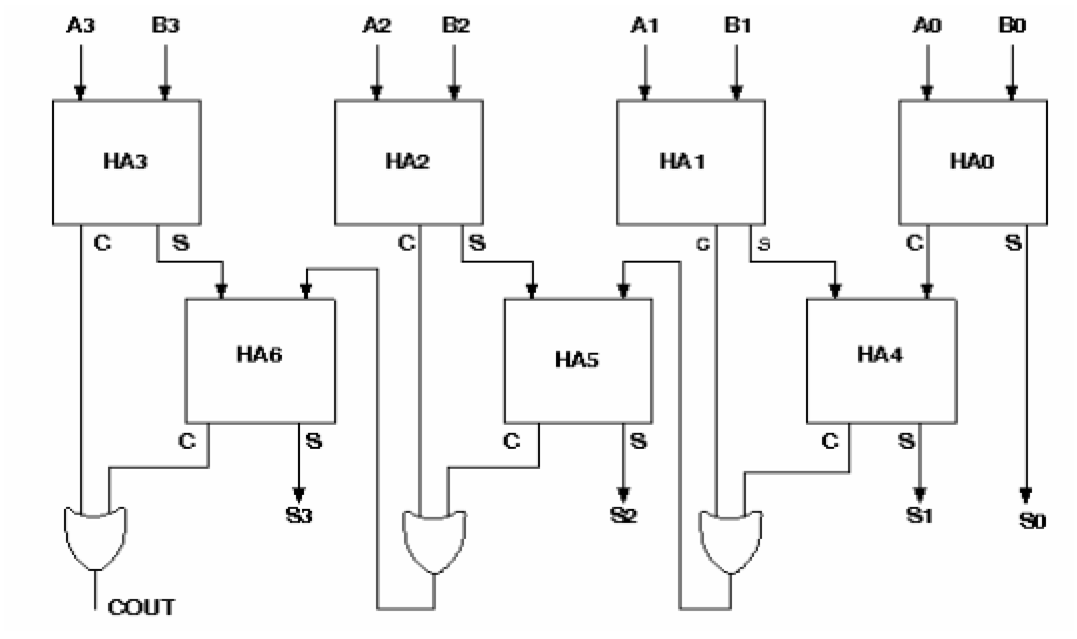

Fig 3: Circuit diagram of Carry look ahead Adder

Result:

Conclusion:

Hence we have implemented, simulated, analyzed carry lookahead adder which gives less propagation delay as compared to ripple carry adder. The carry look ahead adder is used as propagation adder in various multipliers and gives less delay.

Industrial Application:

Carry lookahead adder used in industry in digital logic. A carry-lookahead adder improves speed by reducing the amount of time required to determine carry bits.
The carry-lookahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits of the adder. The **Kogge-Stone adder** and **Brent-Kung adder** are examples of this type of adder.