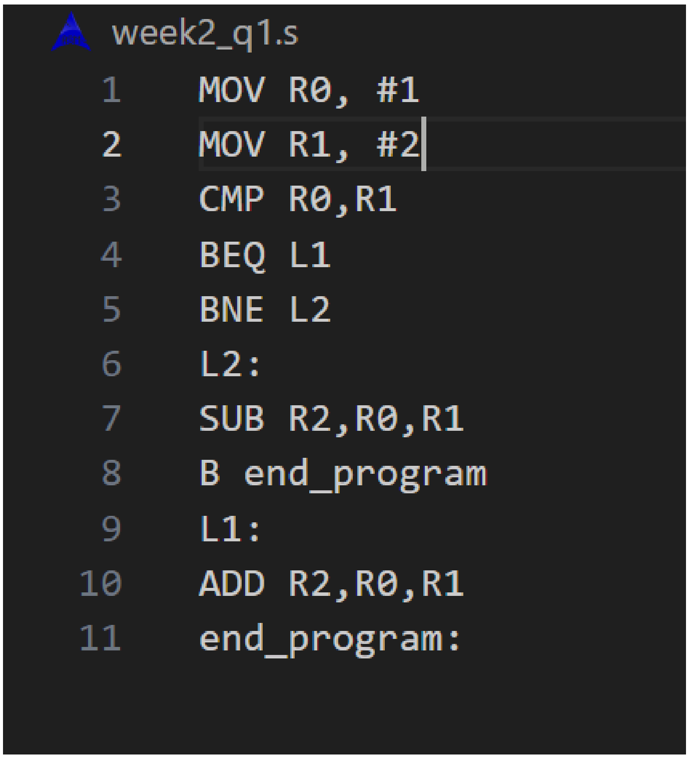
Department of Computer Science & Engineering
Microprocessor & Computer Architecture Lab
Name: Shriya Konduru
SRN:PES2UG22CS546

Lab_1 Programs

UE22CS251B

1 Write an ALP to add if the numbers are equal, otherwise subtract them.

Program:

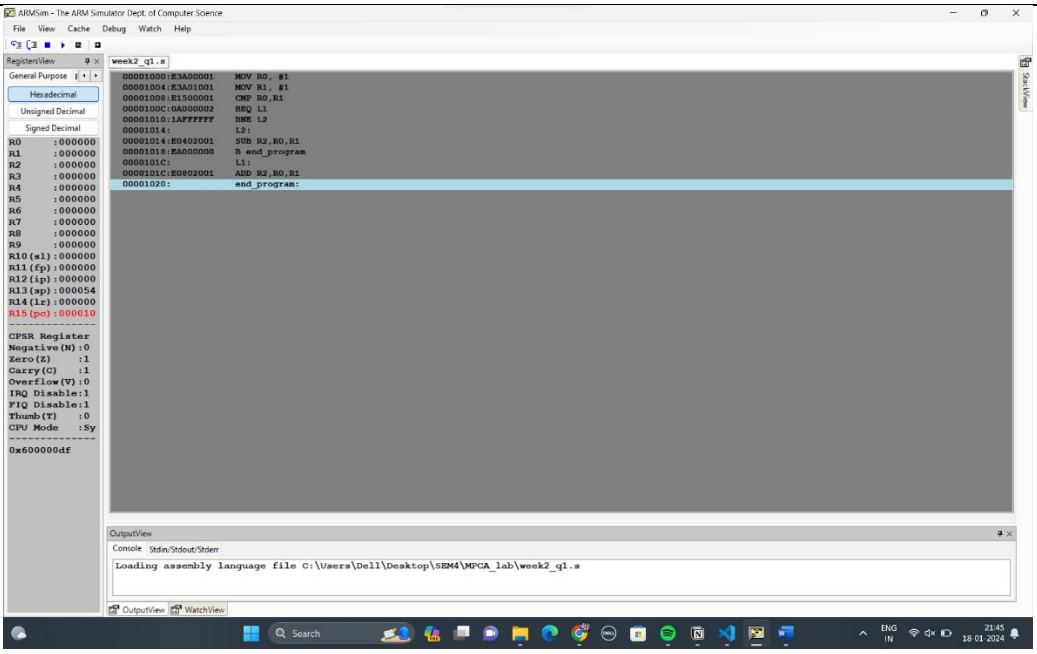


week2_q1.s

```
MOV R0, #1
MOV R1, #2
CMP R0,R1
BEQ L1
BNE L2
L2:
SUB R2,R0,R1
B end_program
L1:
ADD R2,R0,R1
end_program:
```

Output Screen Shot:

Case 1:

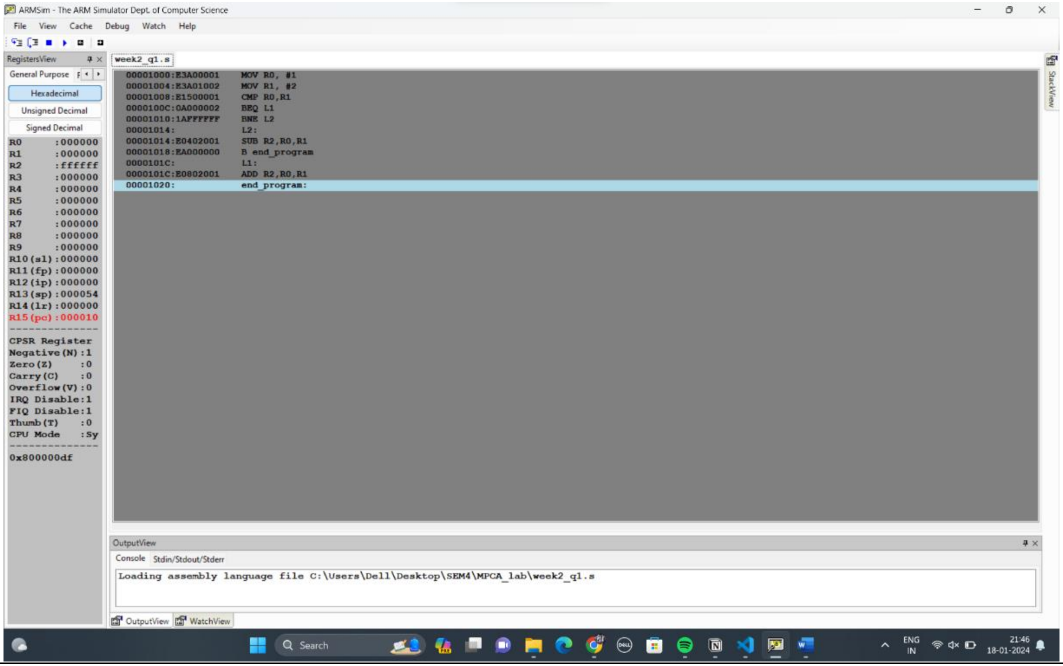


```
00001000:E3A00001    MOV R0, #1
00001004:E3A01001    MOV R1, #1
00001008:E1500001    CMP R0,R1
0000100C:0A000002    BEQ L1
00001010:1AFFFFFF    BNE L2
00001014:            L2:
00001014:E0402001    SUB R2,R0,R1
00001018:EA000000    B end_program
0000101C:            L1:
0000101C:E0802001    ADD R2,R0,R1
00001020:            end_program:
```

```
R0       :000000
R1       :000000
R2       :000000
R3       :000000
R4       :000000
R5       :000000
R6       :000000
R7       :000000
R8       :000000
R9       :000000
R10(sl):000000
R11(fp):000000
R12(ip):000000
R13(sp):000054
R14(lr):000000
R15(pc):000010
--------------
CPSR Register
Negative(N):0
Zero(Z)    :1
Carry(C)   :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :Sy
--------------
0x600000df
```

```
Loading assembly language file C:\Users\Dell\Desktop\SEM4\MPCA_lab\week2_q1.s
```

Case 2:



```
00001000:E3A00001    MOV R0, #1
00001004:E3A01002    MOV R1, #2
00001008:E1500001    CMP R0,R1
0000100C:0A000002    BEQ L1
00001010:1AFFFFFF    BNE L2
00001014:            L2:
00001014:E0402001    SUB R2,R0,R1
00001018:EA000000    B end_program
0000101C:            L1:
0000101C:E0802001    ADD R2,R0,R1
00001020:            end_program:
```

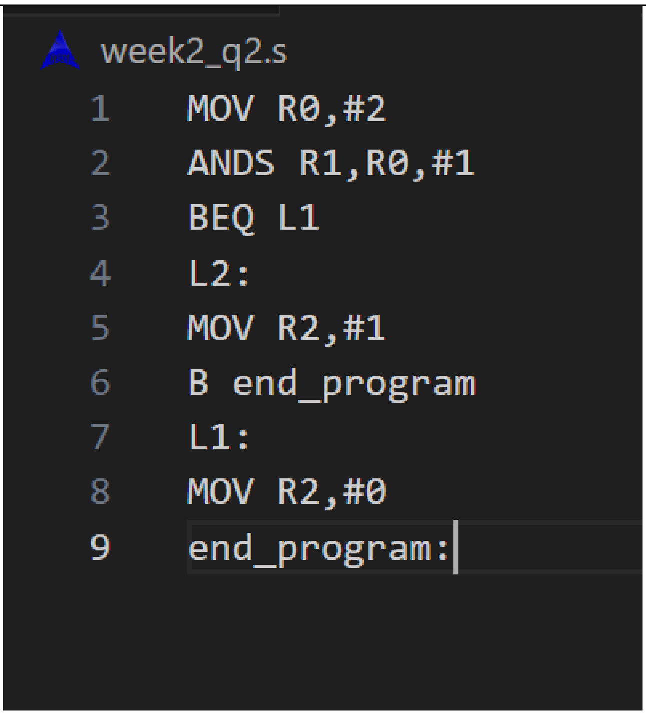
```
R0       :000000
R1       :000000
R2       :ffffff
R3       :000000
R4       :000000
R5       :000000
R6       :000000
R7       :000000
R8       :000000
R9       :000000
R10(sl):000000
R11(fp):000000
R12(ip):000000
R13(sp):000054
R14(lr):000000
R15(pc):000010
--------------
CPSR Register
Negative(N):1
Zero(Z)    :0
Carry(C)   :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :Sy
--------------
0x800000df
```

```
Loading assembly language file C:\Users\Dell\Desktop\SEM4\MPCA_lab\week2_q1.s
```

2 Check if a given number is even or odd.

Note: at the end of the program execution R2 contains 0 if number is even, otherwise R2 contains 1.

Program:

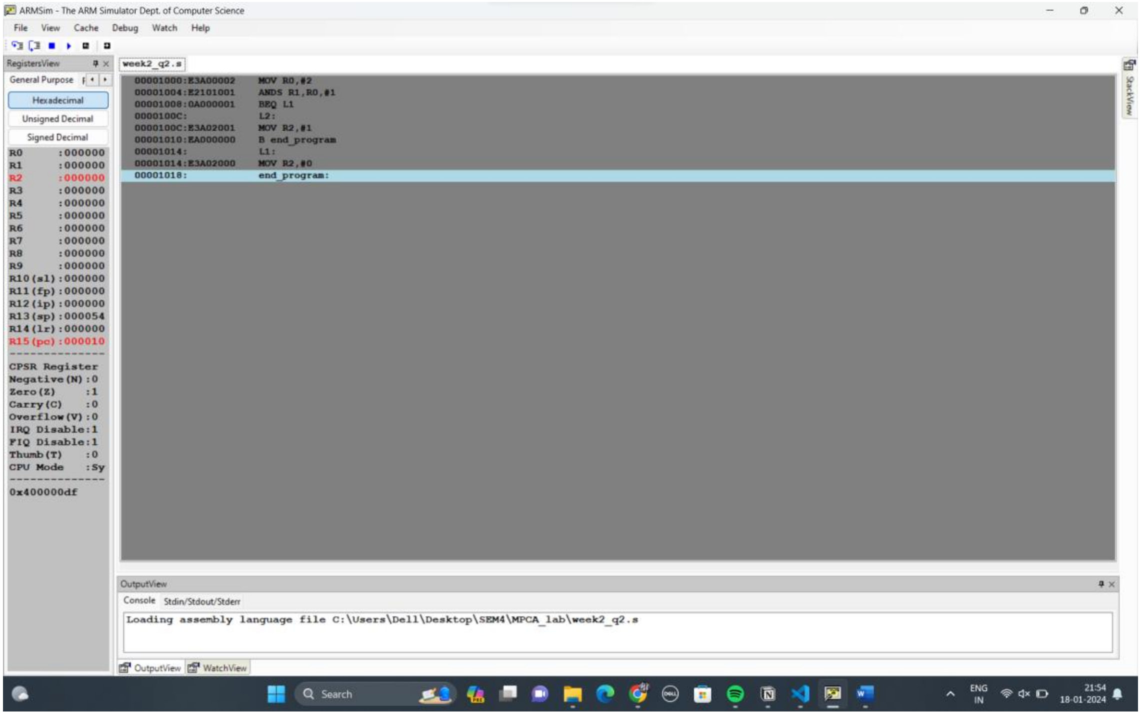


week2_q2.s

```
MOV R0,#2
ANDS R1,R0,#1
BEQ L1
L2:
MOV R2,#1
B end_program
L1:
MOV R2,#0
end_program:
```

Output Screen Shot:

Case 1:

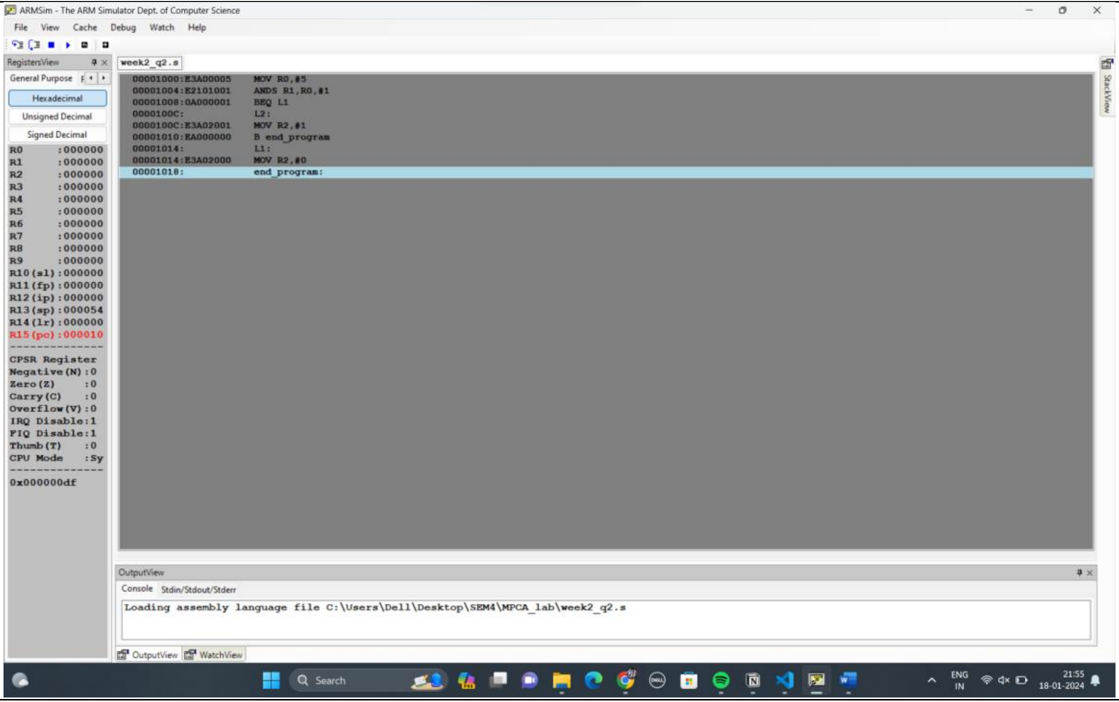


```
00001000:E3A00002    MOV R0,#2
00001004:E2101001    ANDS R1,R0,#1
00001008:0A000001    BEQ L1
0000100C:            L2:
0000100C:E3A02001    MOV R2,#1
00001010:EA000000    B end_program
00001014:            L1:
00001014:E3A02000    MOV R2,#0
00001018:            end_program:
```

```
R0       :000000
R1       :000000
R2       :000000
R3       :000000
R4       :000000
R5       :000000
R6       :000000
R7       :000000
R8       :000000
R9       :000000
R10(sl)  :000000
R11(fp)  :000000
R12(ip)  :000000
R13(sp)  :000054
R14(lr)  :000000
R15(pc)  :000010
---------------
CPSR Register
Negative(N):0
Zero(Z)    :1
Carry(C)   :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :Sy
---------------
0x400000df
```

```
Loading assembly language file C:\Users\Dell\Desktop\SEM4\MPCA_lab\week2_q2.s
```

Case 2:



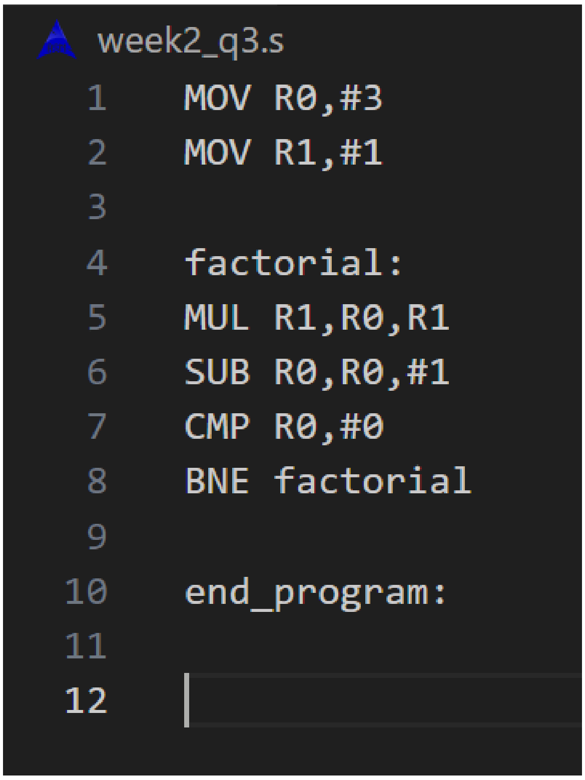
```
R0        :000000
R1        :000000
R2        :000000
R3        :000000
R4        :000000
R5        :000000
R6        :000000
R7        :000000
R8        :000000
R9        :000000
R10(sl):000000
R11(fp):000000
R12(ip):000000
R13(sp):000054
R14(lr):000000
R15(pc):000010
--------------
CPSR Register
Negative(N):0
Zero(Z)     :0
Carry(C)    :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)    :0
CPU Mode    :Sy
--------------
0x000000df
```

```
00001000:E3A00005    MOV R0,#5
00001004:E2101001    ANDS R1,R0,#1
00001008:0A000001    BEQ L1
0000100C:            L2:
0000100C:E3A02001    MOV R2,#1
00001010:EA000000    B end_program
00001014:            L1:
00001014:E3A02000    MOV R2,#0
00001018:            end_program:
```

```
Loading assembly language file C:\Users\Dell\Desktop\SEM4\MPCA_lab\week2_q2.s
```

3 Write a program to find the factorial of a given number.

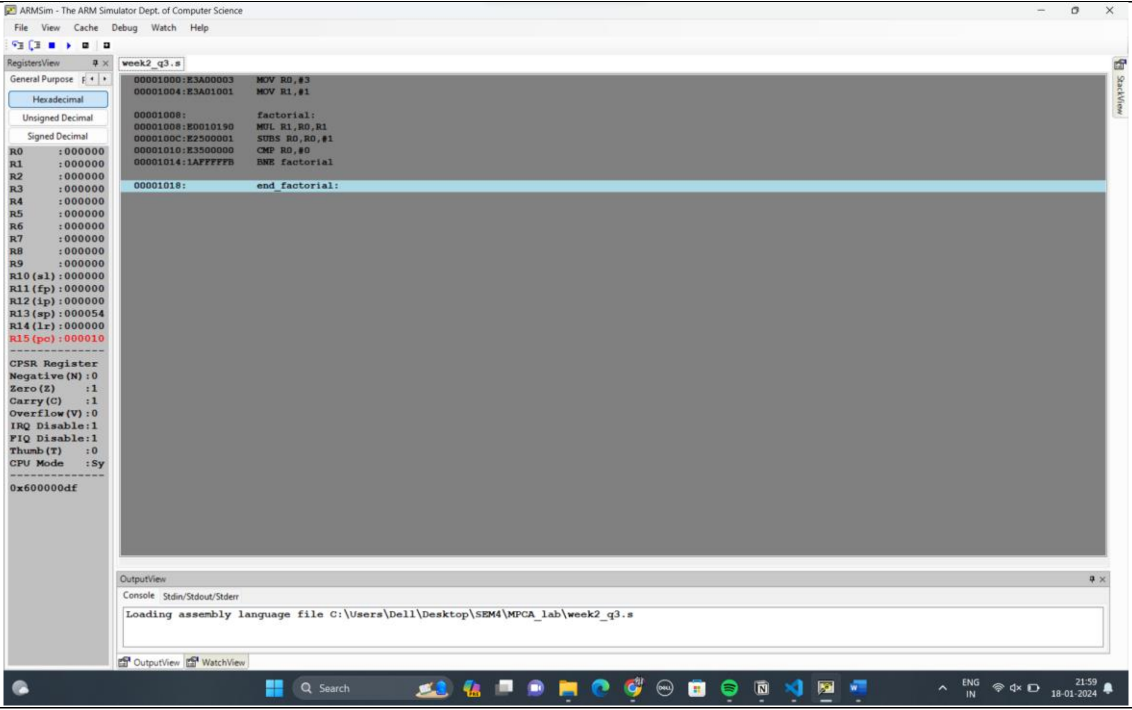
Program:



week2_q3.s

```
MOV R0,#3
MOV R1,#1

factorial:
MUL R1,R0,R1
SUB R0,R0,#1
CMP R0,#0
BNE factorial

end_program:

```

Output Screen Shot:



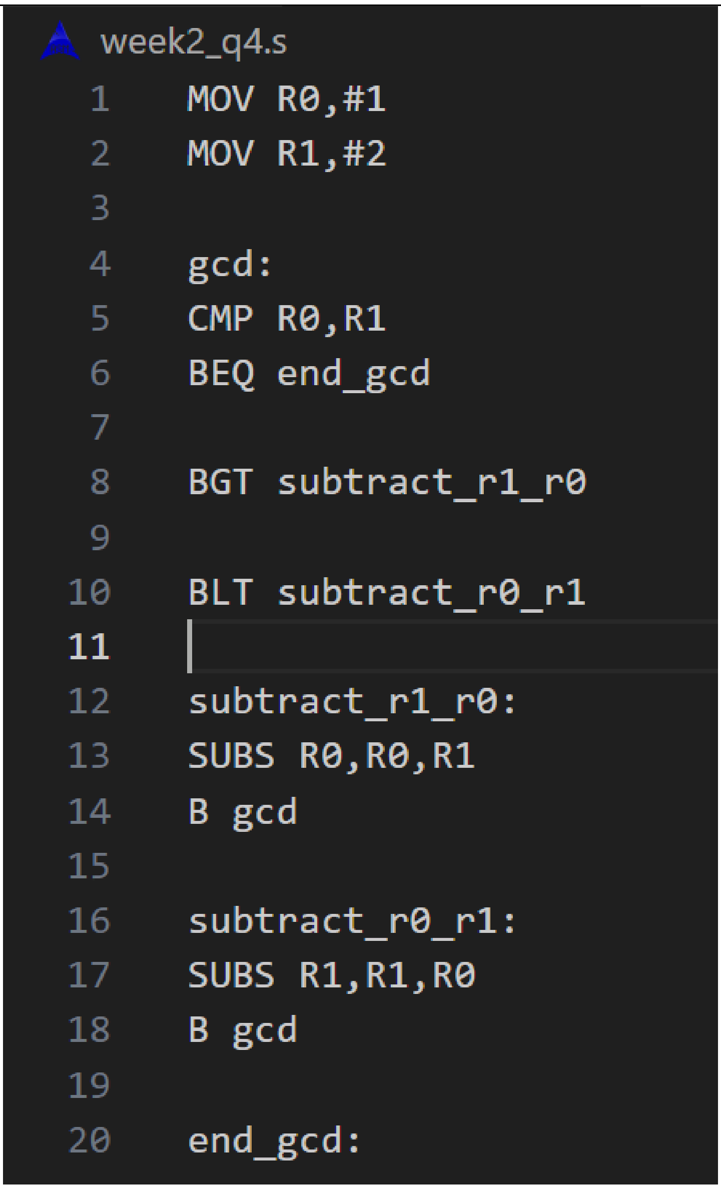
```
00001000:E3A00003    MOV R0,#3
00001004:E3A01001    MOV R1,#1

00001008:            factorial:
00001008:E0010190    MUL R1,R0,R1
0000100C:E2500001    SUBS R0,R0,#1
00001010:E3500000    CMP R0,#0
00001014:1AFFFFFB    BNE factorial

00001018:            end_factorial:
```

```
R0      :000000
R1      :000000
R2      :000000
R3      :000000
R4      :000000
R5      :000000
R6      :000000
R7      :000000
R8      :000000
R9      :000000
R10(sl) :000000
R11(fp) :000000
R12(ip) :000000
R13(sp) :000054
R14(lr) :000000
R15(pc) :000010
--------------
CPSR Register
Negative(N):0
Zero(Z)    :1
Carry(C)   :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :Sy
--------------
0x600000df
```

```
Loading assembly language file C:\Users\Dell\Desktop\SEM4\MPCA_lab\week2_q3.s
```

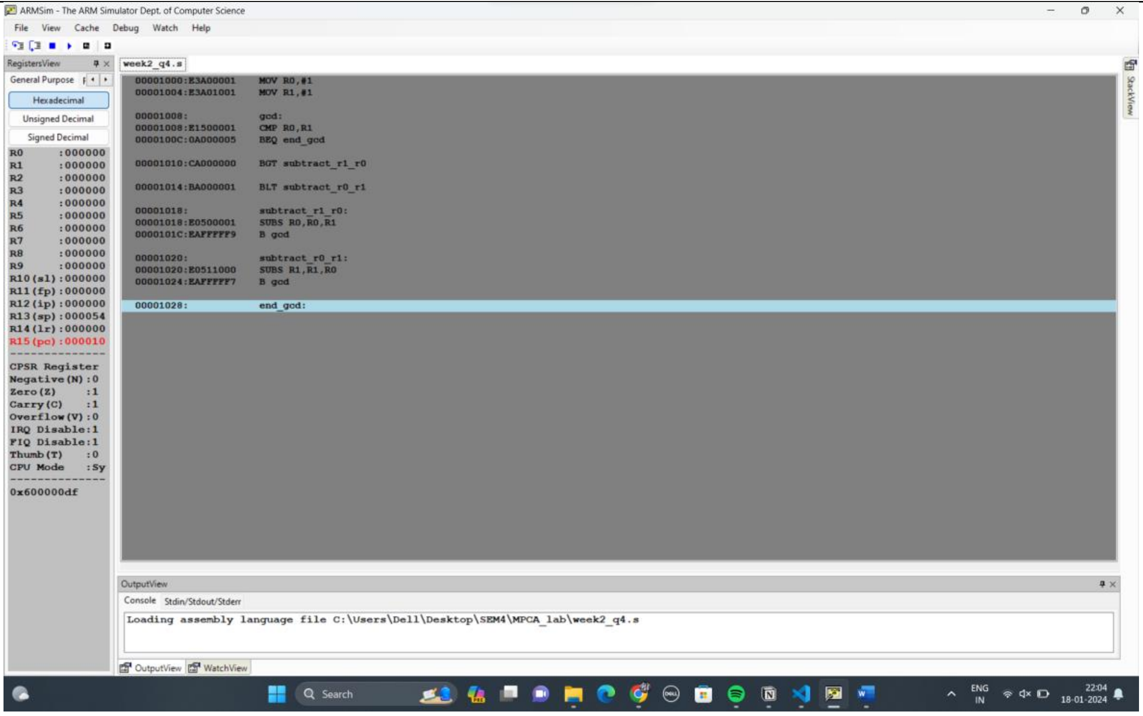
4 Write a program to find GCD of two numbers.

Program:



```
MOV R0,#1
MOV R1,#2

gcd:
CMP R0,R1
BEQ end_gcd

BGT subtract_r1_r0

BLT subtract_r0_r1

subtract_r1_r0:
SUBS R0,R0,R1
B gcd

subtract_r0_r1:
SUBS R1,R1,R0
B gcd

end_gcd:
```

Output Screen Shot:
Case 1:

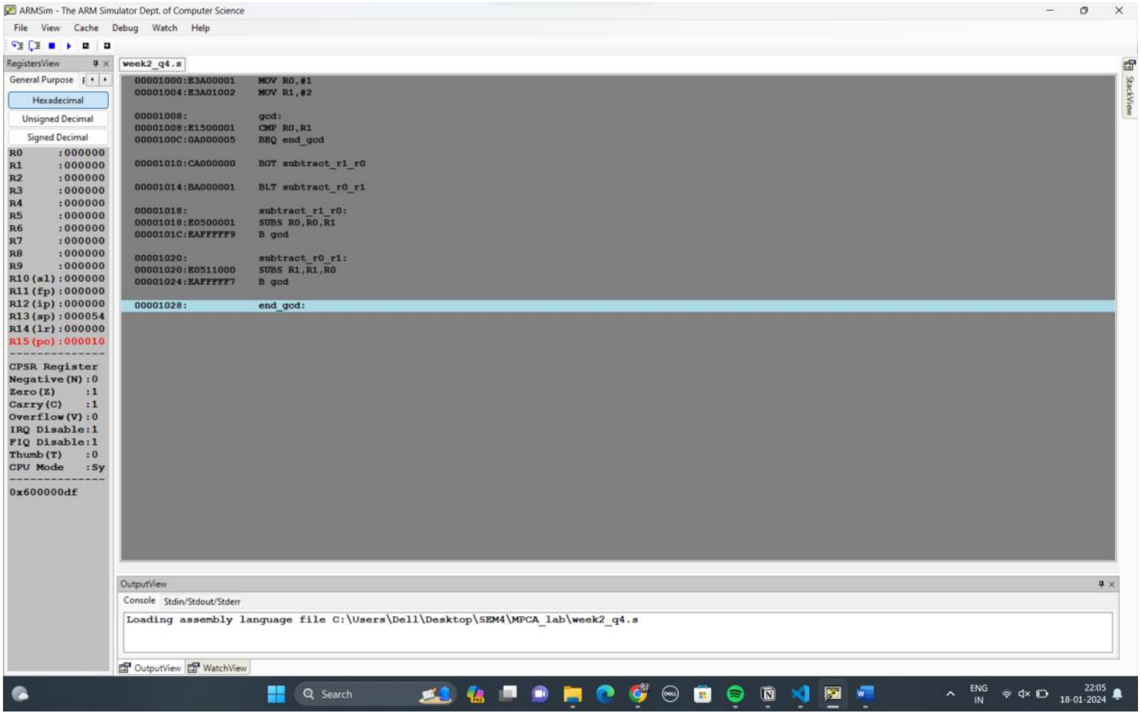


```
R0        :000000
R1        :000000
R2        :000000
R3        :000000
R4        :000000
R5        :000000
R6        :000000
R7        :000000
R8        :000000
R9        :000000
R10(sl):000000
R11(fp):000000
R12(ip):000000
R13(sp):000054
R14(lr):000000
R15(pc):000010
---------------
CPSR Register
Negative(N):0
Zero(Z)     :1
Carry(C)    :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)    :0
CPU Mode    :Sy
---------------
0x600000df
```

```
00001000:E3A00001    MOV R0,#1
00001004:E3A01001    MOV R1,#1

00001008:            gcd:
00001008:E1500001    CMP R0,R1
0000100C:0A000005    BEQ end_gcd

00001010:CA000000    BGT subtract_r1_r0

00001014:BA000001    BLT subtract_r0_r1

00001018:            subtract_r1_r0:
00001018:E0500001    SUBS R0,R0,R1
0000101C:EAFFFFF9    B gcd

00001020:            subtract_r0_r1:
00001020:E0511000    SUBS R1,R1,R0
00001024:EAFFFFF7    B gcd

00001028:            end_gcd:
```

```
Loading assembly language file C:\Users\Dell\Desktop\SEM4\MPCA_lab\week2_q4.s
```

Case 2:

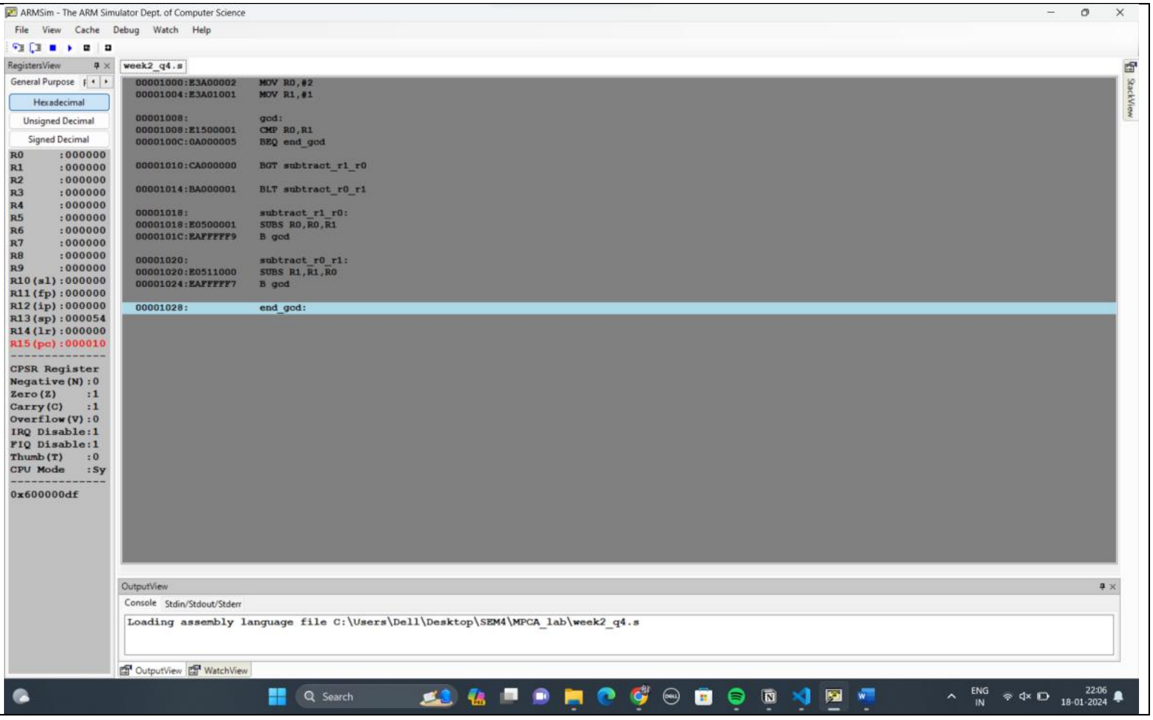


```
R0        :000000
R1        :000000
R2        :000000
R3        :000000
R4        :000000
R5        :000000
R6        :000000
R7        :000000
R8        :000000
R9        :000000
R10(sl):000000
R11(fp):000000
R12(ip):000000
R13(sp):000054
R14(lr):000000
R15(pc):000010
---------------
CPSR Register
Negative(N):0
Zero(Z)     :1
Carry(C)    :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)    :0
CPU Mode    :Sy
---------------
0x600000df
```

```
00001000:E3A00001    MOV R0,#1
00001004:E3A01002    MOV R1,#2

00001008:            gcd:
00001008:E1500001    CMP R0,R1
0000100C:0A000005    BEQ end_gcd

00001010:CA000000    BGT subtract_r1_r0

00001014:BA000001    BLT subtract_r0_r1

00001018:            subtract_r1_r0:
00001018:E0500001    SUBS R0,R0,R1
0000101C:EAFFFFF9    B gcd

00001020:            subtract_r0_r1:
00001020:E0511000    SUBS R1,R1,R0
00001024:EAFFFFF7    B gcd

00001028:            end_gcd:
```

```
Loading assembly language file C:\Users\Dell\Desktop\SEM4\MPCA_lab\week2_q4.s
```

Case 3:



```
00001000:E3A00002     MOV R0,#2
00001004:E3A01001     MOV R1,#1

00001008:             gcd:
00001008:E1500001     CMP R0,R1
0000100C:0A000005     BEQ end_gcd

00001010:CA000000     BGT subtract_r1_r0

00001014:BA000001     BLT subtract_r0_r1

00001018:             subtract_r1_r0:
00001018:E0500001     SUBS R0,R0,R1
0000101C:EAFFFFF9     B gcd

00001020:             subtract_r0_r1:
00001020:E0511000     SUBS R1,R1,R0
00001024:EAFFFFF7     B gcd

00001028:             end_gcd:
```

```
R0       :000000
R1       :000000
R2       :000000
R3       :000000
R4       :000000
R5       :000000
R6       :000000
R7       :000000
R8       :000000
R9       :000000
R10(sl)  :000000
R11(fp)  :000000
R12(ip)  :000000
R13(sp)  :000054
R14(lr)  :000000
R15(pc)  :000010
--------------
CPSR Register
Negative(N):0
Zero(Z)    :1
Carry(C)   :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :Sy
--------------
0x600000df
```

```
Loading assembly language file C:\Users\Dell\Desktop\SEM4\MPCA_lab\week2_q4.s
```

Note:

- Link to upload the file:
  - Will be provided by the respective Theory Teacher
- Upload PDF only.
- Save your file with your SRN _ Name