Faculty of Engineering

AIN SHAMS UNIVERSITY

Third year mechatronics engineering

Computer Organization

Third part of the project

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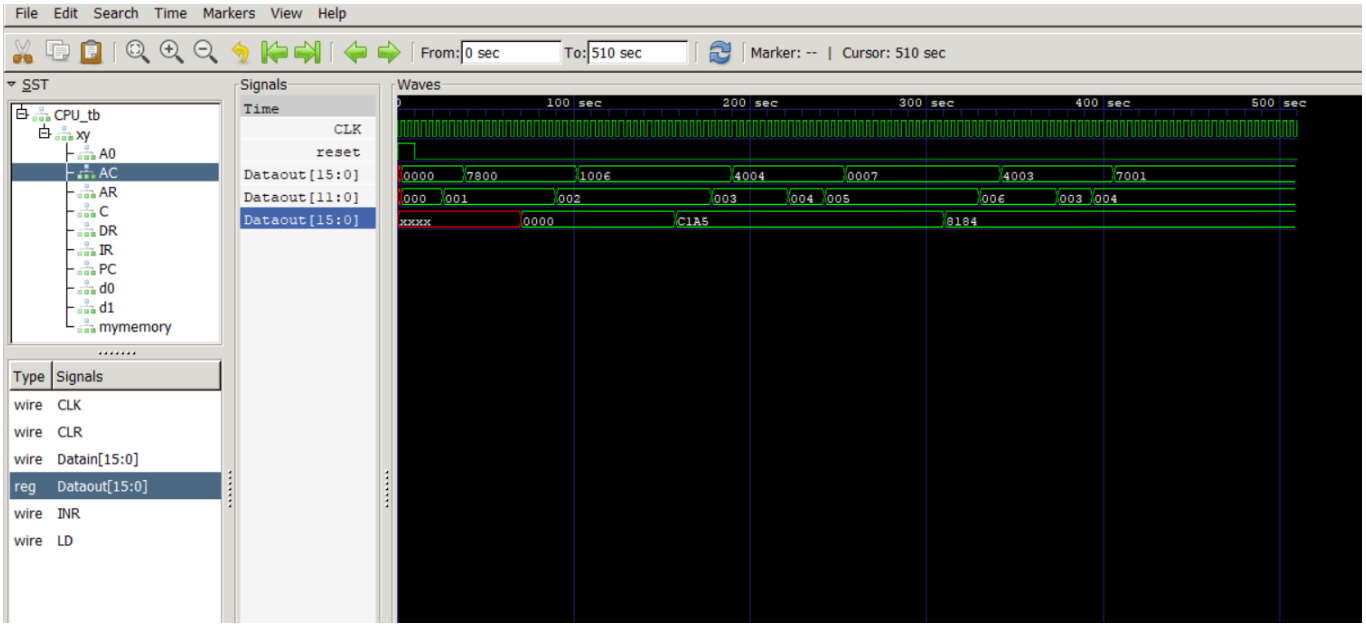
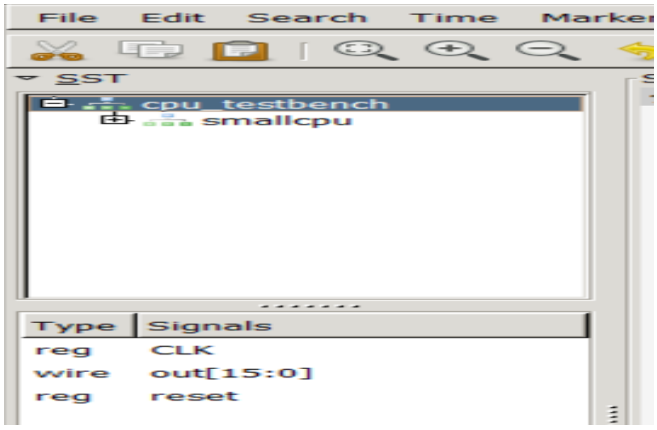
The executed program

Location	Instruction	Ac	Pc	IR
000	CLA	0000	001	7800
001	ADD 006	C1A5	002	1006
002	BUN 004	C1A5	004	4004
003	HLT	8184	004	7001
004	AND 007	8184	005	0007
005	BUN 003	8184	003	4003
006	C1A5			
007	93C6			



Design hints:

1. The top level module will have:
    a. Two inputs only: a *clock* and a global *reset* signal
    b. One output: the accumulator *AC*

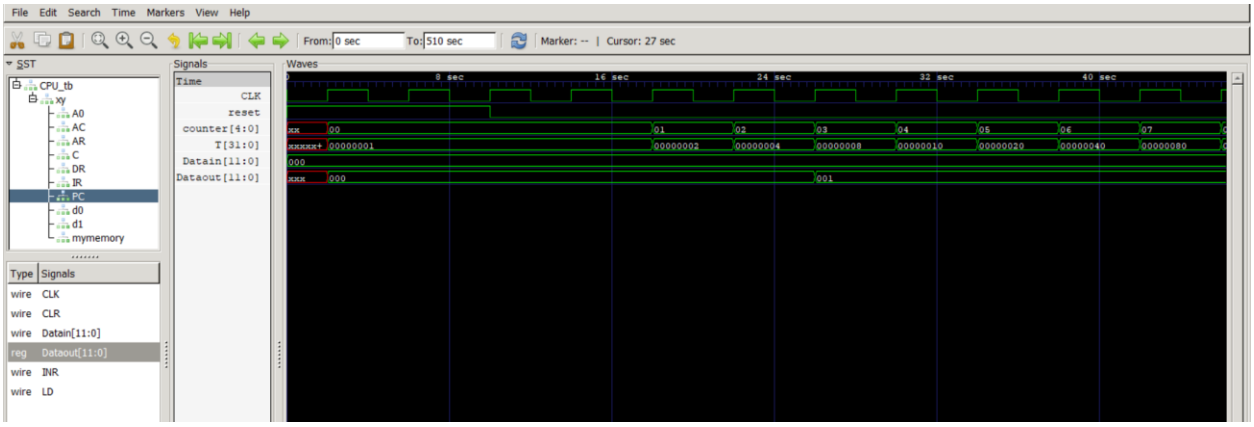


4. The memory module should have a sample test program for the CPU. Therefore, initialize the memory contents in your design with a small program.
5. For simplicity, let the first instruction in your program be at address 0.

```
module memory16(address,datain,dataout,R,W,CLK);
input CLK;
input R;
input W;
input [11:0]address;
input [15:0]datain;
output [15:0]dataout;
wire CLK;
wire R;
wire W;
wire[11:0]address;
wire[15:0]datain;
reg[15:0]dataout;
reg [15:0]memory16[0:4095];
initial
begin
memory16[0]=16'h7800;
memory16[1]=16'h1006;
memory16[2]=16'h4004;
memory16[3]=16'h7001;
memory16[4]=16'h0007;
memory16[5]=16'h4003;
memory16[6]=16'hC1A5;
memory16[7]=16'h93C6;
end
always@(posedge CLK)
begin
if (W==1)begin
memory16 [address]=datain;
end
else if (R==1)begin
dataout=memory16 [address];
end
end
endmodule
```

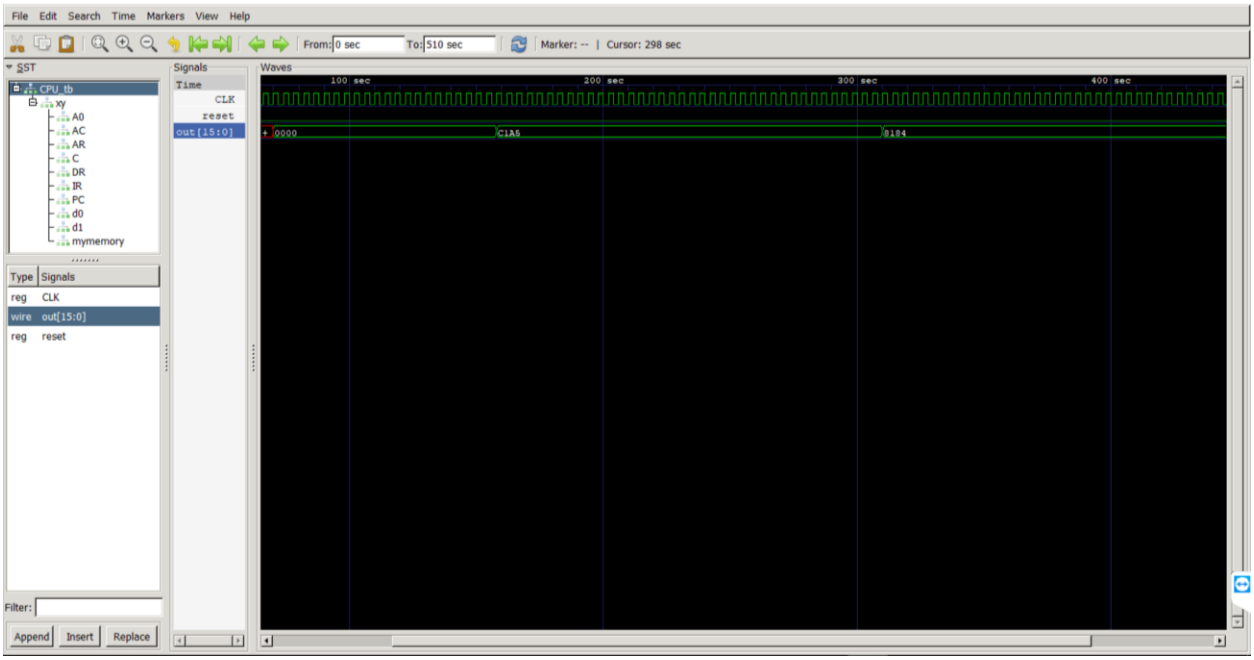
```
mem[0]=7800
mem[1]=1006
mem[2]=4004
mem[3]=7001
mem[4]=0007
mem[5]=4003
mem[6]=c1a5
mem[7]=93c6
```

b. Assert the reset signal for at least one cycle, and then negate it back. This action should clear the PC and begin fetching the first instruction.

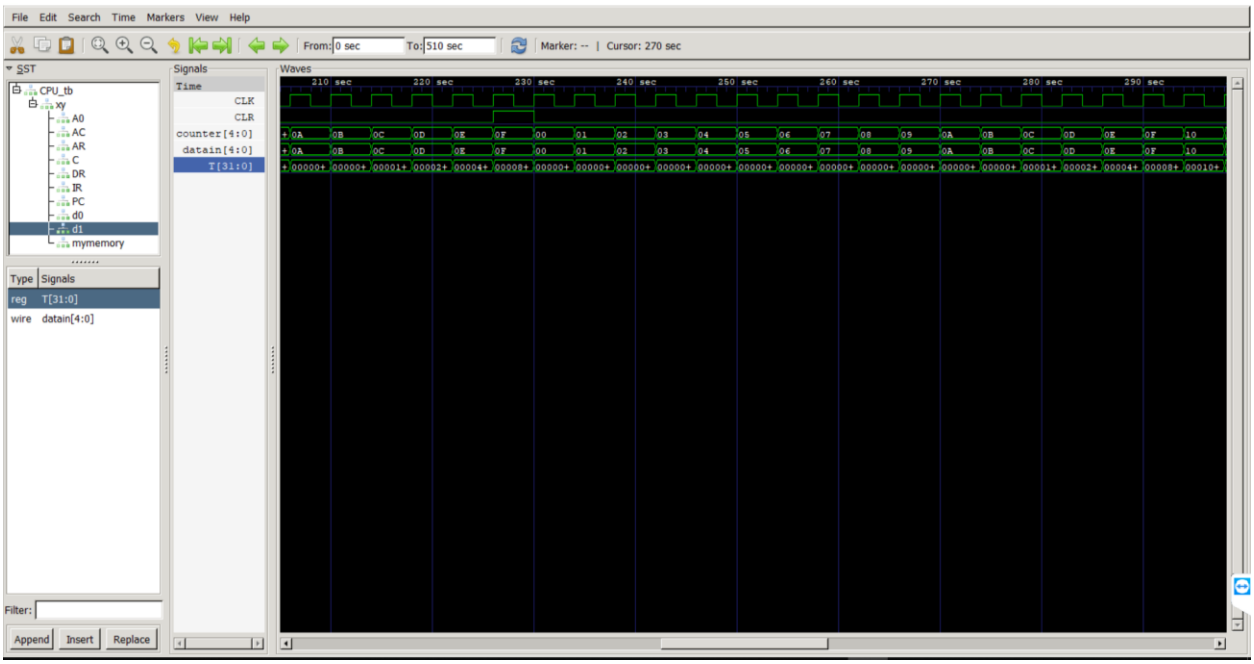


Output of the executed program

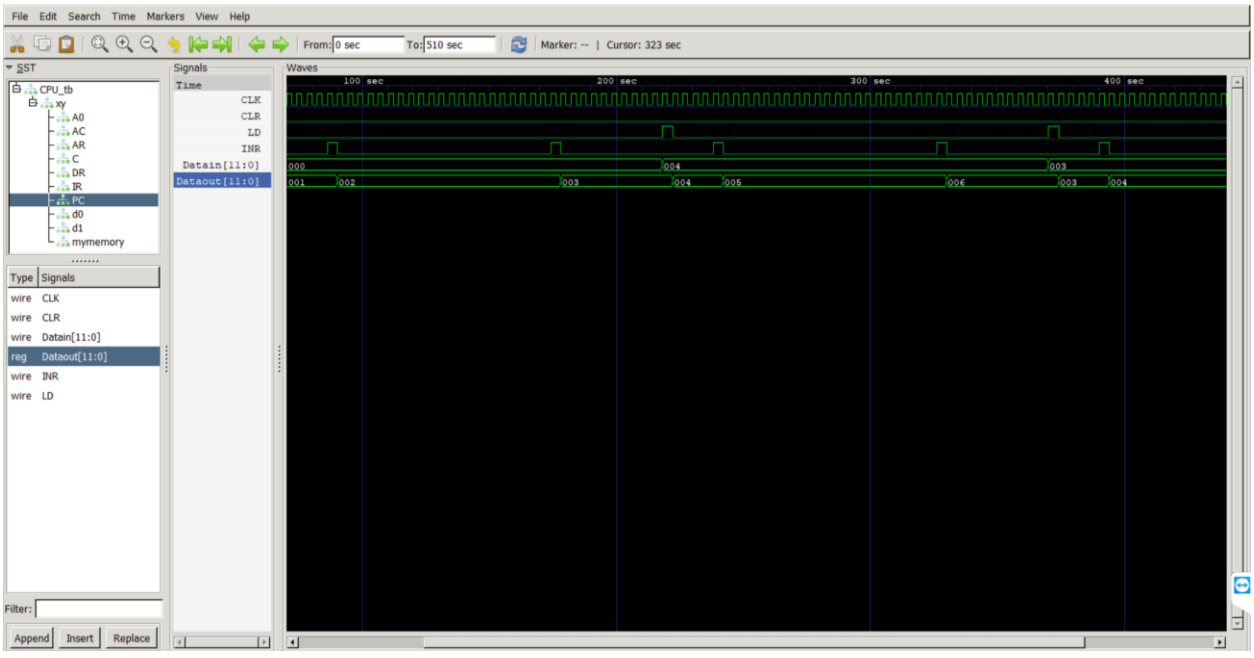
Module CPU



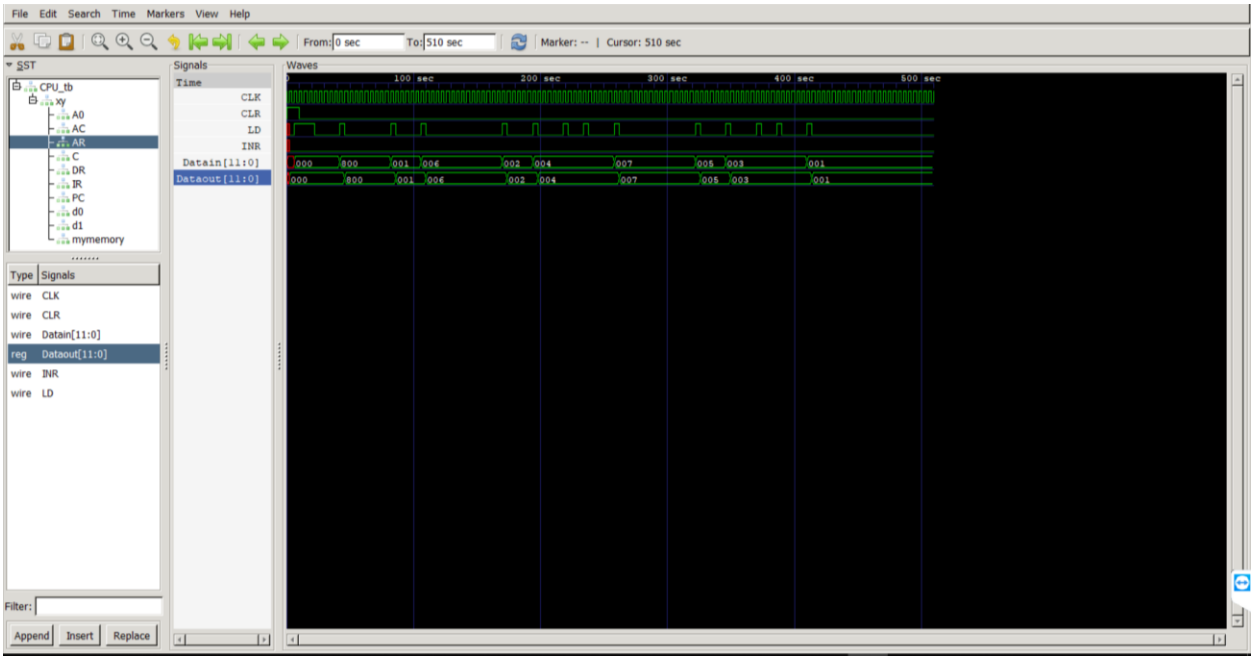
Module Sequencer



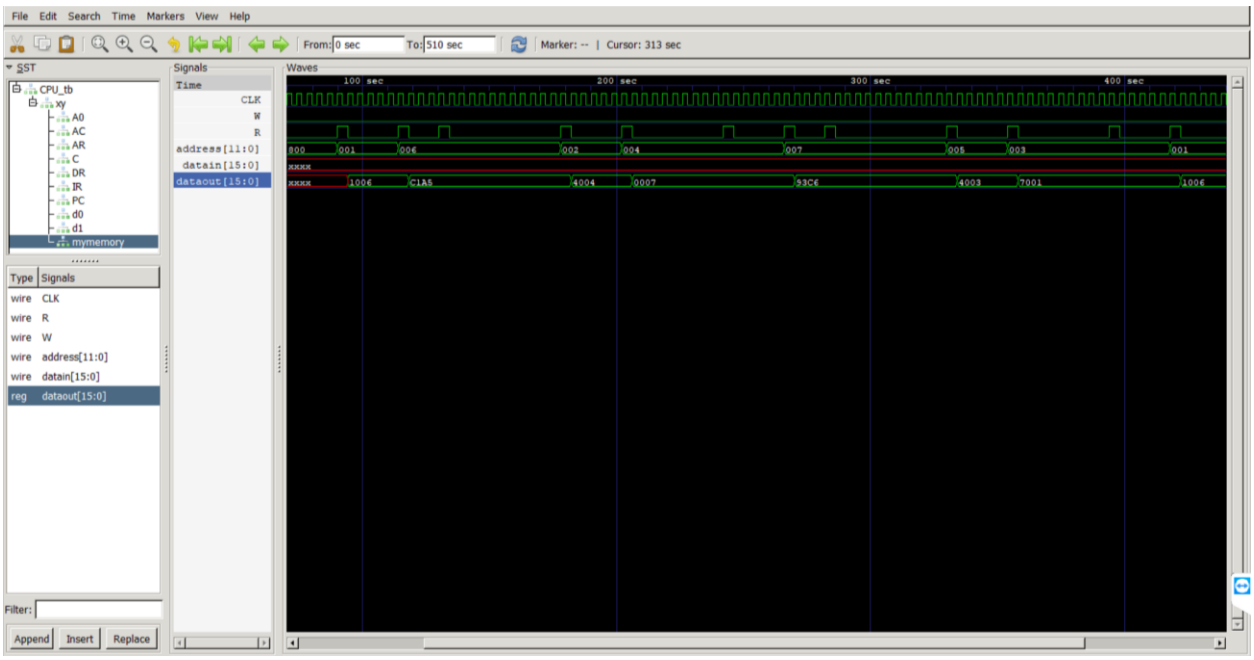
Module PC



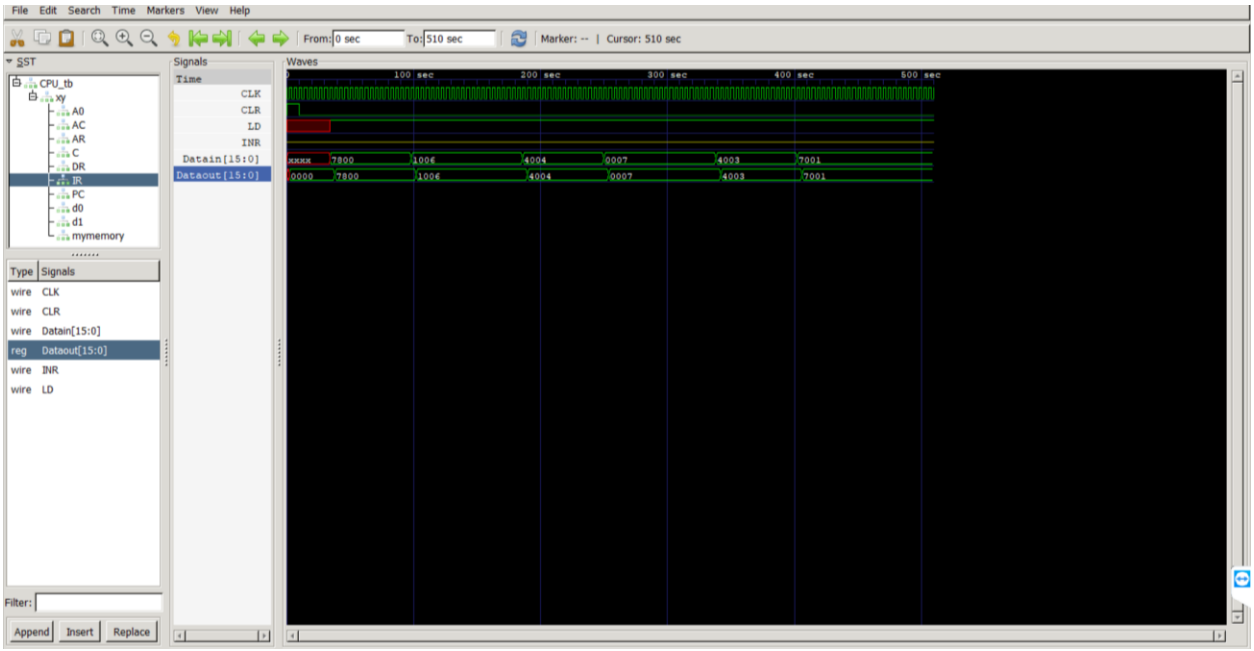
Module AR



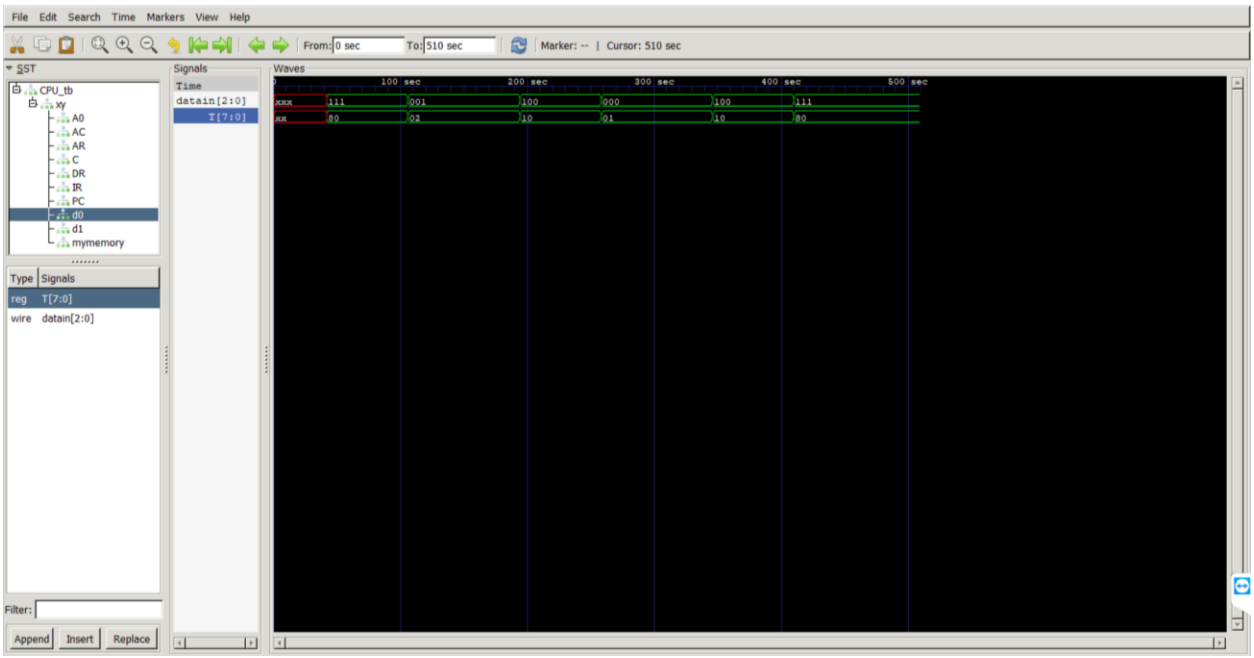
Module memory



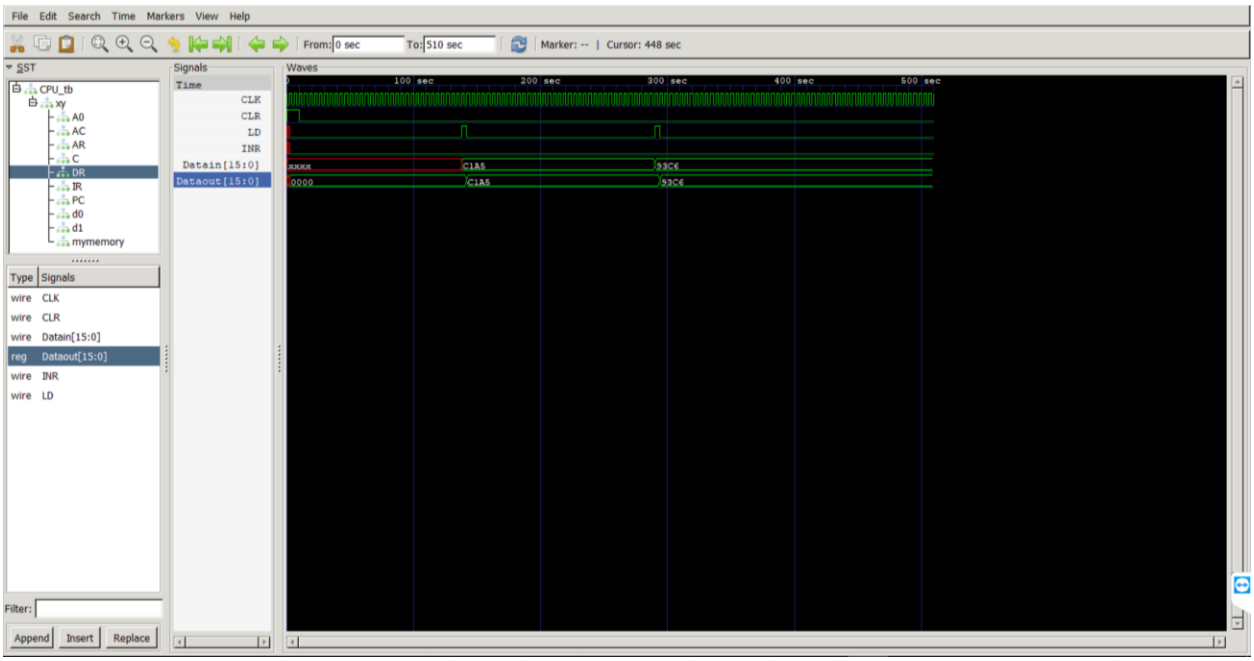
Module IR



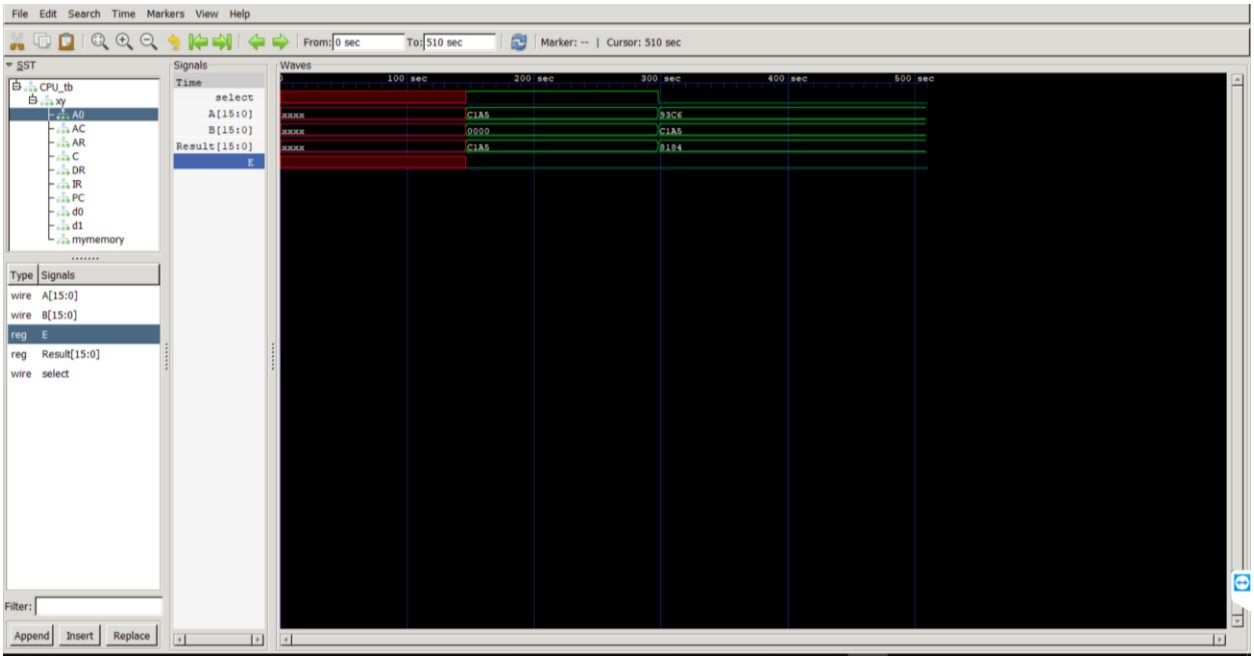
Module decoder (for opcode)



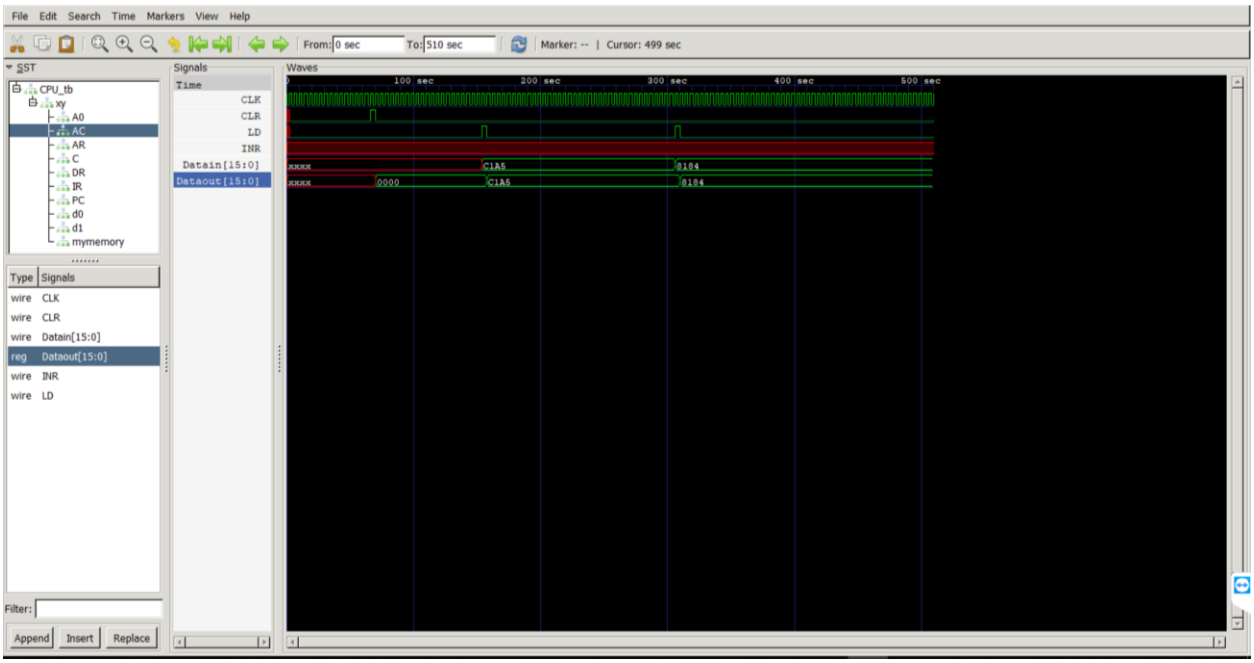
Module DR



Module Alu



Module AC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From: 0 sec
To: 510 sec
Marker: -- | Cursor: 499 sec
SST
CPU_tb
xy
A0
AC
AR
C
DR
IR
PC
d0
d1
mymemory
Type Signals
wire CLK
wire CLR
wire Datain[15:0]
reg Dataout[15:0]
wire INR
wire LD
Filter:
Append
Insert
Replace
Signals
Time
CLK
CLR
LD
INR
Datain[15:0]
Dataout[15:0]
Waves
100 sec
200 sec
300 sec
400 sec
500 sec
xxxx
C1A5
0184
xxxx
0000
C1A5
0184