
# Faculty of Engineering

# AIN SHAMS UNIVERSITY

Third year mechatronics engineering

Computer Organization

Third part of the project

## The implementation details of the design

**Represented by:**

| | |
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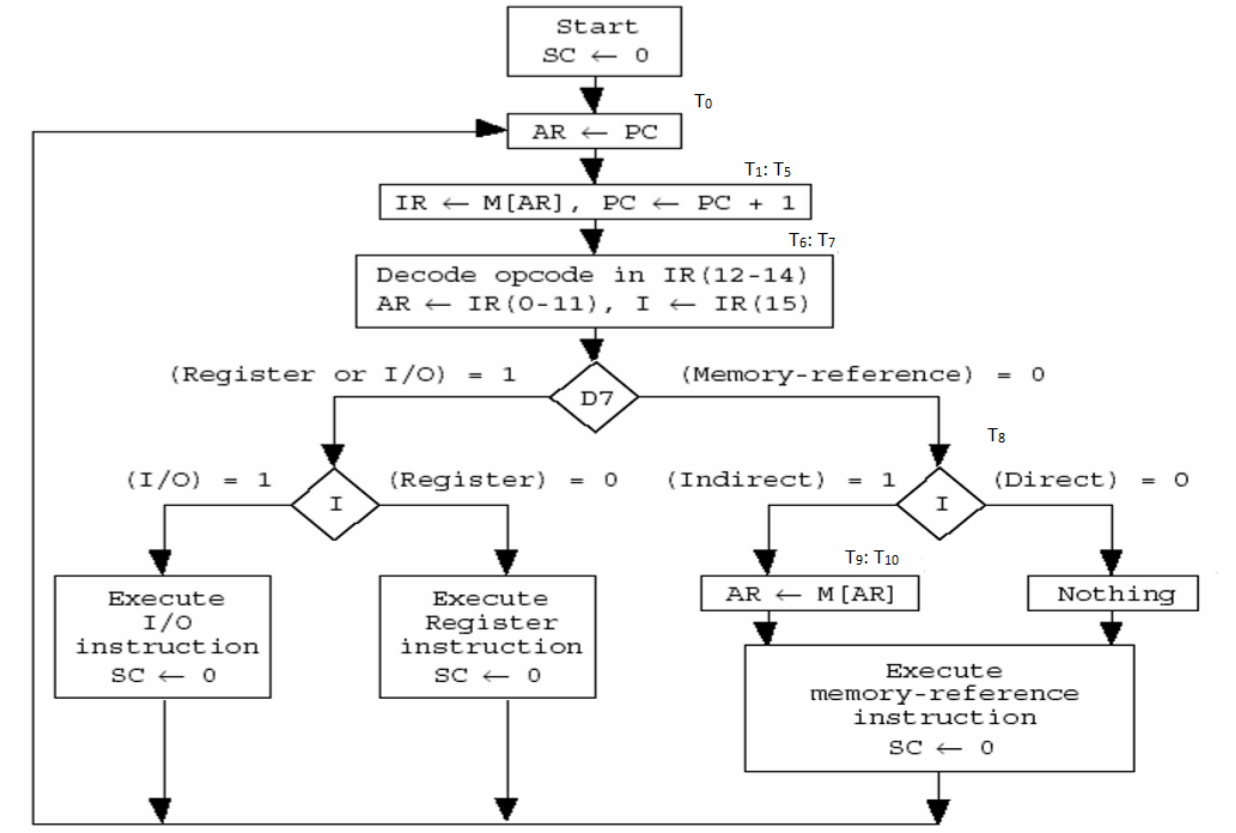
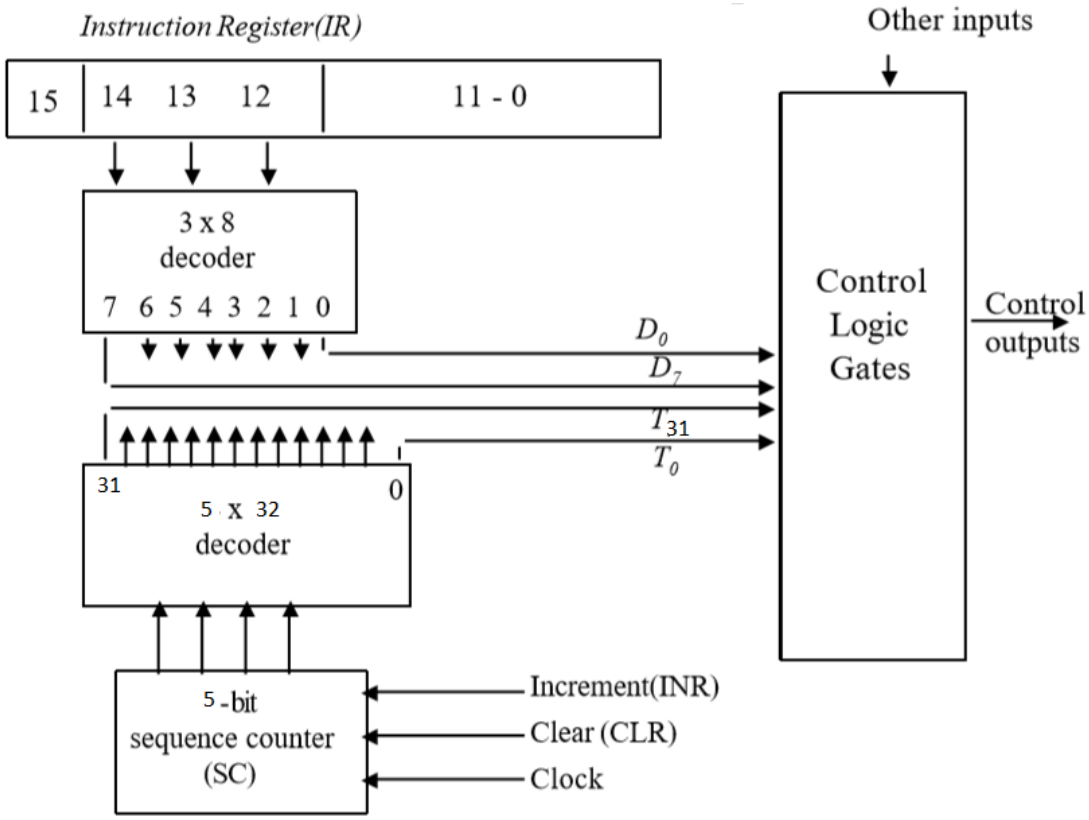
# The sequence of the code




The diagram above shows the program sequence in CPU from fetching the instruction , decoding it and getting the effective address

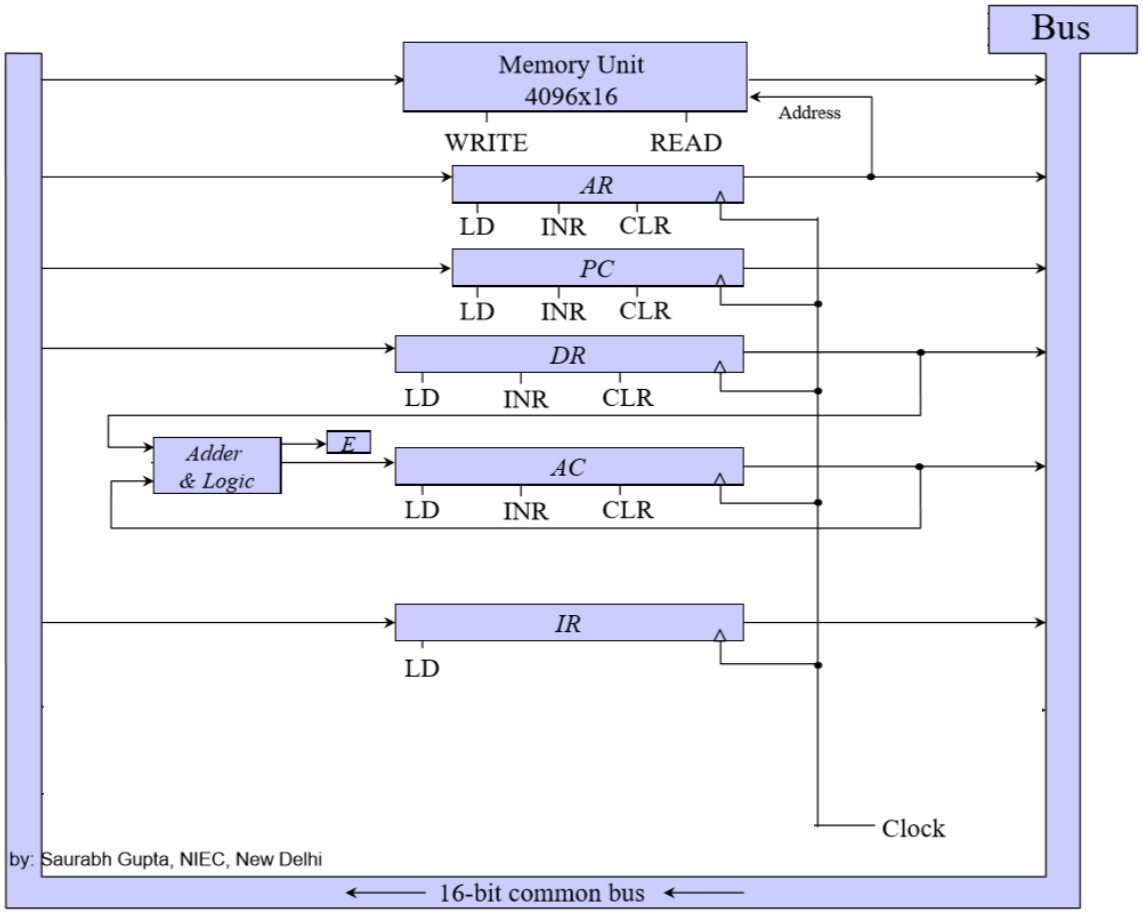
# The sequencer &decoder (for opcode) modules




The sequencer module function is to organize the timing of the microoperations of the CPU from fetching ,decoding and execution.

The decoder module (for opcode) is used to determine which instruction is given from memory , register or input output instruction to instruction register.

# The path of the data in CPU

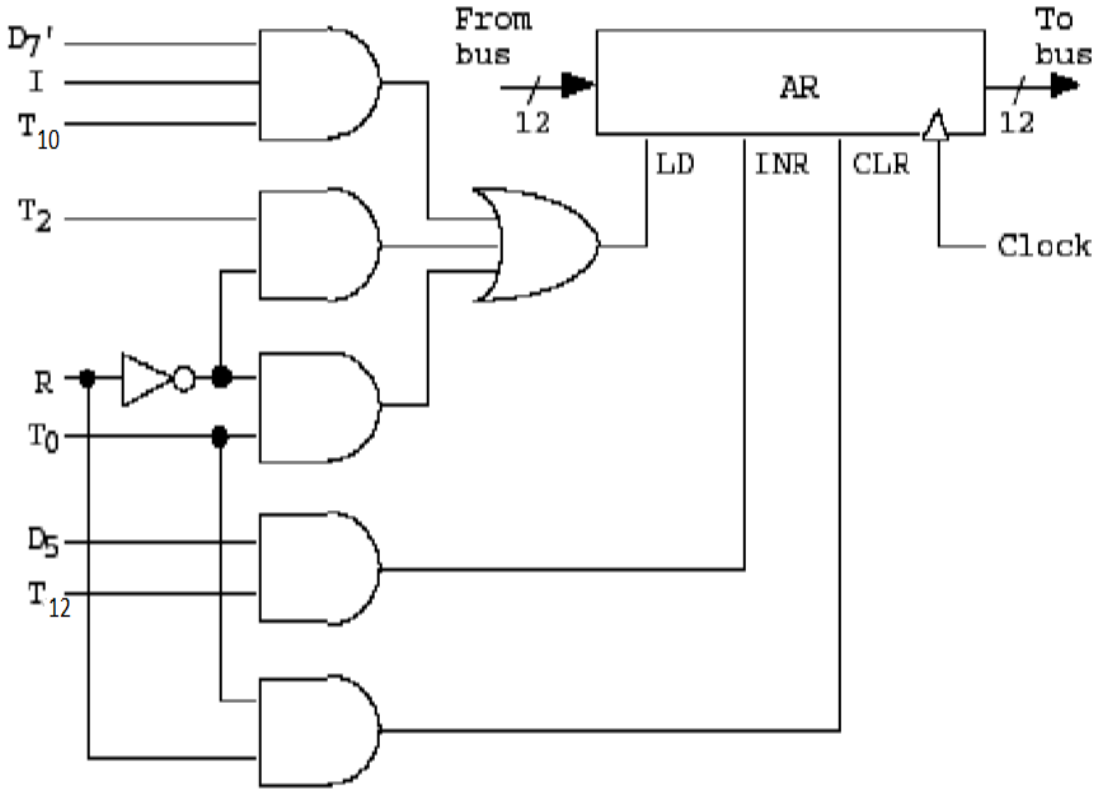



The diagram above shows the path of data in CPU between registers ,ALU and memory .It starts as address move from PC to AR to memory address  then memory get the instruction to IR then from IR to AR , opcode and I-bit to determine type of instruction

*if it is memory instruction , we get the effective address of operand to execute the instruction, the output passes from ALU(if it is and or add only) to DR and finally to AC

*if it is register instruction , the instruction  executed depends on the least significant bits [0:11]

# The AR module



# The AC module