UNIVERSITY OF TEXAS AT DALLAS

Analog Integrated Circuit Design – EECT 6326

Term Project: Design of a High-Gain, High-Speed Op-Amp

By:

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1) Introduction:

In Analog circuit design, Operational Amplifier (Op-Amp) is one of the most important and basic building block. It has applications in both analog as well as digital IC design such as an amplifier, Active filters, as a comparator in ADCs etc.

In this project a two stage Op-Amp with a high gain and speed has been designed, simulated and analyzed in Cadence Virtuoso. For achieving a high gain and low power consumption, the **telescopic cascode topology** has been used in first stage (Differential Input Single Output (DISO) Amplifier) to increase the overall output impedance and hence the overall gain. With this a gain of approximately 77 dB is achieved.

For biasing the circuit a high swing cascode current mirror has been used with the help of 100uA master current source given (for generating a constant tail current) for getting the best possible accuracy in the current mirror. And to bias the first stage cascode and for biasing the 2^{nd} stage current source MOSFET again a current mirror is used which is designed with help of same 100uA master current source.

The designed Op-amp is being used in switched capacitor pipeline Analog to Digital Convertor (ADC).

2) Organization of the Report:

In the report first, some key design decisions and topics has been briefly discussed. After that in part 3 the calculation of some key design parameters has been done. Part 4 the schematic and tables containing key design specifications has be demonstrated. Part 5 Discussed about the plots obtained from the simulation and has been analyzed and then final conclusion about the design has been made in part 6.

3) Derivation of Key Design Parameters:

Since output voltage swings from 0.25 V to 2.25 V, hence the overdrive of the transistors is taken to be less than 0.25 V.

A tail current of 10uA is being taken for low power consumption. And hence the initial guess for the width of every transistors has been made using the following equation:

$$I = \frac{1}{2} k \frac{W}{L} V_{ov}^2$$

Thus, the width can be calculated as follows:

$$W = \frac{2IL}{kV_{ov}^2}$$

Taking L to be 0.35um the initial guess of width of each transistor is calculated and is tabulated in table 2.

3.1) How to achieve high gain?

To achieve a sufficiently high gain for the Op-amp, single stage is not enough even if we increase its gain by using cascode structure for the differential stage. Hence one more gain stage is added and one of the best choice for this purpose is a Common Source (CS) Amplifier. Note that cascode stage leads to poor output swing and for this purpose also (of having better output swing) we need one more stage.

3.2) Problem with multistage Amplifier and its Solution:

Adding more stages to achieve more gain comes with a price of stability issue of the overall system.

To overcome the stability issue Miller Compensation technique has been utilized. The Miller compensation technique introduces RHP zero which affects the Phase Margin of the overall system and hence stability.

To get through the problem of having a RHP zero, a zero nulling Resistance (Rz) in series with the Miller Capacitance (Cc) can be used which effectively cancels the zero by creating a pole at the location of RHP zero.

The value of Rz is approximately given by:

$$R_z = \frac{(C_L + C_c)}{g_{mo} C_c}$$

Where g_{mo} is the trans-conductance of the output stage transistor (here it is M10).

3.3) Calculation of Small Signal Gain:

The gain of the first stage of the Op-amp is given by the following:

$$A_{v1} = g_{m6}[(g_{m7}r_{07}r_{08})||(g_{m4}r_{04}r_{03})] = \mathbf{600.81}$$

And the gain of 2nd stage is given by:

$$A_{v2} = g_{m10}(r_{010}||r_{09}) = \mathbf{11.72}$$

Hence the total gain,

$$A_v = A_{v1} * A_{v2} = 7041.5 = \mathbf{77}\boldsymbol{dB}$$

The output resistance of the Op-amp:

R_{out} = $r_{010}||r_{09}$ = **50.55 kΩ**

4) Schematics and Tabulation of the Results:

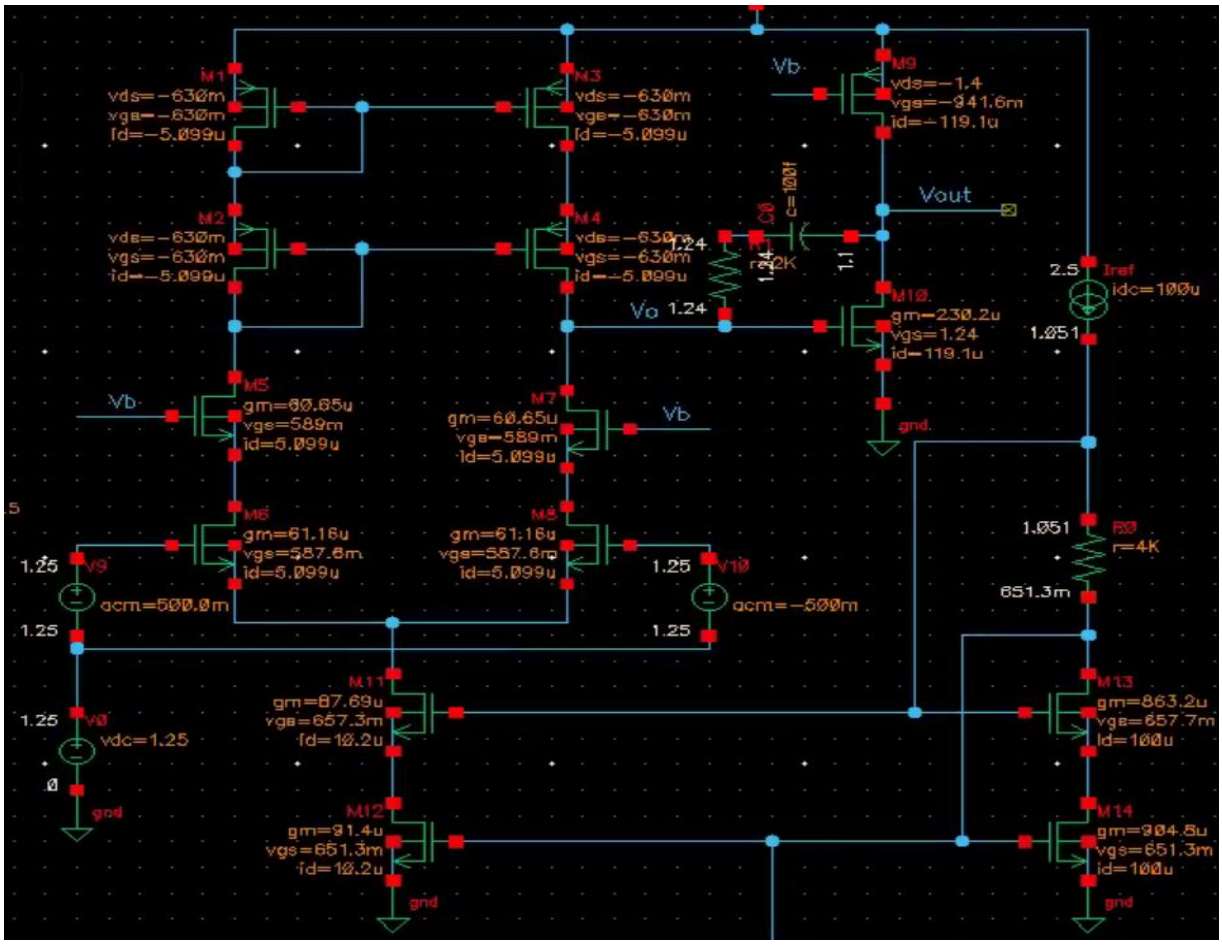

Figure 1: Schematic of two stage telescopic Op-amp without biasing circuit

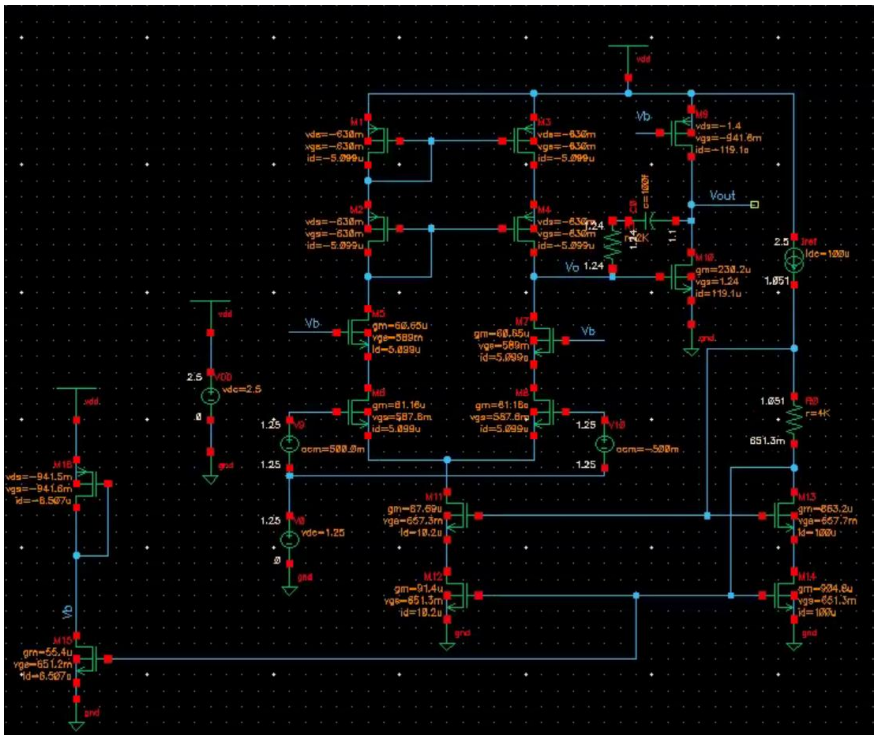

Figure 2: Full schematic of two stage telescopic Op-amp with biasing circuit

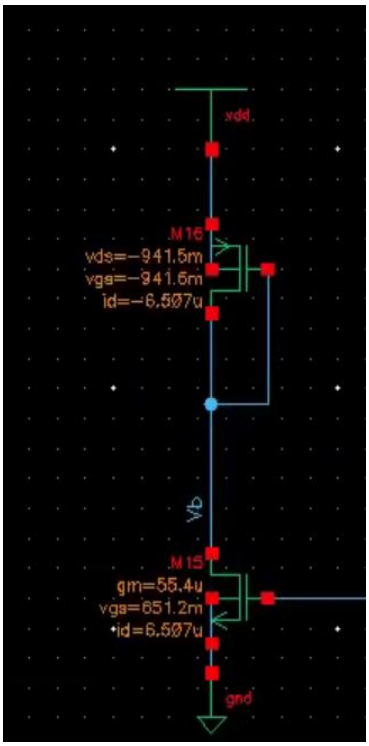

Figure 3: Biasing circuit

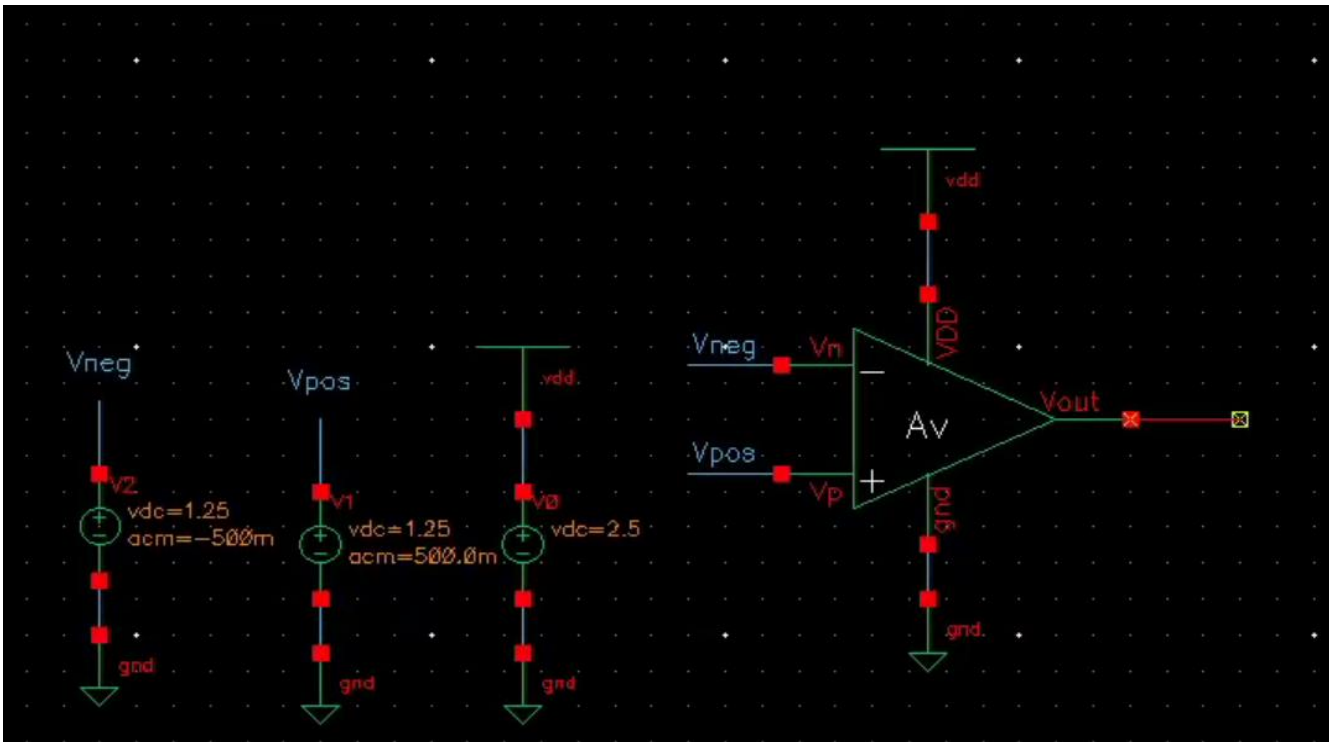

Figure 4: Test bench for measuring open loop parameters of the Op-amp

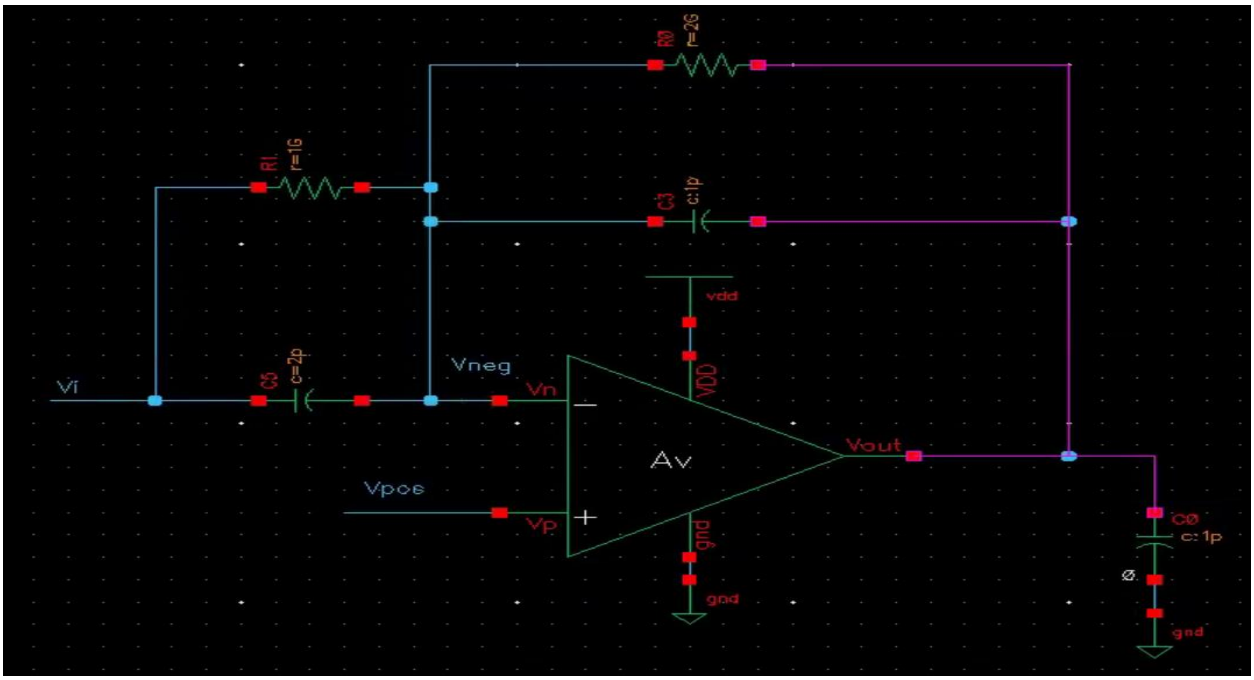

Figure 5: Test bench for measuring closed loop parameters of the Op-amp

Table 1: Showing important design specifications

Design Parameters	Target value	Achieved Value
Closed-loop gain	2X	2.099X
Input voltage range (peak-peak)	1V	1V
Output voltage range (peak-peak)	2V	2.099V
Supply voltage	2.5V	2.5V
Load capacitance	1pF	1pF
Settling error	-75 dB	-21dB
Settling time (Vo rising)	20 ns	87ns
Settling time (Vo falling)	20 ns	98ns
Operating temperature	0-77 ^{o}C	0-77 ^{o}C
Power consumption	N/A	I_Q=129.3uA, V_{dd} = 2.5 V P= I_Q*V_{dd} = 2.5u*129 = 0.3232 mW

Table 2: Dimensions and parameters of the transistors

Transistor(s)	Id (uA)	Gm (m/Ω)	gm/Id (1/mV)	Vov (mV)	W(um) (L = 0.35um)
$M_{1,2,3,4}$	5.112	69.44	13.58	113.3	5
$M_{5,7}$	5.112	60.74	11.88	129.9	1
$M_{6,8}$	5.112	42.97	8.406	150.5	1
M_9	119.1	516.5	4.337	331	10
M_{10}	119.1	230.2	1.933	494.8	1
M_{11}	10.22	92.63	9.06	168.1	1
M_{12}	10.22	91.66	8.965	169.5	1
M_{13}	100	863.2	8.632	180	10
M_{14}	100	904.8	9.048	175.6	10
M_{15}	6.5	55.4	8.514	164.8	0.5
M_{16}	6.5	25.57	3.39	346.1	0.5

Table 3: Compensation capacitor and nulling resistance

Rz	50kΩ
Cc	100fF

5) Simulation Results:

The output waveform of the Op-amp for rising output and falling output has been plotted for different temperatures (0 ^{o}C, 25 ^{o}C and 75 ^{o}C) in figure 6 and 7. It can be seen from the plots that the output is not varying much with temperature and hence confirms the robustness of the Op-amp.

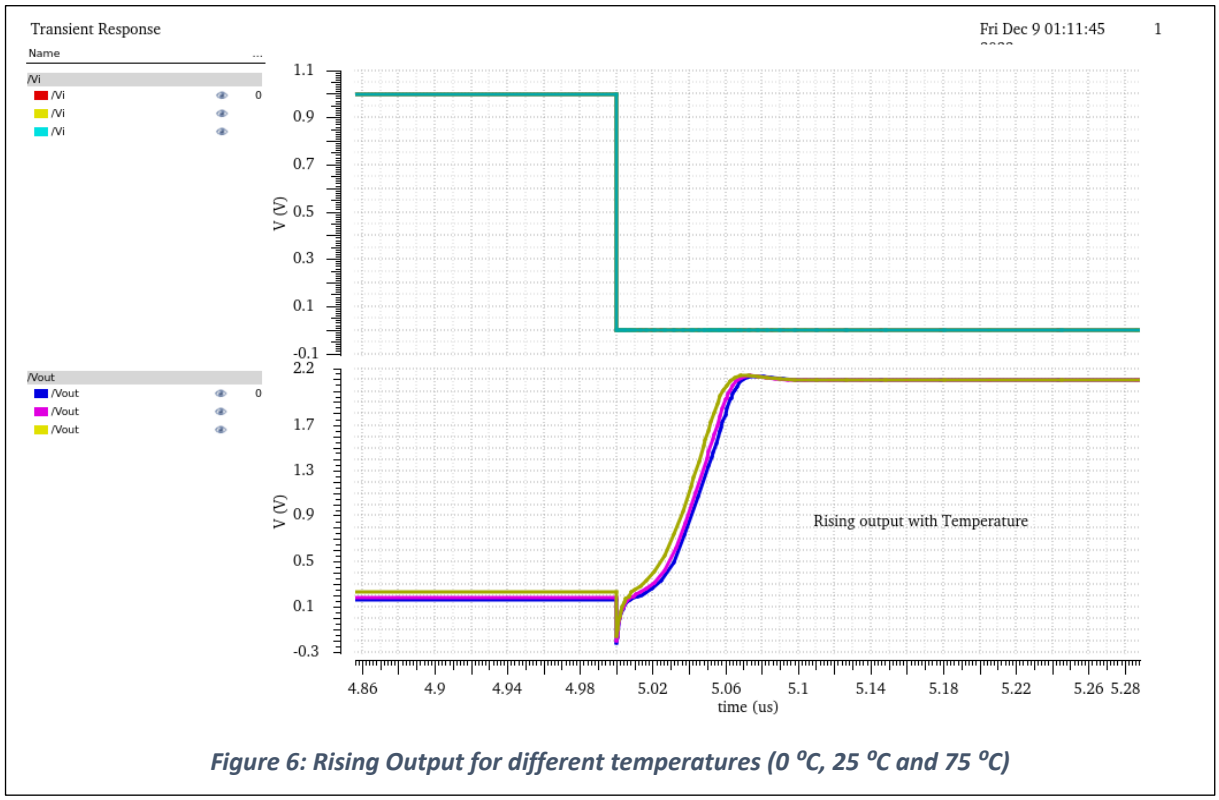

Figure 6: Rising Output for different temperatures (0 ^{o}C, 25 ^{o}C and 75 ^{o}C)

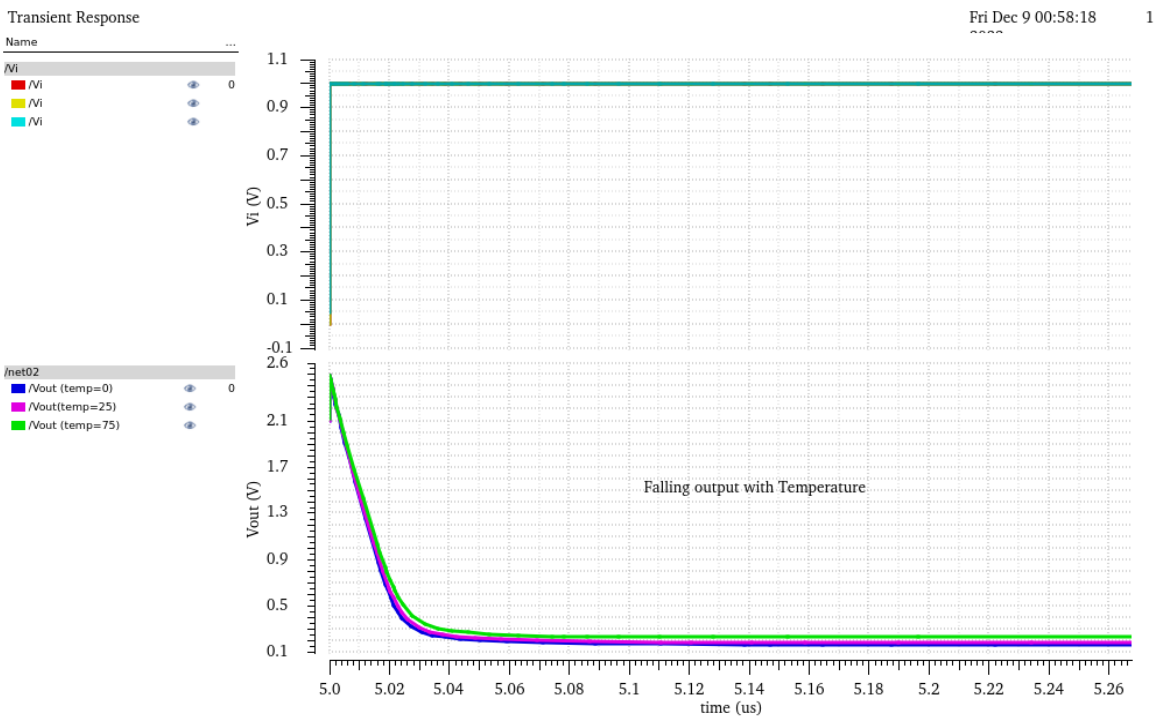

Figure 7: Falling Output for Different temperatures (0 ^{o}C, 25 ^{o}C and 75 ^{o}C)

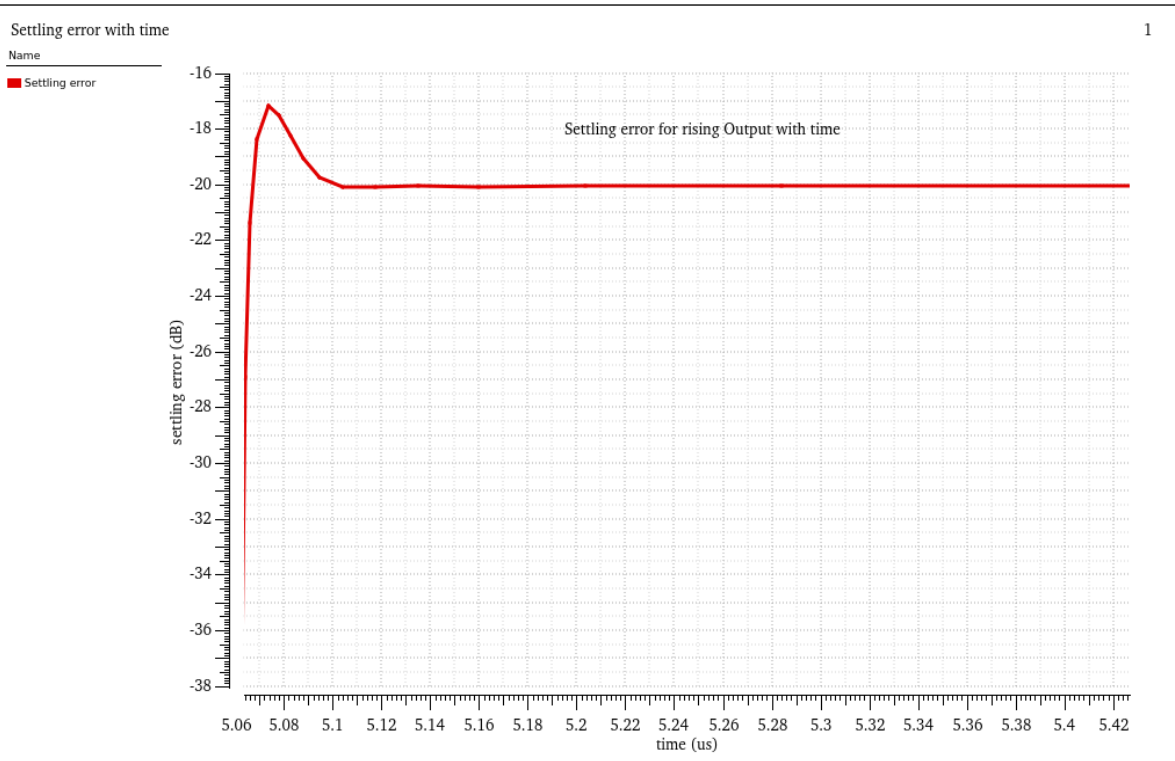

Figure 8: Settling error of the Op-amp with falling input

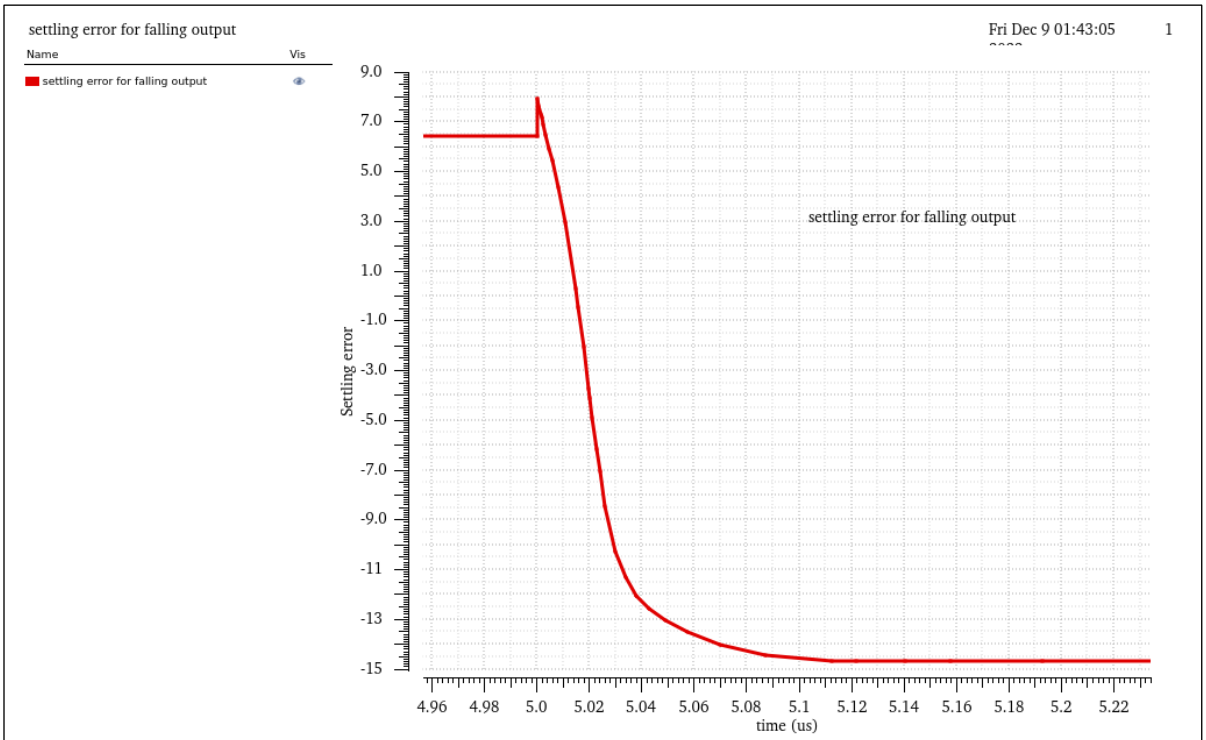

Figure 9: Settling error of the Op-amp with rising input

The figure 10 shows the open loop gain of the Un-Compensated Op-amp. As can be observed from the plot that the DC gain (low frequency gain) is **77.166 dB** but the Phase Margin (PM) is very poor = **-5.3^{o}** which makes it unstable.

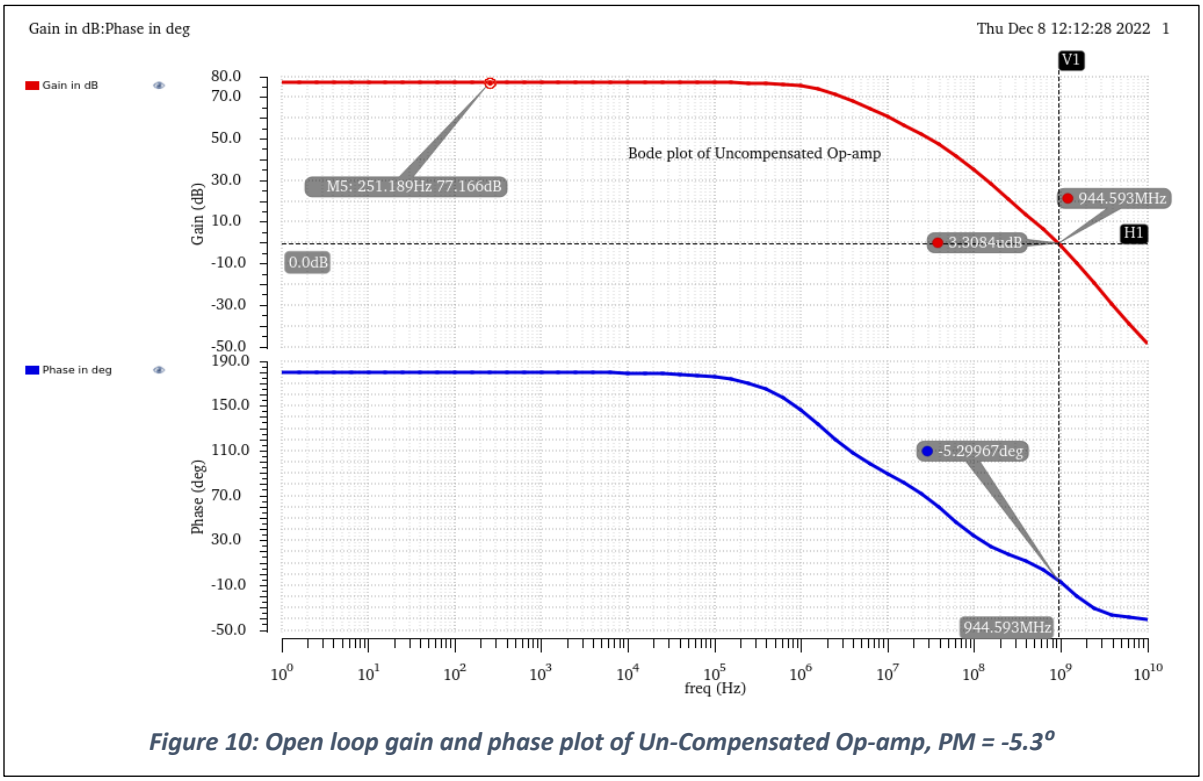

Figure 10: Open loop gain and phase plot of Un-Compensated Op-amp, PM = -5.3^{o}

As shown in figure 11 the open loop gain DC of the Compensated Op-amp (low frequency gain) is **77.166 dB** but Now after the miller compensation the Phase Margin (PM) become = **70.8^{o}** which makes it stable. Also the open loop 3dB bandwidth of the Op-amp is = **11.85 KHz** and the open loop Unity Gain Bandwidth (UGB) of the Op-amp = **89.625 MHz**

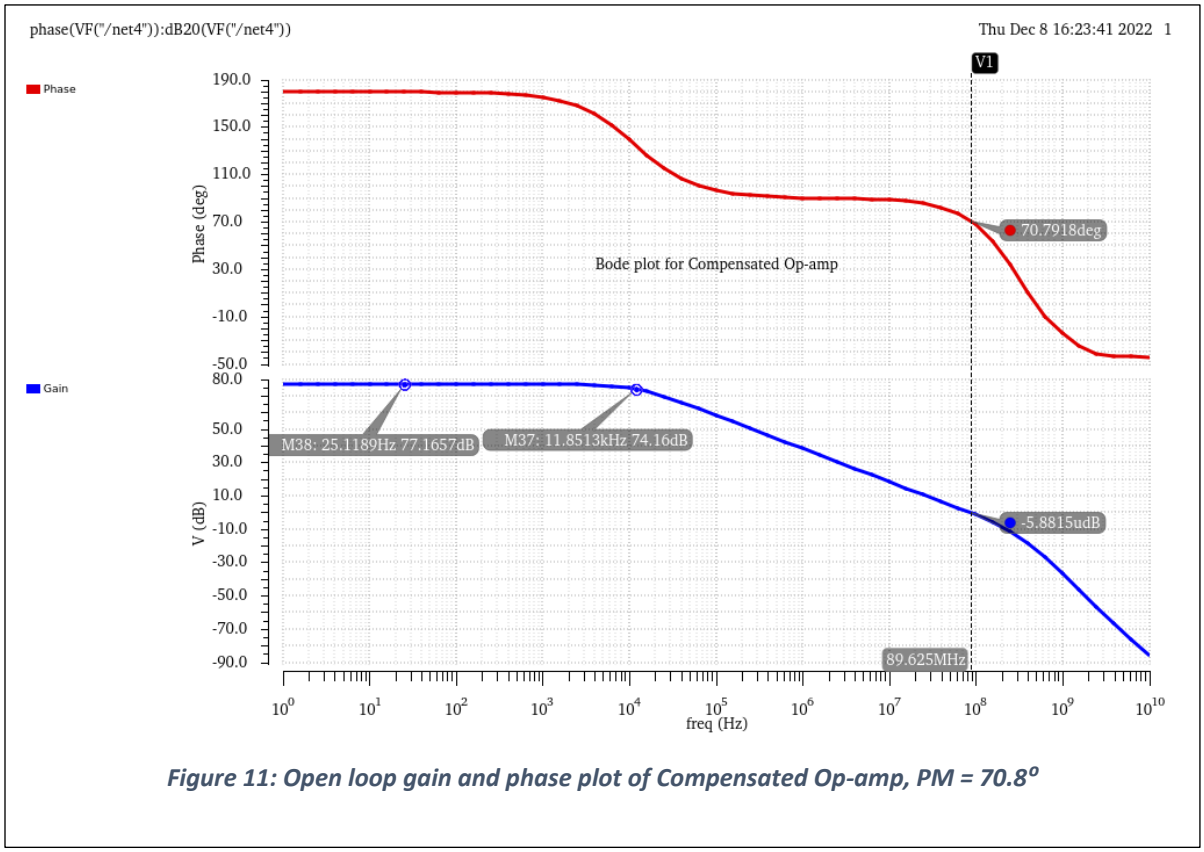

Figure 11: Open loop gain and phase plot of Compensated Op-amp, PM = 70.8^{o}

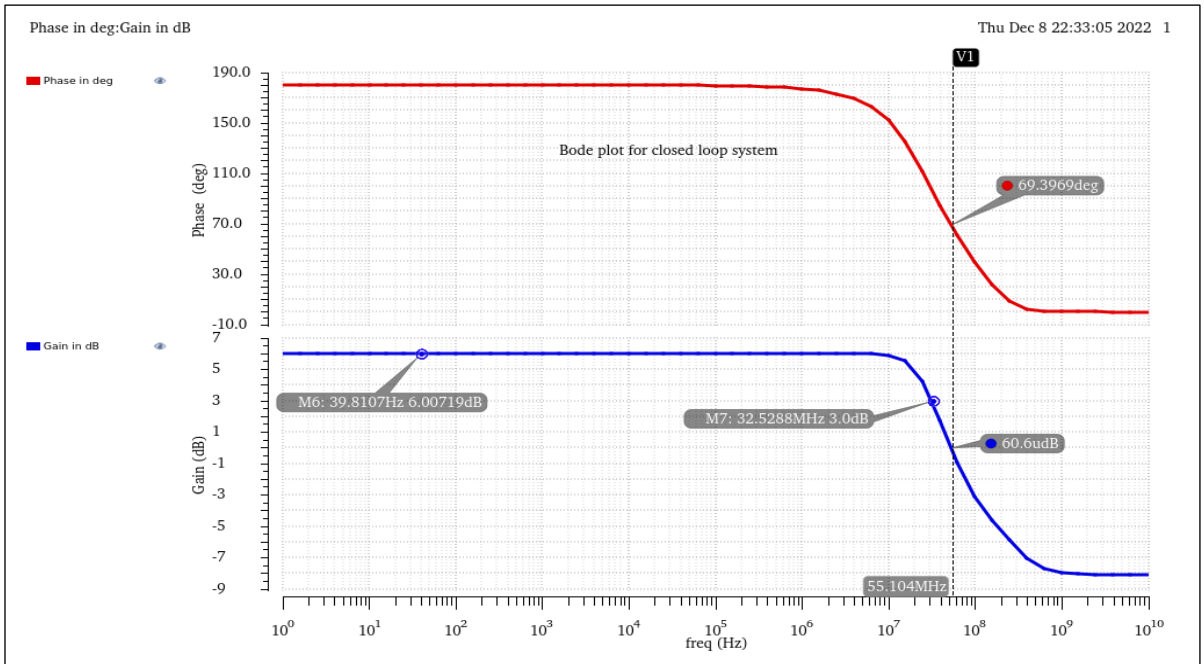

Figure 12: Closed loop gain and phase plot of Compensated Op-amp, PM = 70.8^{o}

As shown in figure 12 the closed loop gain of the Op-amp is approximately **6 dB** which is equivalent to a value of gain **2**. And the Phase Margin (PM) is = **69.4^{o}** which makes it stable. Also the closed loop 3dB bandwidth of the Op-amp is = **32.53 KHz**.

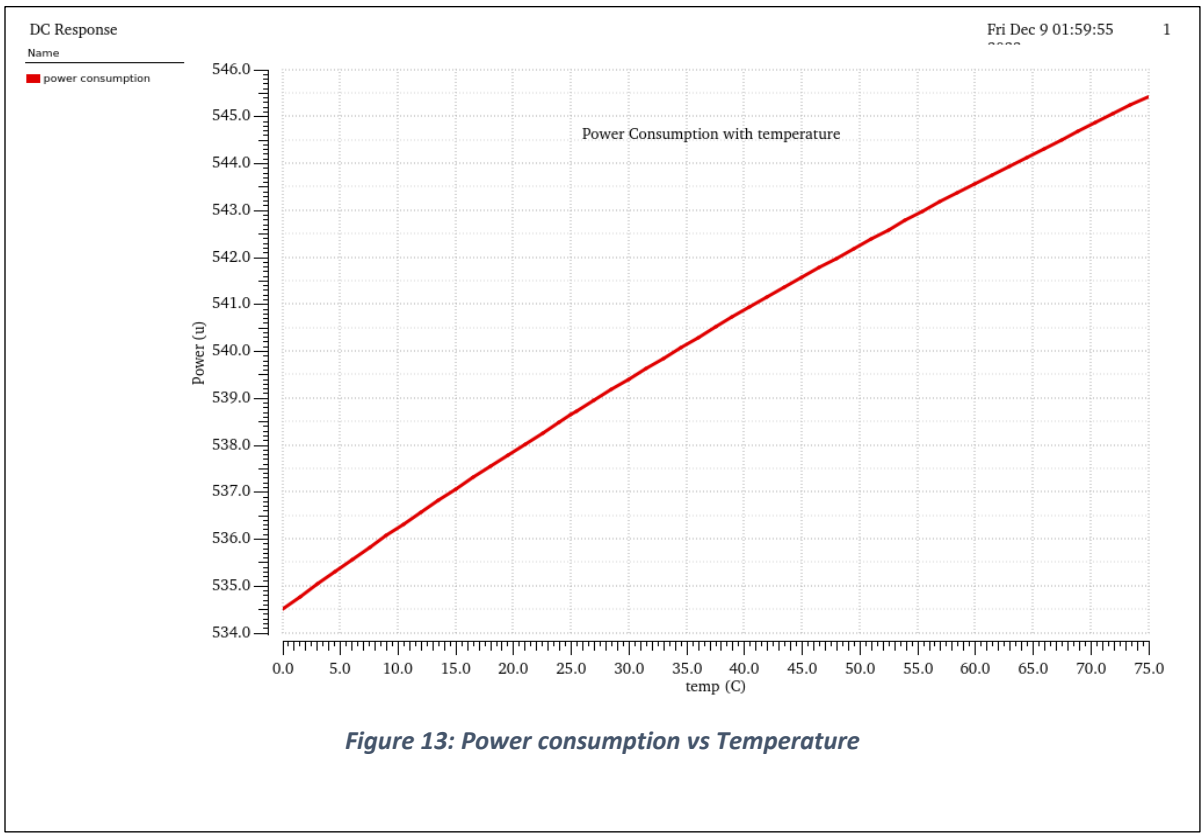

Figure 13: Power consumption vs Temperature

6) Conclusion:

In this project a very high gain (>77dB) two stage telescopic Operational Amplifier with a reasonable fast response has been simulated and analyzed in Cadence virtuoso. The robustness of the Op-amp has also been checked in terms of variation of output voltage with wide range of temperature (0-75^{o}C). Also the power consumption of the Op-amp is also kept within the reasonable limit.