SINGLE-ENDED 10T SRAM CELL WITH IMPROVED STABILITY

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***Abstract*—** A Single- ended 10 transistor SRAM cell with improved stability is proposed . This cell uses a Schmitt Trigger (ST) inverter to improve read ability of the cell. The single ended term means that the cell uses such feature to reduce the power during switching. The simulation is done on a 180 nanometer Cadence technology. The cell gives 1.40 times more read static noise margin than the 6 transistor SRAM cell. During the write zero operation, the cell gives 312 millivolt of WSNM at 0.7 volt. For read operation, the cell provides 3.29 times low power during switching as compared to existing cell.

Keywords- SRAM- Static random access memory, ST- Schmitt Trigger, RSNM- Read static noise margin, WSNM- Write static noise margin.

1. INTRODUCTION

CMOS technology has enabled the semiconductor industry to meet its ever-increasing demand for computation speed and integration density. However, in nanometer-scale geometry, VLSI circuit and system design has many challenges.

2. EXISTING SYSTEM

6 transistor SRAM cell has a simple design but has a problem of data disturbance is along with it. For example, suppose 6T cell has Q= 1 , then QB = 0.

If voltage (at QB) is equal to the threshold voltage of the inverters M1 and M2, transistor M2 is turned ON and the cell losses its content.

The above problem is called as data disturbance.

Thus, the existing 6T cell suffers from read disturbance problem based on the circuit design and it can be overcomed by the proposed 10T SRAM cell.

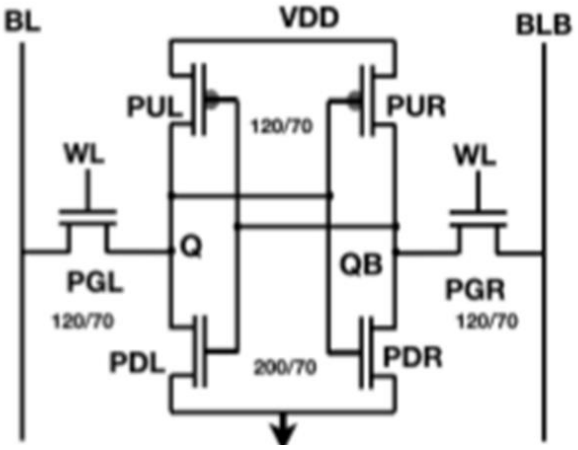

Figure 1 Conventional 6T SRAM Cell

IN1	IN2	OUT
0	0	0
0	1	0
1	0	1
1	1	1

Figure 2 Existing system truth table

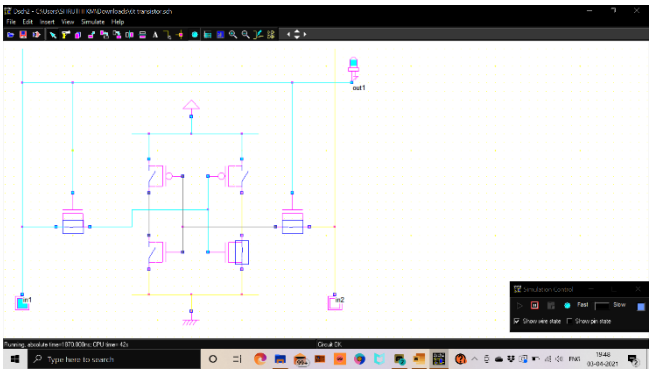

Figure 3 DSCH circuit of 6T SRAM Cell

The above diagram shows the diagram of 6T SRAM cell Using DSCH (Digital Schematic) software. The circuit has two inputs and one output. The output can be either a read or a write.

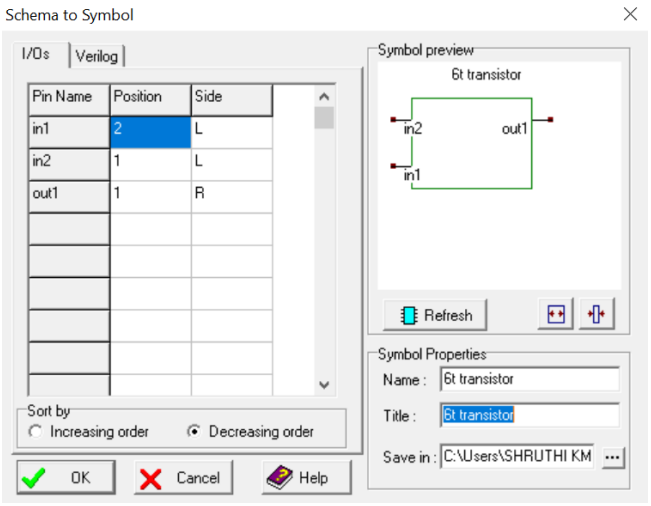

Figure 4 DSCH schema to symbol of 6T SRAM Cell

The above figure gives the schematic of 6T SRAM Cell. It has two inputs and one output.

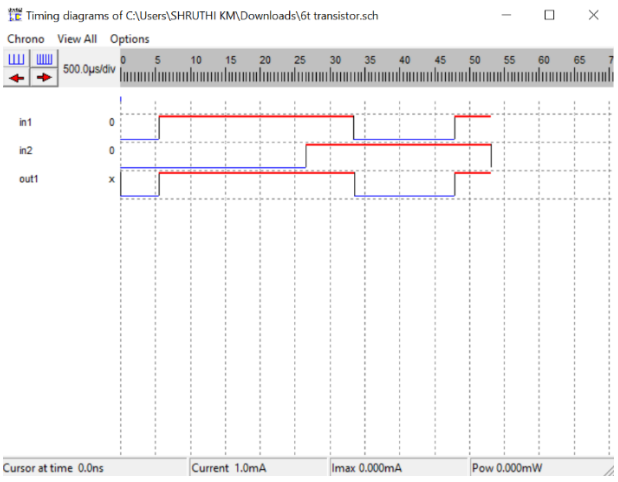

Figure 5 DSCH Timing diagram of 6T SRAM Cell

For different inputs given to the circuit, we get a DSCH Timing diagram which gives the output for the inputs applied.

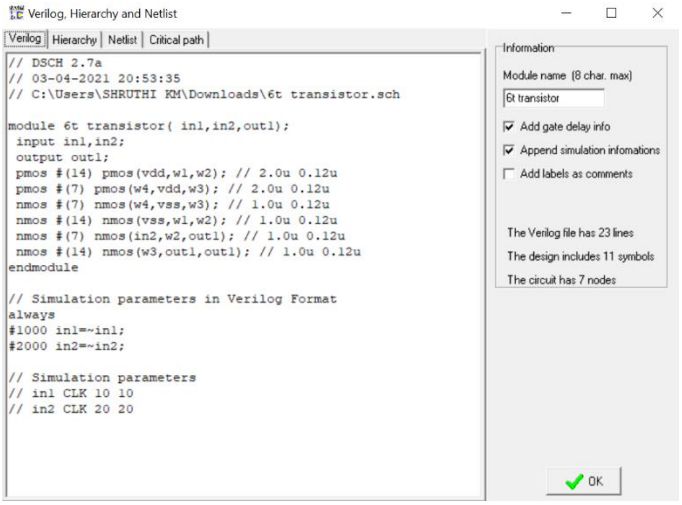

Figure 6 Verilog Code of 6T SRAM Cell

This is the Verilog Code for 6T SRAM cell generated from DSCH software. This code is used in the Microwind software to get the layout of the cell.

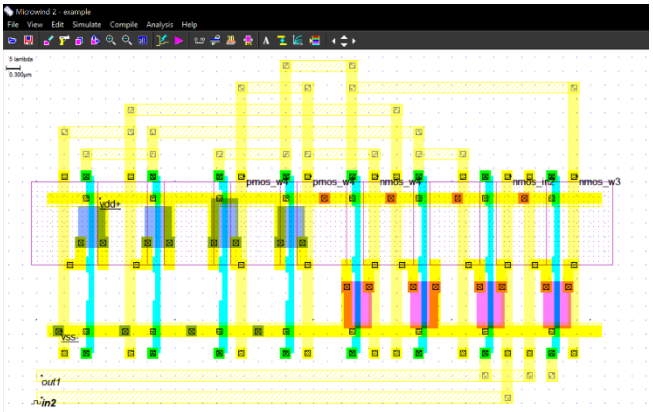

Figure 7 Microwind output for 6T SRAM Cell

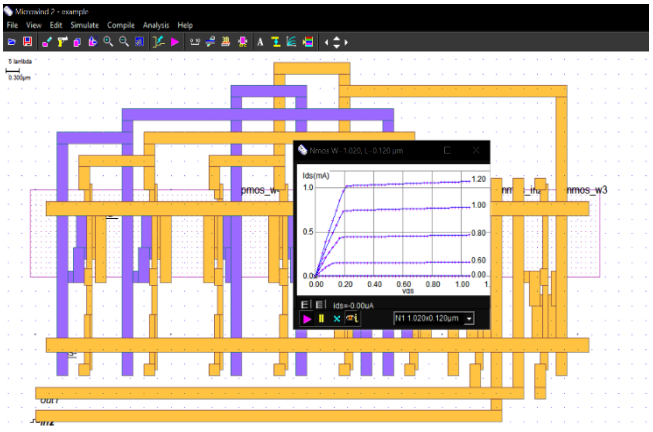

Figure 8 Microwind output with timing diagram for 6T SRAM cell

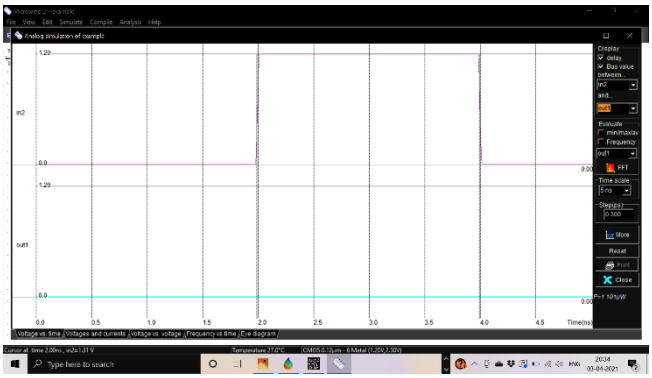

Figure 9 Microwind waveform for 6T SRAM cell

3. PROPOSED SYSTEM

- The cell is made of two Schmitt Trigger inverters. The word lines WWL and WL is used to control M7 and M8 transistors.
- RBL, which means Read bit line is used to read the content from the cell. WBL, which means write bit line which is used to write the content in the cell. The OR Gate in the Figure 10, controls transistor M10.
- From the Figure , One OR Gate is shared by each row of sram cell array.
- During read zero operation, the potential of M9 is raised through PQB node.
- Figure 11 gives the truth table of the 10T SRAM cell.
- Transistor M10 switches ON and the source terminal of M3 is connected to ground.
- Under this situation, Q node is discharged to Word bit line through transistor M7 and to Read bit line through transistors M2 and M8.
- Charge eliminates at node Q, transistor M4 which is a PMOS transistor starts to conduct which tends to increase voltage at node QB .
- Now, node Q is set to logic ‘0’ while QB is set to logic ‘1’ which is a feedback action.
- To write a logic ‘1’ in the 10T cell, WBL is raised to VDD. As a result, transistor M10 is OFF which causes the inverter M1, M2 and M3 which are the left inverters, to float.
- Thus the charges from WBL accumulates at node Q. Due to high value of Q, transistors M5 and M6 starts to conduct which pushes QB to become lower.
- Due to feedback action which is internally present, the node Q gets logic 1 which is Q = 1 while QB becomes low QB = 0.
- When read operation takes place, Read bit line is pre charged to VDD. WR and CS gets logic 1. Due to this. Transistor M10 switches ON.
- Now, if Q= 0 and QB = 1 is present in the cell then Read bit line is discharged to ground through transistors M8,M3 and M10 connected through RBL.
- Suppose, if Q= ‘1’ and QB = ‘0’is present in the cell then Bit Line be at its pre charged level because transistor M3 is in OFF state.
- Thus, in the 10T cell, RBL is discharged to ground position conditionally
- M10 transistor remains switched ON in hold mode.

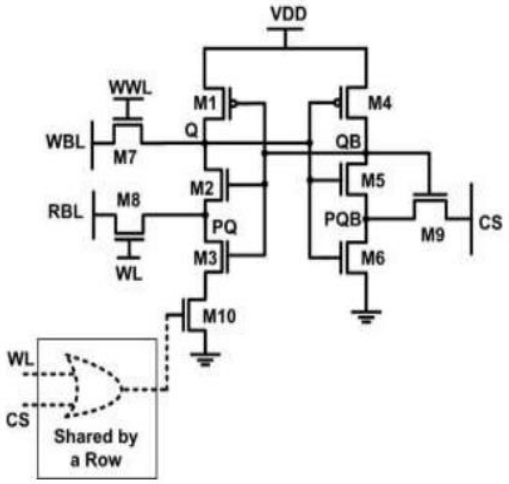

Figure 10 10T SRAM Cell

IN1	IN2	IN3	IN4	OUT1	OUT2
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	0
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	1	1	1
1	1	1	1	1	1

Figure 11 Truth table of 10T SRAM Cell

4. SOFTWARE REQUIREMENTS

Microwind is a tool used to design and get the simulated output at layout level.

DSCH is a software for logic design. It also includes delay and power consumption evaluation. From the Digital schematic software, we can check if the logic circuit is designed correctly which helps to manufacture the correct chip according to the specification and requirements.

5. SIMULATION

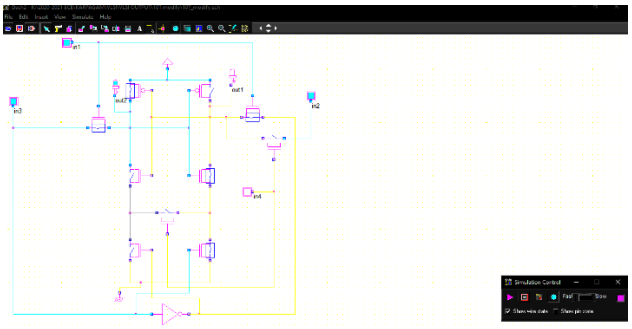

Figure 12 DSCH Circuit of 10T SRAM Cell

The circuit consists of four inputs and two outputs which can be read and write. When logic '1' is applied as input, NMOS of the cell act as logic '1' which means it act as a closed switch and PMOS of the cell act as open switch. Hence the path across NMOS provides conduction path and The circuit gives the output accordingly.

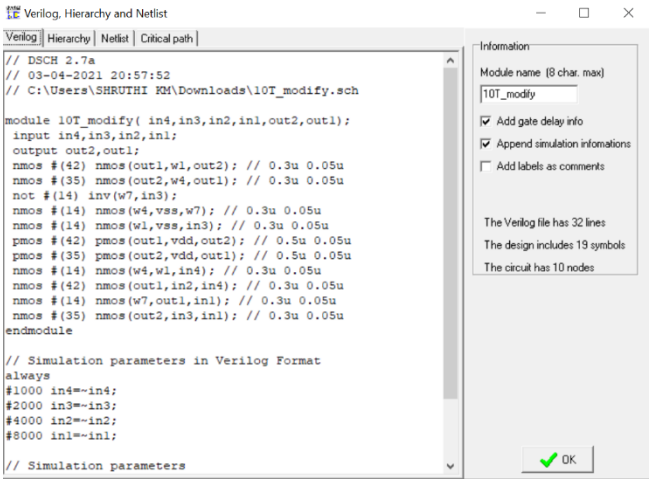

Figure 13 Verilog code of 10T SRAM Cell

The Verilog Code for 10T SRAM Cell is generated in the DSCH Software. This Verilog code is used in the Microwind software to get the layout output of 10T SRAM Cell

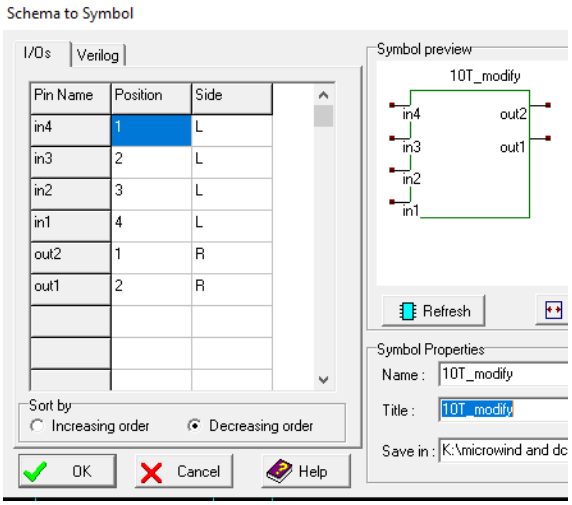

Figure 14 Schema to symbol of 10T SRAM Cell

This figure gives the schematic of the 10T SRAM cell.

It has four inputs and two outputs.

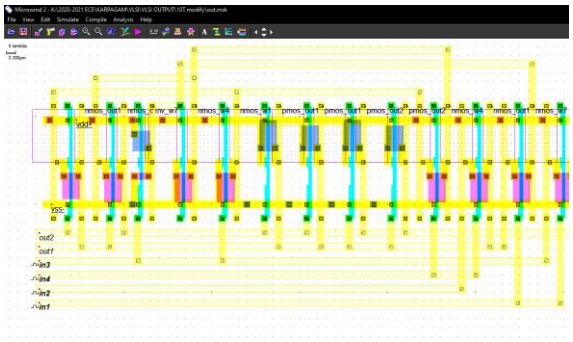

Figure 15 Microwind output of 10T SRAM Cell

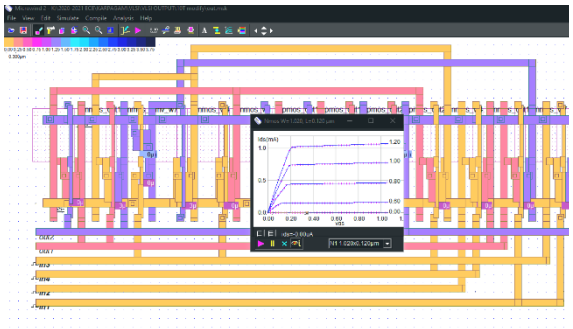

Figure 16 Microwind output with timing diagram for 10T SRAM

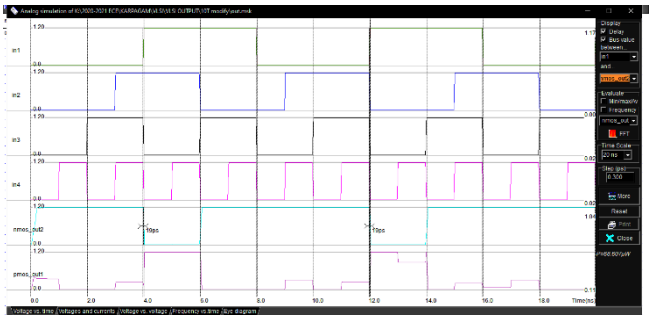

Figure 17 Microwind waveform for 10T SRAM Cell

6. DISCUSSION

The developments of our proposed work are described as follows:

Area efficiency: The 10T SRAM Cell uses the same area used by 6T SRAM cell.

Power consumption: The circuit of 10T SRAM cell uses two cross coupled inverters. This type of a circuit reduces the number of inputs for the transistors which helps in the power reduction even if the number of transistors in the SRAM cell increases.

7. AREA EFFICIENCY

MOS SIZE (µm)	6T Static Random Access Memory (SRAM) Cell	10T Static Random Access Memory (SRAM) Cell
Width of PMOS transistor	0.720µm	0.720µm
Length of PMOS transistor	0.120µm	0.120µm
Width of NMOS transistor	0.240µm	0.240µm
Length of NMOS transistor	0.120µm	0.120µm

Figure 18: Width and length of MOS transistors for 6T and 10T SRAM cell

8. REFERENCES

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