# SINGLE-ENDED 10T SRAM CELL WITH IMPROVED STABILITY

**A PROJECT REPORT**

***Submitted by***

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***in partial fulfillment for the award of the degree***

***of***

**BACHELOR OF ENGINEERING**

***in***

**ELECTRONICS AND COMMUNICATION ENGINEERING**


ST. JOSEPH'S COLLEGE OF ENGINEERING

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April-2021

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# ACKNOWLEDGEMENT

The contentment and elation that accompany the successful completion of any work would be incomplete without mentioning the people who made it possible.

Words are inadequate in offering our sincere thanks and gratitude to our respected Chairman **Dr. B. Babu Manoharan, M.A., M.B.A., Ph.D.**

We express our sincere gratitude to our beloved **Managing Director Mrs. B. Jessie Priya, M.Com., (Commerce) and Director Mr. B. Shashi Sekar, M.Sc.,(Intl. Business)**for their support and encouragement.

We also thank our beloved principal **Dr. Vaddi Seshagiri Rao, M.E, MBA, Ph.D,** for having encouraged us to do our under graduation in Electronics and Communication Engineering in this esteemed college.

We also express our sincere thanks and most heartfelt sense of gratitude to our eminent Head of the Department, **Dr. B Victoria Jancee, M.E., Ph. D** for having extended her helping hand at all times.

It is with deep sense of gratitude that we acknowledge our indebtedness to our supervisor **Mrs. G ANITHA** for her expert guidance and connoisseur suggestion.

We thank all staff members of my department, our family members and friends who have been the greatest source of support to us.

# CERTIFICATE OF EVALUATION

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BRANCH : ELECTRONICS AND COMMUNICATION ENGINEERING

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Submitted for UNIVERSITY VIVA VOCE Examination held on _____

**INTERNAL EXAMINER** **EXTERNAL EXAMINER**

# ABSTRACT

CMOS technology has enabled the semiconductor industry to meet its ever-increasing demand for computation speed and integration density. However, in nanometer-scale geometry, VLSI circuit and system design faces lot of challenges. The portable microprocessor controlled devices contain embedded memory, which presents a large portion of the system-on-chip (SoC). These portable systems need ultralow power consuming circuits to utilize battery for long duration. The power consumption can be minimized using non conventional device structures, new circuit topologies, and optimizing the architecture. Although, voltage scaling has led to circuit operation in subthreshold regime. With minimum power consumption, but there is a disadvantage of exponential reduction in performance. The circuit operation in the subthreshold region has paved path toward ultralow power embedded memories, mainly static RAM's (SRAM). However, in subthreshold regime, the data stability of SRAM cell is a severe problem and worsens with the scaling of MOSFET to sub nanometer technology. Due to this limitations, it becomes difficult to operate the conventional 6-transistor (6T) cell at ultralow voltage (ULV) power supply. In addition, 6T has a severe problem of read disturb which is overcomed by 10T SRAM cell. In this work, a single-ended 10T static random-access memory (SRAM) cell is presented. Proposed cell employs Schmitt trigger (ST) based inverter to enhance read stability. Single ended feature of the cell saves switching power. Simulation is carried on 180nm technology using Cadence. Results revealed that our cell provides 1.40x larger read static noise margin (RSNM) compared to conventional 6T cell at 0.7V. During write '0' proposed cell offers 312mv of write static noise margin (WSNM) at 0.7V. During read operation, our cell offers 3.29x lower switching power compared to 6T cell.

# TABLE OF CONTENTS

# LIST OF TABLES

# LIST OF FIGURES

# LIST OF SYMBOLS, ABBREVIATIONS AND NOMENCLATURE

| S.NO | ABBREVIATION | EXPANSION |
|---|---|---|
| 1. | 10T SRAM | 10 Transistor Static Random Access Memory |
| 2. | 2D | 2 Dimensional |
| 3. | 3D | 3 Dimensional |
| 4. | 6T SRAM | 6 Transistor Static Random Access Memory |
| 5. | ALU | Arithmetic and Logic Unit |
| 6. | BL | Bit Line |
| 7. | BLB | Bit Line Bar |
| 8. | BSIM | Berkeley Short-channel IGFET Model |
| 9. | CAD | Computer Aided Design |
| 10. | CMOS | Complementary metal-oxide semiconductor |
| 11. | CNT | Carbon Nano Tube |
| 12. | CNTFET | Carbon Nano Tube Field Effect Transistor |
| 13. | CPU | Central Processing Unit |
| 14. | CR | Cell Ratio |
| 15. | CS | Control Signal |
| 16. | DC | Direct Current |
| 17. | DDR3- | Double Data Rate 3 |
| 18. | DICE | Dual Interlocked Storage Cell |
| 19. | DRAM | Dynamic Random Access Memory |
| 20. | DSCH | Digital Schematic |
| 21. | DTCO | Design Technology Co-Optimization |
| 22. | EDA | Electronic Design Automation |
| 23. | FDSOI | Fully Depleted Silicon On Insulator |
| 24. | Fin FET | Fin Field effect Transistor |
| 25. | GC-e DRAM | Gain Cell Embedded Dynamic Random Access Memory |
| 26. | HD | High Density |
| 27. | HDL | Hardware Description Language |
| 28. | IC | Integrated Circuit |

| | | |
|---|---|---|
| 29. | IEEE | Institute of Electrical and Electronics Engineering |
| 30. | IFGC | Internal Feedback Gain Cell |
| 31. | IN | Input |
| 32. | INV | Inverter |
| 33. | LSB | Least Significant Bit |
| 34. | LVT | Low Vth Transistor |
| 35. | M-C | Monte-Carlo |
| 36. | MOS | Metal-Oxide Semiconductor |
| 37. | MOSFET | Metal-Oxide Semiconductor Field Effect Transistor |
| 38. | MSB | Most Significant Bit |
| 39. | MTCM | Multi Threshold Complementary metal-oxide semiconductor |
| 40. | NC SRAM | N Controlled Static Random Access Memory |
| 41. | NMOS | N-channel metal-oxide semiconductor |
| 42. | OUT | Output |
| 43. | PDA | Personal Digital Assistant |
| 44. | PFET | P-channel Field Effect Transistor |
| 45. | PMOS | P- channel metal-oxide semiconductor |
| 46. | PP SRAM | PMOS pass transistor Static Random Access Memory |
| 47. | PSPICE | Personal Simulation Program with Integrated Circuit Emphasis |
| 48. | Qcrit | Critical charge |
| 49. | RBB | Reverse Body Biasing |
| 50. | RBL | Read Bit Line |
| 51. | RNM | Retention Noise Margin |
| 52. | ROM | Read Only Memory |
| 53. | RSNM | Read Static Noise Margin |
| 54. | RTL | Register Transfer Level |
| 55. | SE6T SRAM | Single-Ended 6 Transistor Static Random Access Memory |
| 56. | SEU | Single Event Upsets |
| 57. | SGT | Surrounding Gate Transistor |

| | | |
|---|---|---|
| 58. | SNM | Static Noise Margin |
| 59. | SoC | Systems-On-Chip |
| 60. | SPICE | Simulation Program with Integrated Circuit Emphasis |
| 61. | SRAM | Static Random Access Memory |
| 62. | ST | Schmitt Trigger |
| 63. | ST | Sub-Threshold |
| 64. | TCAD | Technology Computer- Aided Design |
| 65. | ULL | Ultra-Low Leakage |
| 66. | UMC | United Microelectronics Corporation |
| 67. | V min | Minimum Voltage |
| 68. | VLSI | Very Large Scale Integration |
| 69. | Vt | Threshold Voltage |
| 70. | WBL | Write Word Lin |
| 71. | WL | Word Line |
| 72. | WSNM | Write Static Noise margin |
| 73. | WWL | Write Word Line |

# CHAPTER 1

# INTRODUCTION

CMOS technology has enabled the semiconductor industry to meet its ever-increasing demand for computation speed and integration density. However, in nanometer-scale geometry, VLSI circuit and system design faces lot of challenges [3]. The gate dielectric thickness has been reduced to a point where the power drained by the gate tunneling current is comparable to the power consumed due to switching activity. Therefore, aggressive scaling of device dimensions, random variations in process, supply voltage and temperature (PVT) are posing major challenges to the future high-performance circuits and system design.

## 1.1 MOTIVATION

The emerging and growing market for portable electronic devices has led the electronic designers to be more conscious of power and energy constraints in their circuit designs. Designers are forced to design more energy-aware circuits and started to develop methods and design rules to increase energy savings. In the sub-threshold region of operation, the power supply voltage of the circuit is lowered below to transistor's threshold voltage. As a consequence, its active and leakage power is reduced dramatically. However, this advance comes at the cost of circuit switching speed. One of the central areas of micro electronic design that it is affected by such design methodology is memory design. This thesis compares a 10T SRAM cell with an improved write margin to a conventional 6T SRAM cell operated in the subthreshold region in 180nm technology using Cadence. The two SRAM cells are compared based on their Static Noise Margins, Read currents, Leakage currents and Static Write Margins while considering the effects of process variations. This comparison gives future designers an insight for future 10T cell designs.

## 1.2 SRAM

### 1.2.1 SRAM TECHNOLOGY

The microscopic variations in number and location of dopant atoms in the channel region of the device induce deviations in device characteristics. These fluctuations are more pronounced in minimum-geometry devices commonly used in area-constraint circuits such as SRAM (static random-access memory) cells. SRAM is a highly used circuit of modern chips. State-of-the-art microprocessor designs devote a large fraction of the chip area to memory structures, e.g., multiple levels of instruction and data caches, translation look-aside buffers, and prediction tables. SRAM constitutes more than half of chip area and more than half of the number of devices in modern designs. As per the prediction of ITRS, embedded cache will occupy 90% of a system on a chip by 2013.

### 1.2.2 SRAM FEATURES

Even today, an H-264 encoder for a high-definition television requires, at least, a 500 kb memory as a search-window buffer that contributes 40% to its total power consumption. Mobile applications demand the design of increasingly larger caches at low standby power budget. It is estimated that transfer of data from main memory, cache, and local registers, costs, respectively, 10, 5, 2 times as much energy as the actual operation on them by an ALU. Hence, the analysis and evaluation of SRAM cell in terms of its design criteria such as read stability, write ability and static noise margin are very important. The SNM model in assumes identical device threshold voltages across all cell transistors, making it unsuitable for predicting the effects of threshold voltage mismatch between adjacent transistors within a cell. Therefore, designers require reevaluation and analysis of static noise margin in scaled technologies to ensure stability of SRAM cell.

Standard 6T SRAM cell suffers from read instability and weak write ability at low voltage operation. Moreover, the more stable a cell during read operation, the more difficult it is to write for changing its content during write operation.

This work proposes a single-ended 6T SRAM cell. It makes the following contributions:

### 1.2.3 SRAM APPLICATIONS

In view of the aforesaid ultralow power requirement and variation issue, a single-ended 6T SRAM cell ((hereafter called SE-6T)) is proposed in this paper. Various design metrics of SE-6T is investigated at nominal supply voltage of 1 V and compared with differential 6T SRAM cell (hereafter called Dif-6T).

Battery operated portable applications such as cell phones and PDAs require extremely low energy consumption for longer battery life. This can be achieved by (a) lowering VDD (supply voltage) and (b) decreasing activity factor by using single bit line and discharging it either for writing “1” or “0”. It is established that the proposed design outperforms Dif-6T in terms of dynamic power consumption (by more than 50%).

Moreover, simulation results using HSPICE confirm that the proposed SE-6T is suitable for implementation in 32 nm CMOS technology

The remainder of the paper is organized as follows. Various failure mechanisms and mode of operations of SRAM cell are briefly reviewed in Section 2. Section 3 briefly discusses read stability, write-ability and impact of scaling on stability of SRAM cell. Section 4 explains read/write operation, cell sizing and dynamic power saving of proposed single-ended 6T SRAM cell. Section 5 presents the simulation results and compares proposed design with differential 6T SRAM cell. Static random-access memory (static RAM or SRAM) is a type of semiconductor random-access memory (RAM) that uses bistable latching circuitry (flip-flop) to store each bit.

SRAM exhibits data remanence,[3] but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. The term static differentiates SRAM from DRAM (dynamic random-access memory) which must be periodically refreshed. SRAM is faster and more expensive than DRAM; it is typically used for CPU cache while DRAM is used for a computer's main memory.

## 1.3 VLSI

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device.

Before the introduction of VLSI technology, most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip.

The electronics industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in large scale integration technologies and system design applications. With the advent of very large scale integration (VLSI) designs, the number of applications of integrated circuits (ICs) in high-performance computing, controls, telecommunications, image and video processing, and consumer electronics has been rising at a very fast pace.

The current cutting-edge technologies such as high resolution and low bit-rate video and cellular communications provide the end-users a marvelous number of applications, processing power and portability. This trend is expected to grow rapidly, with very important implications on VLSI design and systems design.

### 1.3.1 VLSI Design Flow:

The VLSI IC circuits design flow is shown in the figure below. The various levels of design are numbered and the blocks show processes in the design flow.

Specifications comes first, they describe abstractly, the functionality, interface, and the architecture of the digital IC circuit to be designed.

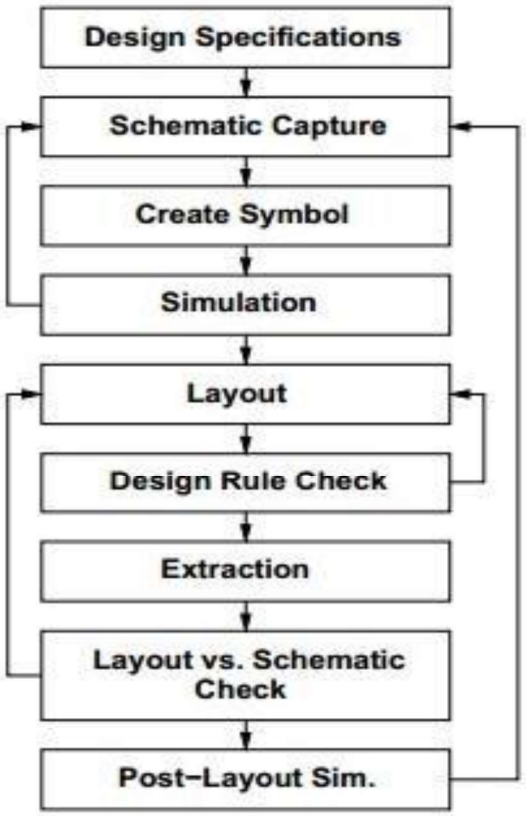



**Figure 1.1 VLSI IC Circuits design flow**

Behavioral description is then created to analyze the design in terms of functionality, performance, compliance to given standards, and other specifications.

RTL description is done using HDLs. This RTL description is simulated to test functionality. From here onwards we need the help of EDA tools.

RTL description is then converted to a gate-level netlist using logic synthesis tools. A gate level netlist is a description of the circuit in terms of gates and connections between them, which are made in such a way that they meet the timing, power and area specifications.

Finally, a physical layout is made, which will be verified and then sent to fabrication.

Y Chart

The Gajski-Kuhn Y-chart is a model, which captures the considerations in designing semiconductor devices.

The three domains of the Gajski-Kuhn Y-chart are on radial axes. Each of the domains can be divided into levels of abstraction, using concentric rings.

At the top level (outer ring), we consider the architecture of the chip; at the lower levels (inner rings), we successively refine the design into finer detailed implementation −

Creating a structural description from a behavioral one is achieved through the processes of high-level synthesis or logical synthesis.

Creating a physical description from a structural one is achieved through layout synthesis.

### 1.3.2 Design Hierarchy-Structural:

The design hierarchy involves the principle of "Divide and Conquer." It is nothing but dividing the task into smaller tasks until it reaches to its simplest level. This process is most suitable because the last evolution of design has become so simple that its manufacturing becomes easier.

We can design the given task into the design flow process's domain (Behavioral, Structural, and Geometrical). To understand this, let’s take an example of designing a 16-bit adder, as shown in the figure below.

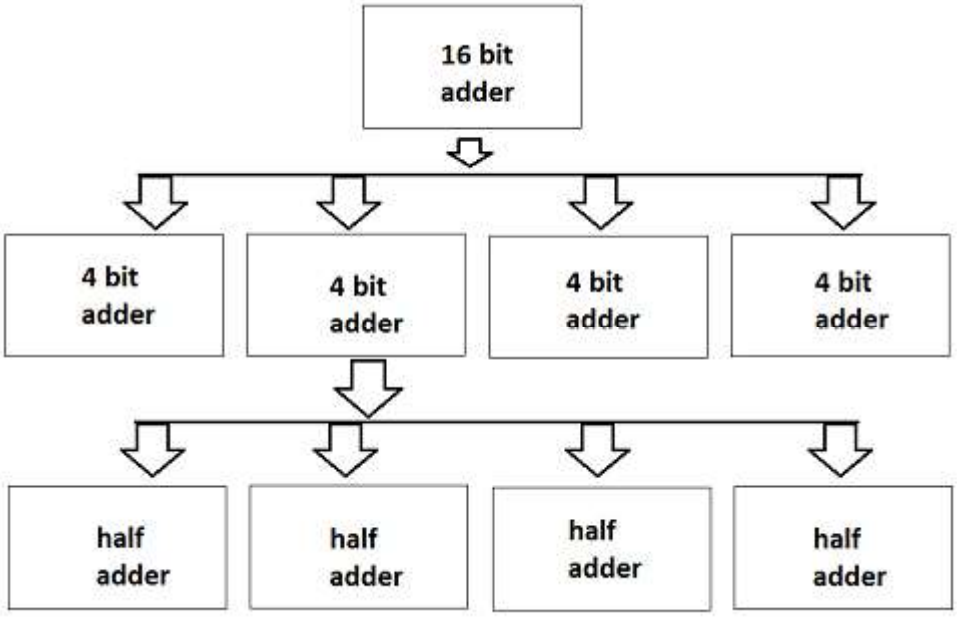



**Figure 1.2 16 bit adder**

Here, the whole chip of 16 bit adder is divided into four modules of 4-bit adders. Further, dividing the 4-bit adder into 1-bit adder or half adder. 1 bit addition is the simplest designing process and its internal circuit is also easy to fabricate on the chip. Now, connecting all the last four adders, we can design a 4-bit adder and moving on, we can design a 16-bit adder.

# CHAPTER 2
# LITERATURE SURVEY

## 2.1 INTRODUCTION

The various research works on the Static Random Access Memory ( SRAM ) cells is discussed and analyzed.

### [1] S.Ataei and J.E.Stine, "A 64 kb approximate SRAM architecture for low-power video applications," IEEE Embedded Systems Letters, 2017.

A voltage-scalable SRAM architecture suitable for video applications where energy can be traded with output signal quality is presented. The proposed 6T SRAM architecture uses three supply voltages to improve the static noise margin during read and write modes and also reduces leakage current in retention mode, hence, it allows aggressive supply voltage scaling for low power multimedia applications. Simulation results in IBM/Global Foundries cmos32soi 32-nm CMOS technology show a 69% power saving and a 63% improvement in image quality for the proposed array compared to a conventional single-supply 64-kB 6T SRAM at 0.70 V, 20 MHz. The proposed design also allows a dynamic power-quality tradeoff at run time and makes the 6T SRAM array a suitable power efficient memory for different video/image applications.

### [2] R.Giterman, , N.Geuli, E.Mentovich, A.Burg, and A. Teman, "An 800-mhz mixed-vt4t igc embedded dram in 28-nm cmos bulk process for approximate storage applications," IEEE Journal of Solid State Circuits, vol. 53, no. 7, pp. 2136–2148, July 2018

Gain-cell embedded DRAM (GC-e DRAM) is an attractive alternative to traditional static random access memory (SRAM) due to its high-density, low-leakage, and

inherent two-ported operation, yet its dynamic nature leads to limited retention time and calls for periodic, power-hungry refresh cycles. This drawback is further aggravated in scaled technologies, where increased leakage currents and decreased in-cell storage capacitances lead to accelerated data integrity deterioration. The emerging approximate computing paradigm utilizes the inherent error-resilience of different applications to tolerate some errors in the stored data. Such error tolerance can be exploited to reduce the refresh rate in GC-e DRAM to achieve a substantial decrease in power consumption at the cost of an increase in cell failure probability. In this paper, we present the first fabricated and fully functional GC-e DRAM in a 28-nm bulk CMOS technology. The array, which is based on a novel mixed-VT four-transistor (4T) gain cell with internal feedback (IFGC) optimized for high performance, features a small silicon footprint and supports high-performance operation. The proposed memory can be used with conservative (i.e., 100% reliable) computing paradigms, but also in the context of approximate computing, featuring a small silicon footprint and random-access bandwidth. Silicon measurements demonstrate successful operation at 800 MHz under a 900-mv supply while retaining between 30% and 45% lower bitcell area than a single-ported six-transistor (6T) SRAM and a two-ported six-transistor (8T) SRAM in the same technology.

**[3] S.Gupta, K.Gupta, and N.Pandey, "A 32-nm subthreshold 7T SRAM bit cell with read assist," IEEE Trans. on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 12, pp. 3473–3483, 2017.**

The implementation of the six-transistor (6T) static random access memory cell in deep sub micrometer region has become difficult due to the compromise between area, power, and performance, with local and global variations only exacerbating the problem further. To impede the read–write conflict of the 6T cell, the seven-transistor (7T) cell with a noise-margin-free read operation has previously been proposed. But it severely lags in terms of its write ability at lower voltages due to its single-ended

write operation. Its single-ended read operation also degrades severely in performance when operating in subthreshold (ST) region. To combat these problems, a 7T cell is proposed which operates in the ST region down to 0.4 V with improved dynamic write ability. The novel topology also helps reduce power consumption by achieving a lower data retention voltage point. A read assist has been proposed to greatly enhance the performance of the single-ended read operation in ST region. Large improvements in various performance metrics of the proposed cell have been attained while simultaneously achieving a low area of $0.254~\mu \text{m}^{2}$ per bit cell on the 32-nm technology node

**[4] R.Giterman, A.Fish, N.Geuli, E.Mentovich, A.Burg, A.Teman, "An 800 MHz mixed-VT 4T gain-cell embedded DRAM in 28 nm CMOS bulk process for approximate computing applications",** *Proc. Eur. Solid State Circuits Conf. (ESSCIRC)***, pp. 308-311, Sep. 2017.**

Gain-cell embedded DRAM (GC-e DRAM) is an attractive alternative to traditional static random-access memory (SRAM) due to its high-density, low-leakage, and inherent two-ported operation, yet its dynamic nature leads to limited retention time and calls for periodic, power-hungry refresh cycles. This drawback is further aggravated in scaled technologies, where increased leakage currents and decreased in-cell storage capacitances lead to accelerated data integrity deterioration. The emerging approximate computing paradigm utilizes the inherent error-resilience of different applications to tolerate some errors in the stored data. Such error tolerance can be exploited to reduce the refresh rate in GC-e DRAM to achieve a substantial decrease in power consumption at the cost of an increase in cell failure probability. In this paper, we present the first fabricated and fully functional GC-e DRAM in a 28-nm bulk CMOS technology. The array, which is based on a novel mixed-VT four-transistor (4T) gain cell with internal feedback (IFGC) optimized for high performance, features a small silicon footprint and supports high-performance

operation. The proposed memory can be used with conservative (i.e., 100% reliable) computing paradigms, but also in the context of approximate computing, featuring a small silicon footprint and random-access bandwidth. Silicon measurements demonstrate successful operation at 800 MHz under a 900-mv supply while retaining between 30% and 45% lower bit cell area than a single-ported six-transistor (6T) SRAM and a two-ported six-transistor (8T) SRAM in the same technology.

**[5] P.Meinerzhagen, A.Teman, R.Giterman, N.Edri, A.Burg, A.Fish, Gain-Cell Embedded DRAMs for Low-Power VLSI Systems-on-Chip, Basel, Switzerland:Springer, 2018**

This book pioneers the field of gain-cell embedded DRAM (GC-e DRAM) design for low-power VLSI systems-on-chip (SoCs). Novel GC-e DRAMs are specifically designed and optimized for a range of low-power VLSI SoCs, ranging from ultra-low power to power-aware high-performance applications. After a detailed review of prior-art GC-e DRAMs, an analytical retention time distribution model is introduced and validated by silicon measurements, which is key for low-power GC-e DRAM design. The book then investigates supply voltage scaling and near-threshold voltage (NTV) operation of a conventional gain cell (GC), before presenting novel GC circuit and assist techniques for NTV operation, including a 3-transistor full transmission-gate write port, reverse body biasing (RBB), and a replica technique for optimum refresh timing. Next, conventional GC bit cells are evaluated under aggressive technology and voltage scaling (down to the subthreshold domain), before novel bit cells for aggressively scaled CMOS nodes and soft-error tolerance as presented, including a 4-transistor GC with partial internal feedback and a 4-transistor GC with built-in redundancy

**[6] S.A.Pourbakhsh, X.Chen, D.Chen, X.Wang, N.Gong, and J.Wang, "Sizing-priority based low-power embedded memory for mobile video applications," in Quality Electronic Design (ISQED), 2016 17th International Symposium on. IEEE, 2016.**

Recently, mobile devices such as smart-phones and tablets have become the most important medium for delivering internet traffic, especially multimedia content, to end users. However, mobile embedded memory incurs large power consumption owing to the highly frequent access and extensive computation. This paper presents a sizing-priority based memory design methodology for low-power mobile video applications. We investigate the size dependent memory failure characteristics and effectively reduce the memory failure rate with low area overhead. Also, we develop a model for the influence of the memory failure on video output, connecting the hardware design process and application requirement. A 64-byte SRAM was fabricated and test results confirm the effectiveness of the proposed technique

## 2.2 A 1.2-V 1.5-Gb/s 72-Mb DDR3 SRAM

A 1.2-V 72-Mb double data rate 3 (DDR3) SRAM achieves a data rate of 1.5 Gb/s using dynamic self-resetting circuits. Single-ended main data lines halve the data line pre charging power dissipation and the number of data lines. Clocks phase shifted by 0°, 90°, and 270° are generated through the proposed clock adjustment circuits. The latter circuits make input data sampled with an optimized setup/hold window. On-chip input termination with a linearity error of ±4.1% is developed to improve signal integrity at higher data rates. A 1.2-V 1.5-Gb/s 72-Mb DDR3 SRAM is fabricated in a 0.10-μm CMOS process with five metals. The cell size and the chip size are 0.845 $\mu m^2$ and 151.1 $mm^2$, respectively.

## 2.3 DESIGN AND ANALYSIS OF LOW POWER SRAM CELLS

The rapid growth of portable battery-operated devices has made low power IC design a priority in recent years. Embedded SRAM units have become an integral part in modern SoCs. Conventional SRAM cell designs are power hungry and poor performers in this new era of fast mobile computing. In this paper, low power SRAM cell designs have been analyzed for power consumption, write delay and write power delay product. Gated VDD and MTCMOS design techniques have been employed to reduce the power consumed by the SRAM cell. These designs are compared with the conventional 6T SRAM cell. The results show that the MTCMOS based SRAM cell is the best performer in terms of power consumption and write delay. It uses 38.1% less power than the conventional 6T SRAM cell. Furthermore, the MTCMOS based SRAM cell is 18.18% faster than the conventional 6T SRAM cell. The Gated VDD SRAM cell also performs well using 16.8% less power than the conventional 6T SRAM cell and is 13.03% faster than the conventional 6T SRAM cell.

## 2.4 A COMPARATIVE STUDY OF NC AND PP-SRAM CELLS WITH 6T SRAM CELL USING 45NM CMOS TECHNOLOGY

Data stability, performance and leakage currents are the few important issues of Static Random-Access Memory (SRAM) due to scaling down the technology. These issues were revisited by making a comparative study of N-Controlled SRAM cell (NC-SRAM) and PMOS pass transistor SRAM cell (PP-SRAM) with conventional 6T SRAM cell. A decrease in Static Noise Margin (SNM) of NC-SRAM and PP-SRAM cells with 6T SRAM cell in hold mode by 60.09% and 0.22% at temperature (T) = 25°C, 63.25% and 3.34% at T = 50°C, 63.82% and 3.37% at T = 100°C respectively. was observed. For the transistors sizing a degradation in write operation of NC-SRAM cell by 7.31% was obtained to compare to 6T SRAM cell, While it is unchanged in case of PP-SRAM cell. Significant reduction in total leakage power is obtained for

NC and PP-SRAM cells compared to 6T SRAM cell by 77.06% and 47.42% at T = 25°C, 76.89% and 48.98% at T = 50°C, 76.87% and 50.94% at T = 100°C respectively, which is due to the gate and sub-threshold leakage currents. Also a 16-bit memory array of 6T was designed, NC and PP SRAM cells. There was a reduction in total leakage power for 16-bit array of NC and PP-SRAM cells by 69.86 %, 50.75 % respectively compared to the 16 bit array of 6T SRAM cell. All the simulations were performed by Cadence Virtuoso (version IC 6.1.6.500.1) tool using gpdk 45nm CMOS process technology.

## 2.5 STABILITY ANALYSIS OF 6T CNTFET SRAM CELL FOR SINGLE AND MULTIPLE CNT'S

Carbon Nano Tube Field Effect Transistor (CNTFET) is a best futuristic device for nano scale range VLSI design than MOSFETs. This is due to the favorable physical properties of CNTFET. In this paper the comparative Stability analysis of a CNTFET based six transistor Static Random Access Memory (6T SRAM) cell was presented for single nano tube CNTFET and multiple nano tubes CNTFET. The SRAM cell stability is measured by Static Noise Margin (SNM) of the cell. The SNM of 6T SRAM is also analyzed for different chiral vectors. The comparison shows that the single tube and low chiral vector values provides high stability of CNTFET 6T SRAM cell than multiple tubes with high chiral vector. The simulation is carried out with 32nm technology.

## 2.6 A 0.6V RETENTION VMIN ULTRA-LOW LEAKAGE HIGH DENSITY 6T SRAM IN 40NM CMOS TECHNOLOGY USING ADAPTIVE SOURCE BIAS

A low retention V min 6T-SRAM is realized in 40nm CMOS technology under source bias condition. A high density (HD), ultra-low leakage (ULL) 6T SRAM cell with an area of 0.242um2 is used. The retention V min of SRAM array was reduced to 0.6V using adaptive source bias scheme. Source bias is applied to achieve ultra-low leakage

during standby mode of operation. Source bias results in loss of stability due to reduced effective rail-to-rail voltage of memory cell and hence becomes difficult to reduce the retention V min of SRAM. An adaptive source bias scheme is used to apply reduced source bias selectively for low retention noise margin (RNM) conditions. We could reduce the retention V min by 100mV to 0.6V compared to 0.7V realized with the conventional scheme. The leakage at FF/125°C was reduced by 30 percent due to reduction of V min from 0.7V to 0.6V. At TT/0.6V/25°C, the target leakage of 0.5pA/Cell was achieved during standby mode of operation.

## 2.7 BODY-BIASING ASSISTED V MIN OPTIMIZATION FOR 5NM-NODE MULTI-VT FD-SOI 6T-SRAM

This work proposes a body-biasing technique to optimize $V_{min}$ of the 6T-SRAM based on 5nm-node multi-$V_t$ FD-SOI devices. Accounting for the process variation, the operating voltage, $V_{min}$, is estimated at 6-sigma yield. By properly selecting the back bias, the lowest $V_{min}$ is achieved for each of the three operation modes: high-performance, standard and low-voltage modes. In high-performance mode, the optimized V min is reduced to 0.491 V at back bias of 0.2 V. The proposed technique offers a design flexibility for optimizing the SRAM performance and yield by adjusting the back bias without complicated process technology requirements.

## 2.8 A TEMPERATURE COMPENSATED READ ASSIST FOR LOW V MIN AND HIGH-PERFORMANCE HIGH DENSITY 6T SRAM IN FIN FET TECHNOLOGY

A low V min, 6T-SRAM is realized in 7nm Fin FET Technology using read and write assist methods. Read margin of the SRAM cell is recovered using a temperature compensated word line lowering scheme. This temperature compensated Read Assist provides additional advantage that lowering on word line is almost process independent that makes Read Assist very robust. This scheme makes design free from tuning after post silicon. Since Proposed Read Assist circuit lowers Word line at high

temperature while lowering at low temperature is very minimal, SRAM writability is not impacted by Read Assist Circuity at low temperature. At low voltage, SRAM performance is limited by Read cycle time. The proposed Read Assist scheme improves Read performance by 200%, which in-turn reflects the gain in operating frequency up to 100%. In the proposed Read assist implementation operating frequency is almost comparable to system when Read Assist is not enabled with added advantage of low voltage enablement

## 2.9 DTCO and TCAD for a 12 Layer-EUV Ultra-Scaled Surrounding Gate Transistor 6T-SRAM

A flow, module steps and key structural elements enabling a surrounding gate transistor (SGT) based 6T-SRAM with 50nm pillar pitch and 0.0205 um2 are presented, with emphasis on process challenges and innovations. A new DTCO/TCAD methodology is used to explore the design space, demonstrate the bit cell functionality and optimize the process. In particular, it is shown that vertical SGT are extremely sensitive to gate misalignment and that buried bottom contact makes the process immune to doping variations and misalignments.

## 2.10 EVALUATION OF THE TEMPERATURE INFLUENCE ON SEU VULNERABILITY OF DICE AND 6T-SRAM CELLS

In this paper, The temperature influence was evaluated on the vulnerability to single event upsets (SEU) of 6-transistor static random-access memory (6T-SRAM) cells and dual interlocked storage cells (DICE). The critical charge (Q crit, minimum charge capable of generating an SEU) is evaluated for 65nm, 45nm, 32nm and 22nm bulk CMOS technologies and temperatures between -50°C and 150°C. A double exponential signal is used to model the current pulse generated by ionizing particles. SPICE simulations have shown that crit is sensibly reduced by the rise of temperature. Q crit variations of up to 88.4% and 99.9% have been calculated for 6T-SRAM and DICE cells, respectively.

## 2.11 DESIGN AND MODELLING OF 6T FIN FET SRAM IN 18NM

In this work Fin FET based of 6T SRAM were designed and characterized these cells in terms of temperature and average power. This SRAMs were designed & stimulated in Cadence using 18nm Fin FET technology.

## 2.12 A 40NM LOW POWER HIGH STABLE SRAM CELL USING SEPARATE READ PORT AND SLEEP TRANSISTOR METHODOLOGY

At lower technology, the static power dissipation and stability of conventional six transistors static random-access memory (SRAM) cell poses a major issue. To address this issue, a novel eleven transistor (11T) SRAM cell for improving read stability and reducing the static power dissipation is proposed in this work. In the proposed 11T SRAM cell, the storing node isolates from the read bit line using separate read port while sleep transistor methodology is explored for power saving. With this the read static noise margin (RSNM) value of proposed design is enhanced by 6x, 2.3x, 2.7x and 1.3x when compared with basic 6T SRAM cell, 11T ST2 SRAM cell, 11T ST1 SRAM cell, ST11T SRAM cell respectively. The write stability is also enhanced by 1.6x over basic 6T SRAM cell, 1.14x over 11T SRAM and penalty of 1.17x when compared with other 11T SRAM cell. Further, using the sleep transistor methodology the static power consumption of the proposed design has been reduced by 4.6x when compared with basic 6T SRAM cell. The proposed 11T SRAM cell has been verified in 40nm CMOS technology node using cadence virtuoso tool.

# CHAPTER 3

# EXISTING SYSTEM AND PROPOSED SYSTEM

## 3.1 EXISTING SYSTEM

- Conventional six transistor (6T) SRAM cell (Figure) has simple architecture but data disturbance problem is associated with it. For instance, suppose conventional 6T cell stores Q= '1' (QB = '0').
- During read, voltage at QB starts to rise due to the voltage division action between transistors M6 and M4.
- If voltage (at QB) attains a level equal to the threshold voltage of the left inverter (M1-M2), it can turn ON transistor M2 and the cell can lose its content.
- This problem is referred to as data disturbance. In order to mitigate data disturbance problem during read, conventional 6T employs a stronger pull down (M4) transistor as compared to the access transistors (M6).
- However, for reliable write operation, access transistor must be stronger than the pull up transistor.
- Thus, the conventional 6T cell suffers from conflicting design requirement on the access transistor.

## 3.2 MECHANISMS AND MODE OF OPERATIONS OF SRAM CELL

Design of SRAM requires the smallest transistors, which are particularly sensitive to process variations. Balancing the trade-offs between small areas, low powers, fast reads/writes are an essential part of any SRAM design. That is, SRAM design requires balancing among various design criteria such as minimizing cell area using smaller transistor, maintaining read/write stability, minimizing power consumption by reducing power supply, minimizing read/write access time, minimizing leakage current, reducing bit line swing to reduce power consumption, improving soft error immunity, etc. Some of the design criteria are conflicting in nature. For example,

higher Cell Ratio (CR) defined in [21] prevents read failure, but results in larger area and increased leakage.

The designer of SRAM should take care of the above design criteria along with various SRAM cell parametric failures such as read failure, write failure, access failure and hold failure. Read failure occurs while reading the content of an SRAM cell. Assume that node QB in Fig. 1 is storing a "0" and BLB is discharging through MN3 and MN1. If the resistance of pull-down transistor MN1 is higher than that of pass transistor MN3,a voltage ripple $VQB$ will be developed due to resistive divider formed by MN1 and MN3. If $VQB$ exceeds the switching threshold of the INV2 formed by MP2 and MN2 the cell state will flip while reading. The read failure can be reduced by increasing the difference between the voltage rise at the node storing "0" and the trip-point of the INV2. This can be achieved by widening pull-down driver NFETs in inverters of the SRAM cell. Write failure is an unsuccessful write to the SRAM cell. Write failure occurs if the node storing "1" cannot be discharged through the access transistors during the word line (WL) turn-on time. The write failure can be reduced by increasing the WL turn-on time with write access time increased, which unfortunately makes SRAM slower. It can also be achieved by making access FETs stronger with respect to load PFETs of the SRAM cell. Access failure occurs if the voltage difference between the two-bit lines at the time of sense amplifier firing remains below the offset voltage of the sense amplifier. Access failure occurs due to the reduction of the bit-line discharging current through the pass transistor and pull-down transistor. Clearly, a faster bit line discharge can be achieved by reducing the resistance in the discharge path by making the pull-down transistor stronger. However, such improvement comes at the price of larger cell area which is not suitable for high density SRAMs. Hold failure occurs due to high-leakage of the NMOS pull-down driver associated with node storing "1". In scaled technology (higher sub threshold and gate leakage current), at lower supply voltage

($VDD$), due to high leakage of the pull-down transistor, the node storing "1" may fall below $VDD$. If that stored voltage becomes lower than the trip-point of the INV1 (Figure)the cell flips in the hold mode. This failure can be avoided by reducing leakage in standby mode using high-$Vt$ (high-threshold voltage) pull-down transistors. This improvement comes at the price of read delay.

## 3.3 PROBABILITY AND DYNAMIC POWER

| Bit-position | BER(1)% | BER(0)% | Power/bit(µw) |
|---|---|---|---|
| X1(MSB) | 0.04 | 0.02 | 0.37 |
| X2 | 0.04 | 0.02 | 0.37 |
| X3 | 0.17 | 0.09 | 0.34 |
| X4 | 0.7 | 0.3 | 0.30 |
| X5 | 2.1 | 0.8 | 0.27 |
| X6 | 10.1 | 2.1 | 0.18 |
| X7(LSB) | 14.7 | 4.07 | 0.16 |

**Table 3.1 Corresponding Probability and Dynamic power**

## 3.4 SRAM'S MODE OF OPERATIONS

An SRAM cell offers the following basic modes of operation:

1) Data retention or standby mode of operation - an SRAM cell is able to retain the data indefinitely as long as it is powered;

2) Read operation - an SRAM cell is able to communicate its stored data and this operation does not affect the data i.e., read operation is non-destructive unlike read operation of DRAM cell;

3) Write operation - the data of an SRAM cell can be set to any binary value regardless of its original stored value.

## 3.5 6T SRAM CELL

Cell size accounts for most of array size

- Reduce cell size at cost of complexity/margins

Read:

- Pre charge bit, bit b
- Raise word line

Write:

- Drive data onto bit, bit b
- Raise word line

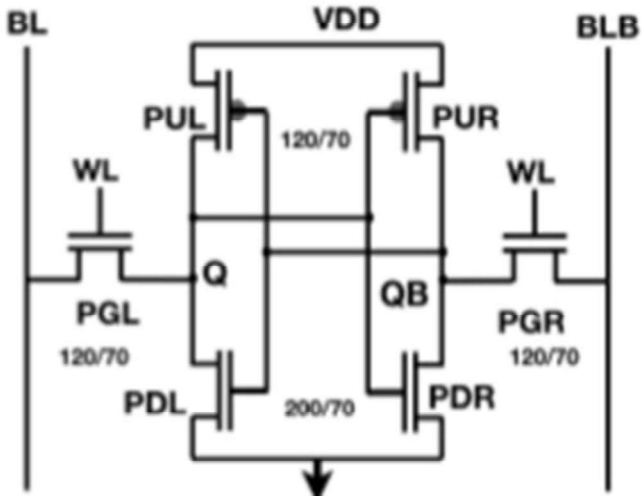



**Figure 3.1 Conventional 6-T SRAM cell**

We have, for the first time, designed approximate memory from the single-ended SRAM cell, called single ended 6-T (SE6T) SRAM cell.

- Since, our proposed SE6T SRAM cell uses only single bit-line for write and single bit-line for read it consumes only 50% of power when compared to conventional 6-T SRAM cell.
- The most striking feature of the proposed SE6T SRAM cell is that BER reduction is obtained by increasing the size of only one transistor unlike that of

the conventional 6-T SRAM cell where all the transistor sizes have to be proportionally increased.

- The proposed SE6T SRAM has higher read margin and comparable write margin to the conventional 6-T SRAM cell.
- The proposed SE6T SRAM cell has lower hold-margin as compared to conventional SRAM, but this is sufficient enough to hold data during the hold operation.
- While SNM is calculated based on DC analysis of SRAM cell, bit-error rate (BER) is obtained from transient analysis which captures both static and dynamic properties of the cell.

### 3.5.1 READ/WRITE OPERATION AND CELL SIZING

Figure shows the proposed design. Before and after each write operation BLB is pre charged. Write operation of SE-6T is initiated by switching MN5 off applying $W$ = "0". This breaks the feedback path and makes writing easier. In the literature single ended 5T SRAM cell is found , which exhibits problem while writing "1" and needs write assist method. BLB carries the complement of the bit to be stored in storage node Q (or equivalently BLB carries the bit to be stored at storage node QB). When WL is asserted high by row decoder (not shown), bit applied on BLB gets complemented and stored at Q. This bit at Q in turn drives INV1 and finally a bit applied to BLB gets stored at QB. Thus, write operation involves two inverters' delay and hence requires longer write time than that of differential 6T SRAM cell.

As MN3 passes a bad "1", at the end of write "1" operation to QB, $VQ2$ is at lower voltage. Just after write operation at hold mode, $W$ is raised high and Q2 gets raised gradually. During this transition time, MP2 may be partially on causing short-circuiting current to pass through MN2 to ground.

### 3.5.2 EXISTING SYSTEM TRUTH TABLE

| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**Table 3.2 Truth table of existing system.**

## 3.6 PROPOSED SYSTEM

- The cell constitutes two ST inverters. Word lines WWL and WL control transistors M7 and M8.
- Write bit line WBL transfer data from write driver to the internal storage node of the cell.
- Read bit line RBL is used to read the cell content. Transistor M10 is controlled by the OR Gate.
- As shown in the Figure, each row of the SRAM array shares one OR Gate. Transistor M9 raises the potential at node PQB during read '0'.
- Thus, helps in mitigating the problem of data disturbance during read. Table 1 shows the truth table of the proposed 10TSRAM cell.
- To write a logic '0' in the proposed 10T cell, WBL and RBL are loaded with logic '0', then WWL and WL are raised to VDD while control signal CS is set to '0'.
- Consequently, M10 turns ON and connects source terminal of M3 to ground.

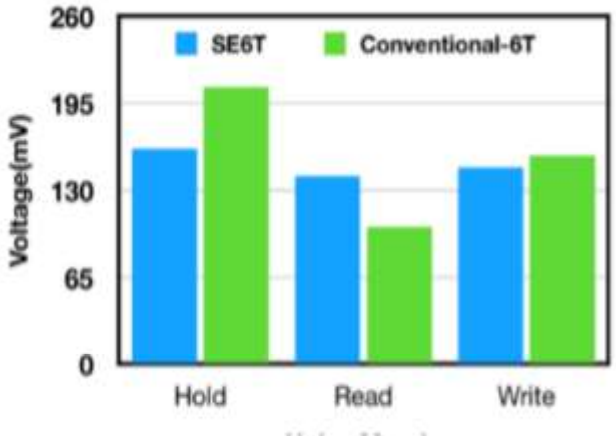
- Under this condition, storage node Q is discharged to WBL through M7 and to RBL through M2 and M8.
- Due to charge elimination at node Q, PMOS transistor M4 starts conducting which causes voltage at node QB to increases.
- Feedback action start to work resulting in node Q is set to logic ‘0’ while QB is set to logic ‘1’.
- To write a logic ‘1’ in the 10T cell, WBL is raised to VDD. Now, WWL is asserted while WL and CS are de-asserted. As a result, M10 is OFF leaving left inverter (M1-M2-M3) to float.
- This allows charges from WBL to be accumulated at node Q. Due to high Q, transistors M5 and M6 start conducting which force QB to become low.
- Due to internal feedback action, a logic ‘1’ is set at Q (Q = ‘1’) while QB becomes low (QB = ‘0’).
- During read operation, RBL is pre charged to VDD. WR and CS are raised to high level. As a result, M10 is ON.
- Now, if a logic ‘0’ (Q= ‘0’ and QB = ‘1’) is stored in the cell then RBL is discharged to ground through transistors M8-M3-M10.
- However, if a logic ‘1’ (Q= ‘1’ and QB = ‘0’) is stored in the cell then BL remains at its pre charged level VDD as M3 is OFF.
- Thus, in the proposed single ended 10T cell, RBL is conditionally discharged to ground.
- During hold mode, WWL and WL are set to low while CS is kept high. Transistor M10 is therefore remains ON in hold mode.
- The two cross-coupled inverters retain the data if the cell supply voltage is ON.

## 3.7 BER

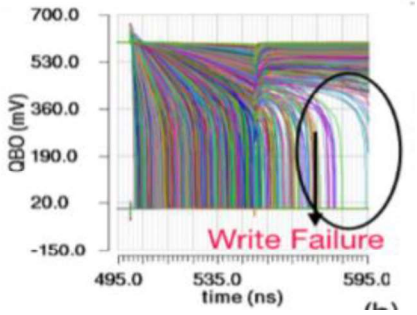
The proposed SE 6T SRAM has higher read margin and comparable write margin to the conventional 6-T SRAM cell. The proposed SE6T SRAM cell has lower hold-margin as compared to conventional SRAM, but this is sufficient enough to hold data during the hold operation. While SNM is calculated based on DC analysis of SRAM cell, bit-error rate (BER) is obtained from transient analysis which captures both static and dynamic properties of the cell. Therefore, in further analysis we have used BER. In multimedia applications SRAM access frequency is typically of the order of 10 MHz Hence, in our work, BER analysis of the SRAM cells is done at 20 MHz (twice of maximum operating frequency). A 1 KB (256x32 bits) embedded SRAM memories is designed in UMC-65 nm technology and compared the results. For 1 KB memory, 20 MHz operating frequency is achievable at a voltage of 0.48 V (in slow NMOS and slow PMOS corner). Hence, all the analyses are done for low supply voltage ranging from 0.550.65 V keeping a minimum 70 mV margin. This margin is added to avoid large errors obtained under process variations at 0.48V. The stability analysis of the SRAM cell is done in terms of bit error rate (BER) at a given voltage considering 6-sigma inter-die local and global process variation and mismatch. A maximum of 100000 Monte-Carlo (M-C) simulations are performed under worst-case process corner in hold, read and write operations of a cell in 1 KB designed memory at 20 M Hz. Total BER is the sum of write BER, read BER and hold BER. For our proposed SE6T SRAM cell there were no read or hold failures found across any process corner, but large write failures were found especially at slow NMOS fast PMOS (SNFP) corner. Figure 3.2 show the 10000 M-C waveforms of write-1 and write-0 operations, respectively. QB node is shown as it updates later than Q. As shown in Figure, write-1 failures are due to timing violations (write-time provided is less than write delay), whereas write-0

failures are the functional failures when write condition ‘PGL> PUL’ is not fulfilled. Both write1 and write-0 errors can be reduced by increasing the width of PGL. Since read and write are decoupled only PGL needs to be sized. Figure shows the 10000 M-C simulated waveform of QB node of conventional 6-T SRAM cell during read operation under worst case process corner fast NMOS and slow PMOS (FNSP). While we expect QB and Q nodes of SRAM cell to remain unaffected during the read operation, this does not happen because of read-disturb they get affected in conventional 6-T SRAM cells and cause read failures as shown in Figure.

## 3.8 NOISE MARGIN




During write-0 operation and 10000 M-C waveform of conventional 6-T SRAM cell during read. Operating voltage = 600 M v



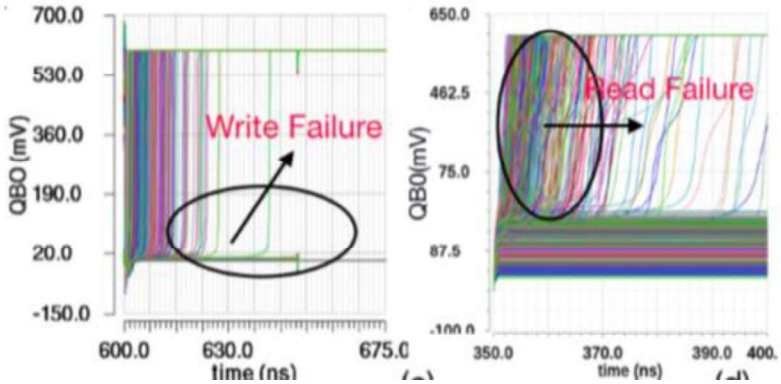



**Figure 3.2 10000 M-C wave form of SE6T SRAM cell during write-1 operation**

To summarize, at lower voltages large write failures occur at SNFP corner in the proposed SE6T SRAM cell, whereas large read failures happen at FNSP corner in the conventional 6-T SRAM cell. To reduce the BER, the SRAM cells are sized. Interestingly, in the proposed SE6T SRAM cell only one transistor needs to be sized, whereas in the conventional 6T SRAM cell, all the transistors have to be proportionally sized. Thus, for lower BER the design incurs very little area and power penalty compared to 6T SRAM cell.

## 3.9 COMPARISON OF SE6T AND 6T SRAM MEMORY FOR DIFFERENT BIT ERROR RATES

To reduce BER in conventional 6T SRAM cell, all the transistor sizes are increased which leads to an increase in area. It is observed that with minimum transistor sizes, the area of 6T SRAM cell implemented in UMC 65nm is about1.01 µm2 and that of SE6T SRAM cell is about 1.03 µm2 which are comparable.

## 3.10 BER VERSUS AREA FOR

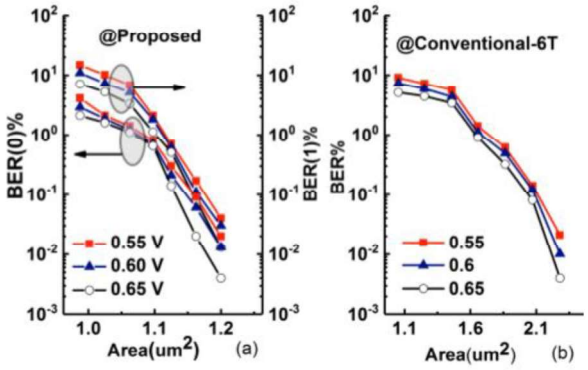



**Figure 3.3 (a) proposed SE6T SRAM cell**

**(b) conventional 6T SRAM cell, operating at 20 MHz in 1 KB array**

However, for lower BER the area of 6T SRAM cell increases significantly as compared to SE6T SRAM cell. For a total BER of 0.05% at operating voltage of 0.55-0.65V, the 6T SRAM cell takes 2.34 µm2, whereas SE6T SRAM cell takes 1.2 µm2 as only one transistor (PGL) needs to be sized. Figure 3.3 (a) and 3.3 (b) show BER with respect to cell area for SE6T and 6T SRAM cells, respectively, for different supply voltages. It is evident from the graph that SE6T cell area increases by only 15% for minimum BER of 0.05%, as compared to about 130% in 6T SRAM cell. The layouts of SE6T and conventional 6T SRAM cells of minimum and maximum sizes are shown in Figure 3.4. The maximum sizes are those required to obtain BER=0.05.

Layout representation of

(a) minimum size SE6T SRAM

(b) maximum size SE6T SRAM

(c) minimum size conventional 6-T SRAM (d) maximum size conventional 6T SRAM in UMC-65 nm technology

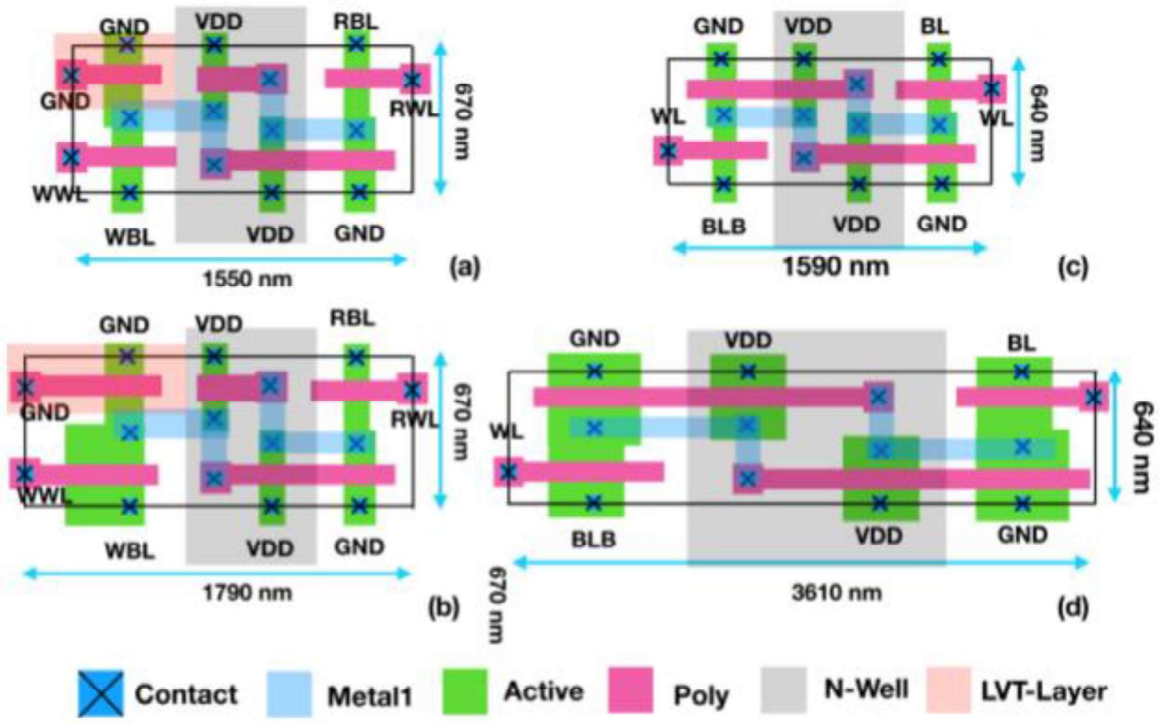



**Figure 3.4 Layout of minimum size SE6T SRAM and maximum size SE6T SRAM.**

**Fig. 3.4(a) and Fig.3.4(b) shows the impact of area increase on dynamic power (read + write) and leakage power of SE6T SRAM cell and conventional 6T SRAM cell respectively**.

For minimum area, the dynamic power of SE6T SRAM cell is 0.16 µW/bit, whereas for 6T SRAM cell it is 0.35µW/bit. The leakage power of SE6T SRAM cell is 30 pW/bit whereas for 6T SRAM cell it is 18 pW/bit. This increased leakage power in SE6T SRAM is because of use of LVT for PDL to preserve hold-0 operation. For BER=0.05, both SE6T and 6T SRAMs are resized (use increased sizes) and dynamic power for SE6T for the resized SRAM cell is 0.37 µW/bit, whereas for 6T SRAM cell it is 0.90 µW/bit. Similarly, leakage for resized SE6T cell is 41.25 pW/bit and that in 6T SRAM cell is 60 pW/bit

Dynamic and leakage power per bit versus cell area for

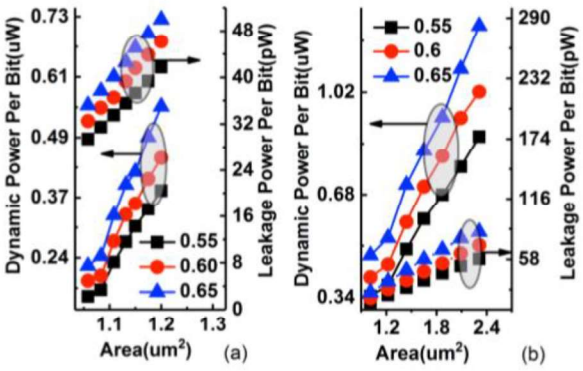



**Figure 3.5 (a) SE6T SRAM Cell**

**(b) conventional 6T SRAM Cell, both operating at 20 MHz in 1 KB array**

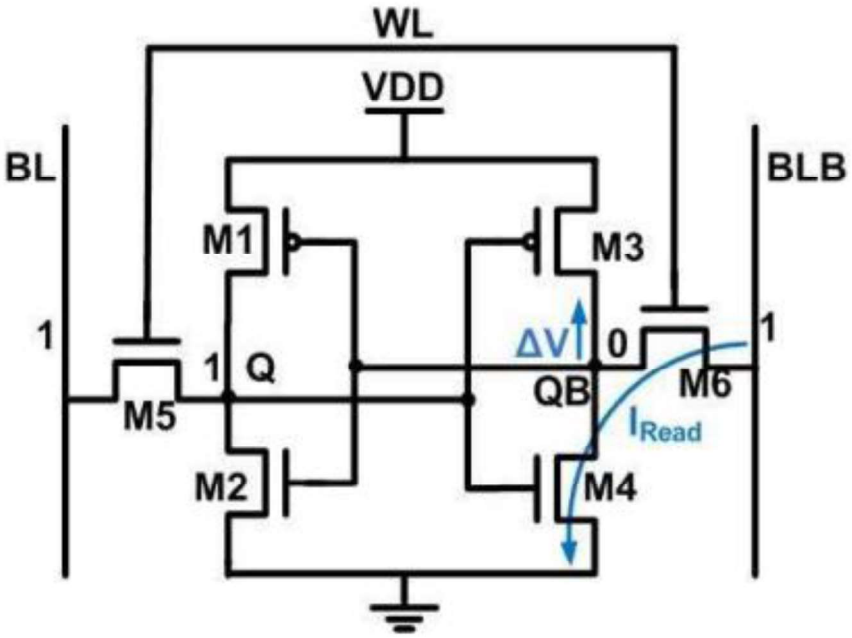



**Figure 3.6 6T SRAM cell**

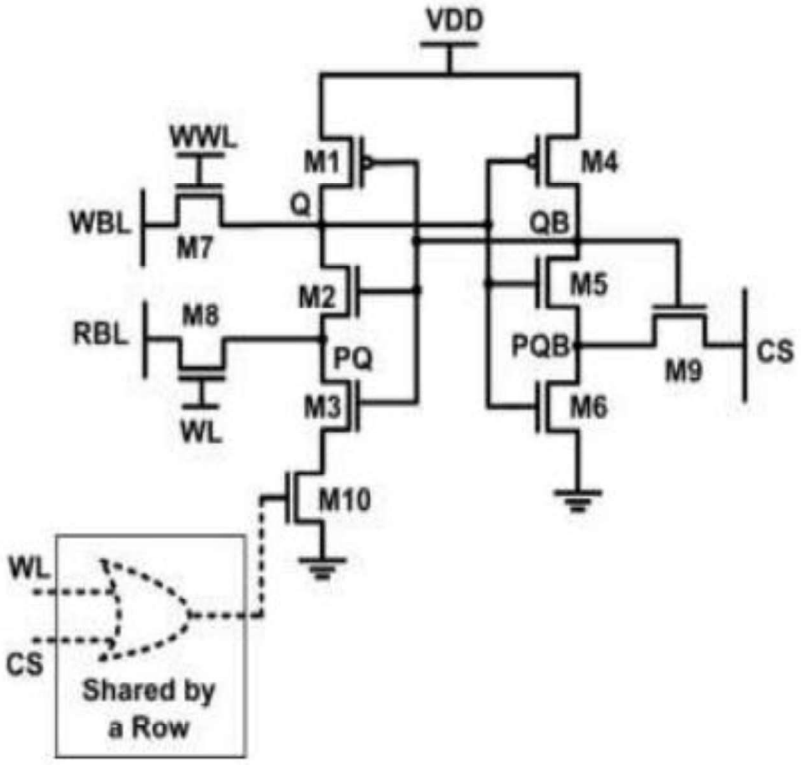



**Figure 3.7 Proposed system (10T SRAM Cell)**

| Operation | WWL | WL | CS | WBL | RBL |
|---|---|---|---|---|---|
| Write0 | '1' | '1' | '0' | '0' | '0' |
| Write1 | '1' | '0' | '0' | '1' | '1' |
| Read | '0' | '1' | '1' | 'X' | '1' |
| Hold | '0' | '0' | '1' | 'X' | '1' |

**Table 3.3 Truth table of the proposed 10T SRAM cell**

SRAM is a type of semiconductor memory which has the ability to retain data as long as the power is turned on. While designing SRAM there are four important design criteria: access time, density, noise margin, and power consumption. It is very difficult to simultaneously achieve all of these constraints at the same time. So depending on

the application, the design needs to be focused to optimize one or more of these design constraints. Similarly, there are several SRAM structures depending upon what is of utmost importance for the application. This subsection briefly highlights several such structures and shows the values of CNT size used for various of these topologies. These numbers of CNTs per transistor are chosen to optimize SRAM cells performance and functionality. It is however important to note the significant difference between CMOS based SRAM and CNTFET based SRAM.

## 3.11 PROPOSED SYSTEM TRUTH TABLE

| IN1 | IN2 | IN3 | IN4 | OUT1 | OUT2 |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 |

| | | | | | |
|---|---|---|---|---|---|
| **1** | **0** | **1** | **1** | **0** | **1** |
| **1** | **1** | **0** | **0** | **1** | **0** |
| **1** | **1** | **0** | **1** | **1** | **0** |
| **1** | **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** | **1** |
| | | | | | |
| **1** | **1** | **1** | **1** | **1** | **1** |

**Table 3.4 Truth table of proposed system**

## 3.12 SOFTWARE REQUIREMENTS

### 3.12.1 DSCH

- DSCH is a software for logic design. Based on primitives, a hierarchical circuit can be built and simulated. It also includes delay and power consumption evaluation.
- Silicon is for 3D display of the atomic structure of silicon, with emphasis on the silicon lattice, the dopants, and the silicon dioxide.

#### 3.12.1.1 NOR EXAMPLE

- We will learn both the design flow and the CAD tools.
- The specifications we are going to see may be different for different foundry and technology.
- Design Example (3 Levels) : NOR Gate – Logic Design – Circuit Design – Layout Design
- Microwind / DSCH NOR Example: Logic
- Open the Schematic Editor in Microwind (DSCH3).

- Click on the transistor symbol in the Symbol Library on the right.
- • Instantiate NMOS or PMOS transistors from the symbol library and place them in the editor window.

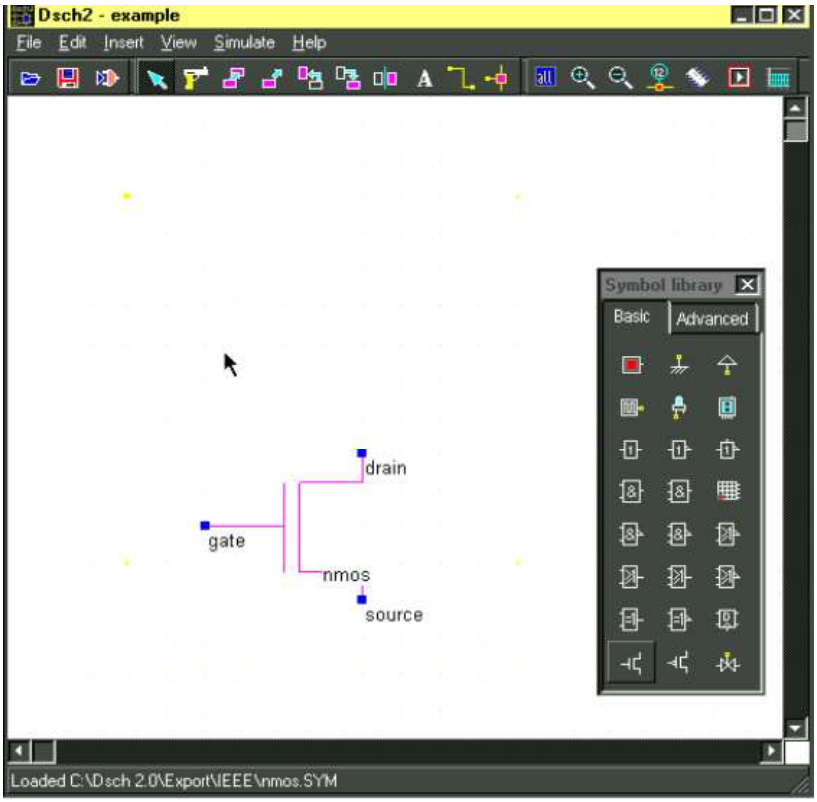



**Figure 3.8 Circuit of NOT gate.**

DSCH is a software for logic design. Based on primitives, a hierarchical circuit can be built and simulated. It also includes delay and power consumption evaluation. Silicon is for 3D display of the atomic structure of silicon, with emphasis on the silicon lattice, the dopants, and the silicon dioxide.

The DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex logic structures. DSCH also features the symbols ,

models and assembly support for 8051 and PIC16F84 controllers. Designers can create logic circuits for interfacing with these controllers and verify software programs using DSCH.

- User-friendly environment for rapid design of logic circuits.
- Supports hierarchical logic design.
- Added a tool on fault analysis at the gate level of digital. Faults: Stuck-at-1,stuck-at-0.

  The technique allows injection of single stuck-at fault at the nodes of the circuit.
- Improved interface between DSCH and Winspice.
- Handles both conventional pattern-based logic simulation and intuitive on-screen mouse-driven simulation.

- Built-in extractor which generates a SPICE netlist from the schematic diagram

  (Compatible with PSPICETM and WinspiceTM ).
- Generates a VERILOG description of the schematic for layout conversion.
- Immediate access to symbol properties (Delay, fanout).
- Sub-micron, deep-submicron, nanoscale technology support.
- Supported by huge symbol library

### 3.12.2 MICROWIND

1. The MICROWIND software allows the designer to simulate and design an integrated circuit at physical description level. Born in Toulouse (France), Microwind is an innovative CMOS design tool for educational market.

2. Microwind is developed as comprehensive package on windows platform to enable students to learn smart design methods and

techniques with more practice. With inbuilt layout editing tools, mix-signal simulator, MOS characteristic viewer and more, it allows students to learn complete design process with ease.

3. Microwind unifies schematic entry, pattern-based simulator, SPICE extraction of schematic, Verilog extractor, layout compilation, on layout mix-signal circuit simulation, cross sectional & 3D viewer, netlist extraction, BSIM4 tutorial on MOS devices and sign-off correlation to deliver unmatched design performance and productivity.

4. With its approach for CMOS design education, Microwind has gained lot followers worldwide. Universities across the globe are using Microwind for budding engineers to teach CMOS concepts with ease. Paving their path for more skilled softwares to be used at later stage of their course work.

5. Microwind is a tool for designing and simulating circuits at layout level. The tool features full editing facilities (copy, cut, past, duplicate, move), various views (MOS characteristics, 2D cross section, 3D process viewer), and an analog simulator.

# CHAPTER 4

# RESULTS AND DISCUSSION

## 4.1 DSCH DESIGN

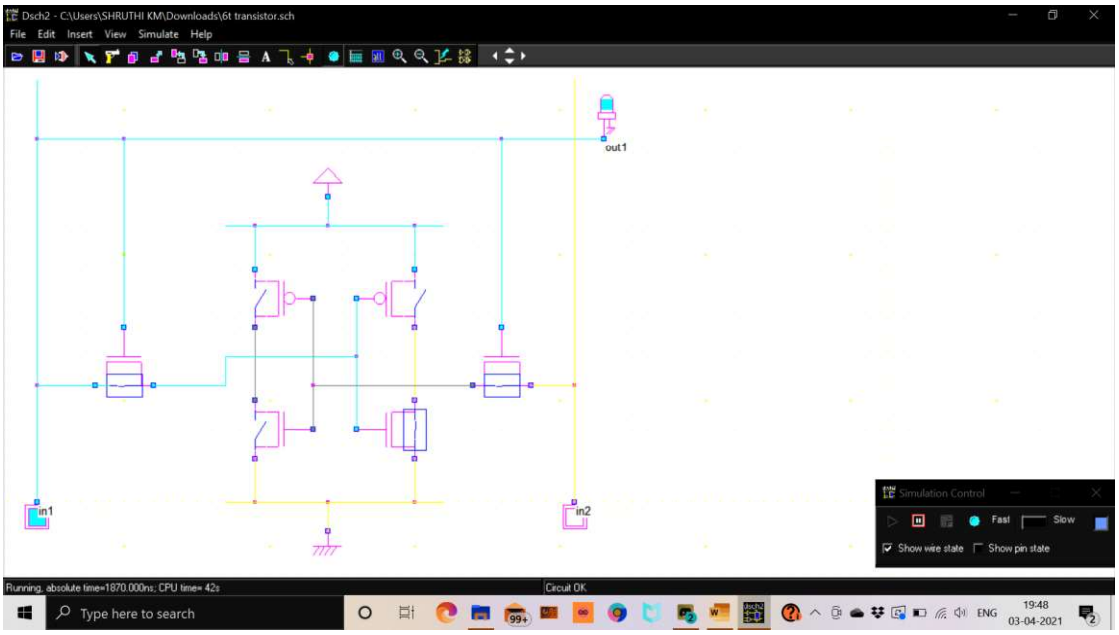



**Figure 4.1 a) Circuit of 6T SRAM Cell**

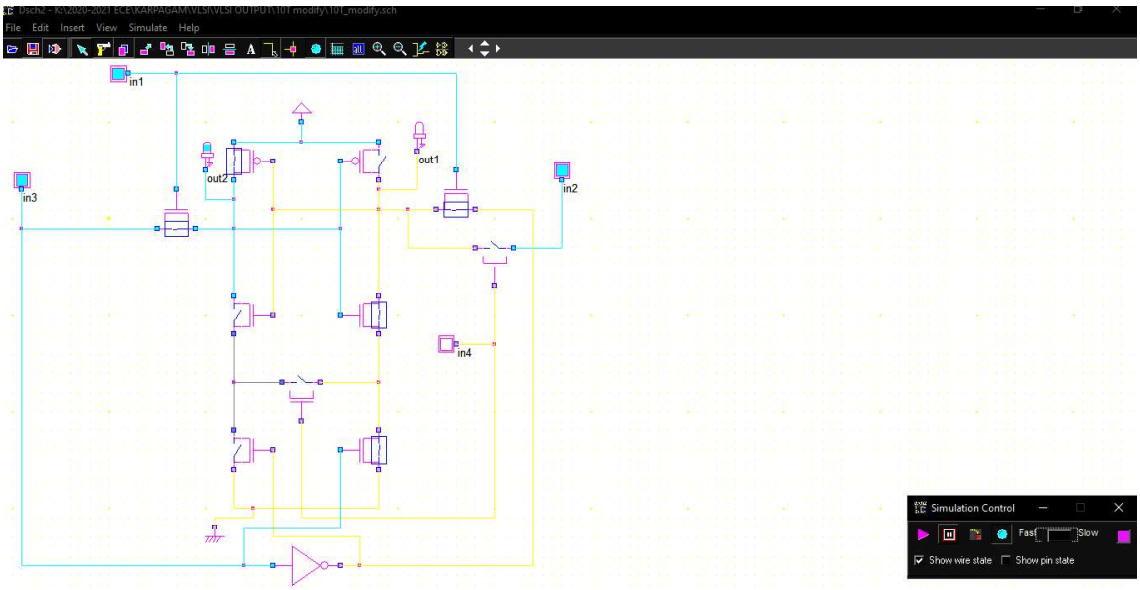



**Figure 4.1 b) Circuit of 10T SRAM cell**

From the above Figures 4.1 (a) and 4.1 (b), the circuit of 6T SRAM cell and 10T SRAM cell is designed using the symbol library in the Digital Schematic software. The requirements of the circuit is dragged to the main screen and connected using wires to design the circuit of the SRAM cells.

## 4.2 DSCH-SCHEMA TO SYMBOL

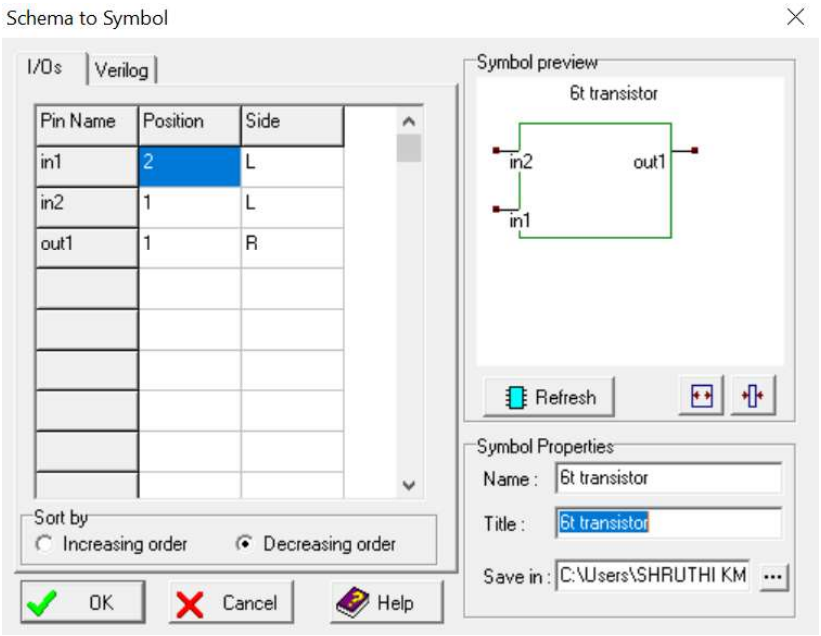



**Figure 4.2 a) DSCH schema to symbol of 6T SRAM cell**

From the above figure, the schematic of the 6T SRAM cell is obtained. There are two inputs and one output which is shown in the schematic. Whereas in 10T SRAM cell, the cell consists of four inputs and two outputs.

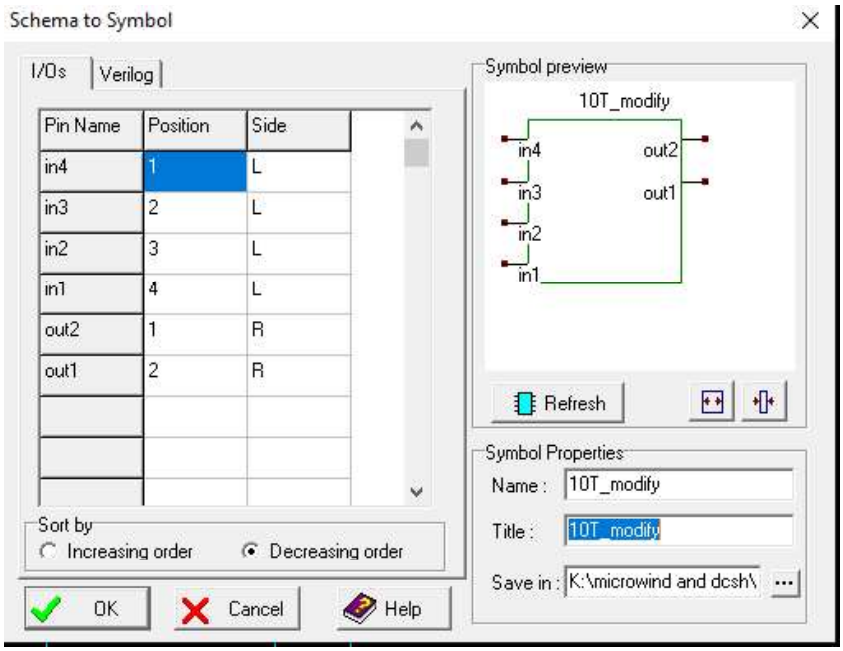



**Figure 4.2 b) DSCH schema to symbol of 10T SRAM cell**

## 4.3 DSCH- TIMING DIAGRAM


**Figure 4.3 a) DSCH Timing diagram of 6T SRAM Cell**

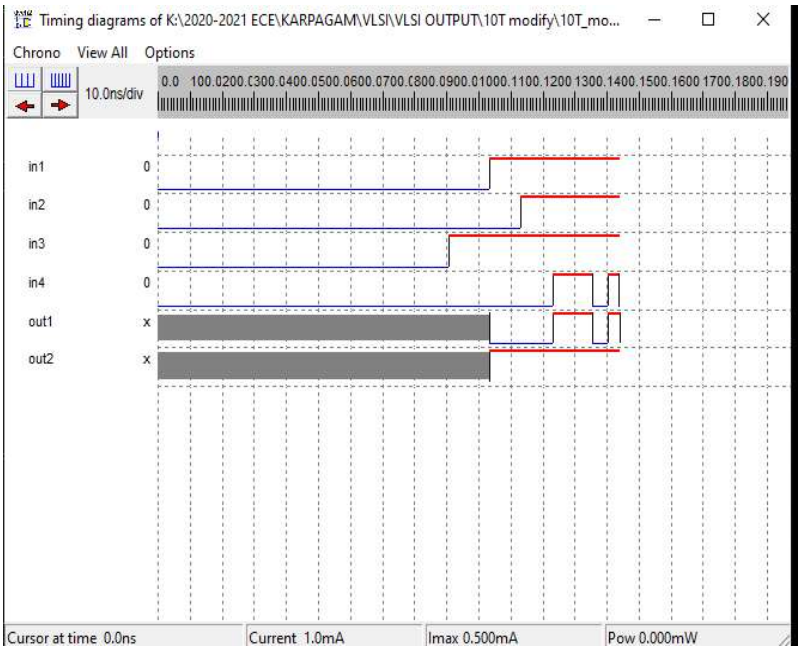



**Figure 4.3 b) DSCH timing diagram of 10T SRAM cell**

From the above Figures 4.3 (a) and 4.3 (b), for different inputs given to the two SRAM cells, we get the corresponding Digital Schematic (DSCH) timing diagram.

## 4.4 VERILOG FILE

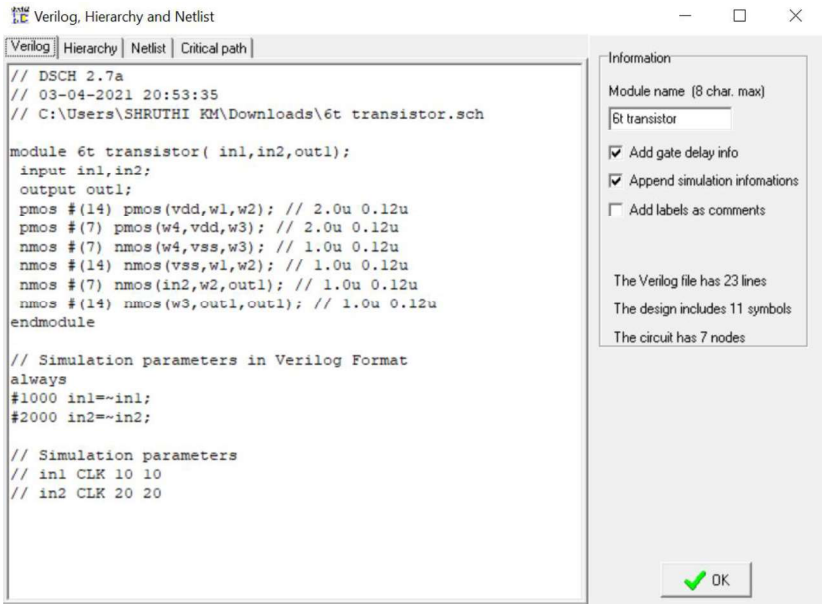


**Figure 4.4 a) Verilog file for 6T SRAM cell**

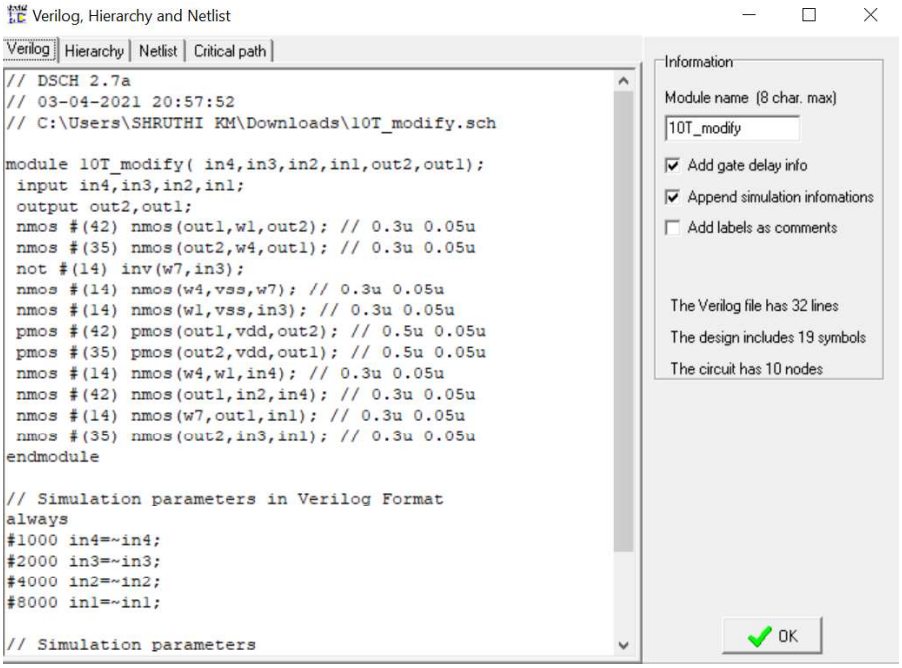



**Figure 4.4 b) Verilog file for 10T SRAM cell**

From the above Figures 4.4 (a) and 4.4 (b), Verilog code for 6T SRAM cell and 10T SRAM cell is obtained. For different SRAM cells designed in Digital Schematic software, Verilog code is generated in the same software.

## 4.5 MICROWIND OUTPUT

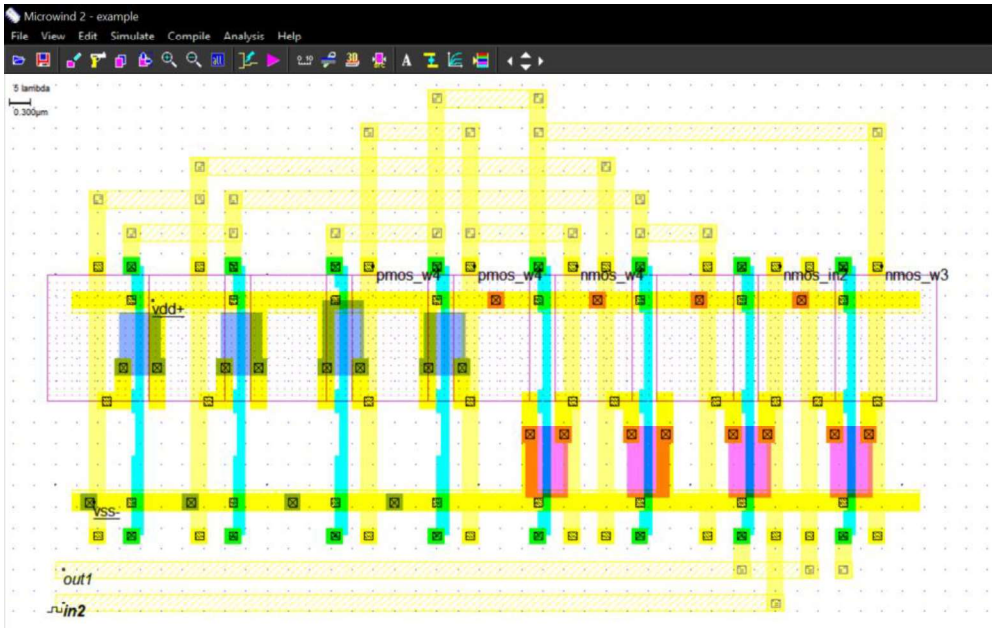



**Figure 4.5 a) Microwind output for 6T SRAM cell**

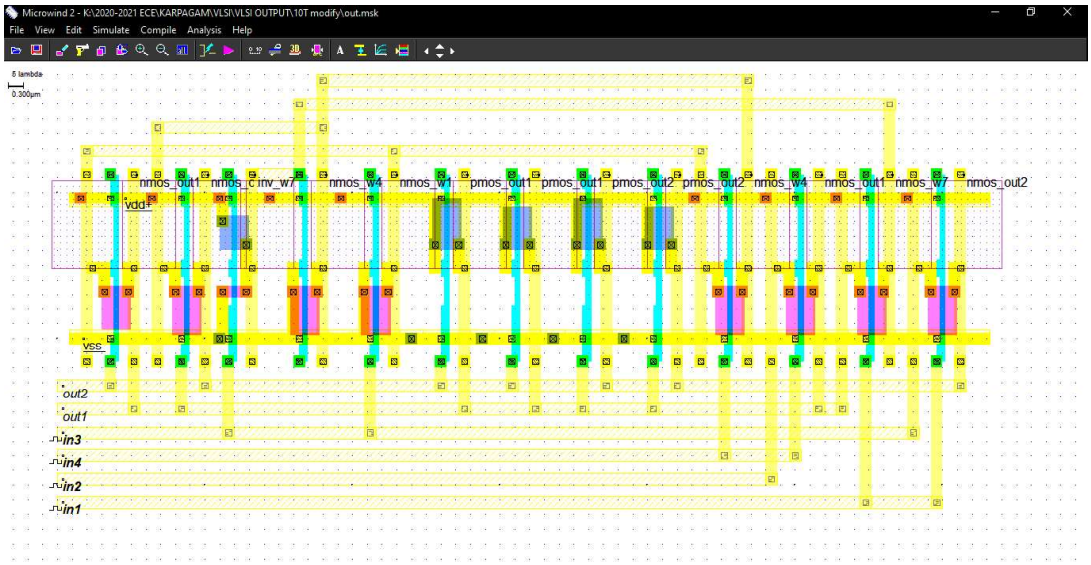



**Figure 4.5 b) Microwind output for 10T SRAM cell**

From the above Figures 4.5 (a) and 4.5 (b), the microwind output is obtained for 6T SRAM cell and 10T SRAM cell which gives the layout level diagram of the cells.

## 4.6 MICROWIND OUTPUT WITH TIMING DIAGRAM

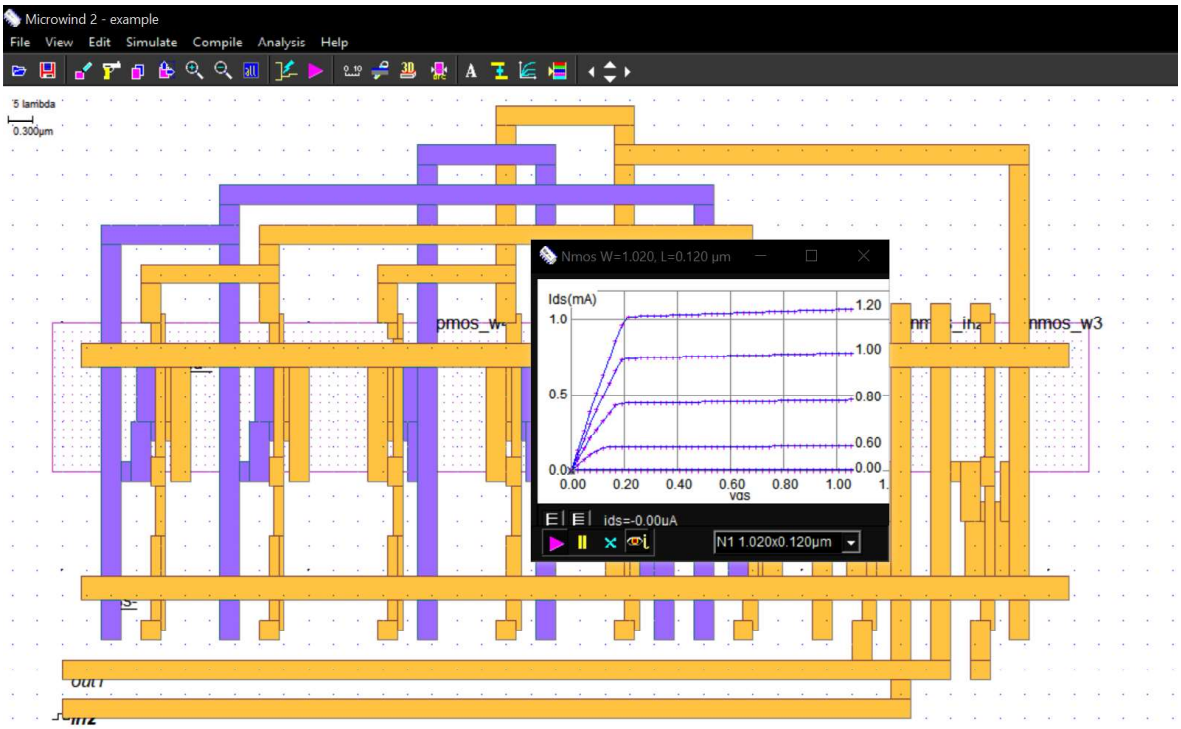



**Figure 4.6 a) Microwind output with timing diagram for 6T SRAM cell**

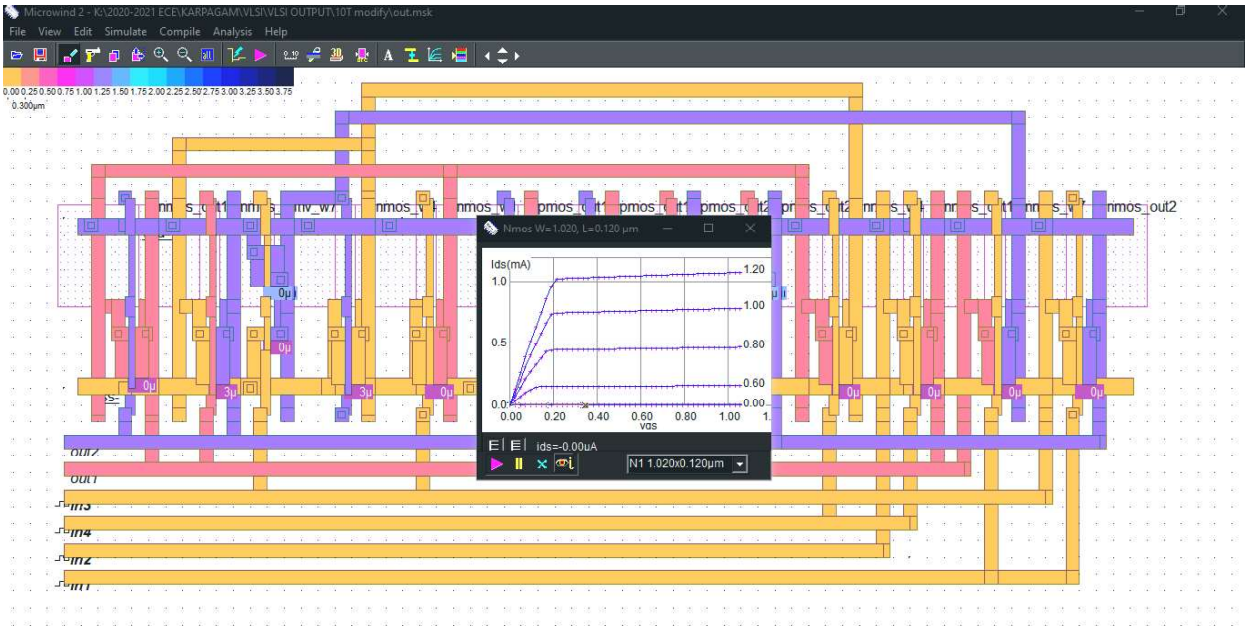



**Figure 4.6 b) Microwind output with timing diagram for 10T SRAM cell**

# 4.7 MICROWIND WAVEFORM

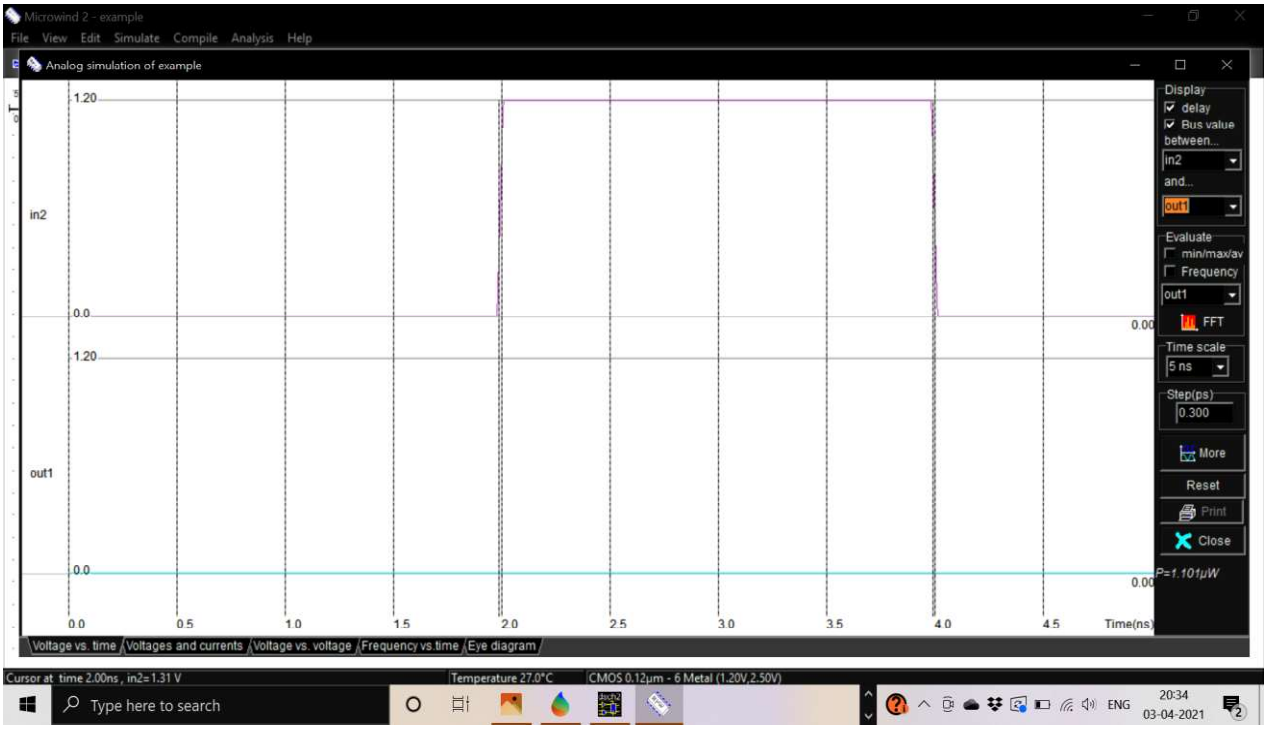



**Figure 4.7 a) Microwind waveform for 6T SRAM cell**

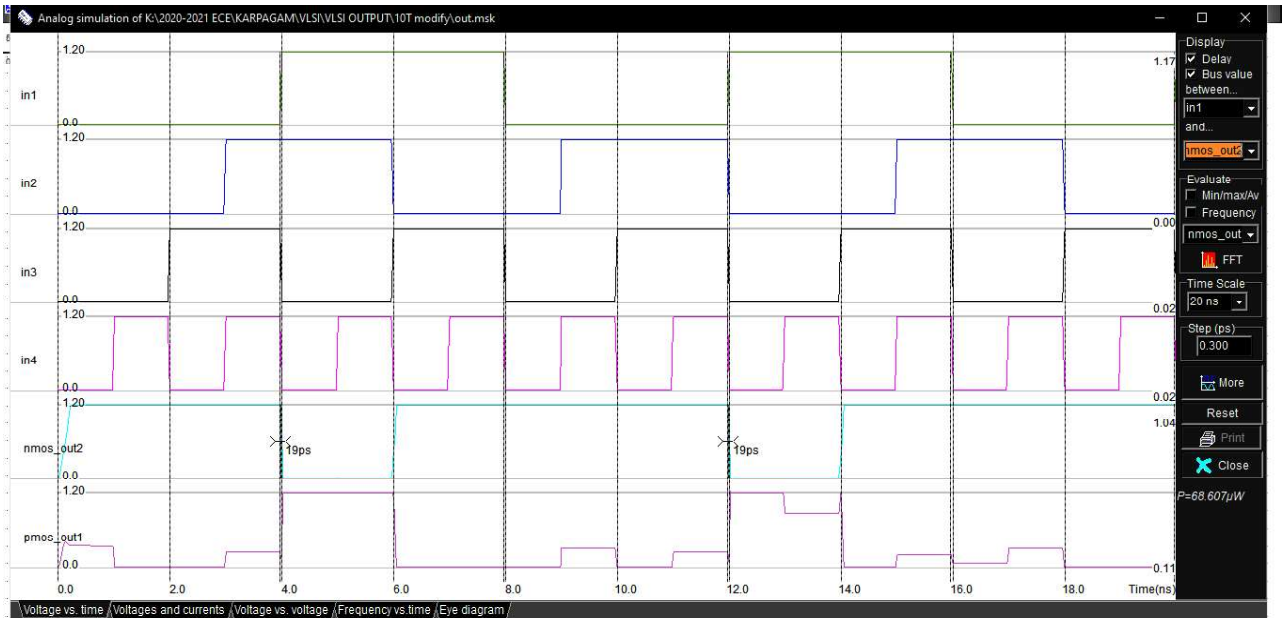



**Figure 4.7 b) Microwind waveform for 10T SRAM cell**

From the above Figures 4.7 (a) and 4.7 (b), the voltage vs voltage, voltage and currents, voltage and time , frequency vs time and eye diagram is obtained for 6T SRAM cell and 10T SRAM cell. For each waveforms, the power consumption is obtained.

## 4.8 AREA EFFICIENCY

| MOS SIZE (µm) | 6T Static Random Access Memory (SRAM) Cell | 10T Static Random Access Memory (SRAM) Cell |
|---|---|---|
| Width of PMOS transistor | 0.720µm | 0.720µm |
| Length of PMOS transistor | 0.120µm | 0.120µm |
| Width of NMOS transistor | 0.240µm | 0.240µm |
| Length of NMOS transistor | 0.120µm | 0.120µm |

**Table 4.1 Width and the length of MOS Transistors for 6T SRAM cell and 10T SRAM cell**

From the above table, it is inferred that the width and length of the PMOS and NMOS transistors of the two SRAM cells is the same. Hence the proposed cell is area efficient as it uses the same area as that of the conventional 6T SRAM Cell.

# CHAPTER 5

## 5.1 CONCLUSION

A Novel 10T SRAM cell is accessible in this paper for high read stability and low energetic power consumption. For low leakage and high-speed circuits concern should be on both the factors speed and power. The proposed 10T SRAM cell provides two separate data access mechanisms for read and write operations. During the read operation, the data storage nodes are completely isolated from the bit lines, thereby improving the read SNM by twice as compared to the read SNM of the conventional 6T SRAM cell. During the write operation, the SRAM cell utilizes the charging/discharging of only one-bit line (BL), resulting in reduction of dynamic power consumption as compared to conventional 6T SRAM cell. Different techniques have been analyzed to reduce the standby leakage current and dynamic power dissipation of the SRAM cell.

## 5.2 FUTURE SCOPE

To perform the write operation in the SRAM cell to flip the data value, nearly full voltage swings is required on the bit line. This full voltage swing on the highly capacitive bit lines will consume a greater amount of power according to the law of CV^2f.Thus voltage swing reduction is an effective way to decrease the power dissipation. The future course of action involves effective reduction of leakage in an SRAM cell. It is proposed here that appropriate leakage reduction techniques would be developed with an emphasis on the reduction of gate voltage. Leakage reduction in SRAM is also possible using self controllable switch either at the upper end of the cell to reduce voltage (USR scheme) or at the lower end of the cell to raise the potential of the ground node (LPR scheme). This method would also be tested for its efficacy when this work is advanced.

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