

AXI4 Lite bus protocol signals

Read Address Channel

Name	Description
ARADDR	Read address (32 bit wide)
ARVALID	Master generates this signal when Read Address and the control signals are valid.
ARREADY	Slave generates this signal when it can accept the read address and control signals.

Read Data Channel

Name	Description
RDATA	Read data (32 bits)
RVALID	Slave generates this signal when Read Data is valid
RREADY	Master generates this signal when it can accept the Read Data and response.

Write Address Channel

Name	Description
AWADDR	Write address (32 bits wide)
AWVALID	Master generates this signal when Write Address and control signals are valid
AWREADY	Slave generates this signal when it can accept Write Address and control signals

Write Data Channel

Name	Description
WDATA	Write data (32 bits)
WVALID	Master generates this signal when valid data is present on the data bus
WREADY	Slave generates this signal indicating that memory accepts the data

Write Response Channel

Name	Description
BVALID	This signal indicates successful completion of data received during a write operation
BREADY	Master generates this signal when it can accept a write response

Global Signals

Name	Description
Clk	Clock source
Reset	Global reset source