PROJECT

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ECE Roll-77

1. ELECTRONICS LOCK

Type -1

DESIGN.SV

module electronic\_lock(input clk,rst,input b ,output unlock,reg [2:0]state);

reg [2:0]st;

parameter SRST = 3'd0 ,S0 = 3'd1 , S01= 3'd2 ,S010 = 3'd3, S0101= 3'd4 , S01011 = 3'd5 ;

always @(posedge clk) begin

if(rst)

st <= SRST;

else

case(st)

SRST : if(b==0) st= S0; else st = SRST;

S0 : if(b==0) st= S0; else st = S01;

S01 : if(b==0) st= S010; else st = SRST;

S010 : if(b==0) st= S0; else st = S0101;

S0101 : if(b==0) st= S010; else st = S01011;

S01011 : if(b==0) st= S0; else st = SRST;

default st = SRST;

endcase

end

assign unlock = (st== S01011) ;

assign state = st;

endmodule

TESTBENCH

module tb\_electronic\_lock;

wire [2:0]t\_st;

wire t\_out;

reg t\_b,t\_clk, t\_rst ;

reg [18:0]data;

integer i=0;

electronic\_lock m(t\_clk, t\_rst, t\_b, t\_out,t\_st);

always #10 t\_clk= ~t\_clk;

initial fork

$dumpfile("tb\_electronic\_lock.vcd");

$dumpvars(1,tb\_electronic\_lock);

$monitor(" i= %0d, Time= %0d, button = %b, data=%b, out= %b state=%d", i,$time,t\_b,data[i],t\_out,t\_st);

t\_clk=0;

t\_rst =1;

data = 19'b1111010100101101011 ;

#20 t\_rst = 0;

#370 $finish;

join

always @(posedge t\_clk) begin

t\_b = data[i];

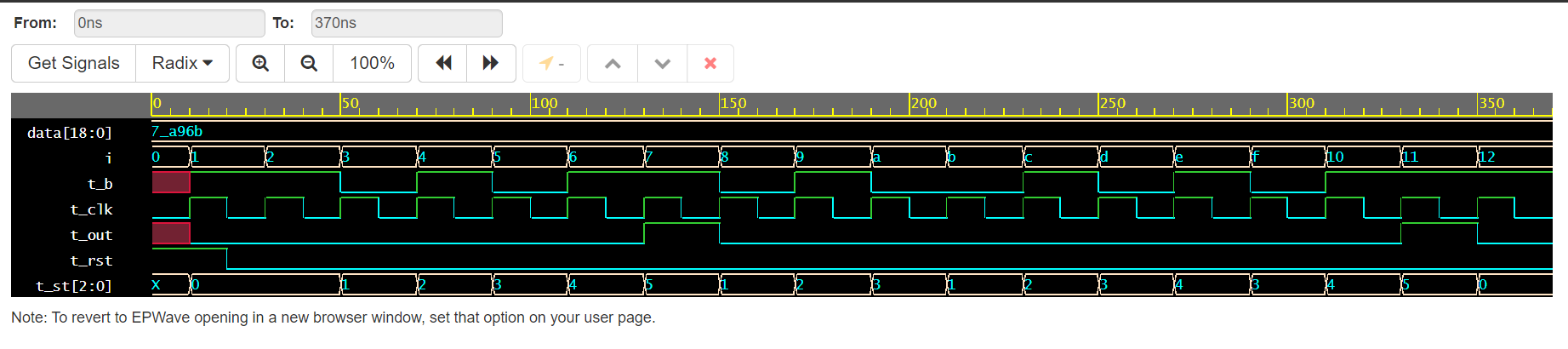
i = i+1;

end

endmodule

OUTPUT

i= 0, Time= 0, button = x, data=1, out= x state=x  
 i= 1, Time= 10, button = 1, data=1, out= 0 state=0  
 i= 2, Time= 30, button = 1, data=0, out= 0 state=0  
 i= 3, Time= 50, button = 0, data=1, out= 0 state=1  
 i= 4, Time= 70, button = 1, data=0, out= 0 state=2  
 i= 5, Time= 90, button = 0, data=1, out= 0 state=3  
 i= 6, Time= 110, button = 1, data=1, out= 0 state=4  
 i= 7, Time= 130, button = 1, data=0, out= 1 state=5  
 i= 8, Time= 150, button = 0, data=1, out= 0 state=1  
 i= 9, Time= 170, button = 1, data=0, out= 0 state=2  
 i= 10, Time= 190, button = 0, data=0, out= 0 state=3  
 i= 11, Time= 210, button = 0, data=1, out= 0 state=1  
 i= 12, Time= 230, button = 1, data=0, out= 0 state=2  
 i= 13, Time= 250, button = 0, data=1, out= 0 state=3  
 i= 14, Time= 270, button = 1, data=0, out= 0 state=4  
 i= 15, Time= 290, button = 0, data=1, out= 0 state=3  
 i= 16, Time= 310, button = 1, data=1, out= 0 state=4  
 i= 17, Time= 330, button = 1, data=1, out= 1 state=5  
 i= 18, Time= 350, button = 1, data=1, out= 0 state=0

WAVEFORM

Type – 2

DESIGN.SV

module electronic\_lock(input clk,rst,b0,b1,output unlock,reg [2:0]state);

reg [2:0]st;

parameter SRST = 3'd0 ,S0 = 3'd1 , S01= 3'd2 ,S010 = 3'd3, S0101= 3'd4 , S01011 = 3'd5 ;

always @(posedge clk) begin

if(rst)

st <= SRST;

else

case(st)

SRST : if(b0) st= S0; else if(b1) st = SRST;

S0 : if(b0) st= S0; else if(b1) st = S01;

S01 : if(b0) st= S010; else if(b1) st = SRST;

S010 : if(b0) st= S0; else if(b1) st = S0101;

S0101 : if(b0) st= S010; else if(b1) st = S01011;

S01011 : if(b0) st= S0; else if(b1) st = SRST;

default st = SRST;

endcase

end

assign unlock = (st== S01011) ;

assign state = st;

endmodule

TESTBENCH.SV

module tb\_electronic\_lock;

wire [2:0]t\_st;

wire t\_out;

reg t\_b0, t\_b1, t\_clk, t\_rst, temp ;

integer i=0;

reg [18:0]data;

electronic\_lock m(t\_clk, t\_rst, t\_b0, t\_b1, t\_out,t\_st);

always #10 t\_clk= ~t\_clk;

initial fork

$dumpfile("tb\_electronic\_lock.vcd");

$dumpvars(1,tb\_electronic\_lock);

$monitor(" i= %0d, Time= %0d, b0=%b, b1=%b, out= %b state=%d", i,$time,t\_b0,t\_b1,t\_out,t\_st);

t\_clk=0;

t\_rst =1;

data = 19'b1101010110101101011 ;

#20 t\_rst = 0;

#350 $finish;

join

always @(posedge t\_clk) begin

data<= data>>1 ;

temp = #10 data[0];

case(temp)

0 : begin t\_b0 <= 1; t\_b1 <=0; end

1 : begin t\_b0 <=0 ; t\_b1 <= 1; end

endcase

i=i+1;

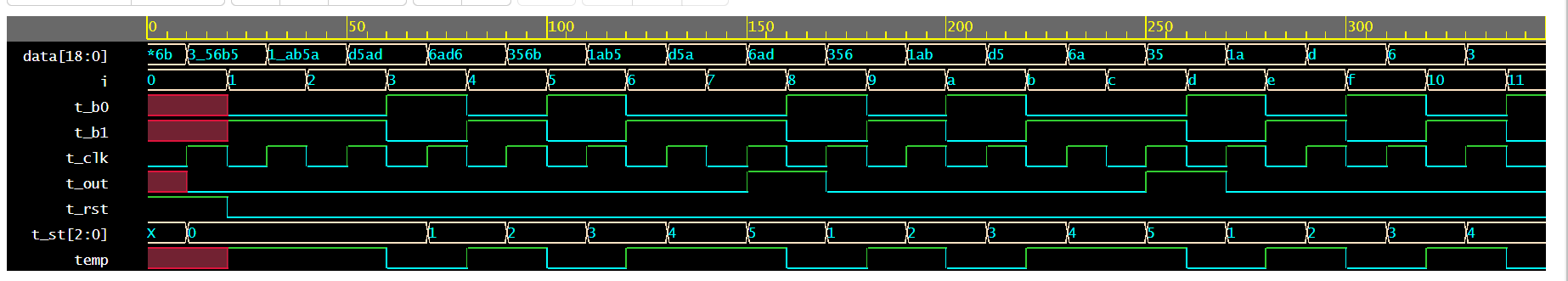
end

endmodule

OUTPUT

i= 0, Time= 0, button = x, data=1, out= x state=x  
 i= 1, Time= 10, button = 1, data=1, out= 0 state=0  
 i= 2, Time= 30, button = 1, data=0, out= 0 state=0  
 i= 3, Time= 50, button = 0, data=1, out= 0 state=1  
 i= 4, Time= 70, button = 1, data=0, out= 0 state=2  
 i= 5, Time= 90, button = 0, data=1, out= 0 state=3  
 i= 6, Time= 110, button = 1, data=1, out= 0 state=4  
 i= 7, Time= 130, button = 1, data=0, out= 1 state=5  
 i= 8, Time= 150, button = 0, data=1, out= 0 state=1  
 i= 9, Time= 170, button = 1, data=0, out= 0 state=2  
 i= 10, Time= 190, button = 0, data=0, out= 0 state=3  
 i= 11, Time= 210, button = 0, data=1, out= 0 state=1  
 i= 12, Time= 230, button = 1, data=0, out= 0 state=2  
 i= 13, Time= 250, button = 0, data=1, out= 0 state=3  
 i= 14, Time= 270, button = 1, data=0, out= 0 state=4  
 i= 15, Time= 290, button = 0, data=1, out= 0 state=3  
 i= 16, Time= 310, button = 1, data=1, out= 0 state=4  
 i= 17, Time= 330, button = 1, data=1, out= 1 state=5  
 i= 18, Time= 350, button = 1, data=1, out= 0 state=0

WAVEFORM



3.VENDING MACHINE

DESIGN.SV

module vending\_mcn(input clk,rst,input [3:0]in, output reg out, output [1:0]state);

reg [1:0]st;

parameter S0 = 2'b00 , S5= 2'b01 ,S10 = 2'b10, S15= 2'b11 ;

always @(posedge clk) begin

if(!rst)

st <= S0;

else

case(st)

S0 : if(in== 5) st= S5; else st = S10;

S5 : if(in == 5) st= S10; else if(in == 10) st = S15;

S10 : if(in == 5) st= S15; else st = S15;

S15 : if(in == 5) st= S5; else st = S10;

default st = S0;

endcase

end

assign out = (st== S15) ;

assign state =st;

endmodule

TESTBENCH.SV

module tb\_vending\_mcn;

wire t\_out;

reg t\_clk, t\_rst;

reg [1:0] state;

reg [3:0]data;

vending\_mcn m(t\_clk, t\_rst, data, t\_out, state);

always #10 t\_clk= ~t\_clk;

initial begin

$dumpfile("tb\_vending\_mcn.vcd");

$dumpvars(1,tb\_vending\_mcn);

$monitor(" Time= %0d, data=%b, out = %b", $time,data,t\_out);

t\_clk=0;

t\_rst =0;

#2 t\_rst = 1;

#9 data = 5;

#19 data = 5;

#31 data = 5;

#150 $finish;

end

endmodule

OUTPUT

Time= 0, data=xxxx, out = x  
 Time= 10, data=xxxx, out = 0  
 Time= 11, data=0101, out = 0  
 Time= 70, data=0101, out = 1  
 Time= 90, data=0101, out = 0  
 Time= 130, data=0101, out = 1  
 Time= 150, data=0101, out = 0  
 Time= 190, data=0101, out = 1  
 Time= 210, data=0101, out = 0

WAVEFORM

