MIPS Instruction Set

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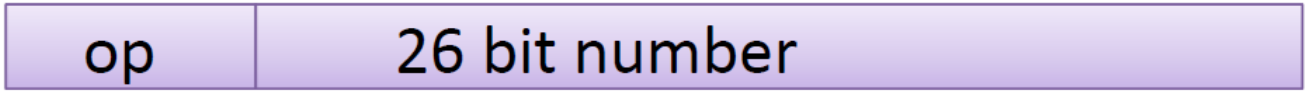
Summary of Instructions learnt

Instructions	Format
add, sub, addi, subi	R, I
and, or, andi, ori	R, I
slt, slti	R, I
beq, bne	I
j	J
lw, sw	I
lui	I

MIPS ISA features - encoding

- addi, lui, beq, bne, lw, sw I - format

- j, jal J - format



- add, jr R - format

MIPS ISA features - summary

- All instructions of same size
- Only 3 formats
- Fair number of GP registers
- Simple operations – either arith/logic or memory access or control transfer
- Limited addressing modes
- Separate fields for src1, src2 and dest

Location of operands – R/M

- R-R Both operands in registers
- R-M one operand in register and one in memory
- M-M Both operands in memory
- R+M Combines R-R, R-M and M-M

How many operand fields?

- 3 address machine — r1 = r2 + r3
- 2 address machine — r1 = r1 + r2
- 1 address machine — Acc = Acc + x

  Acc is implicit
- 0 address machine — add values on top of stack

Register organizations

- Register-less machine
- Accumulator based machine
- A few special purpose registers
- Several general purpose registers
- Large number of registers / register windows

MIPS ISA features - addressing

Purpose

Operand sources

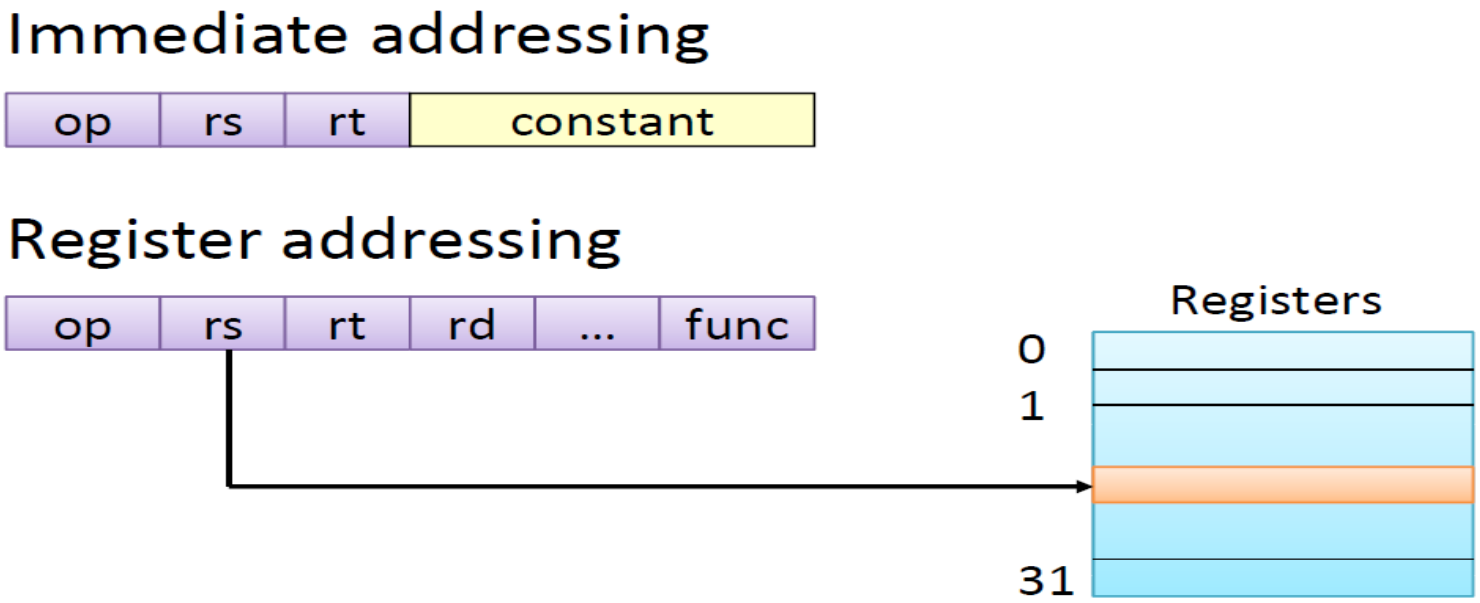
Result Destinations

Jump targets

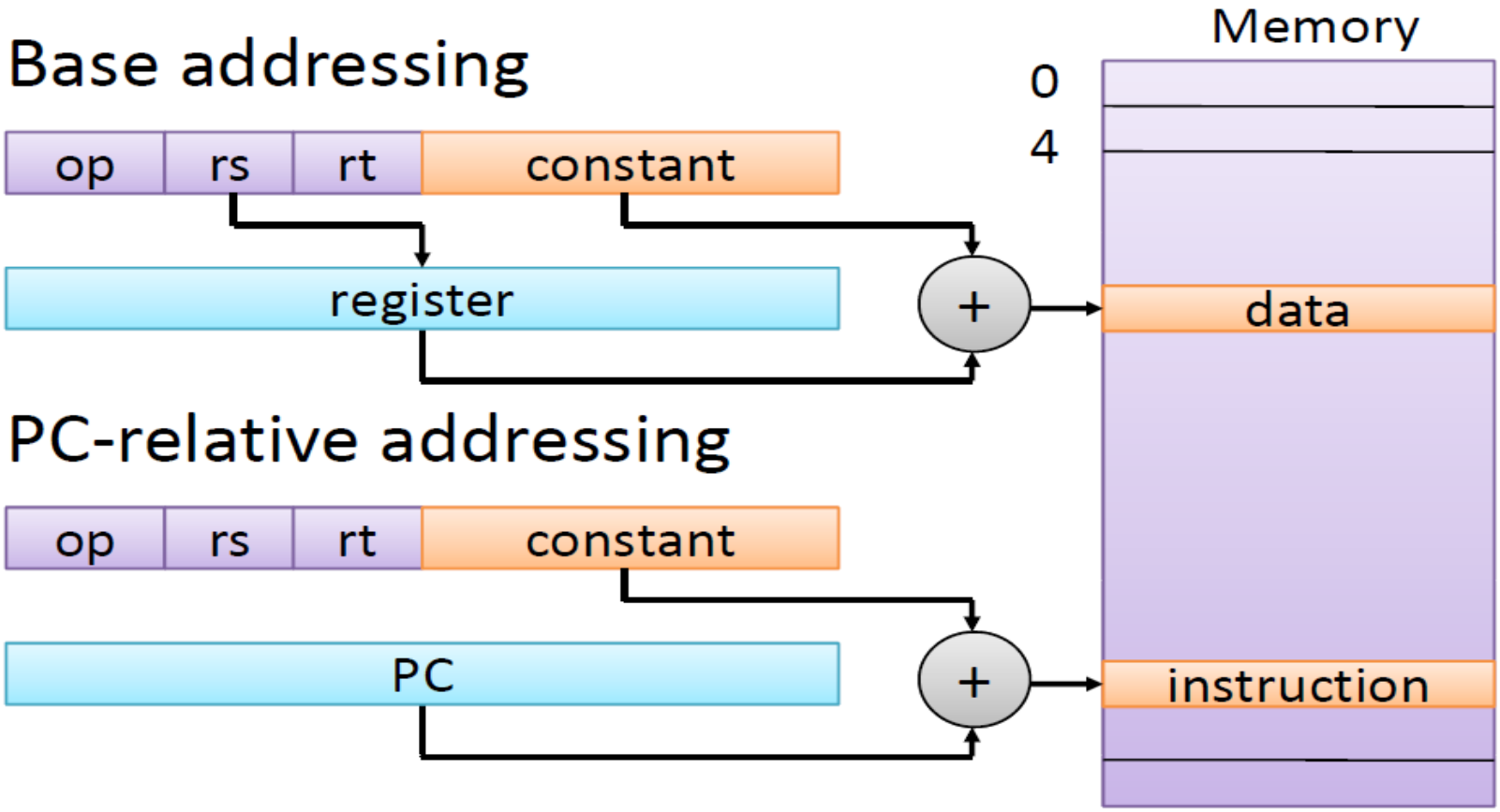
Addressing modes

- Immediate
- Register
- Base/index
- PC relative
- (pseudo) Direct
- Register indirect

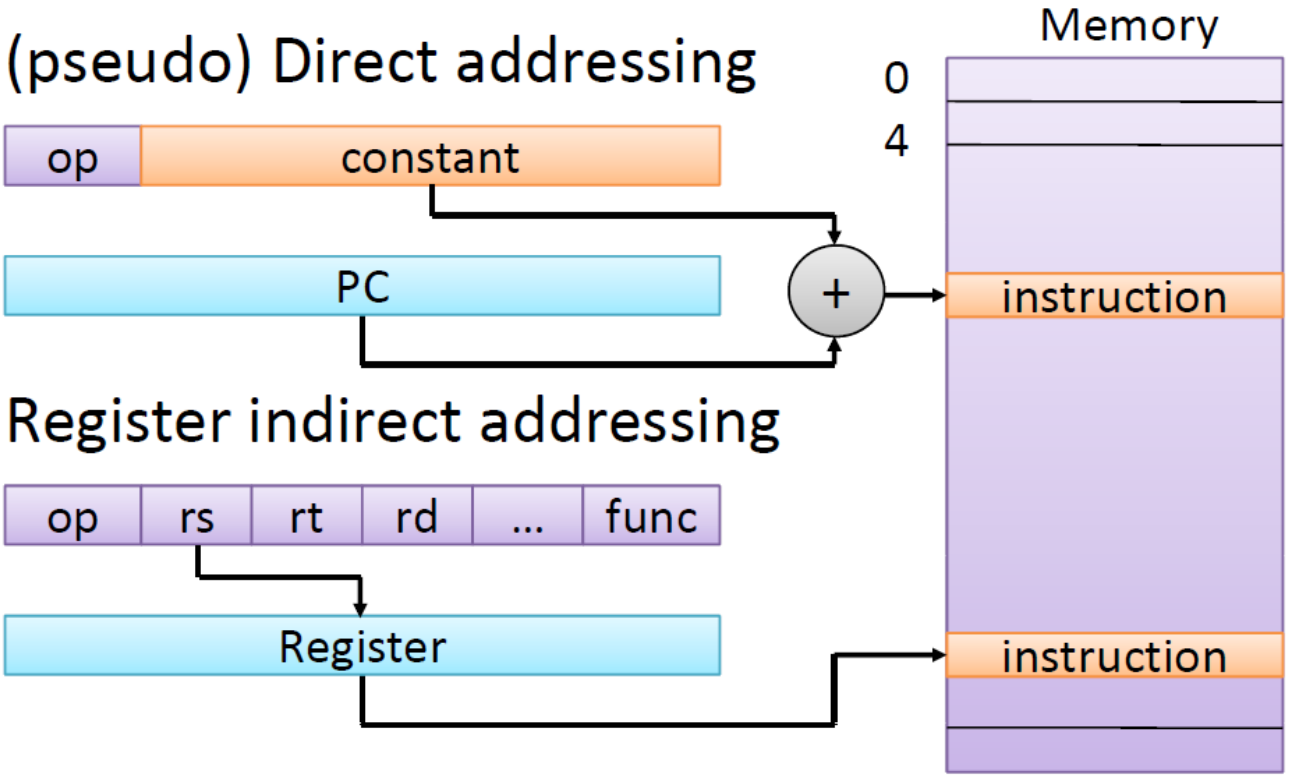
MIPS addressing modes - 1



MIPS addressing modes - 2



MIPS addressing modes - 3



RISC vs. CISC

Reduced (vs. Complex) Instruction Set Computer

- Uniformity of instructions
- Simple set of operations and addressing modes
- Register based architecture with 3 address instructions

RISC Philosophy

- 1970s John Cocke at IBM
- Majority of combinations of orthogonal addressing modes and instructions were not used
  - By most programs generated by compilers
- Difficult in many cases to write a compiler
  - To take advantage of the features provided by conventional CPUs.

RISC examples

- Virtually all new instruction sets since 1982 have been RISC
  - SUN's SPARC (S*calable* P*rocessor* ARC*hitecture*)
  - HP's PA-RISC
  - ARM (Advance RISC Machine)
  - Motorola's PowerPC (P*erformance* O*ptimization* W*ith* E*nhanced* R*ISC Performance Computing,*)
  - DEC's Alpha
  - MIPS
  - CDC 6600 (1960's)