Indian Institute of Technology BHU, Varanasi

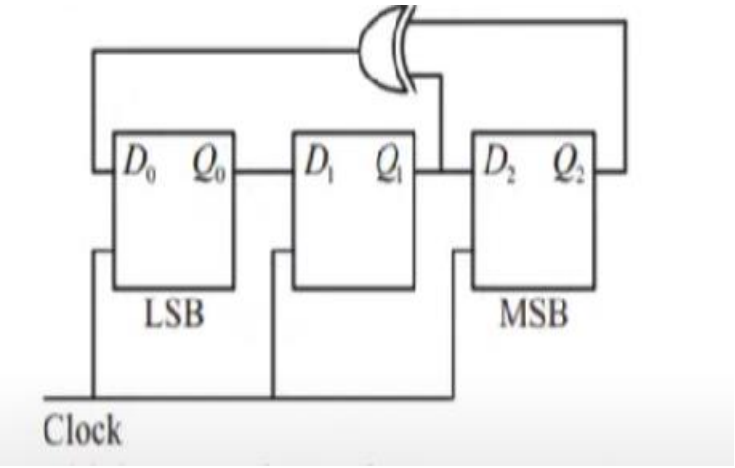
Department of Electronics Engineering

Digital Circuits and Systems (EO-203)

End- Sem Examination, Date: April 25,2022

Maximum Marks- 40 **Attempt all Questions**

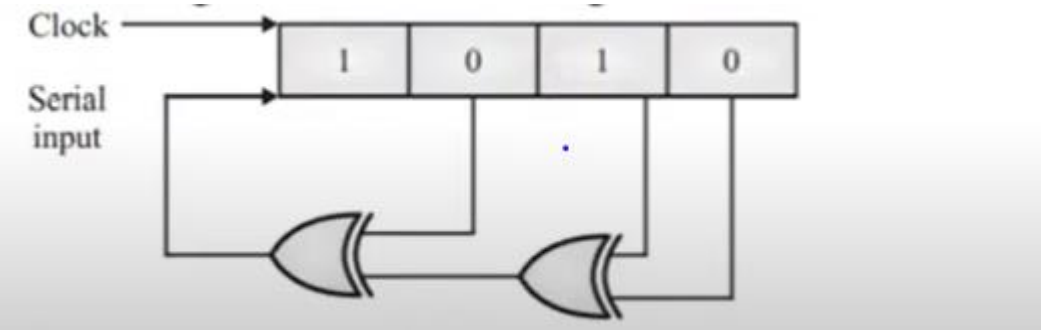
Q1. Consider the circuit given below with initial state Q0 = 1, Q1= Q2= 0. The state of the circuit is given by the value of 4Q2+2Q1+Q0. Find the correct state sequence (Marks 5)



Q2- Please provide the minimized version of the expression F (A, B, C, D) = ∑ (0, 1, 2, 8, 9, 12, 13) with d (A, B, C, D) = ∑ (10, 11, 14, 15) is? (Marks 5)

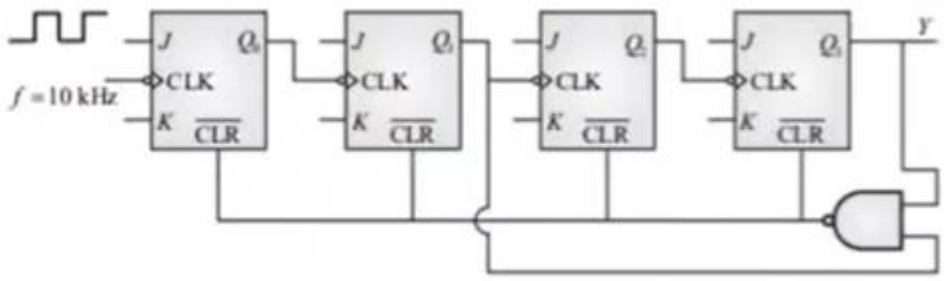
Q3. A traffic signal cycles from green to yellow, yellow to red, and red to green. In each cycle green is turned on for 70 seconds, yellow is turned on for 5 seconds and the red is turned on for 75 seconds. This traffic light has to be implemented using a finite state machine (FSM). The only input to this FSM is a clock to 5 second period. Determine the number of clock pulses required to complete the cycle and the number of flip-flops required to implement this FSM. (Marks 5)

Q4. The shift register shown below in the figure is initially loaded with the bit pattern 1010. Subsequently, the shift register is clocked and with each clock pulse, the pattern gets shifted by one position to the right. With each shift, the bit at the serial input is pushed to the left most position (MSB). After how many clock pulses will the content of the shift register becomes 1010 again? (Marks 5)



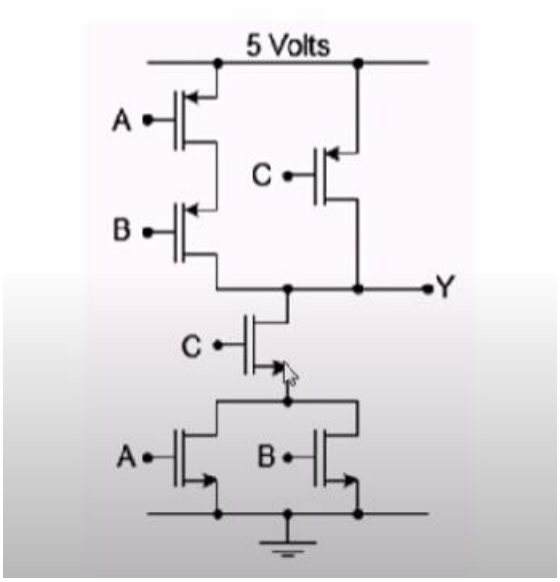
Q5. Design a 3 bit Binary to Gray code convertor using ROM (Marks 5)

Q6. In the figure given below, the J and K inputs of all the four flip flops are made high. Find the frequency of the signal at the output. (Marks 5)

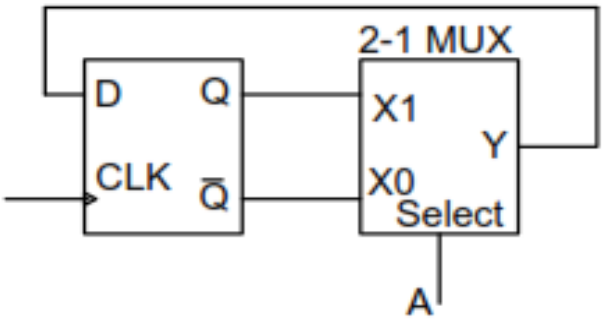


Q7. Find the logic functionality (Y) realised by the circuit shown below.

(Marks 5)



Q8- Please draw the state transition diagram for the circuit shown below:
(Marks 5)



Good Luck
