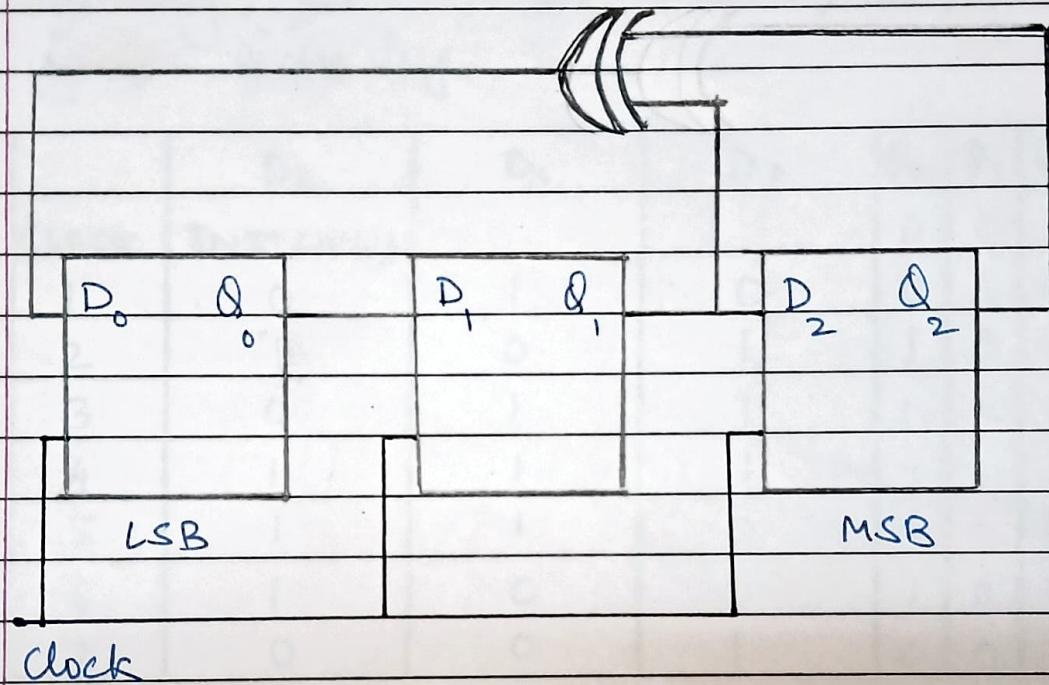


NAME - ATHARVA BHATT ROLL NO - 20095019
 BRANCH - ELECTRONICS ENGINEERING
 EO203- END SEMESTER EXAMINATION

(Q. 1.



Initial state, $Q_0 = 1, Q_1 = 0, Q_2 = 0$.

The truth table for the D-type flip flop

CLK	D	Q	Q'	
$\downarrow \Rightarrow 0$	X	Q	Q'	Memory, No change
$\uparrow \Rightarrow 1$	0	0	1	Reset $Q \Rightarrow 0$
$\uparrow \Rightarrow 1$	1	1	0	Set $Q \Rightarrow 1$

Symbols \downarrow and \uparrow indicate the direction of the clock pulse. D-type flip flops are assumed to be positive edge triggered here.

Now, from the circuit,

$$D_1 = Q_0, D_2 = Q_1, D_0 = Q_1 \oplus Q_2,$$

Initially, $Q_0 = 1, Q_1 = Q_2 = 0$, so, the sequence is given by,

CLOCK	D ₂ INITIALLY	D ₁	D ₀	Q ₂	Q ₁	Q ₀	STATE
1	0	1	0	0	1	0	(1)
2	1	0	1	1	0	1	(5)
3	0	1	1	0	1	1	(3)
4	1	1	1	1	1	1	(7)
5	1	1	0	1	1	0	(6)
6	1	0	0	1	0	0	(4)
7	0	0	1	0	0	1	(1)

where state of the circuit,
 $\text{STATE} = 4Q_2 + 2Q_1 + Q_0$.

Therefore, the correct state sequence of the circuit is, 1 [001], 2 [010], 5 [101], 3 [011], 7 [111], 6 [110], 4 [100].

\Rightarrow State sequence of the circuit is,
1, 2, 5, 3, 7, 6, 4.

P.T.O.

NOTE :

The truth table of a XOR gate is,

$$Q = A \oplus B.$$

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

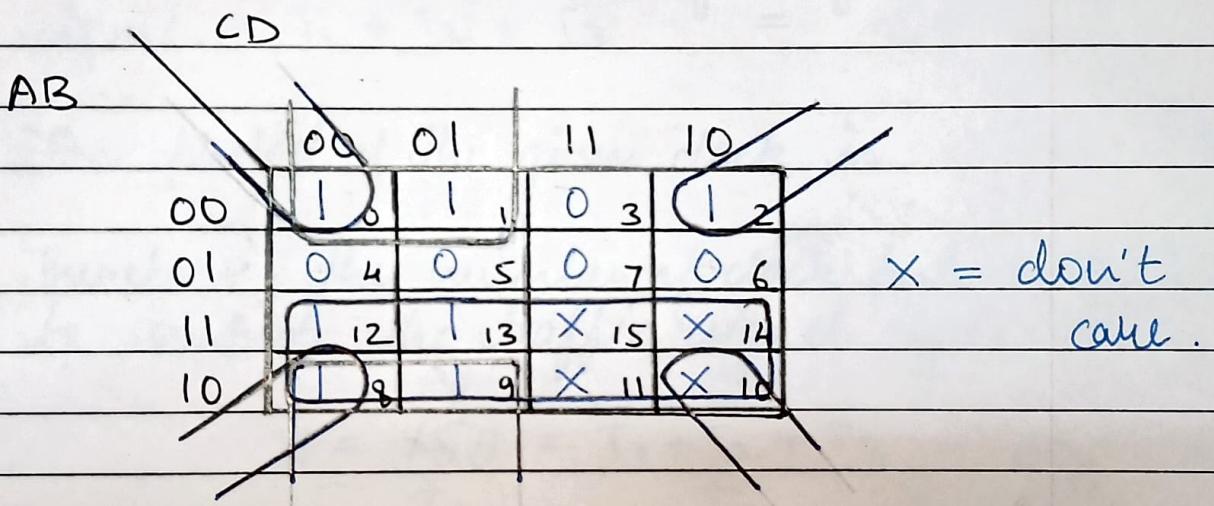
Truth
Table.

Q. 2.

Given, $F(A, B, C, D) = \Sigma(0, 1, 2, 8, 9, 12, 13)$

with $d(A, B, C, D) = \Sigma(10, 11, 14, 15)$
 (Don't care)

Therefore, the K-map is as follows,



$$f(A, B, C, D) = A + \overline{B} \overline{C} + \overline{B} \overline{D}$$

\Rightarrow Thus, the minimized version of the expression in SOP form is,

$$f(A, B, C, D) = A + \overline{B} \overline{C} + \overline{B} \overline{D}$$

$f(A, B, C, D) = \text{minimized expression of } F(A, B, C, D) \text{ with } d(A, B, C, D).$

P.T.O.

Now for realization using logic gates.

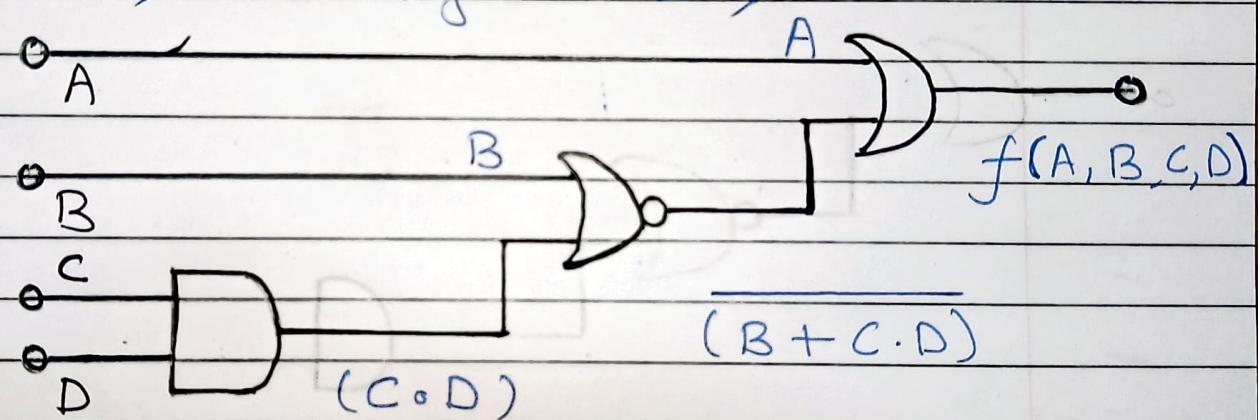
$$f(A, B, C, D) = A + \overline{B}\overline{C} + \overline{B}\overline{D}$$

$$= A + \overline{B}(\overline{C} + \overline{D})$$

$$= A + \overline{B}(C \cdot D) \quad (\text{by De-Morgan's law})$$

$$f(A, B, C, D) = A + (B + \overline{C} \cdot \overline{D})$$

Thus, the realization is,



Q. 3.

In each cycle,

Green is turned on for $T_1 = 70$ sec.

Yellow is turned on for $T_2 = 5$ sec.

Red is turned on for $T_3 = 75$ sec.

Thus, total time for one cycle of the traffic signal $= T_1 + T_2 + T_3 = 150$ sec.

Time period of the given clock is 5 sec. (T_c)

Therefore, the number of clock pulses required to complete the traffic signal cycle (n),

$$n = \frac{150}{T_c} = \frac{T_1 + T_2 + T_3}{T_c} = 30$$

$\Rightarrow \therefore$ The number of clock pulses required to complete the traffic signal cycle is 30.

Now, let the number of flip-flops required to implement this FSM be K .

The possible number of states using K flip-flops is 2^K . (Two states for each flip-flop.)

Since $n = 30$, i.e., we need 30 clock cycles or 30 states.

P.T.O.

$$\therefore 2^k \geq 30$$

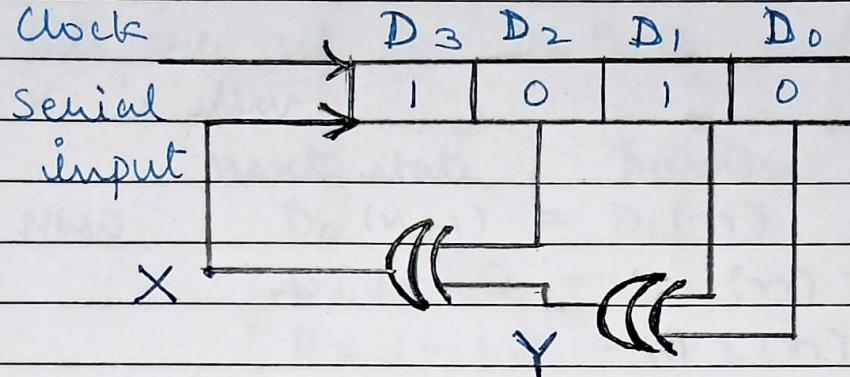
$$\Rightarrow k \geq \log_2(30)$$

$$\Rightarrow k \geq 4.907$$

$$\Rightarrow \underbrace{k}_{\text{~~~~~}} = 5 \quad (\text{nearest integer})$$

5 flip-flops are required to implement
this FSM.

Q. 4.



Initially loaded with the bit-pattern 1010.

Now, from the given circuit,

$$Y = D_0 \oplus D_1, \quad X = D_2 \oplus Y$$

$$\therefore X = D_2 \oplus D_1 \oplus D_0. \quad \left\{ \begin{array}{l} \text{XOR is associative,} \\ \text{commutative.} \end{array} \right.$$

The truth table of $Q = A \oplus B$ (XOR gate),

	A	B	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	0

Thus, truth table of $X = D_0 \oplus D_1 \oplus D_2$,

	D ₂	D ₁	D ₀	X	D ₂	D ₁	D ₀	X
	0	0	0	0	1	0	0	1
	0	0	1	1	1	0	1	0
	0	1	0	1	1	1	0	0
	0	1	1	0	1	1	1	1

Thus, X is high when odd number of bits are set in $D_2 D_1 D_0$ and otherwise X is low.

next state	previous state	
$D_0(n+1) = D_1(n)$	$D_1(n)$	according to
$D_1(n+1) = D_2(n)$	$D_2(n)$	the question,
$D_2(n+1) = D_3(n)$	$D_3(n)$	
$D_3(n+1) = X$.		
$X = D_0(n) \oplus D_1(n) \oplus D_2(n)$		

Initially, the bit pattern $(D_3 D_2 D_1 D_0)$ is 1010
 \therefore after one clock pulse,

$$\therefore D_0 = 0, D_1 = 1, D_2 = 0, \therefore X = 1$$

$$\therefore D_0(n+1) = D_1 = 1$$

$$D_1(n+1) = D_2 = 0$$

$$D_2(n+1) = D_3 = 1$$

$$D_3(n+1) = X = 1$$

Thus, bit pattern after 1 clock pulse is 1101.
 After next clock pulse,

$$D_0 = 1, D_1 = 0, D_2 = 1, D_3 = 1$$

$$\therefore D_0(n+1) = D_1 = 0$$

$$\therefore D_1(n+1) = D_2 = 1$$

$$\therefore D_2(n+1) = D_3 = 1$$

$$\therefore D_3(n+1) = X = 1 \oplus 1 \oplus 0 = 0$$

Thus, bit pattern after two clock pulses is 0110.

This can be confirmed in a similar fashion as shown in the table below,

CLOCK PULSE	PRESENT STATE				X	NEXT STATE			
	D ₃	D ₂	D ₁	D ₀		D ₃	D ₂	D ₁	D ₀
↑ (1)	1	0	1	0	1	1	1	0	1
↑ (2)	1	1	0	1	0	0	1	1	0
↑ (3)	0	1	1	0	0	0	0	1	1
↑ (4)	0	0	1	1	0	0	0	0	1
↑ (5)	0	0	0	1	1	1	0	0	0
↑ (6)	1	0	0	0	0	0	1	0	0
↑ (7)	0	1	0	0	1	1	0	1	0

⇒ Therefore, after 7 clock pulses, the content of the shift register becomes 1010 again.

Q.S.

3-bit Binary to 3-bit Gray code conversion using ROM.

There are three input variables (3-bit binary) and three output variables (3-bit gray code).

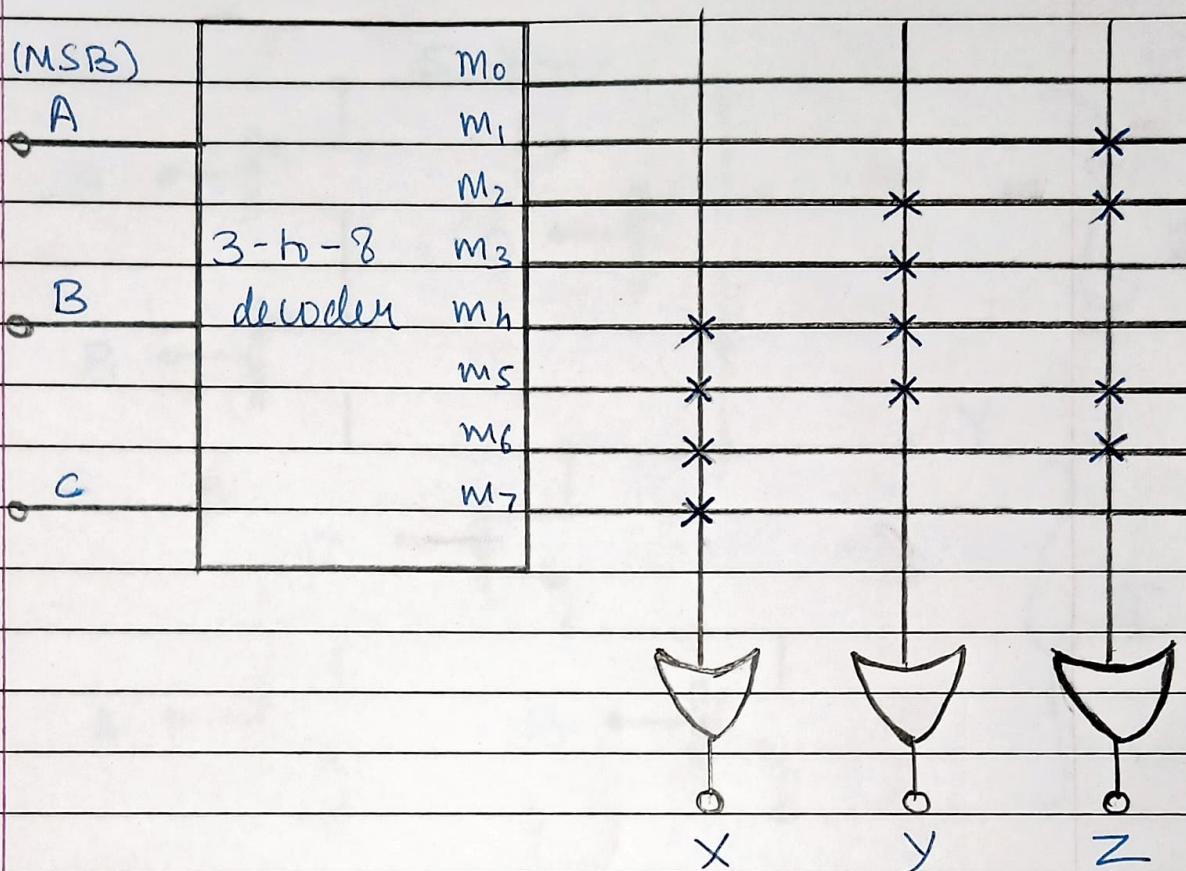
Thus, to implement this with ROM, a $2^3 \times 3$ ROM or 8×3 ROM is required.

The truth table is shown below,

	BINARY			GRAY CODE		
	A	B	C	X	Y	Z
	0	0	0	0	0	0
	0	0	1	0	0	1
	0	1	0	0	1	1
	0	1	1	0	1	0
	1	0	0	1	1	0
	1	0	1	1	1	1
	1	1	0	1	0	1
	1	1	1	1	0	0

The inputs and outputs with ROM and the internal fusible junctions after programming are shown in the following figure,

P.T.O.

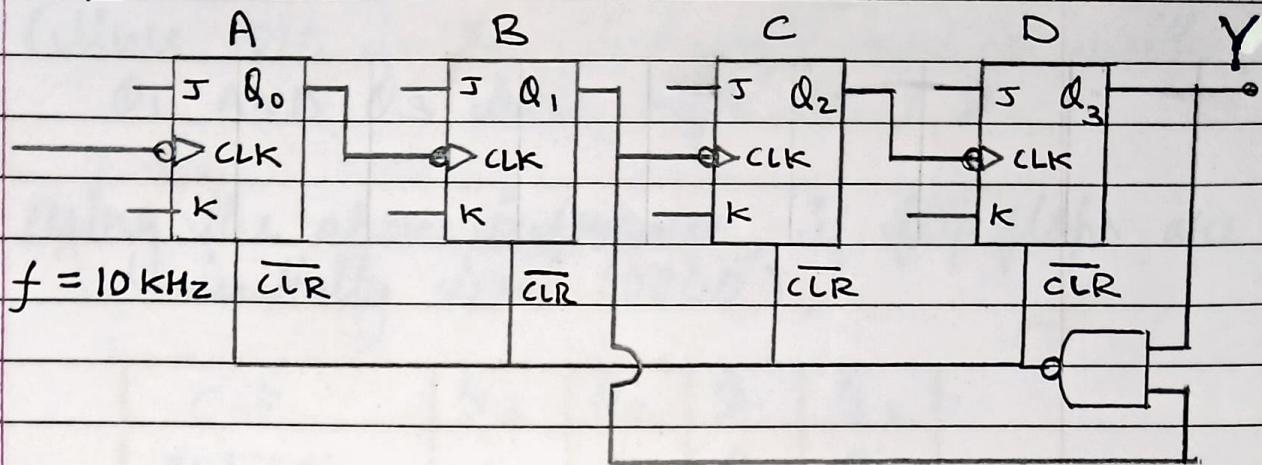


Logic diagram with PLD notation using ROM.

The connected input variables are indicated by cross (X) at junctions and unconnected inputs are left blank.

\Rightarrow 3-bit Binary to Gray code converter has been designed using a ROM.

Q. 6.



The J and K inputs of all the four flip flops are made high. $\therefore J = 1, K = 1$ for all the flip flops, thus, all the flip flops are in toggling condition.

Thus, all 4 flip flops toggle for each clock pulse (negative edge triggered).

Now, Q_0 acts as a clock for flip flop B, Q_1 for C and Q_2 for D. Since all the flip flops are negative edge-triggered,

- (B) Q_1 toggles when $Q_0 \ 1 \rightarrow 0$
- (C) Q_2 toggles when $Q_1 \ 1 \rightarrow 0$
- (D) Q_3 toggles when $Q_2 \ 1 \rightarrow 0$
- (A) Q_0 toggles when $clk \ 1 \rightarrow 0$.

Also, from the circuit, $CLR = \overline{Q_1} \overline{Q_3}$,

$\therefore CLR = Q_1 Q_3$. Thus $CLR = 1$ when $Q_1 = 1$ and $Q_3 = 1$. Thus, the flip flops clear at $(Q_3 Q_2 Q_1 Q_0) = 1010$.

Since 1010 is the first state reached with Q_1 AND Q_3 both high i.e., 1.)

Using the above inferences, if flip flops are initially clear (0000),

	CLK	Q_3	Q_2	Q_1	Q_0
INITIAL		0	0	0	0
1		0	0	0	1
2		0	0	1	0
3		0	0	1	1
4		0	1	0	0
5		0	1	0	1
6		0	1	1	0
7		0	1	1	1
8		1	0	0	0
9		1	0	0	1
10		1	0	1	0

(CLK at falling edge 1 \rightarrow 0)

For output frequency, we need the no. of states,

0000 \rightarrow 0001 \rightarrow 0010 \rightarrow --- \rightarrow 1010

(flip flops clear at 1010, returning to 0000 again).

\therefore 0 to 9 (in decimal representation)

\therefore Number of states = 10 and $Y = Q_3$.

P.T.O.

Now, the given clock frequency $(F) = 10 \text{ kHz}$

Thus, the frequency of the signal at output,

$$f_{\text{output}} = \frac{F}{\text{no. of states}} = \frac{F}{10} = \frac{10 \text{ kHz}}{10} = 1 \text{ kHz}$$

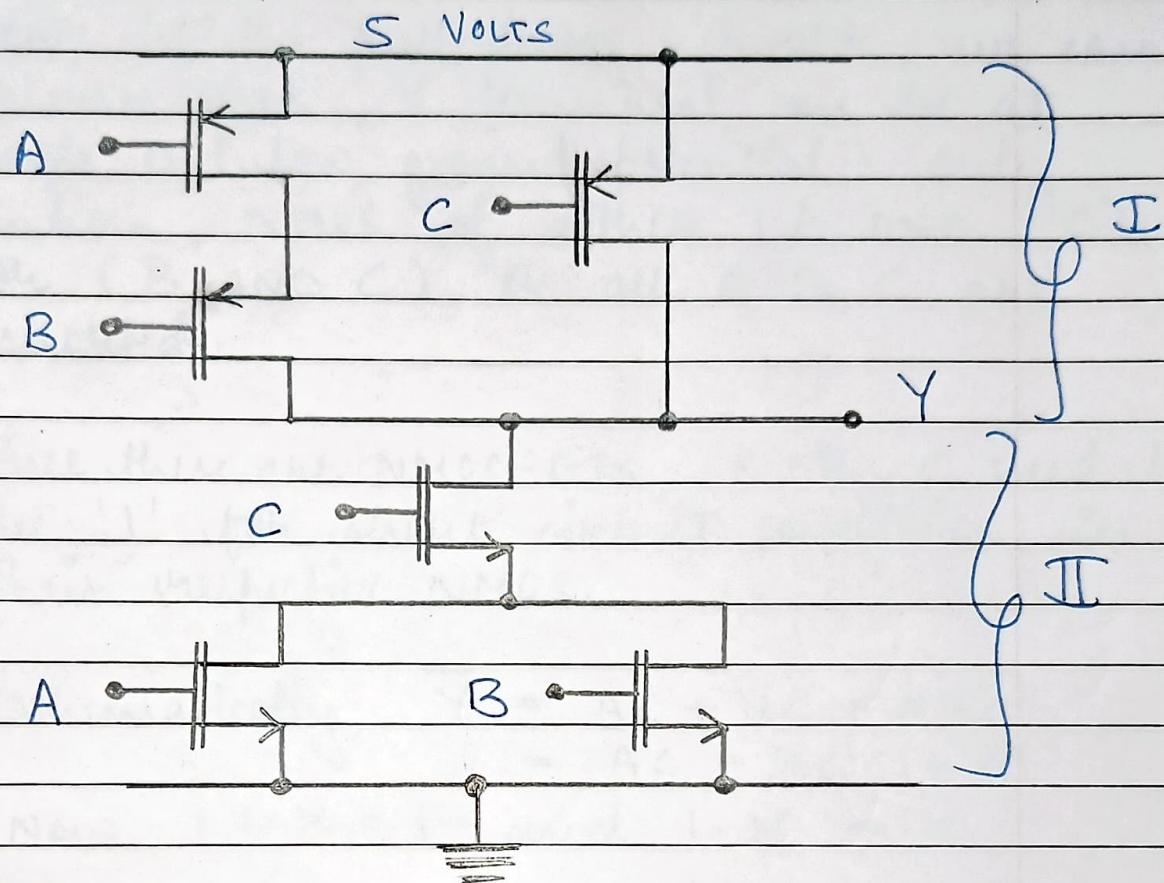
$$\Rightarrow f_{\text{output}} = 1 \text{ kHz}$$


(One cycle of counter completes in 10 pulses
of the given clock)

\Rightarrow The frequency of the signal at output $= 1 \text{ kHz}$.



Q. 7.



The part - I in the given circuit is a full-up network with PMOS and part - II is a full-down network with NMOS.

Now, the characteristics of PMOS are as given below,

Gate	Behaviour
0	Short circuit
1	Open circuit

and the characteristics of NMOS -

Gate	Behaviour
0	Open circuit
1	Short circuit

Now, in the pull-down network, we can observe that Y terminal can be at logic 0 (low, ground potential) only when NMOS of either (A AND C) OR (B AND C) or all A, B, C are shorted.

Since these are NMOSFETs, A, B, C need to be '1' for short circuit condition in their respective NMOS.

$$\text{Mathematically, } \bar{Y} = AC + BC + ABC \\ = AC + BC(1+A)$$

$$\text{Now } 1+X=1 \text{ and } 1 \cdot X = X$$

$$\therefore \bar{Y} = AC + BC = C(A+B)$$

$$\text{Now } Y = \overline{\bar{Y}} = \overline{C(A+B)} = \overline{C} + \overline{(A+B)}$$

(using De Morgan's law)

$$\Rightarrow Y = \overbrace{\overline{C}} + \overbrace{\overline{A} \cdot \overline{B}} \text{ (using De Morgan's law)}$$

\Rightarrow Thus, logic functionality of given circuit is,

$$Y = \overbrace{\overline{A} \cdot \overline{B}} + \overline{C}$$

A similar analysis can be done on the pull-up network,

Y terminal can be at logic (1) [+5 volts] only when PMOS of (A AND B) OR C is shorted.

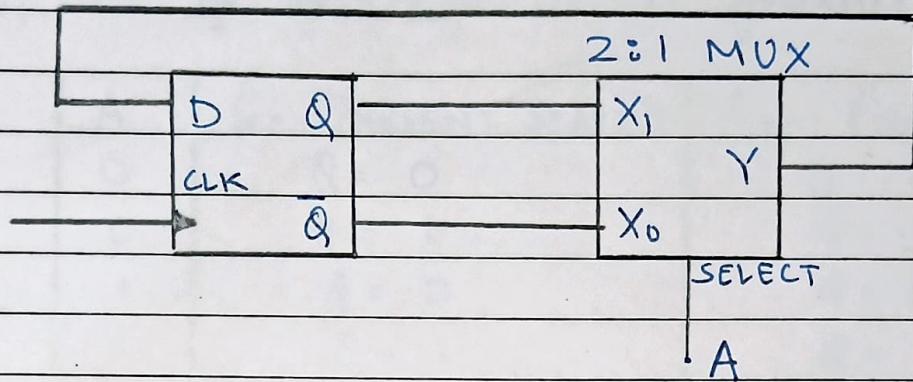
Since, these are PMOS, A, B, C should be logic '0' for shorted condition.

$$\therefore Y = \overline{C} + \overline{A} \cdot \overline{B}$$

⇒ The logic functionality (Y) realised by the given circuit is,

$$Y = \overline{A} \cdot \overline{B} + \overline{C}$$

Q. 8.



The output expression (Y) of the 2:1 MUX,

$$Y = \bar{A}X_0 + AX_1 \quad (1)$$

Also, in a D-flip flop, the next state Q_{n+1} is given by,

$$Q_{n+1} = D \quad (2) \quad \text{(after a clock pulse)}$$

From the given circuit, $D = Y$, $X_1 = Q$ and $X_0 = \bar{Q}$.

Therefore, from eqn (1),

$$D = \bar{A}\bar{Q} + A\bar{Q} \quad (3)$$

From eqn (3) into eqn (2),

$$Q_{n+1} = \bar{A}\bar{Q} + A\bar{Q}$$

$$Q_{n+1} = \underbrace{\bar{A}}_{\text{OR}} \underbrace{\bar{Q}_n}_{\sim} + A\bar{Q}_n \quad (4)$$

P.T.O.

Thus, the truth table is as follows,

A	Q_n (PRESENT STATE)	Q_{n+1} (NEXT STATE)
0	$Q = 0$	$Q = 1$
0	$Q = 1$	$Q = 0$
1	$Q = 0$	$Q = 0$
1	$Q = 1$	$Q = 1$

\Rightarrow Therefore, the state transition diagram for the given circuit is,

