CSE-312:Computer Architecture

End-semester exam

Max marks: 50   Date: 01/05/2011

- Answer all questions and each question carries 10 marks.
- Answer all parts of a question together. Do not scatter them across the answer script.
- A separate assignment tab has been created for mid-semester in the MS Teams class. Write your answers on paper, scan and then submit in this assignment tab of MS Teams before tomorrow 2nd May, 11:00 AM. Answer sheet must be a single pdf file.
- Do not forget to mention your Roll number, Name, and Branch in the answer sheet. The name of the submitted copy should be your roll number.

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1 A) Consider the following memory-address accesses in a direct-mapped caching scheme in the following order: 000100, 100101, 010110, 001111, 101110. Show each memory access mentioning cache-hit or miss where cache size is 2^R bytes (read: 2 to the power R) where $R = 1 +$ (last digit of your roll-no %3).

E.g. if your roll-no is 19074054, your cache-size is 4 bytes ($R = 1 +4\%3 = 1+1 = 2$, $2^2 = 4$). [5]

B) Consider cache-memory of 16 bytes. Show with diagrams 2-way and 4-way set-associative caching of the same memory accesses as in 1A. [5]

2. Consider 64-bit addressing scheme with 2^R kilobytes of page-size where $R =$ last-digit of your roll number % 3 [e.g. if your roll-no is 19074054, your page-size is 2kB ($R = 4\%3 = 1$; 2, $2^1 = 2$). Assume 4 bytes of space required for an entry in the page-table.
   A) Find total page-table size. [3]
   B) Diagrammatically show the address translation scheme with all necessary details (physical address lines, page table entries, page-offset etc.) [7]

3. With diagrams, show the steps followed for the instruction
   A) **add \$1, \$2, \$3** in single cycle implementation [5]
   B) **sw \$t5, 8(\$t3)** in multi-cycle implementation [5]

4. A) Consider a machine with a floating point unit. Assume functional unit delays as follows
   memory: 3 ns., ALU and adders: 3 ns., FPU add: 8 ns., FPU multiply: 16 ns., register file access (read or write): 2 ns.
   multiplexors, control unit, PC accesses, sign extension, wires: no delay
   Assume instruction mix as follows
   all loads take same time and comprise 30%
   all stores take same time and comprise 20%
   R-format instructions comprise 27%
   branches comprise R%

jumps comprise (7 - R) %

FP adds and subtracts take the same time and totally comprise 8%

FP multiplys and divides take the same time and totally comprise 8% (where R = 1 + last-digit of your roll-number % 5)

Compare the performance of (a) a single-cycle implementation using a fixed-period clock with (b) one using a variable-period clock where each instruction executes in one clock cycle that is only as long as it needs to be. [7]

B) Write short note on either **page-fault** or **locality of reference.** [3]

5. a) "Having a large number of processor registers makes it possible to reduce the number of memory accesses needed to perform complex tasks." Devise a simple computational task to show the validity of this statement for a processor that has for registers compared to another that has only two registers. [5+5]

b) Assume that $s0 holds the value 128_{ten}.

   i) For the instruction *add* $t0, $s0, $s1, what is the range(s) of values for $s1 that would result in overflow?

   ii) For the instruction *sub* $t0, $s0, $s1, what is the range(s) of value for $s1 that would result in overflow?

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