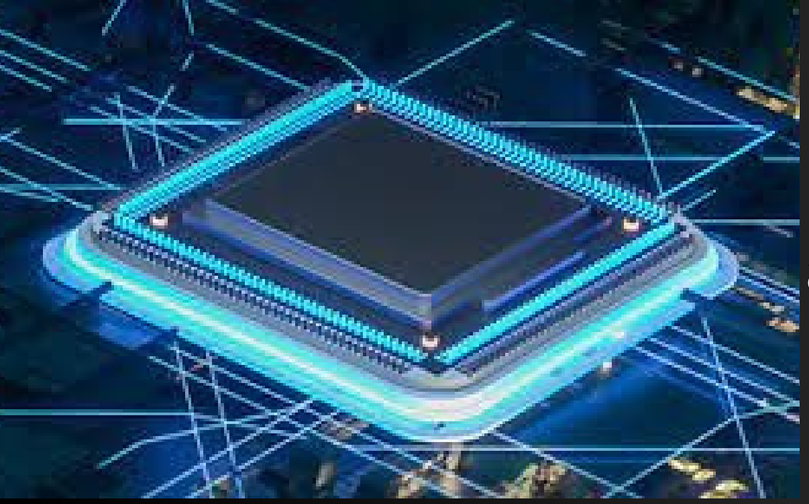
JLR’S CHIPLET CHALLENGE

HIGH PREP PROBLEM STATEMENT

Presented By -

EcoMotion Voyagers

22JE0932,22JE0823,22JE0306,22JE0120,22JE0651,22JE0640



The semiconductor industry is undergoing a major shift with the introduction of chiplets, offering a revolutionary alternative to traditional monolithic SoCs. Chiplets address the rising costs and complexities of advanced ICs by integrating diverse functions in a modular design.

Chiplets consist of a self -contained semiconductor die that,when combined with other dies through advanced packing techniques , forms a complex integrated circuit similar to a a monolithic integrated circuit.

Chiplet Revolution: Enhances scalability, cost-efficiency, and performance by integrating diverse functions in a modular way.

Advantages: Provides tailored solutions, faster time-to-market, and reduced costs through easy upgrades and integration.

Challenges: Requires efficient power, thermal management, and standardized interfaces (e.g., UCIe) for seamless operation

Heterogeneous Integration: Chiplets allow for the integration of different technologies (general-purpose processing, domain-specific accelerators, memory) within the same package, improving system performance.

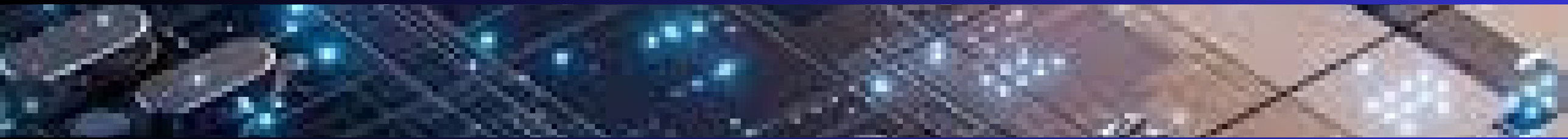
Adoption: Intel, Nvidia, AMD are leading adoption with growing industry ecosystem support.

Opportunities: Chiplets cater to automotive and other sectors needing customized, domain-specific solutions.

- System-on-Chip (SoC) in automotive applications integrates essential components like CPU, memory, and specialized accelerators into a single chip to handle multiple functions efficiently

Automotive SoC Architecture typically includes:

- Processing units for engine control, battery management, and sensor data processing.
- Communication interfaces (e.g., CAN, Ethernet) for vehicle networks.
- Real-time control systems for safety-critical functions like ADAS (Advanced Driver Assistance Systems) and infotainment.
- SoCs help reduce the number of discrete components, improve system reliability, and increase processing power for complex tasks like autonomous driving and powertrain optimization.



Key Limitations of SoCs in Automotive Applications

Thermal Management Issues: SoCs face significant challenges with heat dissipation due to the integration of multiple functions into a single die. This becomes critical in EVs where high-performance tasks like battery management and autonomous driving generate excessive heat, leading to **overheating risks.

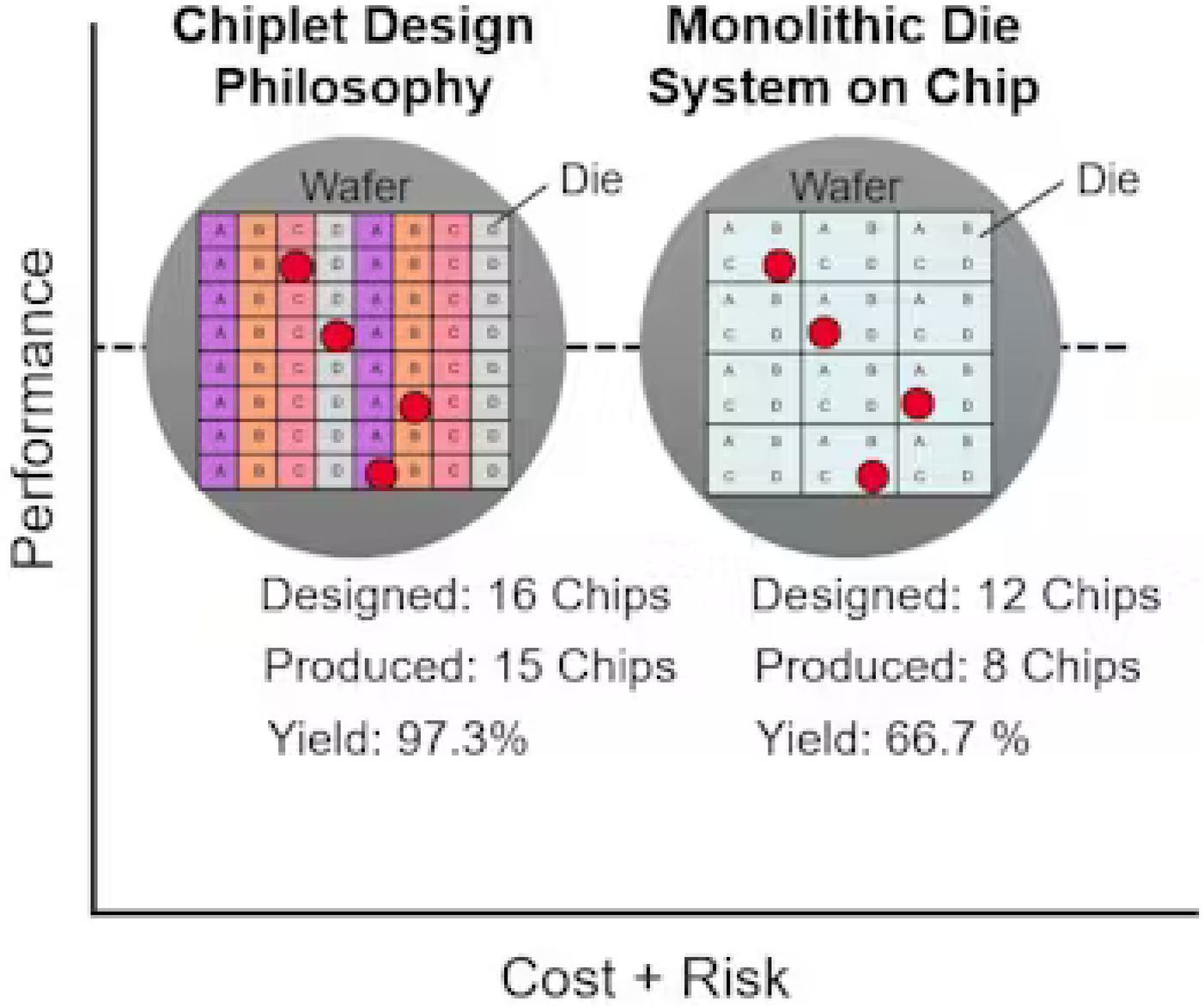
Scalability Constraints: Traditional monolithic SoCs lack modularity, making it difficult to scale or upgrade individual components. In fast-evolving EV technologies, upgrading a single function (e.g., AI processing) may require an entire SoC redesign, increasing time and cost.

Power Consumption: SoCs consume a substantial amount of power, especially when performing complex tasks like real-time data processing for ADAS. This can lead to **battery drain in EVs**, reducing vehicle efficiency and range.

Customization Challenges: The all-in-one nature of SoCs limits the ability to tailor solutions for specific EV applications or individual OEM needs. Automotive manufacturers like JLR need **flexible solutions** that can adapt to evolving vehicle requirements, something SoCs struggle with.

Manufacturing Complexity and Costs: - As SoCs become more advanced, the complexity of manufacturing increases significantly, driving up production costs. **Yield issues** with advanced nodes add to the cost, making them less attractive for large-scale EV adoption.

Why JLR Chooses Chiplets:JLR aims to overcome these SoC limitations by adopting chiplet technology, which offers better thermal management, scalability, and flexibility while reducing costs. Chiplets allow for **modular design**, enabling JLR to upgrade individual parts of the system without redesigning the entire SoC, making it ideal for the rapidly evolving EV landscape.



Monolithic approach

4 different functions in one big die

Fn: A (CPU)	Fn: B (Memory)
Fn: C (I/O)	Fn: D (Power)

Chiplet approach

4 different dies for 4 different functions

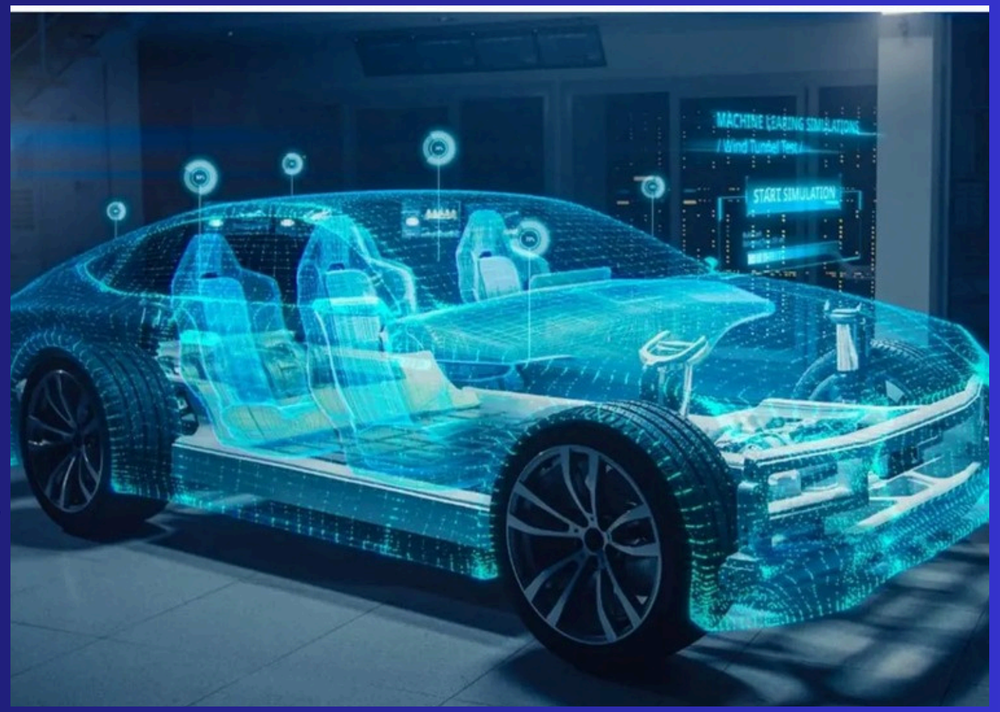
Die: A	Die: B
Die: C	Die: D

Applications of Chiplet Technology in EV

Advanced Driver Assistance Systems (ADAS) & Autonomous Driving:

ADAS/AV processors require advanced silicon nodes, high-performance computing, and AI/ML capabilities within a compact design.

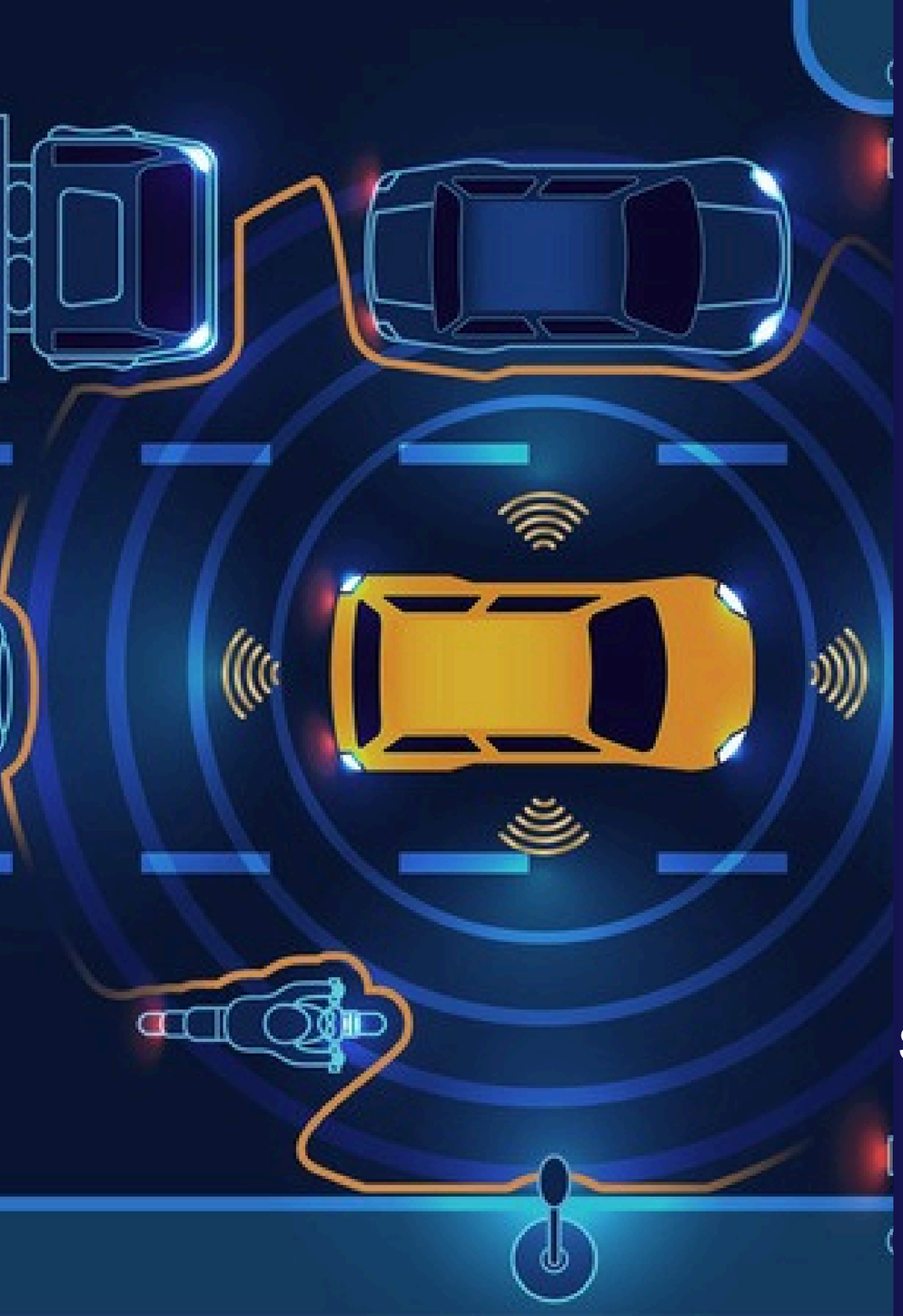
Heterogeneous packaging technologies enable optimization of performance and cost while enhancing time-to-market. Future vehicles will integrate diverse silicon products using 2.5D/3D packaging, making cost-effective, high-performance SoCs with chiplet architectures essential for mainstream adoption over the next 5-10 years.



Infotainment Systems:

Chiplets reduce ownership costs and separate safety from non-safety applications, driving hardware virtualization.

They facilitate the development of open platforms for software-defined digital cockpits, supporting a new generation of high-performance, heterogeneous SoCs necessary for complex, cross-domain applications in modern vehicles.



System-on-Chip (SoC) in ADAS Systems

Applications: SoCs power key ADAS features like Lane-Keeping Assistance (LKA), Automatic Emergency Braking (AEB), and Driver Monitoring Systems (DMS). They process sensor data in real-time to ensure vehicle safety and improve driver assistance.

Advantages: High computational power for handling complex tasks like image recognition and sensor fusion.
Energy efficiency to prevent overheating and battery drain.
Scalability to support various ADAS features across different vehicle models.
Compact integration, reducing hardware size and weight.

Limitations: High development costs for custom SoC designs.
Heat management challenges due to intense computations.
Software complexity and ensuring compatibility across systems.
Security and reliability concerns, needing robust cybersecurity measures.

Benefits of Chiplets for Electric Vehicles (EVs)

As electric vehicles (EVs) evolve, enhancing energy efficiency and power distribution is crucial for improving performance and range. Traditional monolithic system designs face challenges in managing power demands, while chiplet-based architectures offer a solution by modularizing system-on-chip (SoC) designs into smaller, specialized components.

Key Benefits of Chiplets:

Modular Design and Power Scalability: Chiplets enable optimized designs for specific functions, reducing energy overhead and routing power efficiently.

Optimized Power Delivery:Each chiplet can have its own Voltage Regulation Module (VRM), allowing tailored power delivery and minimizing losses through techniques like Dynamic Voltage and Frequency Scaling (DVFS).

Improved Thermal Management: Distributing power generation across multiple chiplets enhances thermal management, critical in the harsh conditions of EV powertrains.

Energy Efficiency in Powertrain Electronics:ask-specific optimization reduces energy demands of critical components, improving overall system efficiency.

Scalability and Integration Flexibility: Chiplets facilitate the integration of new features and simplify power distribution, allowing for a distributed power network.

Chiplet architectures thus maximize energy efficiency, enhance thermal management, and extend vehicle range, making them essential for the future of energy-efficient EV systems.

Powering the Future: Transformative Trends in Automotive Semiconductors

The automotive industry is undergoing a significant transformation influenced by advanced technologies and sustainability efforts, reshaping semiconductor demand. Jaguar Land Rover (JLR) is at the forefront of this change, focusing on electric vehicles (EVs), advanced driver assistance systems (ADAS), and connected car technologies.

Electrifying the Future: The Rise of Electric Vehicles

EV Surg: EV sales reached 14 million units in 2023, representing 18% of total vehicle sales. Projections suggest growth to 29 million units by 2030.

Sustainability Drives Change: Global governments are promoting electric mobility, expanding the EV charging infrastructure market from $7.9 billion in 2022 to approximately $49.2 billion by 2030.

JLR's EV Commitment: JLR aims for 100% electric vehicle production by 2030, investing in battery technologies and partnerships with semiconductor manufacturers.

Driving Safety: The Transformative Power of ADAS

Advancing Safety: The global ADAS market is projected to reach $96 billion by 2024, with key components like cameras and sensors driving costs.

Widespread Adoption: By 2023, around 50% of new vehicles will include ADAS, with JLR targeting 60% integration by 2025.

Enhancing the Driving Experience:** ADAS improves safety and convenience with features like adaptive cruise control and lane-keeping assist.

Connected Cars

V2X Communication: Enhances safety and traffic management.

Over-the-Air Updates: 70% of drivers prefer remote updates.

Data Insights:Generates valuable data for personalized services.

Revenue Streams:Opportunities for subscriptions and data monetization.

Software-Defined Future

Agile Systems: Software delivery reduces hardware reliance.

Rapid Features: 60% of new features expected to be software-driven by 2025.

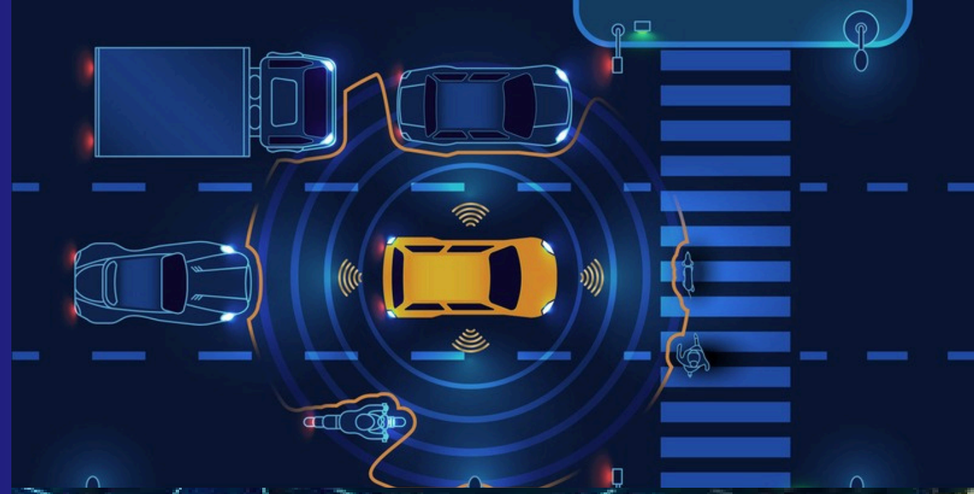
R&D Investment: JLR plans to invest £2.5 billion to enhance software capabilities.

Semiconductor Demand

Rising Demand: Driven by EVs, ADAS, and connected cars.

Innovative Solutions: Development of high-performance processors and sensors.

Partnerships: Collaborations foster innovation in automotive technology.



Industry Context

Jaguar Land Rover (JLR) has established strategic partnerships with NVIDIA and Wolfspeed to enhance its autonomous driving (ADAS) and electric vehicle (EV) capabilities.**

JLR and NVIDIA:

- Starting in 2025, JLR will integrate the NVIDIA DRIVE platform across its vehicle lineup
- This platform enables Level 3 autonomous driving, advanced safety features, and AI services for monitoring drivers and occupants
- Key reasons for the partnership include NVIDIA's AI expertise, the modularity of the DRIVE platform, and its proven leadership in automotive technology.

JLR and Wolfspeed (Semiconductors for EVs):

- JLR partners with Wolfspeed for silicon carbide semiconductors critical to enhancing EV powertrains.
- These components improve energy efficiency and battery performance while supporting high-voltage conditions.
- The partnership leverages Wolfspeed's expertise in semiconductor technology and ensures a reliable supply chain for JLR’s luxury EVs.

Overall, these collaborations position JLR at the forefront of autonomous and electric vehicle development, aligning with their sustainability goals and commitment to luxury driving experiences.

LEVELS OF AUTONOMOUS DRIVING

0
NO AUTOMATION
The driver has full control of the driving tasks.

1
DRIVER ASSISTANCE
The vehicle features a single automated system.

2
PARTIAL AUTOMATION
The vehicle can perform steering and acceleration.

3
CONDITIONAL AUTOMATION
The vehicle can control most driving tasks.

4
HIGH AUTOMATION
The vehicle performs all driving tasks under certain conditions.

5
FULL AUTOMATION
The vehicle performs all driving tasks under all conditions.

Micro-Architecture of Chiplet-Based Processors in ADAS and Infotainment

Sensor Technologies:

Micro-Architecture: Integrate chiplets for processing data from various sensors (cameras, RADAR, LIDAR, ultrasonic) to ensure high throughput.

Interconnects: High-speed links between chiplets handling different sensor data for real-time processing and fusion.

AI and Machine Learning :

Micro-Architecture: Dedicated chiplets for AI algorithms (computer vision, deep learning) to enhance decision-making in ADAS.

Interconnects: Fast communication paths between AI chiplets and sensor data processors for immediate insights.

V2X Communication:

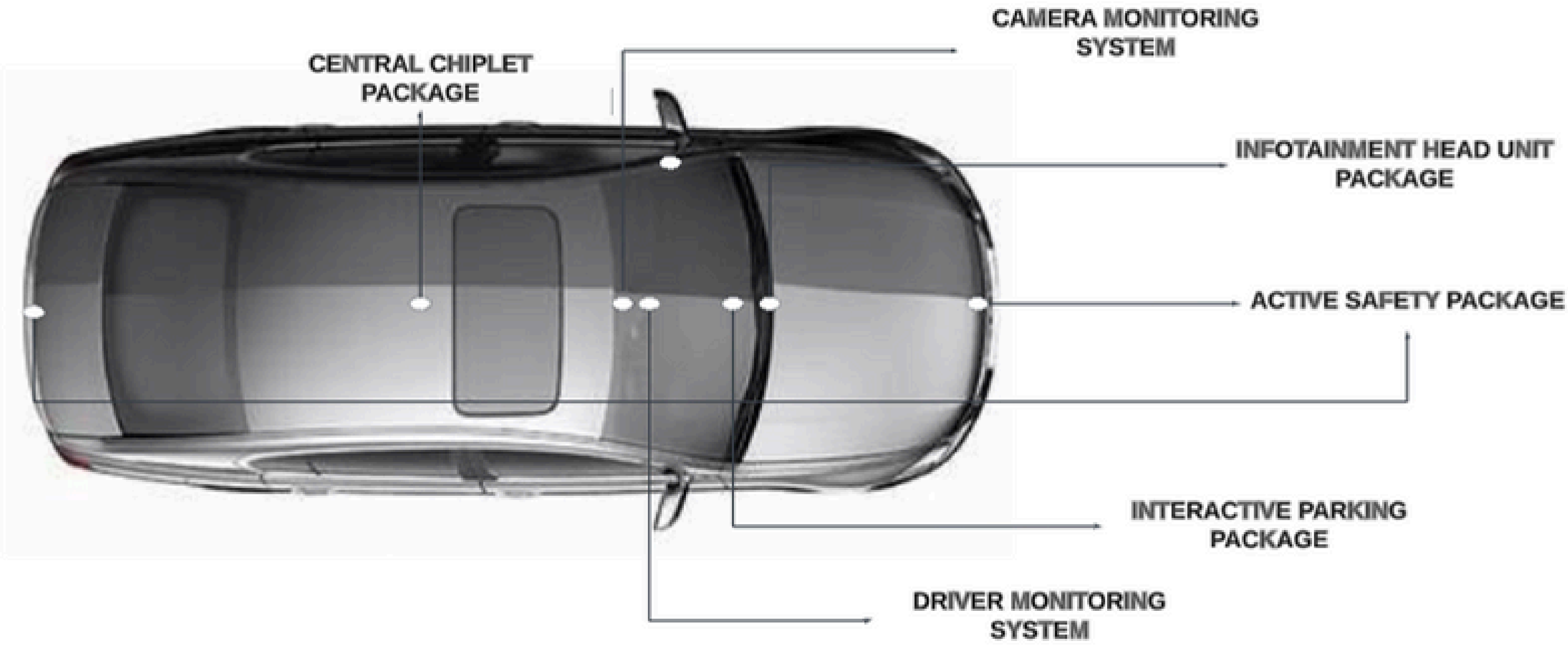
Micro-Architecture: Chiplets focused on V2X protocols and data processing for vehicle and infrastructure communication.

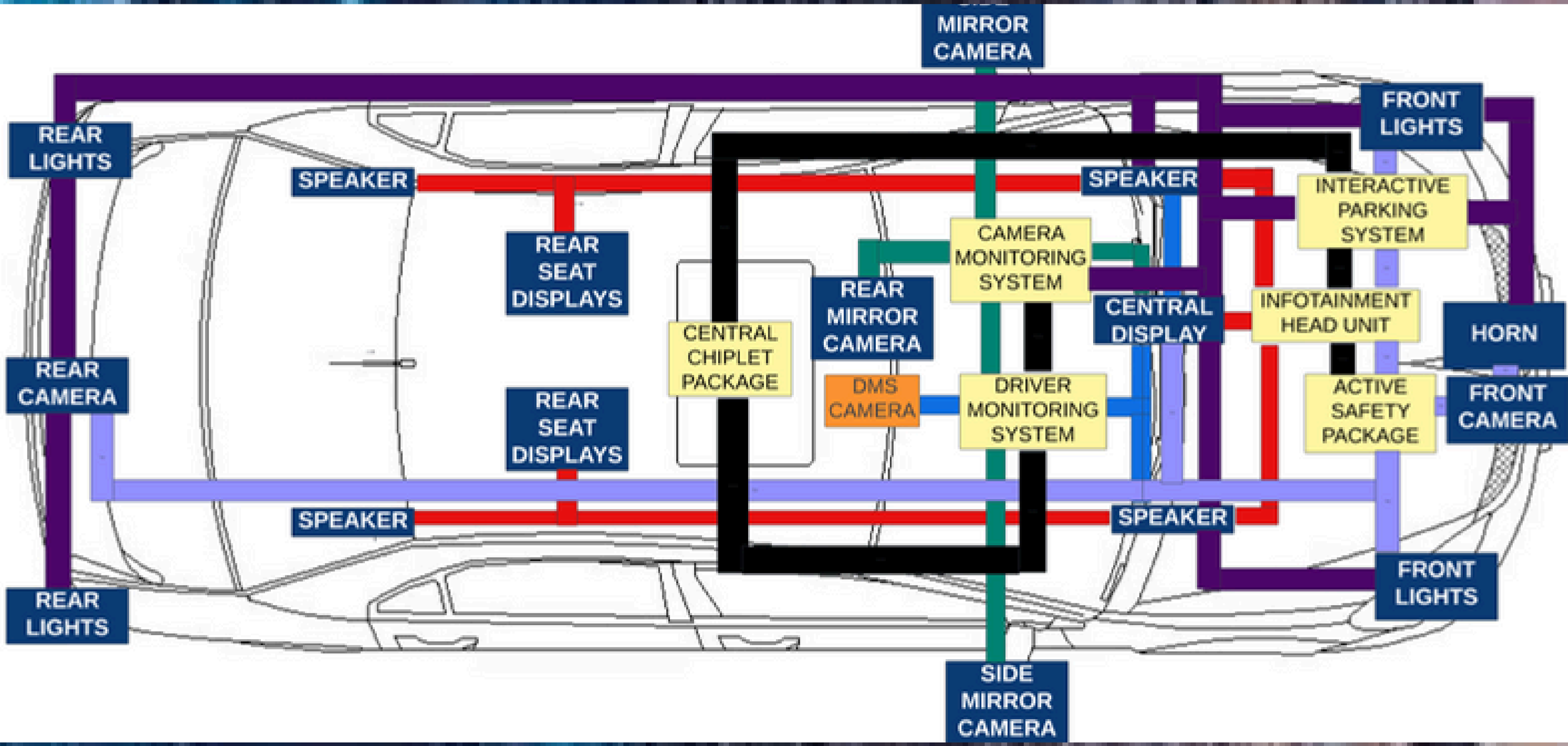
Interconnects: Efficient connections to ensure low-latency data exchange between chiplets managing V2V and V2I communications.

Edge Computing:

Micro-Architecture: Chiplets designed for on-board processing, minimizing reliance on cloud infrastructure for faster decision-making.

Interconnects: Direct links between edge processing chiplets and sensors to reduce latency.


CAMERA MONITORING SYSTEM
CENTRAL CHIPLET PACKAGE
INFOTAINMENT HEAD UNIT PACKAGE
ACTIVE SAFETY PACKAGE
INTERACTIVE PARKING PACKAGE
DRIVER MONITORING SYSTEM


MIRROR CAMERA
FRONT LIGHTS
REAR LIGHTS
SPEAKER
SPEAKER
INTERACTIVE PARKING SYSTEM
REAR SEAT DISPLAYS
CAMERA MONITORING SYSTEM
REAR MIRROR CAMERA
CENTRAL DISPLAY
INFOTAINMENT HEAD UNIT
HORN
REAR CAMERA
CENTRAL CHIPLET PACKAGE
DMS CAMERA
DRIVER MONITORING SYSTEM
ACTIVE SAFETY PACKAGE
FRONT CAMERA
REAR SEAT DISPLAYS
SPEAKER
SPEAKER
FRONT LIGHTS
REAR LIGHTS
SIDE MIRROR CAMERA

To maintain a competitive edge, JLR should design the following chiplets in-house while procuring others off-the-shelf:

In-House Design for Differentiation:

Custom ADAS & Autonomous Driving Chiplets

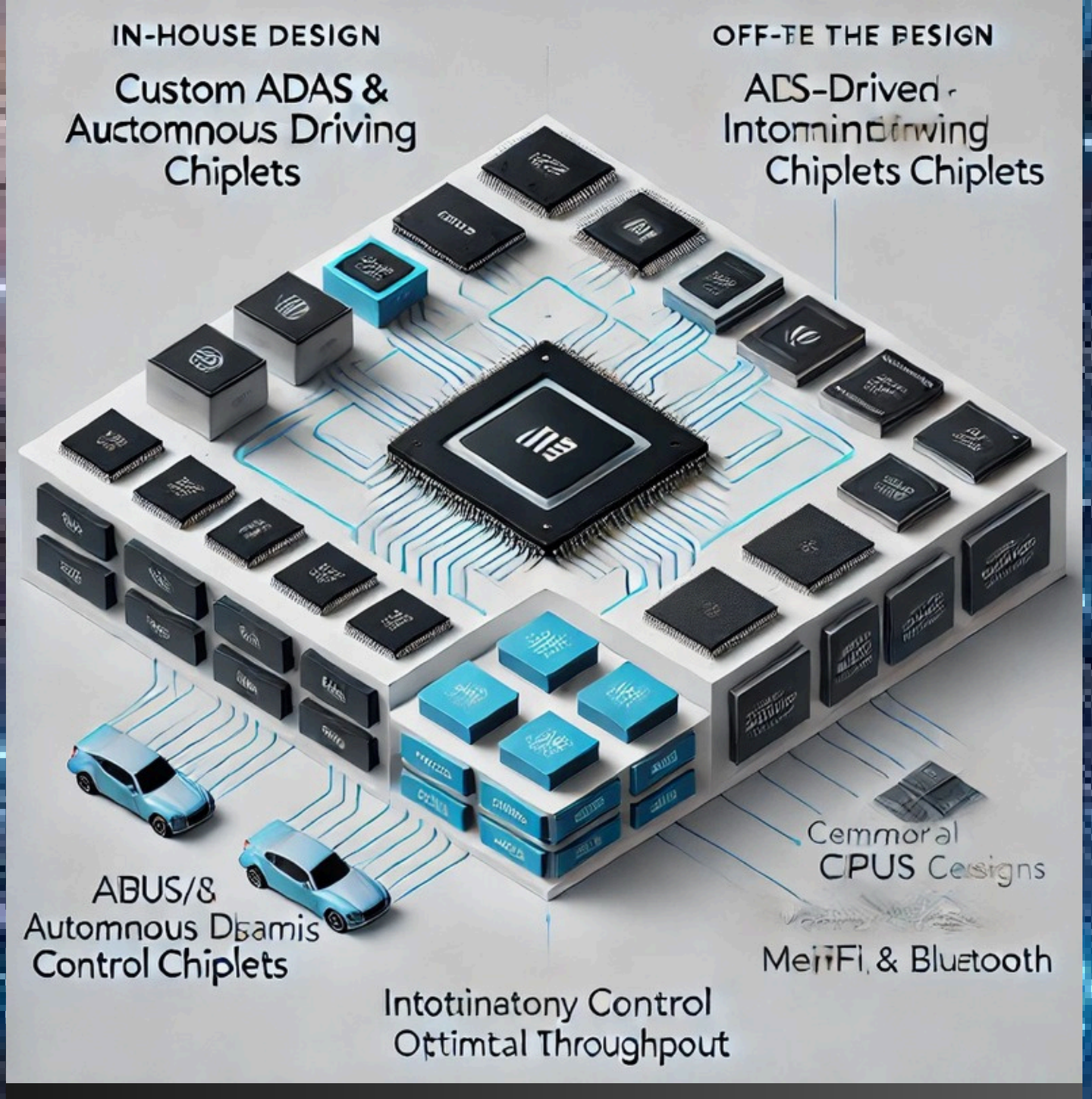
Why?-Unique algorithms and sensor fusion tailored for JLR’s vehicles can improve safety, response, and comfort, differentiating from competitors.

AI-Driven Infotainment & Personalization Chiplets

Why?- Developing custom infotainment chips will allow JLR to offer personalized experiences like AI-based navigation, user profiles, and seamless connectivity, enhancing the luxury feel.

Vehicle Dynamics Control Chiplets

Why?- Custom-designed chips for real-time control of suspension and traction will optimize driving performance, especially for electric and hybrid models, providing a superior driving experience


IN-HOUSE DESIGN
Custom ADAS &
Auctomnous Driving
Chiplets
OFF-TE THE BESIGN
ADS-Driven
Intonmin Driwing
Chiplets Chiplets
Cemmoral
CPUS Cesigns
MeiFi & Bluetooth
ABUS/&
Automnous Dbamis
Control Chiplets
Intotiinatony Control
Ottimtal Throughpout

Key Communication Technologies:

SerDes (Serializer/Deserializer): High-speed data transfer between chiplets; reduces I/O pins and enhances bandwidth.

PCIe (Peripheral Component Interconnect Express): Efficient, low-latency communication in chiplet systems.

CXL (Compute Express Link):Next-gen standard for high-performance computing; connects memory and accelerators

HBI (High Bandwidth Interconnect): Optimized for high-speed data transfer in 3D ICs.

Die-to-Die (D2D) Interconnect: Seamless, low-latency communication between dies in the same package.

Essential IPs for Chiplet Communication:

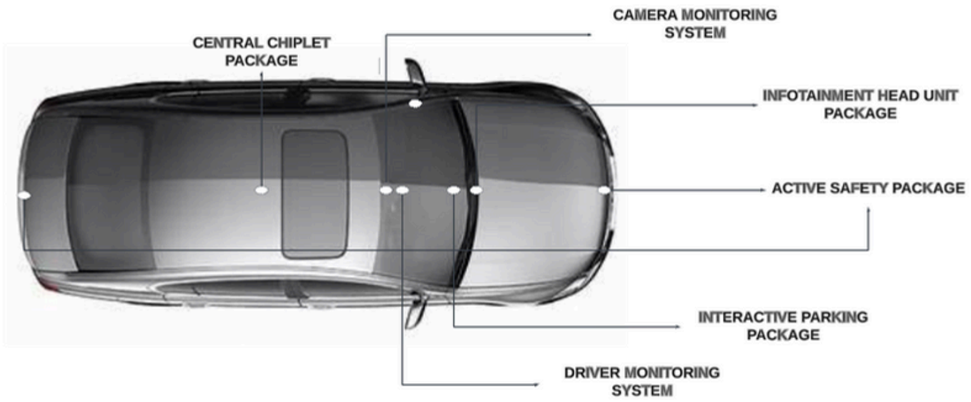
Interconnect IPs: Pre-designed cores like Network on Chip (NoC) ensure efficient communication.

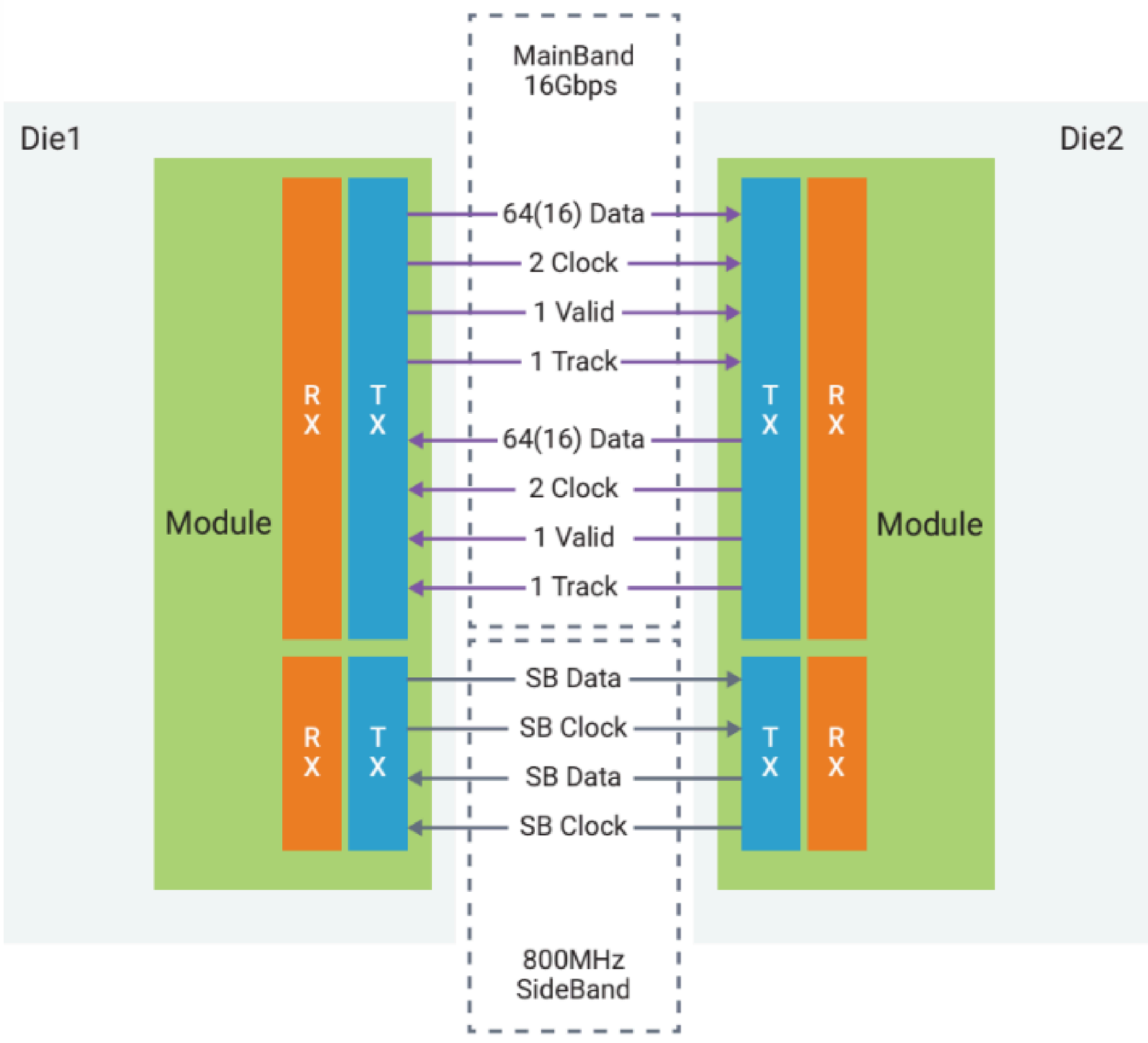
PHY Layer IPs: Facilitate electrical and optical signaling for data transfer.

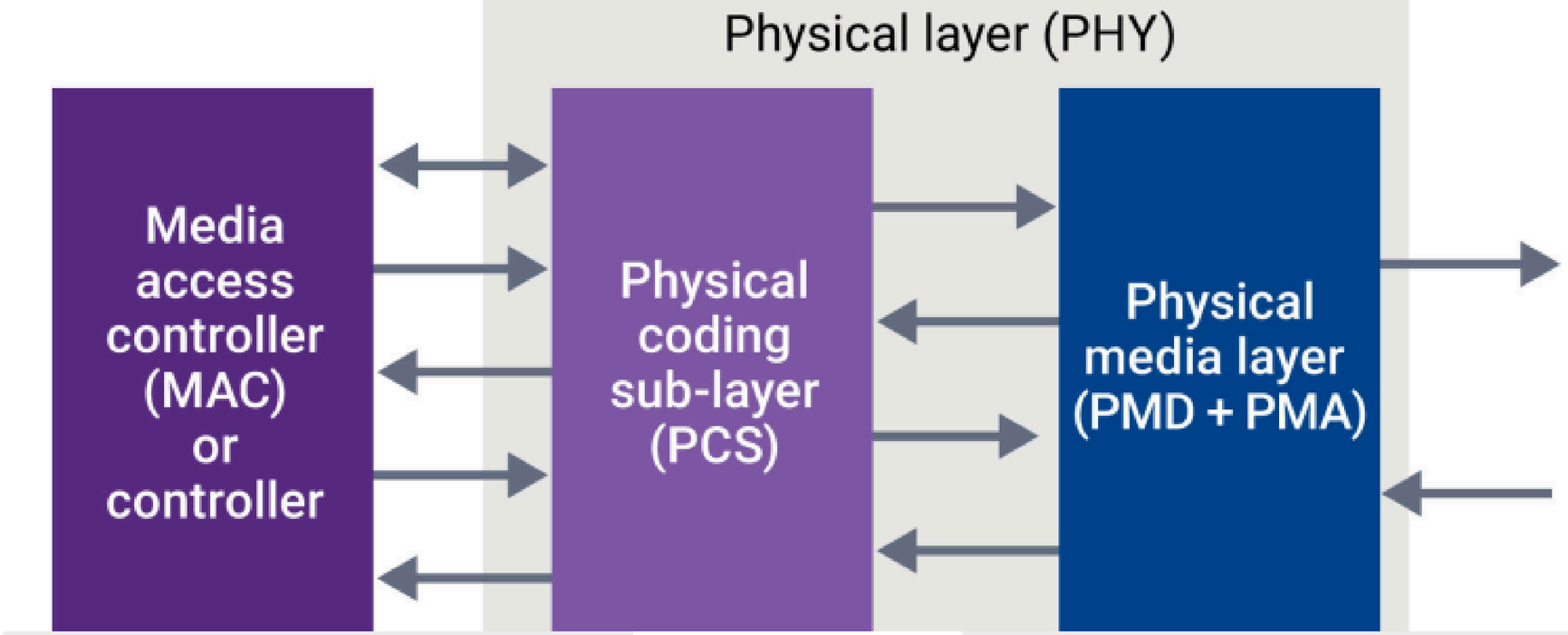
Cache Coherence IPs: Manage memory communication for multi-core processors.

Security IPs: Ensure secure communication with encryption and authentication.

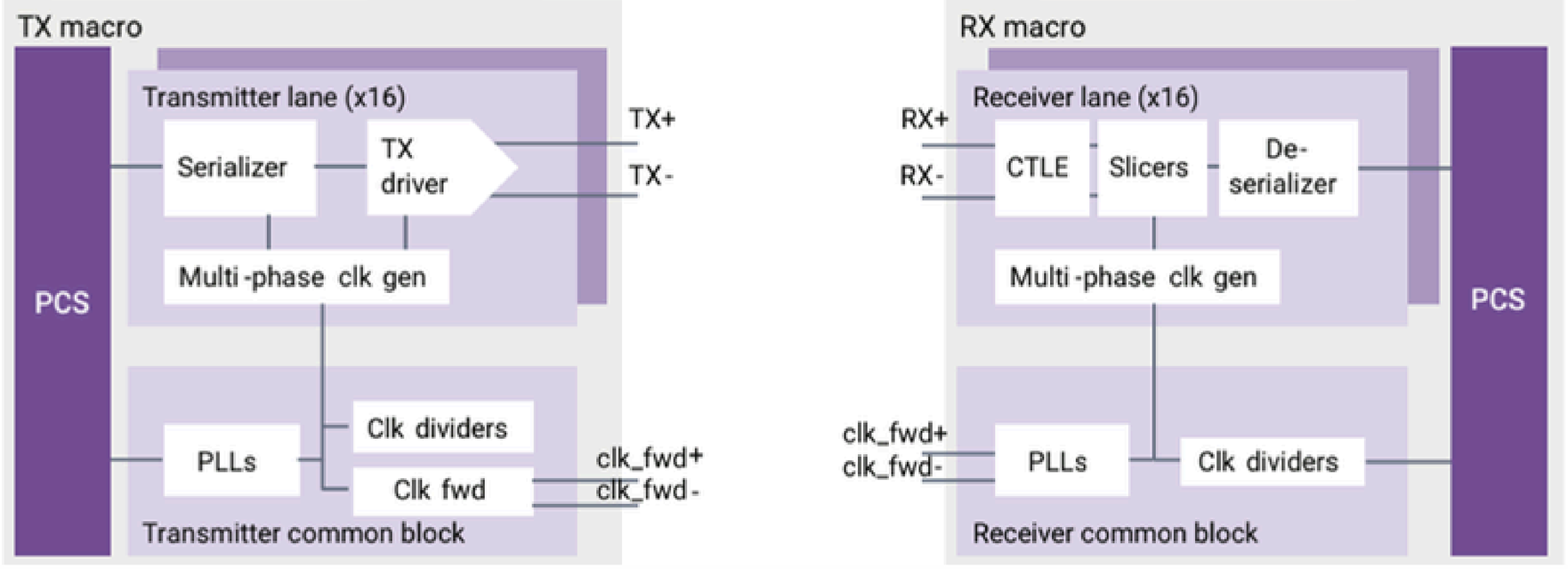
UCIe PHY IP architecture

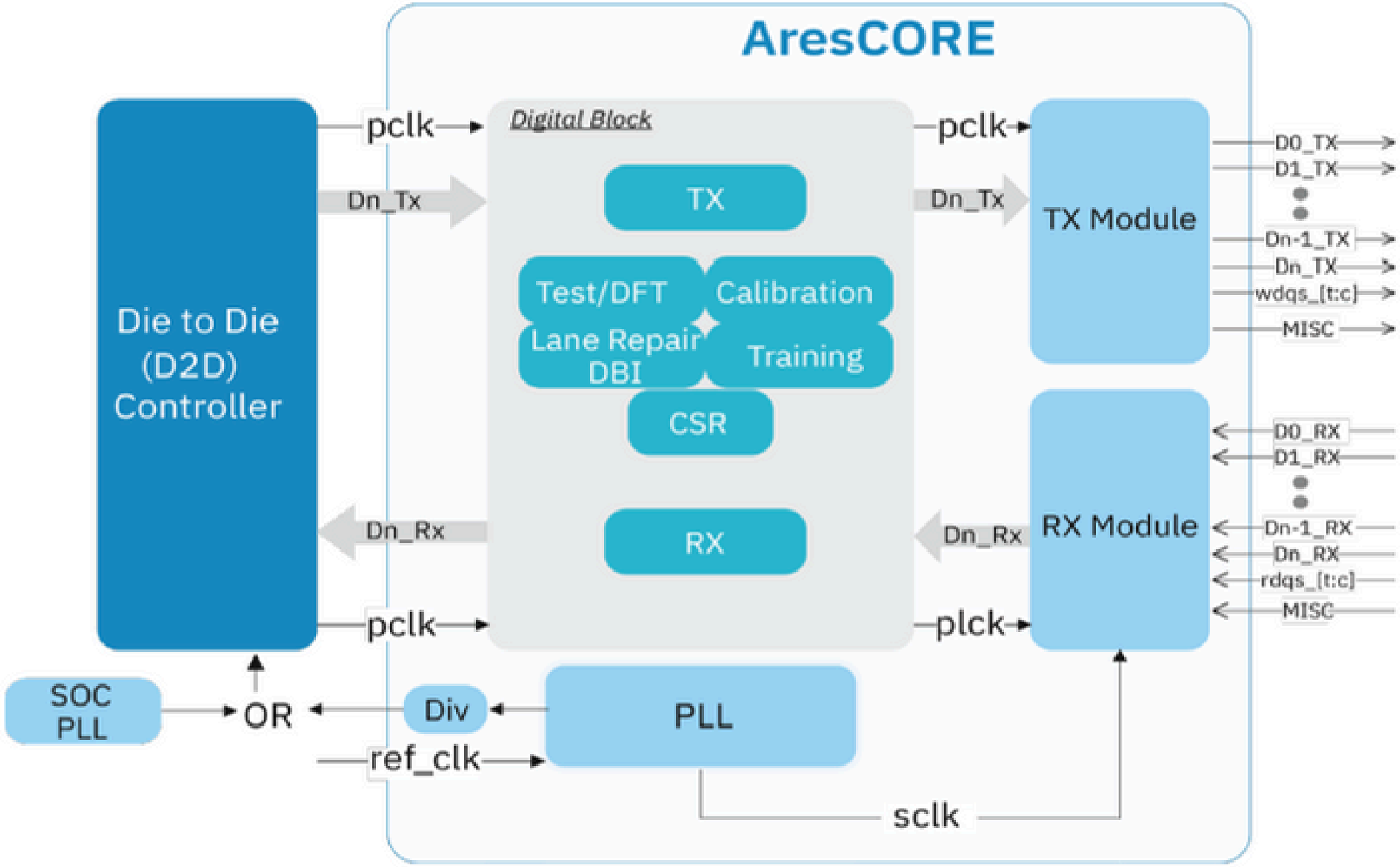





Physical layer (PHY)
Media access controller (MAC) or controller
Physical coding sub-layer (PCS)
Physical media layer (PMD + PMA)

XSR PHY IP


TX macro
Transmitter lane (x16)
Serializer
TX driver
TX+
TX-
Multi-phase clk gen
PCS
Clk dividers
PLLs
Clk fwd
clk_fwd+
clk_fwd-
Transmitter common block
RX macro
Receiver lane (x16)
RX+
RX-
CTLE
Slicers
De-serializer
Multi-phase clk gen
PCS
clk_fwd+
clk_fwd-
PLLs
Clk dividers
Receiver common block



D2D IP BLOCK DIAGRAM

Interconnect Technology for Automotive Chiplets

Recommended Technology: Optical Interconnects for Chiplets

Latency and Communication Efficiency

Latency - Optical interconnects can achieve latencies as low as 2 ns, significantly outperforming traditional electrical interconnects, which range from 5–15 ns. This low latency is crucial for real-time processing in automotive applications, such as Advanced Driver-Assistance Systems (ADAS).

Communication Efficiency: Optical interconnects provide a bandwidth of up to 400 Gbps per channel, allowing for high data rates essential for handling large volumes of sensor data, reducing bottlenecks in communication.

Research indicates that optical interconnects reduce power consumption by approximately 50% compared to electrical solutions, making them more suitable for energy-efficient automotive systems .

Cybersecurity and Reliability Strategies

Secure Communication:

Encryption Protocols: Implement end-to-end encryption (e.g., AES-256) for data integrity and confidentiality.

Secure Authentication: Use multi-factor authentication and secure key management to prevent unauthorized access.

- **Reliable Communication:**

Redundant Paths: Design optical networks with multiple pathways to ensure continuous operation in case of failure.

Real-Time Monitoring: Incorporate monitoring systems to detect anomalies and trigger automatic failover mechanisms.

Safety Consideration: Unlike server applications, automotive chiplets must ensure safety-critical data transmission, emphasizing reliability and security .

Innovative Approaches Beyond 2.5D/3D

Hybrid Optical-Electrical Interconnects: Integrate both optical and electrical connections to leverage the benefits of both technologies. This approach allows high-speed data transfer with the flexibility of traditional wiring for lower-speed signals, optimizing performance based on data needs.

Dynamic Load Balancing: Develop algorithms that dynamically allocate communication resources based on real-time demand, ensuring optimal performance and reliability even in fluctuating operational conditions.

Technology Type	Latency (ns) \	Bandwidth (Gbps)
Optical Interconnect	2	400
Electrical Interconnect	5-15	Up to 25

Challenges in Chiplet Integration

1. Thermal Interaction and Cooling

Heat Dissipation: Chiplets generate significant heat; effective cooling is critical.

Solutions: Use liquid metal thermal interface materials (TIMs)** for better thermal management.

2. Die-to-Die Interconnect Standards

Standardization: Essential for reliable connections and signal integrity.

3. Mechanical Durability

Harsh Environment: Chiplets must withstand vibration and shocks.

Protection: Use shock-absorbing materials and robust housing designs.

4. Scalability and Manufacturability

Design Standardization: Necessary for IP reuse and efficient prototyping.

Thermal Challenges in High-Performance Automotive Electronics

Increased Power Density: Modern semiconductor chips face thermal management challenges due to rising power densities and shrinking dimensions. For example, a power MOSFET measuring 10.4 mm × 6.73 mm × 2.36 mm can dissipate 83 W at 25 °C.

Material Innovations: High thermal conductivity materials are needed to manage heat effectively.

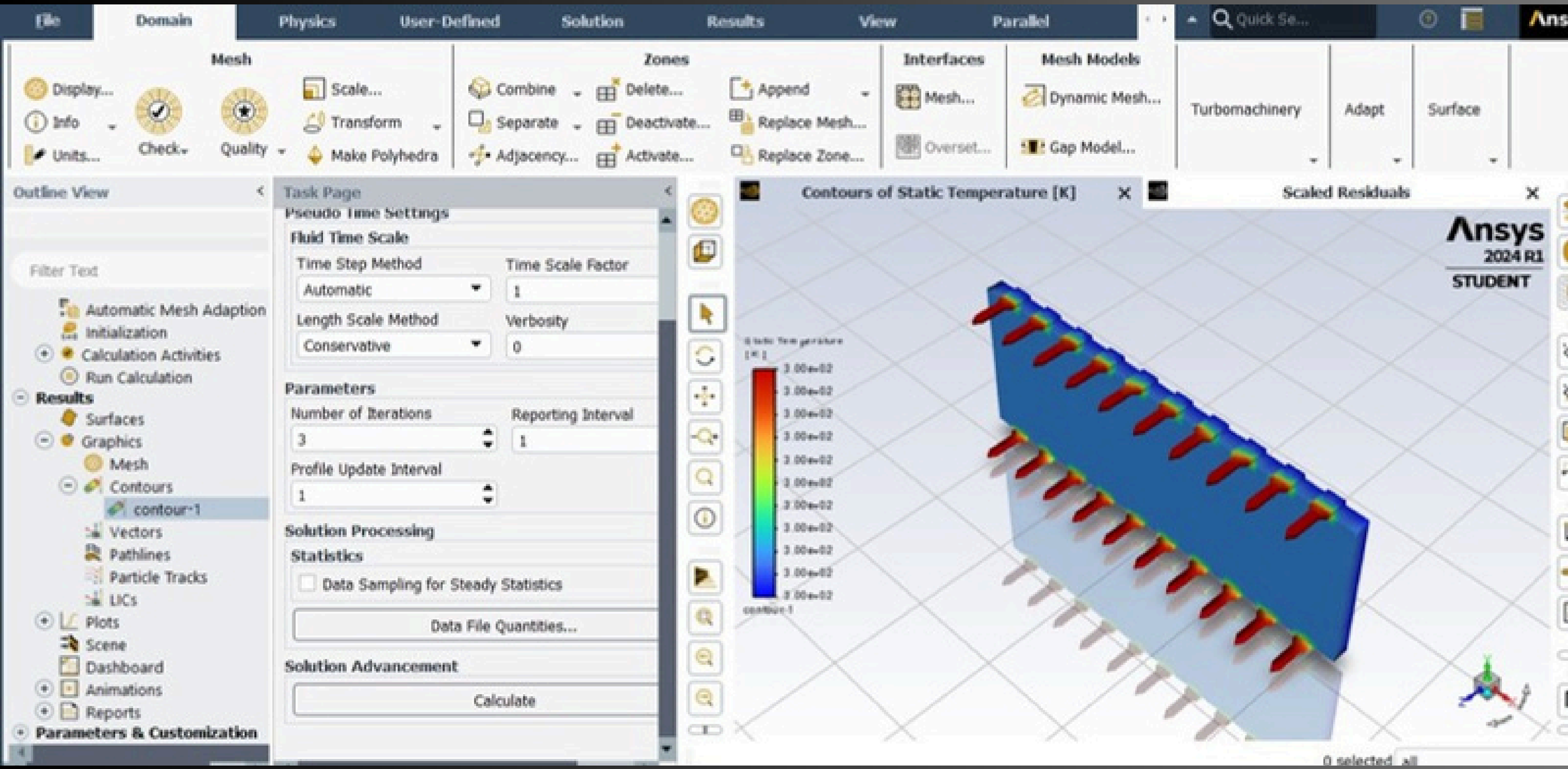
Metal Matrix Composites (MMCs) and thermally conductive polymers are recommended for ECU housings.

Carbon Nanotubes (CNTs) can improve thermal interface materials, enhancing heat dissipation.

Cooling Technologies:Pumped liquid cooling and advanced thermal materials can significantly improve heat management.

Phase-change materials (PCMs) and microchannel cooling solutions are effective in reducing thermal resistance, with microchannel heatsinks fabricated directly on silicon chips.

Overall, innovative materials and cooling techniques are crucial for meeting the thermal management demands of automotive electronics.


File
Domain
Physics
User-Defined
Solution
Results
View
Parallel
Quick Se...
Mesh
Display...
Info
Units...
Check
Quality
Scale...
Transform
Make Polyhedra
Zones
Combine
Separate
Adjacency...
Delete...
Deactivate...
Activate...
Append
Replace Mesh...
Replace Zone...
Interfaces
Mesh...
Overset...
Mesh Models
Dynamic Mesh...
Gap Model...
Turbomachinery
Adapt
Surface
Outline View
Filter Text
Automatic Mesh Adaption
Initialization
Calculation Activities
Run Calculation
Results
Surfaces
Graphics
Mesh
Contours
contour-1
Vectors
Pathlines
Particle Tracks
LICs
Plots
Scene
Dashboard
Animations
Reports
Parameters & Customization
Task Page
Pseudo Time Settings
Fluid Time Scale
Time Step Method
Automatic
Time Scale Factor
1
Length Scale Method
Conservative
Verbosity
0
Parameters
Number of Iterations
3
Reporting Interval
1
Profile Update Interval
1
Solution Processing
Statistics
Data Sampling for Steady Statistics
Data File Quantities...
Solution Advancement
Calculate
Contours of Static Temperature [K]
Scaled Residuals
Ansys
2024 R1
STUDENT
0 selected

Tree Outline

- A: Fluid Flow (Fluent)
  - XYPlane
  - ZXPlane
  - YZPlane
  - Import1
  - 1 Part, 1 Body

Sketching | Modeling

Details View

Details	
Bodies	1
Volume	...
Surface Area	...
Faces	247
Edges	776
Vertices	532

Graphics

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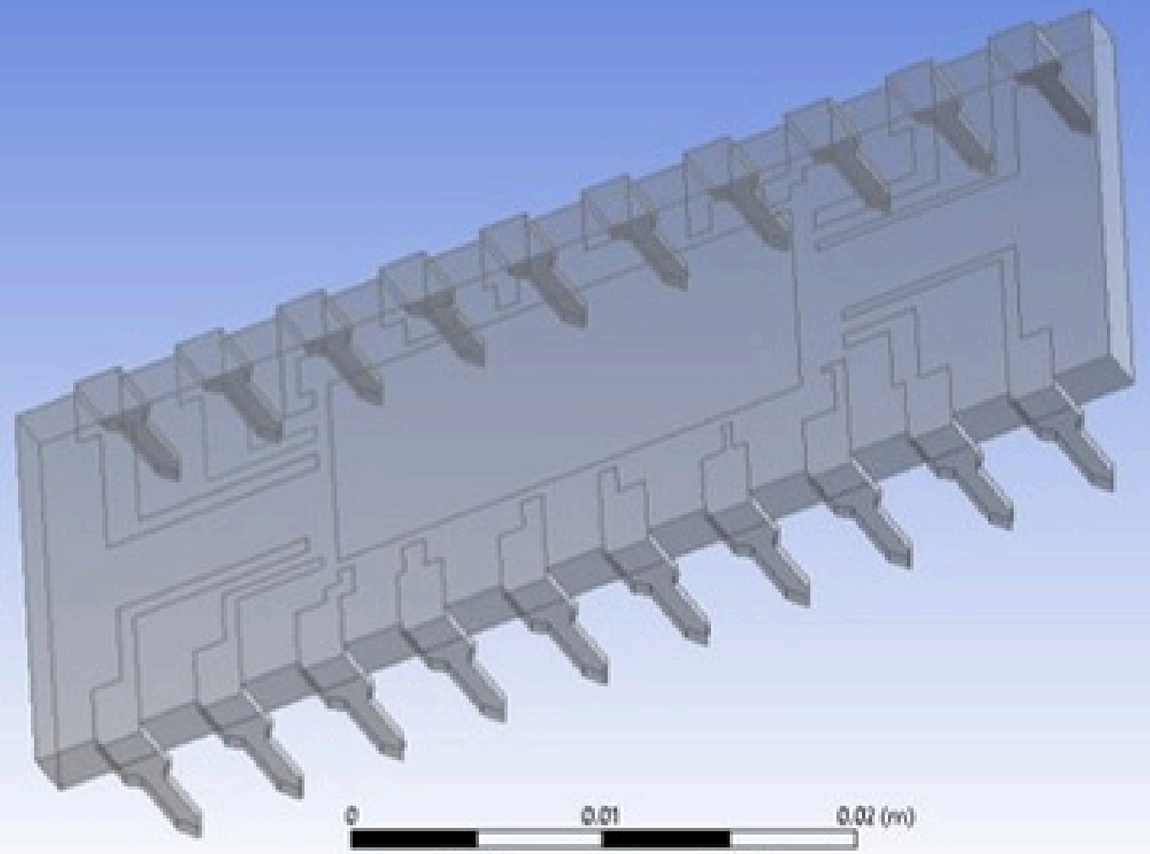
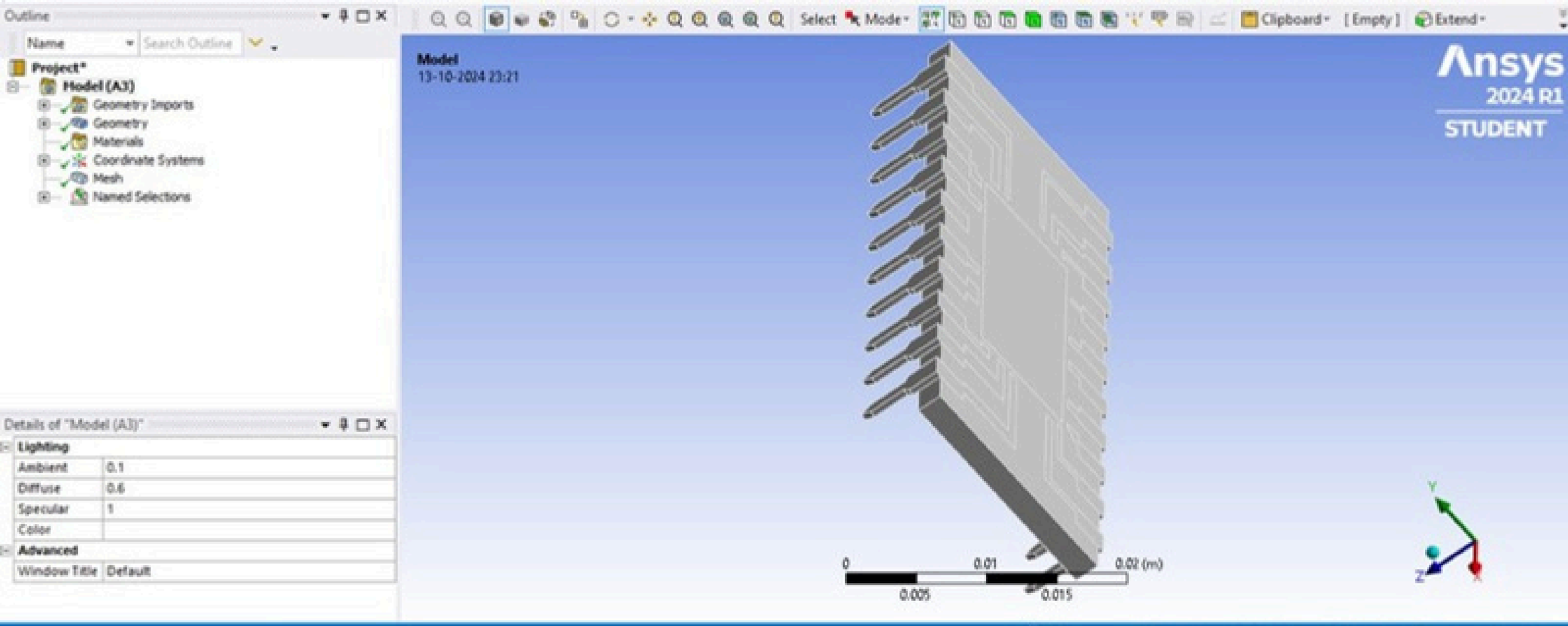


0 0.01 0.02 (m)
0.005 0.015

Y
X
Z

Model View | Print Preview


Outline
Name
Search Outline
Project*
Model (A3)
Geometry Imports
Geometry
Materials
Coordinate Systems
Mesh
Named Selections
Details of "Model (A3)"
Lighting
Ambient 0.1
Diffuse 0.6
Specular 1
Color
Advanced
Window Title Default
Select
Mode
Clipboard
[Empty]
Extend
Model
13-10-2024 23:21
Ansys
2024 R1
STUDENT
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0.01
0.02 (m)
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Conclusion

Jaguar Land Rover (JLR) should adopt chiplet technology to enhance its automotive applications, particularly in Advanced Driver-Assistance Systems (ADAS) and in-vehicle infotainment. This integration enables modular design, allowing for optimized performance and scalability.

For communication, JLR must prioritize low latency and high efficiency while implementing robust cybersecurity measures to ensure reliable operation in safety-critical environments. This distinction is crucial as automotive applications demand greater reliability than server systems.

Thermal management will be pivotal, and advanced cooling solutions, such as microchannels or phase-change materials, should be adopted to dissipate heat efficiently.

In relation to Moore's Law, while it has historically driven chip performance improvements, its potential to continue doing so may face limitations as we approach physical and economic constraints in semiconductor technology. However, chiplet technology can help circumvent some of these limitations by allowing for more flexible and scalable designs, ultimately aligning with the spirit of Moore’s predictions.

THANK YOU