## Vidyavardhini's College of Engineering and Technology

## Department of Artificial Intelligence & Data Science

AY: 2024-25

Class:

SE.

Semester:

TIL

Course Code:

CSC 304 Course Name:

DIGITAL LOGIC & COMPUTER ARCHITECTURE

Name of Student:	SHRUTI GAUCHANDRA
Roll No. :	15
Assignment No.:	06
Title of Assignment:	Compare Serial/Paraellel processing & ISA,
Date of Submission:	
Date of Correction:	

## **Evaluation**

Performance Indicator	Max. Marks	Marks Obtained
Completeness	5	
Demonstrated Knowledge	3	3
Legibility	2	
Total	10	8

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Completeness	5	3-4	1-2
Demonstrated Knowledge Legibility	3	2	1
Legibility	2	1	0

Checked by

Name of Faculty

: MS KSHITIJA GHARAT

Signature

: (Kharat

Date







