Vidyavardhini's College of Engineering and Technology

Department of Artificial Intelligence & Data Science

AY: 2024-25

Class:	SE	Semester:	III
Course Code:	CSC304	Course Name:	DIGITAL LOGIC & COMPUTER ARCHITECTURE

Name of Student:	SHRUTI GAUCHANDRA
Roll No. :	15
Assignment No.:	01
Title of Assignment:	Convert one number system to another and realize logic circuits using basic gates
Date of Submission:	06/08/24
Date of Correction:	06/08/24

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Demonstrated knowledge	5	4
Legibility	3	2
Completeness and timely submission	2	2
Total	10	8

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Demonstrated Knowledge	5	3-4	1-2
Legibility	3	2	1
Completeness and Timely submission	2	1	0

Checked by

Name of Faculty : MS. KSHITIJA GHARAT

Signature : Gharat

Date : 6/8/24

Q1. Convert Octal $(532.125)_8$ to decimal, binary and hexadecimal

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① Octal to Decimal

Whole part: 532

$= (5 \times 8^2) + (3 \times 8^1) + (2 \times 8^0)$

$= (5 \times 64) + (3 \times 8) + (2 \times 1)$

$= 320 + 24 + 2$

$= 346$

Fractional part: .125

$= (1 \times 8^{-1}) + (2 \times 8^{-2}) + (5 \times 8^{-3})$

$= \left(1 \times \frac{1}{8}\right) + \left(2 \times \frac{1}{64}\right) + \left(5 \times \frac{1}{512}\right)$

$= 0.125 + 0.03125 + 0.009765625$

$= 0.166015625$

∴ Result: $346 + 0.166015625$

$= 346.0166015625$

∴ $(532.125)_8 = (346.0166015625)_{10}$

② Octal to Binary:

5 3 2 . 1 2 5

$= 101\ 011\ 010.\ 001\ 010\ 101$

$= 101011010.001010101$

∴ $(532.125)_8 = (101011010.001010101)_2$

(5) Octal to Hexadecimal

By using binary representation of the Octal number

$(532.125)_8 = (101011010.001010101)_2$

$= 0001\ 0101\ 1010 . 0010\ 1010\ 1000$

$1\quad 5\quad 10 . 2\quad 10\quad 8$

$= A \qquad = A$

$(532.125)_8 = (15A.2A8)_{16}$

Ans: $(532.125)_8 = (346.166015625)_{10}$

$(532.125)_8 = (101011010.001010101)_2$

$(532.125)_8 = (15A.2A8)_{16}$

Q2. Convert $(29)_{10}$ into gray code:

→ $(29)_{10}$

Binary representation is

2	29	
2	14	1
2	7	0
2	3	1
	1	1

LSB

2	29	1
2	14	0
2	7	1
2	3	1
	1	1

MSB

$\therefore (29)_{10} = (11101)_2$

Binary code : 1 1 1 0 1

⊕ ⊕ ⊕ ⊕

↓ ↓ ↓ ↓ ↓

Gray code : 1 0 0 1 1

$(11101)_2 = (10011)_{Gray\ code}$

$\therefore (11101)_2 = (10011)_{Gray\ code}$

Q3. Explain the Von-Neumann architecture.

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① Von-Neumann computer architecture was proposed in 1945. It was later known as Von-Neumann architecture.

② There are two types of computers.
   (a) Fixed Program Computers.
   (b) Stored Program Computers.

③ (a) Fixed Program Computers - Their function is very specific and they couldn't be programmed eg: Calculators

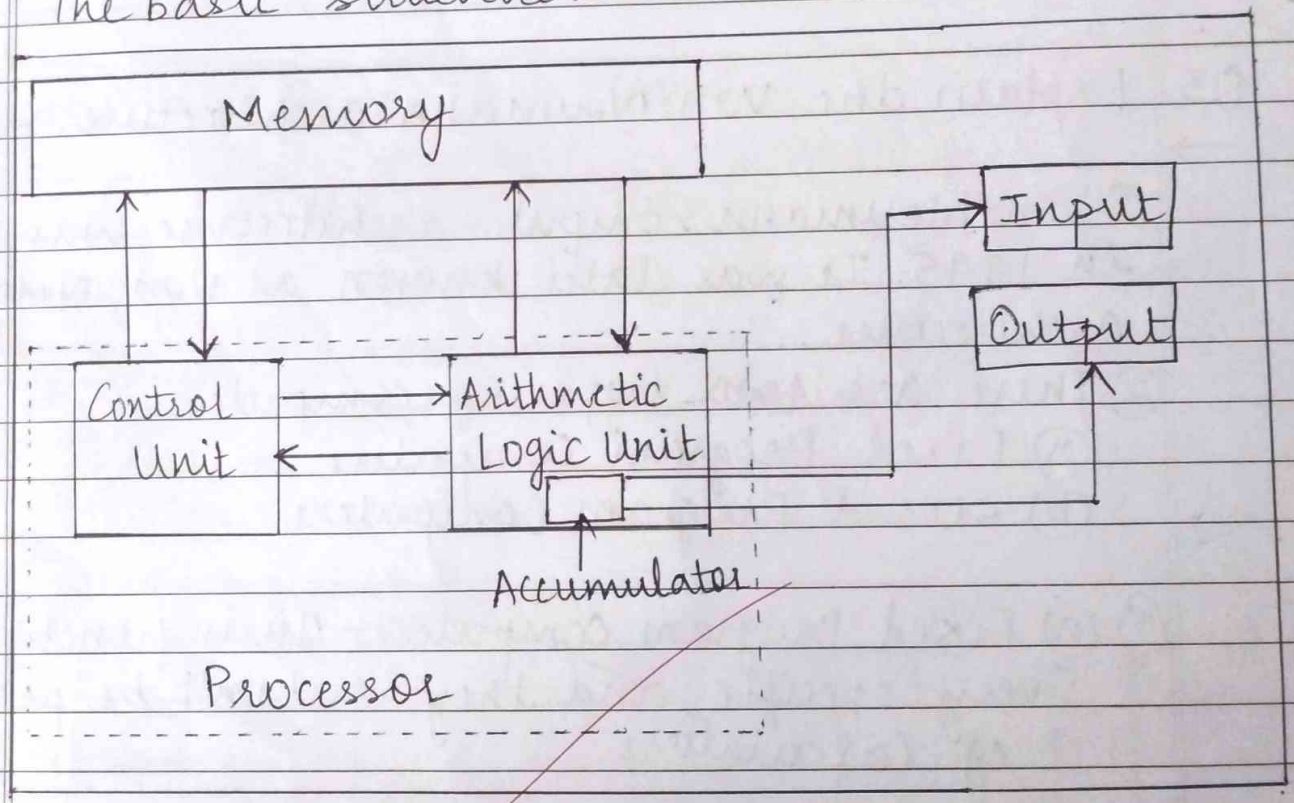
   (b) Stored Program Computers - These can be programmed to carry out many different tasks, applications are stored on them, hence the name.

④ The mordern computers are based on a stored-

program concept introduced by John Von Neumann.

In this stored-program concept, programs and data are stored in a seperate storage unit called memories. This novel idea meant that a computer built with this architecture would be much easier to reprogram.

The basic structure is :



It is also known as IAS computer is having three basic units :

(a) Central Processing Unit
(b) The Main Memory Unit
(c) The Input/Output Device.

⑥ The Central Processing Unit is an electric circuit used for the execution of computer program. It has major components:

(i) Control Unit (CU)
(ii) Arithmetic & Logic Unit (ALU)
(iii) Variety of registers:

(i) Control Unit: A control unit (CU) handles all processor control signals, it directs all input and output flow, fetches code for instructions and controls how data moves around the system.

(ii) Arithmetic & Logic Unit (ALU): The arithmetic logic unit is that part of the CPU that handles all the calculations the CPU may need, eg: Addition, Subtraction, Comparisions. It performs Logical Operations, & Arithmetic operations.

(iii) Registers: These refer to high-speed storage areas in CPU. Types of registers used in are:

ⓐ Main Memory Unit - Accumulator: Stores the results of calculations made by ALU
ⓑ Program Counter (PC): Keeps track of the memory location of the next instructions to be dealt with. The PC then passes this next address to Memory Address Register (MAR)
ⓒ Memory Address Register (MAR): It stores the memory locations of instructions that

need to be fetched from the memory or stored into the memory.

(d) Memory Data Register (MDR): It stores instructions fetched from memory or any data that is to be transferred to, and stored in, memory.

(e) Current Instruction Register (CIR): It stores the most recently fetched instructions while it is waiting to be coded and executed

(f) Instruction Buffer Register (IBR): The instruction that is not to be executed immediately is placed in the instruction buffer register IBR.

(7) Input/Output Devices: Program or data is read into main memory from the input device or secondary storage under the control of CPU input instruction. Output devices are used to output the information from a computer.

If some results are evaluated by computer and it is stored in the computer, then with the help of output devices, we can present them to the user.

(8) Buses: Data is transmitted from one part of a computer to another, connecting all major internal components to the CPU and memory, by the means of Buses.

Types:

(i) Data Bus:

It carries data among the memory unit, the I/O devices, and the processor.

(ii) Address Bus:

It carries the address of data (not the actual data) between memory and processor

(iii) control Bus:

It carries control commands from the CPU (and status signals from other devices) in order to control and co-ordinate all the activities within the computer