Vidyavardhini's College of Engineering and Technology

Department of Artificial Intelligence & Data Science

AY: 2024-25

Class:	SE	Semester:	III
Course Code:	CSC304	Course Name:	DIGITAL LOGIC & COMPUTER ARCHITECTURE

Name of Student:	SHRUTI GAUCHANDRA
Roll No. :	15
Assignment No.:	05
Title of Assignment:	Apply concepts of Cache Parameters
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Completeness	5	4
Demonstrated Knowledge	3	3
Legibility	2	1
Total	10	8

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Completeness	5	3-4	1-2
Demonstrated Knowledge Legibility	3	2	1
Legibility	2	1	0

Checked by

Name of Faculty : MS. KSHITIJA GHARAT

Signature : Gharat

Date : 11/10/24

Q1. Consider a 4-way set associative mapped cache with block size 4 KB. The size of the main memory is 16 GB and there are 10 bits in the tag.
Find – 1) Size of cache memory
2) Tag directory size.

→ Given:
- Cache type: 4-way set associative
- Block size = 4 KB
- Main Memory = 16 GB
- Tag size = 10 bits

Main memory size = 16 GB = 2^{34} bytes
Block size = 4 KB = 2^{12} bytes.

Since the block size is 4 KB, we need 12 bits to select a word.
Word bits = 12 bits

Tag (10 bits)	Set (12 bits)	Word (12 bits)

From the cache layout
- Tag = 10 bits
- Set = 12 bits
- Word = 12 bits

Total adress bits = 34 bits

a) Cache size = $2^{12} \times 4 \times 2^{12} = 2^{26}$ bytes
= 64 MB.

b) Tag directory size $= 2^{12} \times 4$
$= 2^{14}$ entries
$= 16$ K entries

Q2. The diagram shows an instruction stored in memory address 200 and 201. The address part of instruction has value 500. The computer has a processor register by name R1 having value 400. Calculate / Find the effective address and contents of AC register for all the addressing modes discussed in the previous topic

i. Register mode
ii Register indirect mode
iii Direct address mode
iv Indirect address mode
v Relative mode
vi Index mode
vii Intermediate mode

	Address	Memory	
PC = 200	200	Load to AC	Mode
	201	Address = 500	
R1 = 400	202	Next instruction	
	.		
XR = 100	400	700	
	600	900	
AC	800	300	

→ Given -

PC (Program counter) = 200

R1 = 400

XR = 100

AC (Accumulator)

Memory values

Address	Loaded to AC	Memory
200	Address = 500	
201	Next instr	
399		450
400		700
500		800
702		325
800		300

(i) Register mode:

- Effective Address : NO memory lookup, data is directly in the register.
- AC content - Value in register.
- Result - The value of R1 = 400.

(ii) Register Indirect mode:

- Effective Address = The address stored in the register.
- AC content = Value of R1.
- Result - R1 = 400

Memory address = 700

(iii) Direct Address Mode
- Effective Address - The address is given directly by instruction.
- AC Contents - Memory address = 500
- Result : PC = 200
  M. Address = 500
  Content of AC = 800

(iv) Indirect Address Mode
- Effective Address - The address stored at the given memory address.
- AC Contents - Value stored at final effective address.
- Result - Content of 500 = 800
  Content of memory address 800 = 300

(v) Relative Mode
- Effective Address - The address is relative to Program Counter (PC)
- AC Contents - Value stored at effective address
- Result - Effective address = 700
  Memory content at 700 = 800

(vi) Index Mode :
- Effective Address - The address is given by adding an index to the base address
- AC Contents - Value stored at indexed address.

- Result - Base address = 500 and XR = 100
  Effective address = 600
  Memory at 600 = 900

(vi) Immediate Mode

- Effective Address: No memory address, the operand is part of the instruction itself
- AC Contents. - Immediate value
- Result - The instruction contains the value 500, so AC = 500

Addressing Mode	Effective Address	AC Contents
• Register Mode	-	400
• Register indirect Mode	400	700
• Direct Address Mode	500	800
• Indirect Address Mode	800	300
• Relative mode	700	800
• Index mode	600	900
• Intermediate mode	-	500