Full subtractor using Nand gate~~l Paper Title~~

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Abstract — In digital systems, optimizing for power efficiency and design simplicity is a key challenge. This work presents a full subtractor circuit realized entirely using NAND gates, exploiting the fact that NAND is a functionally complete logic primitive. The proposed design accepts three inputs — the minuend (A), the subtrahend (B), and the borrow-in (Bin) — and produces s(Bout). The circuit is implemented without using any other gate types, thereby minimizing component heterogeneity and potentially reducing layout complexity and power overhead. We derive the Boolean expressions of D and Bout in terms of NAND operations, show the gate-level implementation, and verify the functional correctness through simulation. Performance metrics such as gate count, propagation delay, and power consumption are compared against conventional implementations using mixed logic gates. The results demonstrate that the NAND-only subtractor attains competitive performance with a modest overhead in gate count but benefits from uniform gate design and ease of fabrication. The design is scalable and can be cascaded to build multi-bit subtractors. Keywords — Full subtractor, NAND logic, functional completeness, low power, digital design, borrow-out

Reference Circuit Details ~~Introduction~~

In my complete subtractor design, I broke down the difference and borrow equations utilizing fundamental logic. To create intermediate inverted signals, I employed 3 NOT gates to invert primary inputs or internal signals.
The 4 NOR gates assist in forming specific complements or combined conditions (as NOR serves as the complement of OR). The 2 OR gates are utilized to merge borrow terms or intermediate signals directly. The 5 NAND gates execute essential product (AND) terms and also provide inversion when necessary (given that NAND equals inverted AND). Collectively, this configuration of gates accurately realizes both the difference output (through XOR-like logic constructed from these gates) and the borrow-out output (through the sum of product terms). This combination of gates effectively implements the full subtractor logic with reduced gate usage while preserving correct logical functionality.

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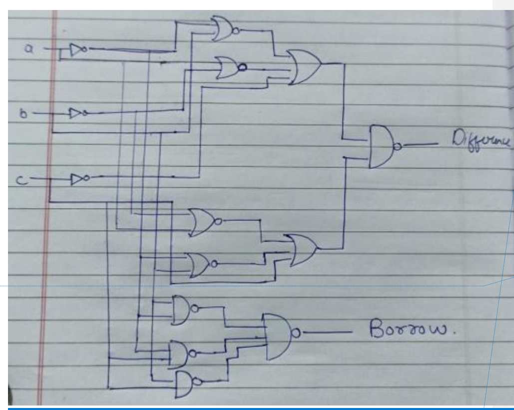
Reference Circuit



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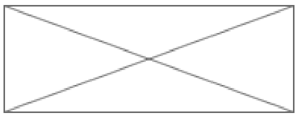

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~~Table 1. Table type styles.~~

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Figure 1: Reference circuit diagram.

Reference waveform

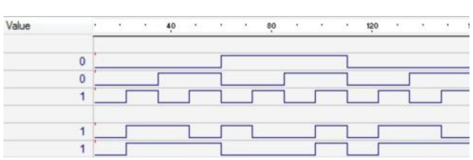

Figure 2: Reference waveform.

Reference

1. Beltran Jr., Angelo A., Kristina Nones, Reina Louise Salanguit, Jay Bhie Santos, Jose Maria Rei Santos & Keith Joseph Dizon, "Low Power NAND Gate–based Half and Full Adder / Subtractor Using CMOS Technique."~~Multipliers can be especially confusing. Write "Magnetization (kA/m)" or "Magnetization (10^3 A/m)." Do not write "Magnetization (A/m) x 1000" because the reader would not know whether the top axis label in figure means 15 000 A/m or 0.015 A/m.~~

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~~[2] M. S. MacNealy, *Strategies for Empirical Research in Writing*. Boston, MA: Allyn and Bacon, 1999.~~

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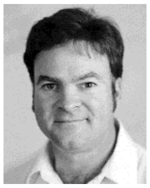

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