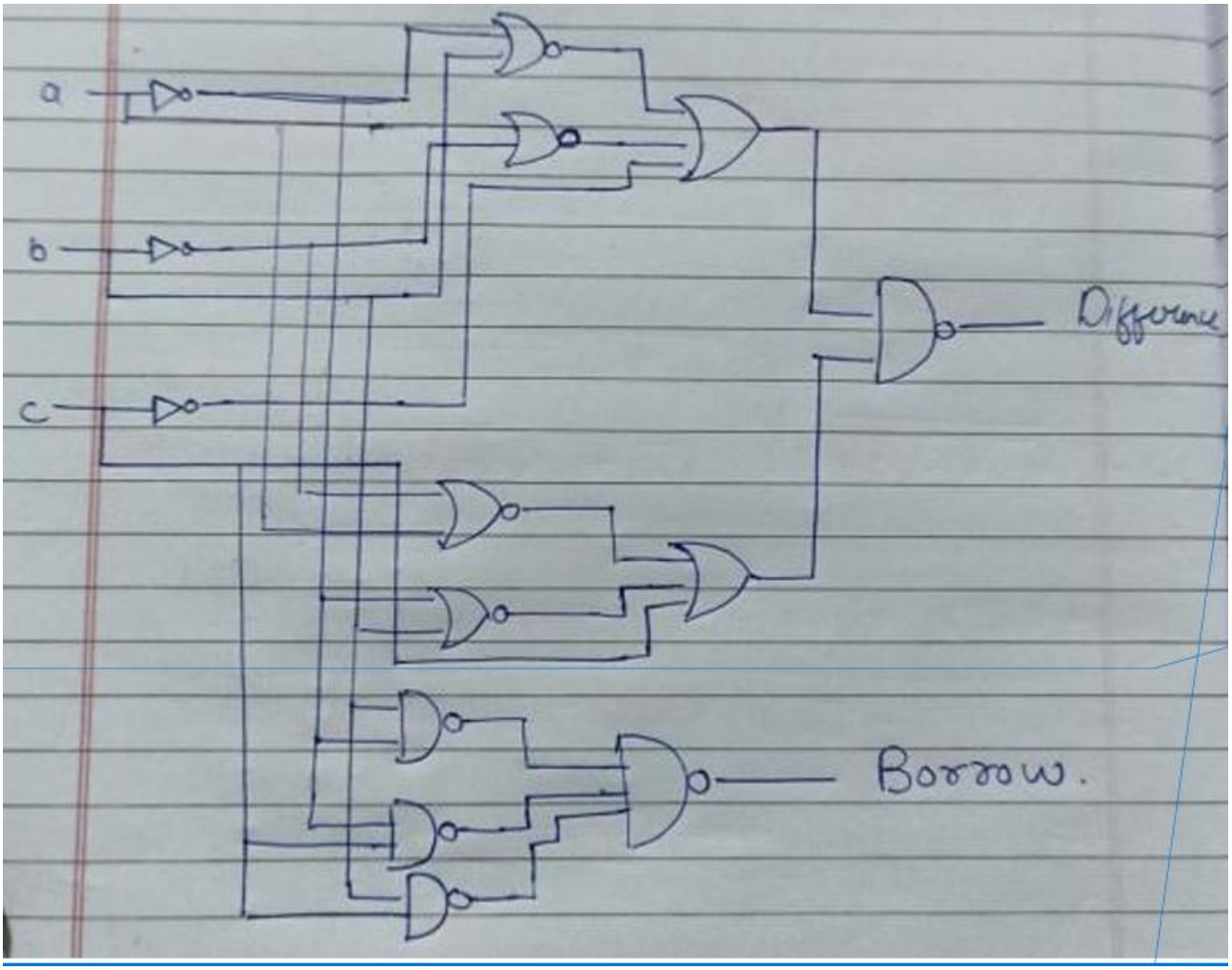
Project title : Full subtractor using nand gate

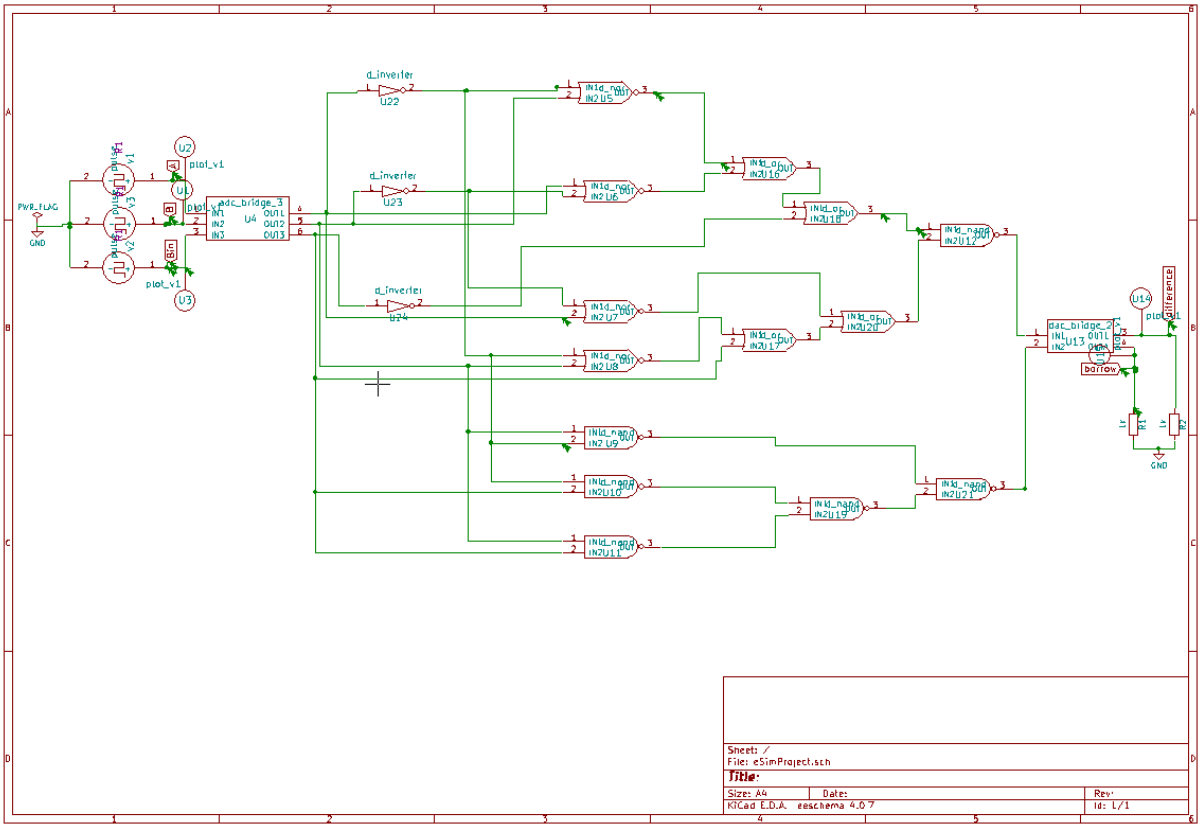
Objective :

In order to learn how various logic gates can be combined to perform binary subtraction, the goal of this experiment is to design, implement, and verify the operation of a Full Subtractor circuit using a combination of 6 NAND gates, 4 OR gates, 4 NOR gates, and 3 NOT gates. To show how different logic gate combinations can be used to implement arithmetic operations in digital electronics, the primary goal is to design and validate a Full Subtractor circuit using six NAND, four OR, four NOR, and three NOT gates.

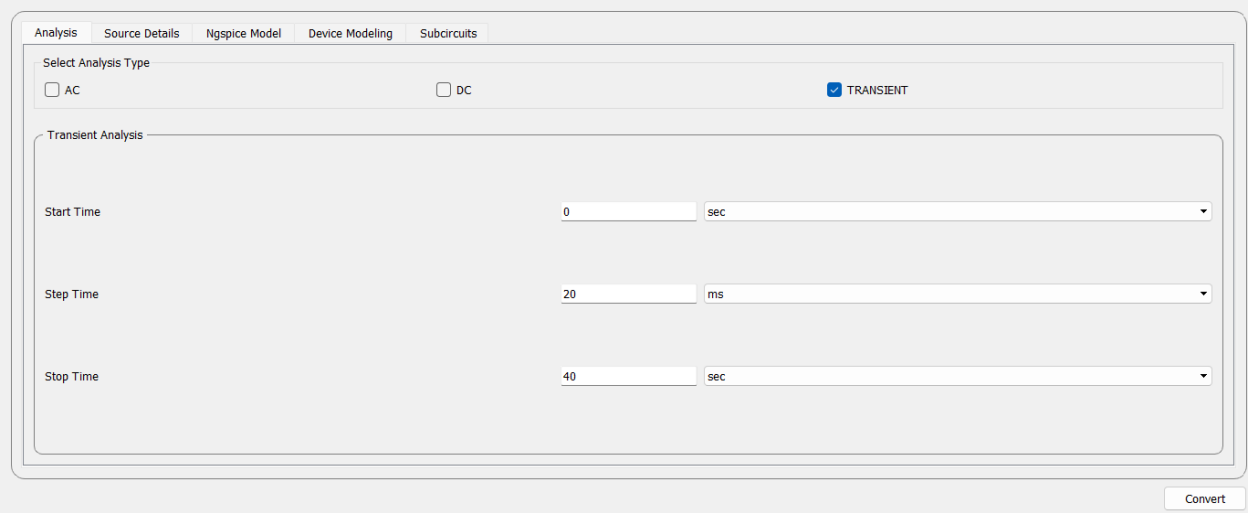
Circuit diagram:

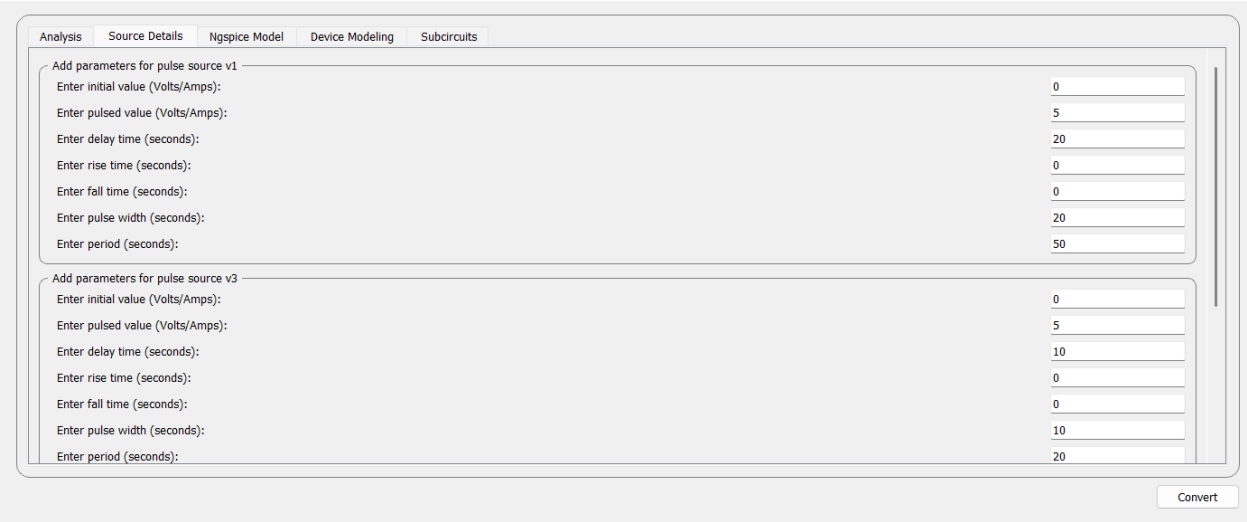


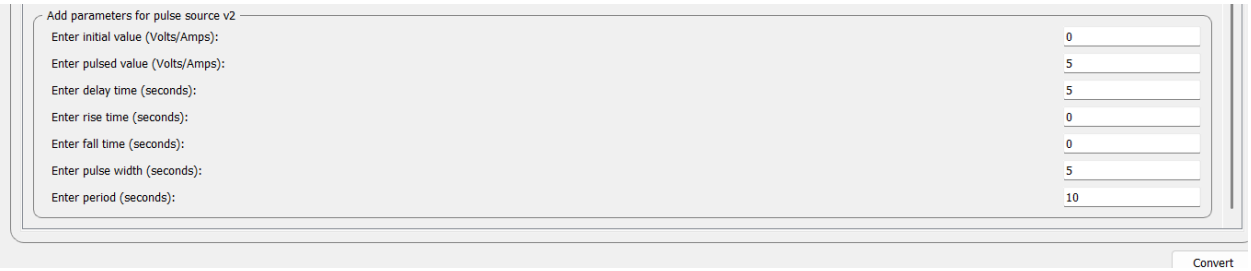
Circuit schematic:



Source details :



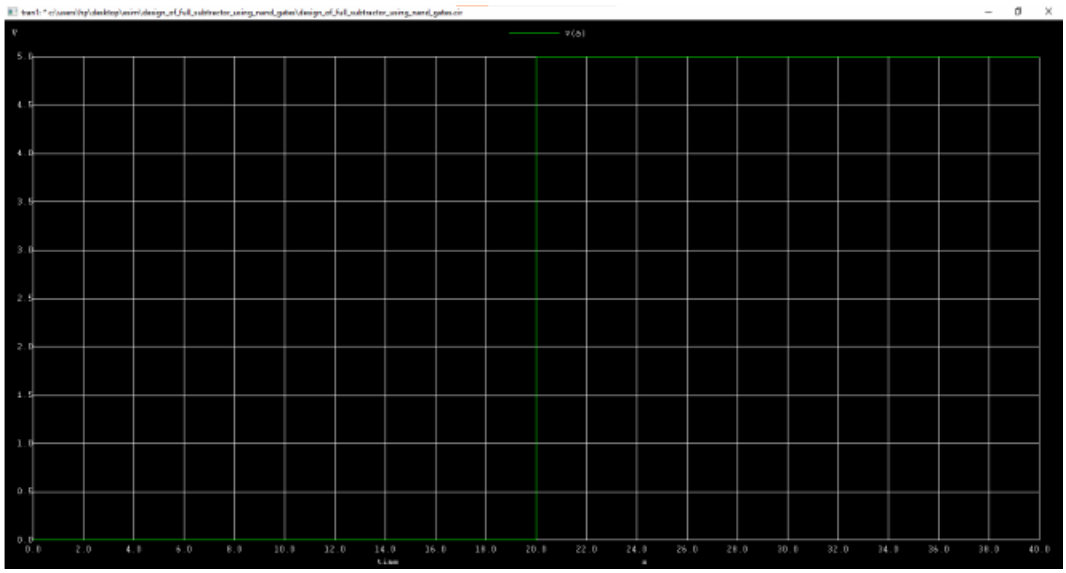




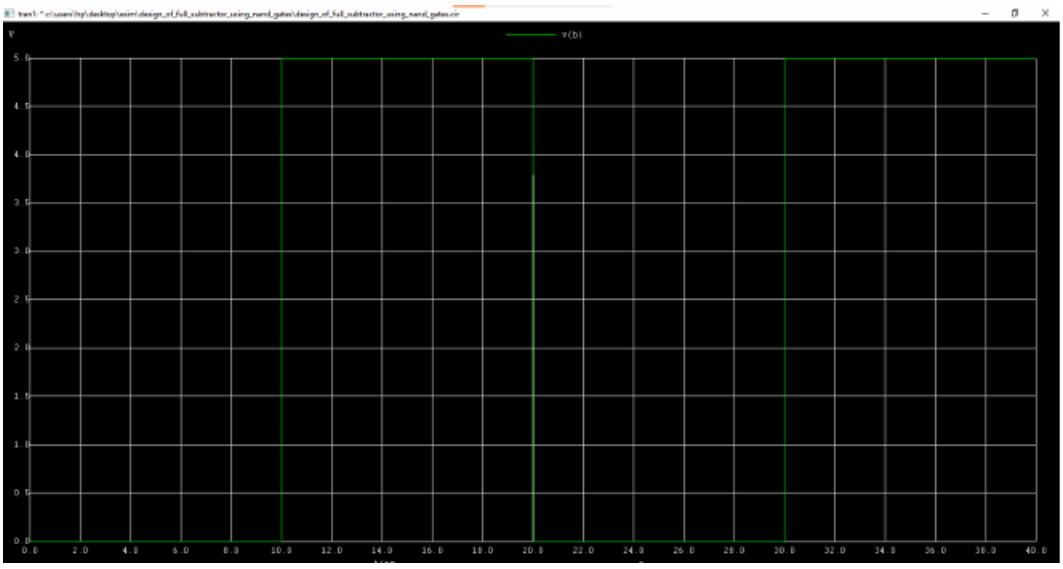
Simulation Result :

Input :

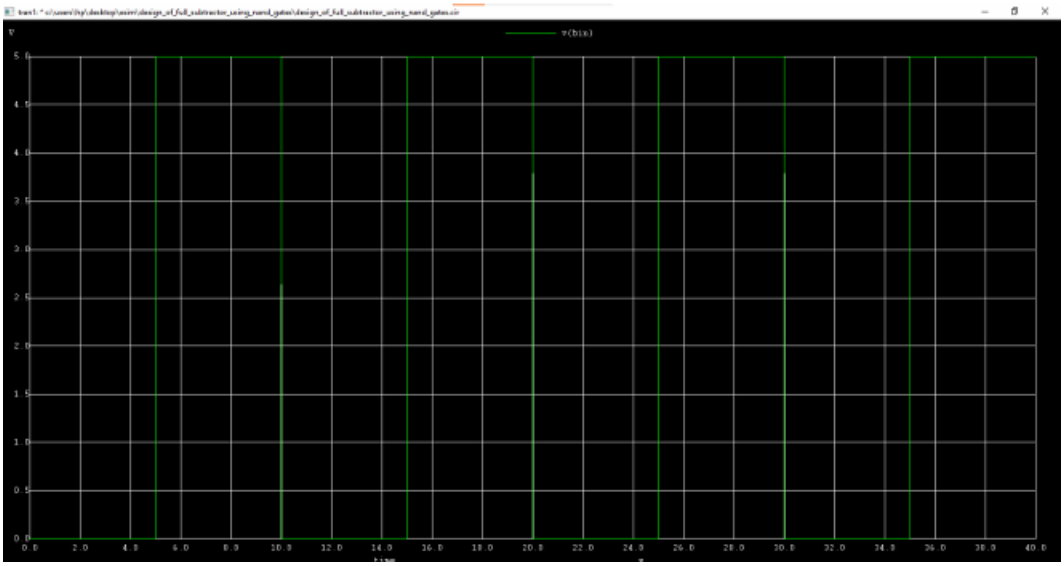
A



B

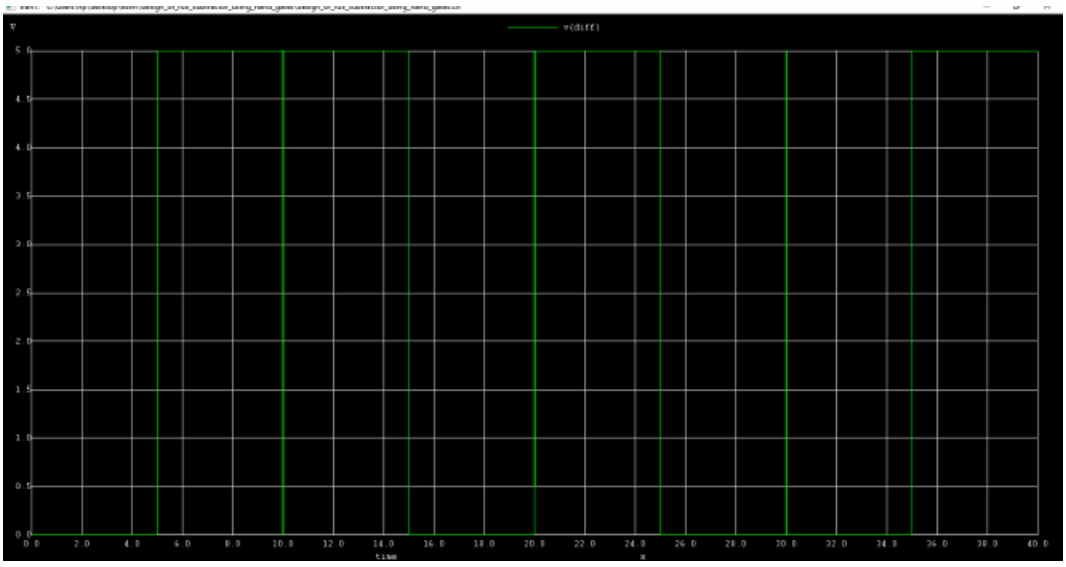


Bin

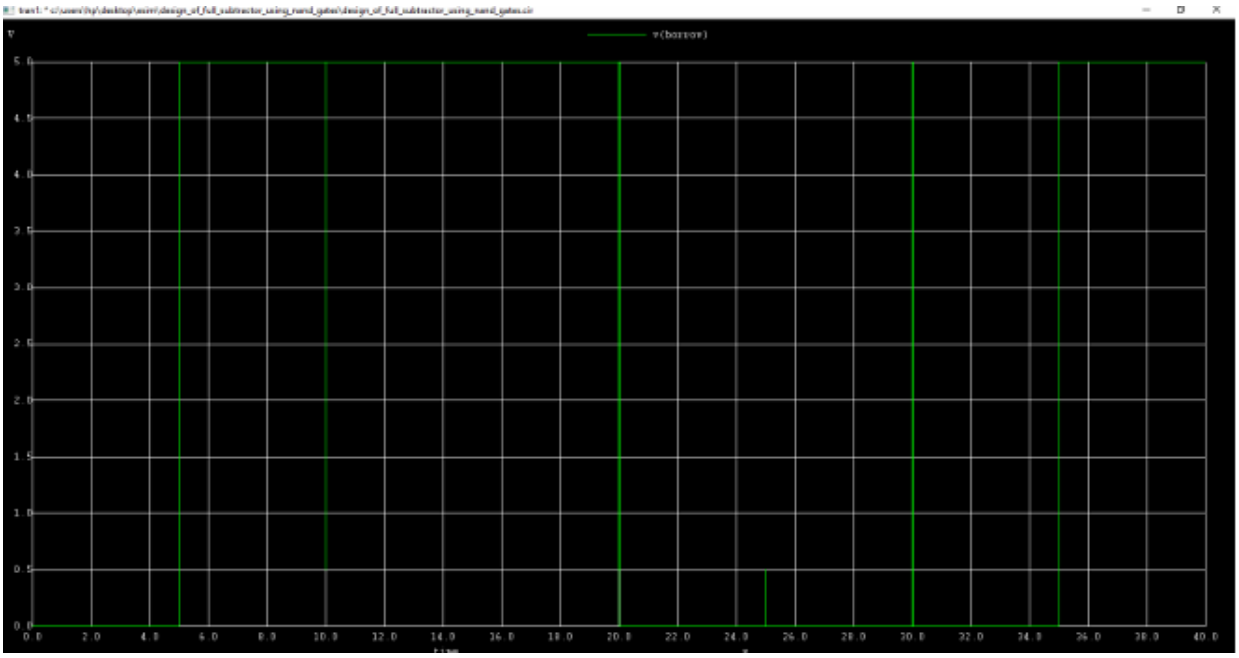


Output :

Difference



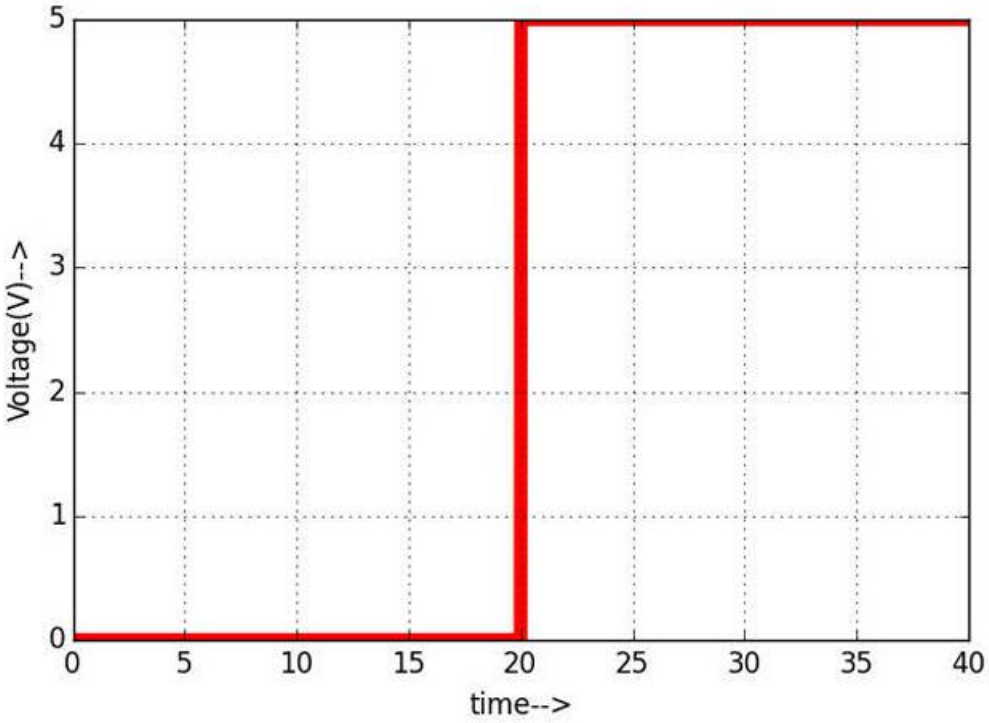
Borrow



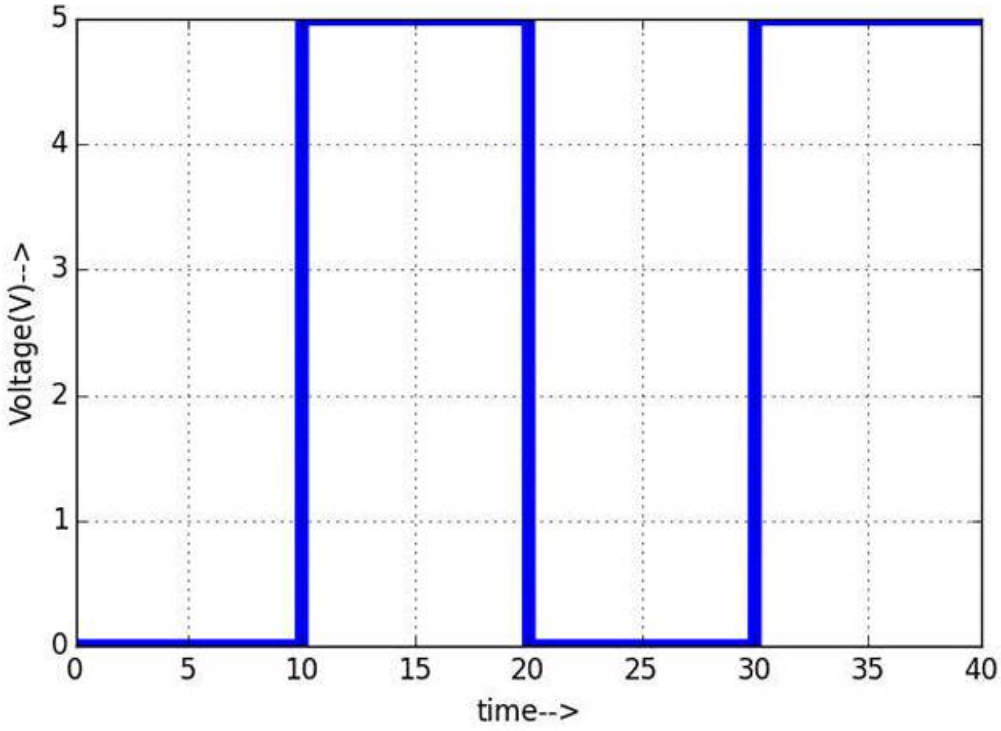
Python plot :

Input :

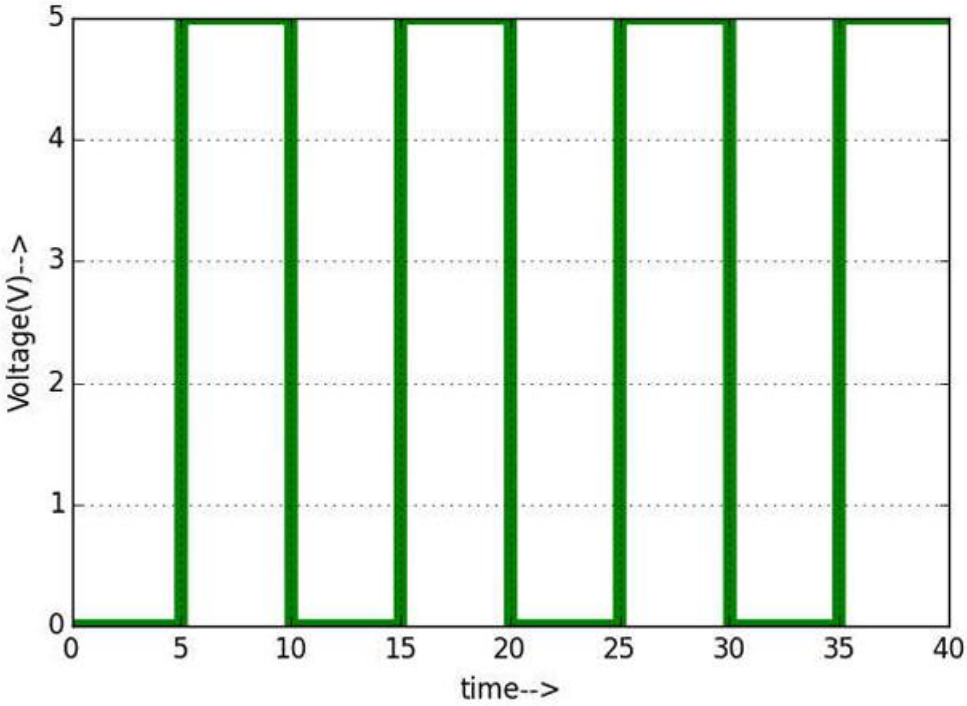
A



B

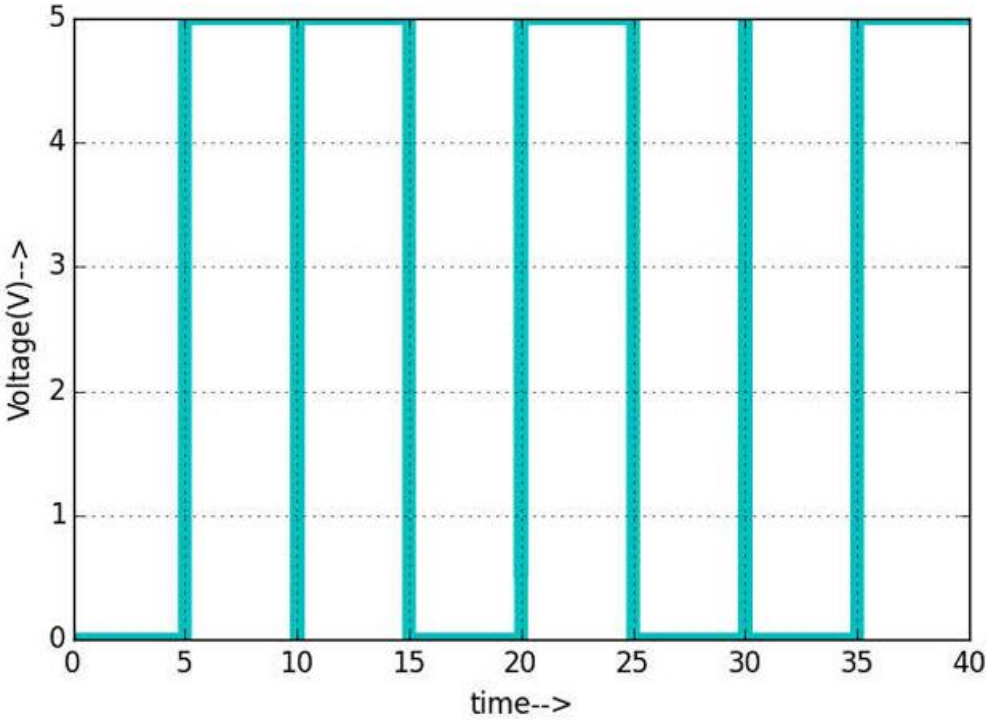

Voltage(V)-->
time-->
0
1
2
3
4
5
0
5
10
15
20
25
30
35
40

Bin

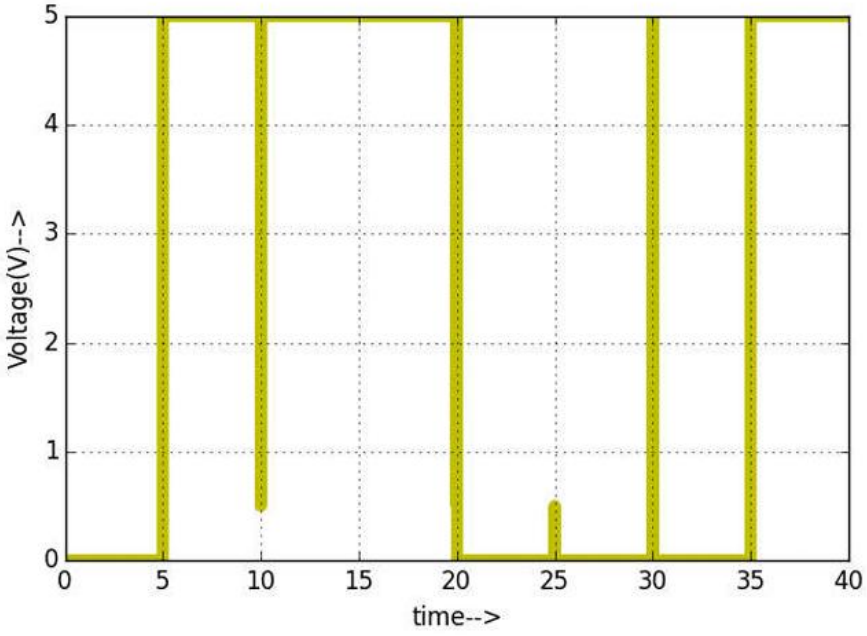

Voltage(V)-->
time-->
0
1
2
3
4
5
0
5
10
15
20
25
30
35
40

Output :

Difference



Borrow



Conclusion : The waveforms successfully generated and we got the simulation result .