

1. What is microprocessor?

It is a program controlled semi conductor device (IC), which fetches, decodes and execute instructions.

2. What are the basic units of microprocessor?

The basic units or blocks of microprocessor are ALU, an array of registers and control unit.

3. What is a bus?

Bus is a group of conducting lines that carries data, address and control signals.

4. Why data bus is bi-directional?

The microprocessor is to fetch (read) the data from memory or input device for processing and after processing it has to store (write) the data to memory or output devices. Hence the data bus is bi-directional.

5. Why address bus is unidirectional?

The address is an identification number used by the microprocessor to identify or access a memory location or input/output device. It is an output signal from the processor. Hence the address bus is unidirectional.

6. Define machine cycle?

Machine cycle is defined as the time required to complete one operation of accessing memory input/output, or acknowledging an external request. This cycle may consists of three to six T-states.

7. Define T-state?

T-state is defined as one subdivision of operation performed in one clock period. These subdivisions are internal states synchronized with the system clock, and each T-state is precisely equal to one clock period.

8. What is an instruction cycle?

The sequence of operations that a processor has to carry out while executing the instruction is called instruction cycle. Each instruction cycle of processor contains a number of machine cycles.

9. What is fetch and execute cycle?

The instruction cycle is divided into fetch and execute cycles. The fetch cycle is executed to fetch the opcode from memory. The execute cycle is executed to decode the instruction and to perform the work instructed by the instruction.

10. List the flags of 8085?

There are five flags in 8085. They are sign flag, zero flag, auxiliary carry flag, parity flag and carry flag.

11. What does memory-mapping mean?

The memory mapping is the process of interfacing memories to microprocessor and allocating addresses to each memory location.

12. What is opcode fetch cycle?

The opcode fetch cycle is a machine cycle executed to fetch the opcode of an instruction stored in memory. Each instruction starts with opcode fetch machine cycle.

13. What are the instructions used to control the interrupts?

- EI
- DI

- RIM
- SIM
-

14. What is polling?

In polling, the microprocessor's software simply checks each of the I/O devices every so often. During this check, the microprocessor tests to see if any device needs servicing.

15. What are the different types of interrupts?

- Hardware
- Software

Hardware interrupts- The interrupts where the CPU pins are used to receive interrupt requests , are called hardware interrupts.

Software interrupts – This interrupt is caused by the execution of the instruction. These are special instructions supported by the microprocessor.

16. What are the types of hardware interrupts?

- ❖ TRAP
- ❖ RST 7.5
- ❖ RST 6.5
- ❖ RST 5.5
- ❖ INTR

17. Difference between memory mapped I/o and I/O mapped I/o?

Memory mapped I/O	I/O mapped I/O
1. In this device address is 16- bit. Thus Ao to A15 lines are used to generate the device address	1. In this device address is 8-bit. Thus Ao to A7 or A8 to A15 lines are used to generate device address.

2. MEMR and MEMW control signals are used to control read and write I/O operations.	2. IOR and IOW control signals are used to control read and write I/O operations.
3. Instructions available are LDA,STA,MOV R,M , ADD M etc	3. Instructions available are IN and OUT.
4. Data transfer is between any register and I/O device.	4. Data transfer is between accumulator and I/O device.
5. Decoding 16-bit address may require more hardware.	5. Decoding 8-bit address will require less hardware.

18. Describe the function of the following pins in 8085?

a) READY b) ALE c) IO/M d) HOLD e)SID and SOD

READY – It is used by the microprocessor to sense whether a peripheral is ready or not for data transfer. If not, the processor waits. It is thus used to synchronize slower peripherals to the microprocessor.

ALE – In 8085 , A₀ to A₇ lines are multiplexed and lower half of address (A₀ to A₇) is available only during T₁ of the machine cycle. The latching of lower half address from the multiplexed address lines by using ALE signal.

IO/M - indicates whether I/O operation or memory operation is being carried out.

HOLD – This signal indicates that another master is requesting for the use of address bus, data bus and control bus.

SID(Serial Input Data) – This input signal is used to accept serial data bit by bit from the external device.

SOD(Serial Output Data) – This is an output signal which enables the transmission of serial data bit by bit to the external device.

Timing Diagram

Instruction	No. of m/c cycles	No. of T-states	Name of cycles
1. MVI A, 8-bit	2	7	Opcode Fetch, Memory Read
2. STA address	4	13	Opcode fetch,MR,MR,MW
3. LXI rp,data(16)	3	10	OF,MR,MR
4. LHLD 16-bit	5	16	OF,MR,MR,MW,MW
5. MVI M,data(8)	3	10	OF,MR,MW
6. CMP reg(8)	1	4	OF
7. ADD reg(8)	1	4	OF
8. CMA	1	4	OF
9. CMC	1	4	OF
10. ADD M	2	7	OF,MR
11. CMP M	2	7	OF,MR
12. LDA address	4	13	Of,MR,MR,MR
13. DAD rp	3	10	OF,Bus Idle,Bus Idle
14. INR M	3	10	OF,MR,MW
15. XTHL	5	16	OF,MR,MR,MW,MW
16. JMP address3	3	10	OF,MR,MR
17. J condition	2	7	OF,MR
18. PUSH rp	3	10	OF,MW,MW
19. POP rp	3	10	OF,MR,MR
20. CALL address	5	18	OF,MR,MR,MW,MW
21. RET	3	10	OF,MR,MR
22. RST	3	12	OF,Mw,MW
23. MOV r,M	2	7	OF,MR
24. MOV M,r	2	7	OF,MW
25. IN address	3	10	OF,MR,I/O Read
26. OUT address	3	10	OF,MR,I/O Write

19. Comparison between full address decoding and partial address decoding?

Full Address Decoding	Partial Address decoding
1. All higher address lines are decoded to select the memory or I/O device.	1. Few higher address lines are decoded to select the memory or I/O device.
2. More hardware is required to design decoding logic.	2. Hardware required to design decoding logic is less and sometimes it can be eliminated.
3. Higher cost for decoding circuit.	3. Less cost for decoding circuit.
4. No Multiple addresses.	4. It has a advantage of multiple addresses.
5. Used in large systems	5. Used in small systems

20. What is ALE?

The ALE (Address latch enable) is a signal used to demultiplex the address and data lines using an external latch. It is used to enable the external latch.

21. Where is the READY signal used?

READY is an input signal to the processor, used by the memory or input/output devices to get extra time for data transfer or to introduce wait states in the bus cycles.

22. Give some examples of port devices used in 8085 microprocessor based system?

The various port devices used in 8085 are
8212,8155,8156,8255,8355,8755.

23. What is the need for timing diagram?

The timing diagram provides information regarding the status of various signals, when a machine cycle is executed. The knowledge of timing diagram is essential for system designer to select matched peripheral devices like memories, latches, ports etc from a microprocessor system.

24. What operation is performed during first T-state of every machine cycle in 8085?

In 8085, during the first T-state of every machine cycle the low byte address is latched into an external latch using ALE signal.

25. What is interrupt acknowledge cycle?

The interrupt acknowledge cycle is a machine cycle executed by 8085 processor to get the address of the interrupt service routine in order to service the interrupt device.

26. What is vectored and non-vectored interrupt?

When an interrupt is accepted, if the processor control branches to a specific address defined by the manufacturer then the interrupt is called vectored interrupt. In Non-vectored interrupt there is no specific address for storing the interrupt service routine. Hence the interrupted device should give the address of the interrupt service routine.

27. List the software and hardware interrupts of 8085?

Software interrupts : RST 0,RST 1,RST 2,RST 3,RST 4,RST 5,RST 6,RST 7

Hardware interrupts : TRAP,RST 7.5,RST 6.5,RST 5.5, INTR.

28. What is TRAP?

The TRAP is a non-maskable interrupt of 8085. It is not disabled by processor reset or after recognition of interrupt.

29. How clock signals are generated in 8085 and what is the frequency of the internal clock?

The 8085 has the clock generation circuit on the chip but an external quartz crystal or LC circuit or RC circuit should be connected at the pins X1 and X2. The maximum internal clock frequency of 8085 is 3.03MHz.

30. Define stack?

Stack is a sequence of RAM memory locations defined by the programmer.

31. What is program counter? How it is useful in program execution?

The program counter keeps track of program execution. To execute a program the starting address of the program is loaded in program counter. The PC sends out an address to fetch a byte of instruction from memory and increments its content automatically.

32. Define opcode and operand?

Opcode(operation code) is the part of an instruction that identifies a specific operation. Operand is a part of instruction that represents a value on which the instruction acts.

33. How the 8085 processor differentiates a memory access and I/O access?

The memory access and I/O access is differentiated using IO/\overline{M} signal. The 8085 processor asserts IO/\overline{M} low for memory operation and high for I/O operations.

34. When the 8085 processor checks for an interrupt?

In the second T-state of the last machine cycle of every instruction, the 8085 processor checks whether an interrupt request is made or not.

35. Why interfacing is needed for I/O devices?

Generally I/O devices are slow devices. Therefore the speed of I/O devices does not match with the speed of microprocessor. And so an interface is provided between system bus and I/O devices.

36. What is interrupt I/O?

If the I/O device initiate the data transfer through interrupt then the I/O is called interrupt driven I/O.

37. What is a port?

The port is a buffered I/O, which is used to hold the data transmitted from the microprocessor to I/O devices and vice versa.

38. What is the need for interrupt controller?

The interrupt controller is employed to expand the interrupt inputs. It can handle the interrupt request from various devices and allow one by one to the processor.

39. What is synchronous data transfer scheme?

For synchronous data transfer scheme, the processor does not check the readiness of the device after a command have been issued for read/write operation. For this scheme the processor will request the device to get ready and then read/write to the device immediately after the request.

40. What is asynchronous data transfer scheme?

In asynchronous data transfer scheme, first the processor sends a request to the device for read/write operation. Then the processor keeps on polling the status of the device. Once the device is ready, the processor executes a data transfer instruction to complete the process.

41. What are the internal devices of 8255?

The internal devices of 8255 are port-A, port-B, port-C. The ports can be programmed for either input or output function in different operating modes.

42. What is USART?

The device which can be programmed to perform Synchronous or Asynchronous serial communication is called USART (Universal Synchronous Asynchronous Receiver Transmitter). Eg: INTEL 8251

43. What is scanning in keyboard and what is scan time?

The process of sending a zero to each row of a keyboard matrix and reading the columns for key actuation is called scanning. The scan time is the time taken by the processor to scan all the rows one by one starting from first row and coming back to the first row again.

44. What is programmable peripheral device?

If the function performed by the peripheral device can be altered or changed by a program instruction then the peripheral device is called programmable device. It has control register. The device can be programmed by sending control word in the prescribed format to the control register.

45. What is baud rate?

The baud rate is the rate at which the serial data are transmitted. Baud rate is defined as (The time for a bit cell). In some systems one bit cell has one data bit, then the baud rate and bits/sec are same.

46. What are the tasks involved in keyboard interface?

The tasks involved in keyboard interfacing are sensing a key actuation, Debouncing the key and generating key codes(Decoding the key). These tasks are performed software if the keyboard is interfaced through ports and they are performed by hardware if the keyboard is interfaces through 8279.

47. How a keyboard matrix is formed in keyboard interface using 8279?

The return lines, RL0 to RL7 of 8279 are used to form the columns of keyboard matrix. In decoded scan lines SL0 to SL3 of 8279 are used to form the rows of keyboard matrix. In encoded scan mode, the output lines of external decoder are used as rows of keyboard matrix.

48. What is GPIB?

GPIB is the General Purpose interface Bus. It is used to interface the test instruments to the system controller.

49. Advantages of differential data transfer?

1. Communication at high data rate in real world environment.
2. Differential data transmission offers superior performance.
3. Differential signals can help induced noise signals.

50. Features of INTEL 8259?

1. It manage 8 interrupt request.
2. The interrupt vector addresses are programmable.
3. The priorities of interrupts are programmable.
4. The interrupt can be masked or unmasked individually.

51. What is meant by micro controller?

A device which contains the microprocessor with integrated peripherals like memory, serial ports, parallel ports, timer/counter, interrupt controller, data acquisition interfaces like ADC, DAC is called micro controller.

52. List the features of 8051 micro controllers?

- Single supply +5v operation using HMOS technology.
- 4096 bytes program memory on-chip.
- 128 data memory on chip.
- 4 register banks
- 2 multiple modes, 16 bit timer/counter
- Extensive Boolean processing capabilities.
- 64KB external RAM size.
- 32 bi-directional I/O lines.
-

53. Explain the operating mode 0 of 8051 serial port?

In this mode serial data enters and exists through RXD, TXD outputs the shift clock. 8-bits are transmitted or received:8-data bits(LSB first). The baud rate is fixed at 1/12 the oscillator frequency.

54. Explain the operating mode 2 of 8051 serial port?

In this mode 11 bits are transmitted (through TXD) or received (through RXD): a start bit(0), 8 data bits(LSB first), a programmable 9th data bit and a stop bit(1).

On transmit, the 9th data bit can be assigned the value 0 or 1. On receive, the 9th data bit go into the RB8 in special function register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

55. Explain the mode 3 of 8051 serial port?

In this mode, 11 bits are transmitted (through TXD) or (received (through RXD): a start bit(0), 8 data bits(LSB first), a programmable 9th data bit and a stop bit(1).It is same as mode 2 except the baud rate. The baud rate in mode 3 is variable.

56. Explain the interrupts of 8051 micro controller?

- External interrupt 0 (IE0) – Highest priority
- Timer interrupt 0 (TF0)
- External interrupt 1 (IE1)
- Timer interrupt 1 (TF1)
- Serial port Interrupt
 - Receive interrupt (RI) | - lowest priority
 - Transmit interrupt (TI)

57. How many bytes of internal RAM and ROM supported by 8051 micro controller?

128 bytes of internal RAM and 4 bytes of ROM.

58. Define machine cycle of 8051?

8051 machine cycle consists of 6 states, S1 through S7. One state is made up of 2 clock pulses. Thus 12 clock period constitute one machine cycle. Two clock periods in a state is termed as phase 1 and phase 2.

59. What are the special function of port 0 of 8051?

Port 0 is used as a multiplexed low order address/data bus during the external memory access. When ALE is enabled, the address on port 0 pins are latched and bus is ready to act as a data bus when ALE is low.

60. What are the alternative function of port 3 of 8051?

Serial data input (P3.0), serial data output (P3.1), external interrupt 0 (P3.2), external interrupt 1 (P3.3), external input for timer 0(P3.4), external input for timer 1 (P3.5), external memory write pulse (P3.6), external memory read (P3.7) are the alternative functions of port 3.

61. What are the use of scratch pad area of internal RAM of 8051?

In internal RAM 80 bytes constitutes the scratch pad area. The scratch pad bytes can be programmed as a general purpose registers.

62. What are the flags supported by 8051 controller?

- Carry flag
- Auxiliary carry flag
- Over flow flag
- General purpose user flag
- Register bank select bit one
- Register bank select bit zero
- Parity flag

63. What is meant by Power-on- Reset in 8051 controller?

When RESET pin is activated, the 8051 jumps to address location 0000H. This is called as Power-on-Reset. Reset pin is considered as a sixth interrupt source of 8051.

64. What are the significance of SFRs?

SFRs denotes Special function Registers of 8051 controller. All the controller registers such as port latches, timer register, peripheral control register, accumulator, PC and DPTR all are available in SFR region.

65. What are the different group of instructions supported by 8051?

- Data Transfer Group
- Arithmetic Group
- Logical Group
- Branching Group
- Bit manipulation Group

66. Write a program to mask the 0th and 7th bit using 8051?

```
MOV A,#data
ANL A,#81
MOV DPTR,#4500
MOVX @DPTR,A
LOOP: SJMP LOOP
```

67. List the addressing modes of 8051?

- Direct addressing
- Register addressing
- Register indirect addressing
- Implicit addressing
- Immediate addressing
- Index addressing
- Bit addressing

68. Write about CALL statement in 8051?

There are two CALL instructions. They are

- LCALL(Long call)
- ACALL(Absolute call)

69. Write about the jump statement?

There are three forms of jump. They are

- ❖ LJMP (Long jump) – 16 bit address
- ❖ AJMP(Absolute jump) – 11 bit address
- ❖ SJMP (Short jump) – relative address

70. Write a program to find the 2's complement using 8051?

```
MOV A, R0
CPL A
INC A
```

71. Write a program to swap two numbers using 8051?

```
MOV A,# data
SWAP A
```

72. Write a program to subtract two numbers & exchange the digits using 8051?

```
MOV A,#9F
MOV R0,#40
SUBB A,R0
SWAP A
```

73. What are the different types of Address decoding Techniques?

Absolute decoding/Full decoding
Linear decoding/Partial decoding

74. Comparison between full address decoding and Partial address decoding?

Full address decoding	Partial address decoding
1. All higher address lines are decoded to select the memory or I/O device.	1. Few higher address lines are decoded to select the memory or I/O device.
2. More hardware is required to design decoding logic.	2. Hardware required to design decoding logic is less and sometimes it can be

	eliminated.
3. Higher cost for decoding circuit.	3. Less cost for decoding circuit.
4. No multiple addresses.	4. It has a disadvantage of multiple addresses. (Shadow addresses)
5. Used in large systems.	5. Used in small systems.

75. What is the significance of wait state generator?

This is used to transfer data between slower I/O device and the microprocessor. In some applns, the speed of I/O systems is not compatible with the microprocessor's timings. So the microprocessor has to confirm whether the peripheral is ready or not. If READY pin is high, the peripheral is ready otherwise 8085 enters in to wait state.

76. What is a Non-maskable interrupt?

It is unaffected by any mask or interrupt enable. Eg: TRAP

77. What is a Data pointer register?

The data pointer register (DPTR) consists of a high byte(DPH) and a low byte (DPL) functions to hold 16 bit address. It may be manipulated as a 16-bit data register or as independent 8-bit registers. It serves as a base register in indirect jumps, look up table instructions and external data transfer.

78. What are the operating modes of 8279?

1. Input modes

- Scanned keyboard
- Scanned sensor matrix
- Strobed input

2. Display modes

- Left entry (Type writer mode)
- Right entry (Calculator mode)

79. What are the different functional units in 8279?

CPU interface section

Keyboard section

Display section

Scan section

80. What are the priority modes in 8259?

- a. Fully nested mode
- b. Special fully nested mode
- c. Rotating Priority mode
- d. Special Masked mode
- e. Polled mode

81. What is IMR(Interrupt mask register)?

IMR stores the masking bits of the interrupt lines to be masked. This register can be programmed by an operation command word (OCW).

82. What is priority resolver?

It determines the priorities of the bits set in the Interrupt request register (IRR). The bit corresponding to the highest priority interrupt input is set in the ISR during INTA input.

83. What is the use of IRR?

The interrupt request register is used to store all the interrupt levels which are requesting the service. The eight interrupt inputs sets corresponding bits of the Interrupt Request Register upon the service request.

84. What is Interrupt service register(ISR)?

The interrupt service register stores all the levels that are currently being serviced.

85. What is the difference between SHLD and LHLD?

SHLD- Store HL register pair in memory.

This instruction is used to store the contents of H and L register directly in to memory.

LHLD- Load HL register pair from memory.

This instruction copies the contents of memory location given with in the instruction in to the L register and the contents of next memory location in to the H register.

86. What is the difference between STAX and LDAX?

STAX rp – Store the contents of Accumulator register (A) in memory location whose address is specified by BC or DE register pair.

LDAX rp – Load Accumulator register (A) with the contents of memory location whose address is specified by BC or DE register pair.

87. Write an assembly language program to transfer data from memory block B1 to memory block B2?

```
                MVI C,0AH; Initialize counter
                LXI H, 2200H; Initialize source memory pointer
                LXI D, 2300H; Initialize destination memory pointer
Loop:           MOV A,M; Get byte from source memory block
                STAX D; Store byte in the destination memory block
                INX H; Increment source memory pointer
                INX D; Increment destination memory pointer
                DCR C; Decrement counter
                JNZ Loop ; If counter ≠ 0 repeat
                HLT
```

88. What are the types of branching instructions?

1. Jump instructions
2. Call and Return instructions

3. Restart instructions

89. Write an assembly language program to add 2 BCD numbers?

```
LXI H,2200H; Initialize pointer
MOV A,M ; Get the first number
INX H; Increment the pointer
ADD M ; Add two numbers
DAA ; Convert HEX to valid BCD
STA 2300; store the result
HLT
```

90. Explain the instruction LXI rp,data (16)?

LXI rp, data(16) – Load 16 –bit immediate data to specified register pair or stack pointer. The rp is 16 – bit register pairs such as BC, DE, HL or stack pointer.

91. Write the difference between LDA and STA instruction?

LDA – Load data in to Accumulator register(A) directly from the address specified with in the instruction.

STA – Store the contents of Accumulator register(A) to the address specified with in the instruction.

92. What are the types of rotate instructions?

```
RLC – Rotate Accumulator Left
RRC- Rotate Accumulator Right
RAL – Rotate Accumulator Left through Carry
RAR - Rotate Accumulator Right through Carry
```

93. What are the operating modes of 8255?

1. Bit set/Reset mode
2. I/O modes
 - a)mode 0 : Simple input/output
 - b)mode 1 : Input/output with handshake

c)mode 2 : Bi-directional I/O data transfer

94. What are the priority modes in 8259?

1. Fully nested mode
2. Special fully nested mode
3. Rotating priority mode
4. Special mask mode
5. Poll mode

95. What is the use of SWAP function in 8051?

SWAP A : Swap nibbles with in the Accumulator bytes.

It interchanges the low and high order nibbles of the Accumulator (bits 0-3 and bits 4-7)

96. What is SCON?

SCON is the serial port control register , which contains not only the mode selection bits (SM0 – SM2 ,REN), but also the 9th data bit for transmit and receive (TB8 and RB8) and the serial port interrupt bits (TI and RI).

SM0 – Serial port mode control bit 0

SM1 – Serial port mode control bit 1

SM2 – Serial port mode control bit 2

REN – Receiver enable control bit

TB8 – Transmit bit 8

RB8 – Receive bit 8

TI – Transmit Interrupt flag

RI – Receive interrupt flag

97. How we calculate the Baud rate for serial port in mode 0?

Baud Rate = Oscillator frequency/12

98. What is the significance of TXD and RXD pins in 8051?

TXD – Transmit data pin for serial port in UART mode. Clock output in shift register mode.

RXD – Receive data pin for serial port in UART mode. Data I/O pin in shift register mode.

99. Write two examples of Register indirect Addressing modes in 8051?

MOV A,@R0 ; Load the contents pointed by R0 in A.

ADD A,@R1 ; Add the contents of A and the contents pointed by R1.

100. What is Accumulator Register?

It is an 8 – bit register. It holds a source operand and receives the result of the arithmetic instructions (Addition, Subtraction, Multiplication and Division)

16 - Marks Questions

1. With Neat diagram, explain the Architecture of 8085?

- Block diagram
- Explanation

2. Explain the instruction sets of 8085?

- Data transfer instructions
- Arithmetic instructions
- Logical instructions
- Branching instructions
- Machine control instructions

3. Explain the interrupt structure of 8085?

- TRAP
- RST 7.5
- RST 6.5
- RST 5.5

- INTR

4. Draw the timing diagram of STA address?

4 machine cycles.

- Opcode Fetch
- Memory Read
- Memory Read
- Memory Write

5. Explain about Memory interfacing?

- Explanation

6. Write the Assembly language program to sort a set of numbers in Ascending order?

- ❖ Program
- ❖ Output

7. Write an Assembly language program to find the largest number in an array?

- ❖ Program
- ❖ Output

8. With neat block diagram, explain the Architecture of 8279?

- Block diagram
- Explanation

9. Write an Assembly language program to add two BCD numbers?

- Program
- Output

10. With neat block diagram, explain the Architecture of PPI?

- Block diagram
- Explanation

11. With neat block diagram, explain the Architecture of 8253?

❖ Block diagram

❖ Explanation

12. With neat block diagram, explain the Architecture of USART?

➤ Block diagram

➤ Explanation

13. Explain the operating modes of 8279?

Input modes

- Scanned keyboard
- Scanned sensor matrix
- Strobed input

Display modes

- Left entry (Type writer mode)
- Right entry (Calculator mode)

14. Explain the operating modes of 8255?

Bit set/Reset mode

I/O modes

- a) mode 0 : Simple input/output
- b) mode 1 : Input/output with handshake
- c) mode 2 : Bi-directional I/O data transfer

15. Explain the operating modes of PPI?

16. Explain the operating modes of USART?

17. Explain the operating modes of 8259?

- Fully nested mode
- Special fully nested mode
- Rotating priority mode

- Special mask mode
- Poll mode

18. Explain the Architecture of 8259?

- Block diagram
- Explanation

19. Explain the instruction sets of 8051?

- ❖ Types
- ❖ Explanation

20. Explain the interrupt structure of 8051?

- ❖ Types
- ❖ Explanation

21. How 8279 is interfaced with 8085?

- Diagram
- Explanation

22. How stepper motor is interfaced with 8085?

- Diagram
- Explanation

23. Explain about Servo motor interfacing?

24. Explain the Addressing modes of 8051?

- Direct addressing
- Register addressing
- Register indirect addressing
- Implicit addressing
- Immediate addressing
- Index addressing

- Bit addressing

25. Explain the Addressing modes of 8085?

- Direct addressing
- Register addressing
- Register indirect addressing
- Immediate addressing
- Implied Addressing

26. Write an Assembly language program to generate square wave using Digital to Analog interface?

- Program
- Output

27. Compare A/D and D/A interfacing?

28. Explain the Serial communication in 8051?

29. Explain the Architecture of 8051?

- Block diagram
- Explanation

30. Write an Assembly language program to add two 16-bit numbers using 8051?

- Program
- Output