

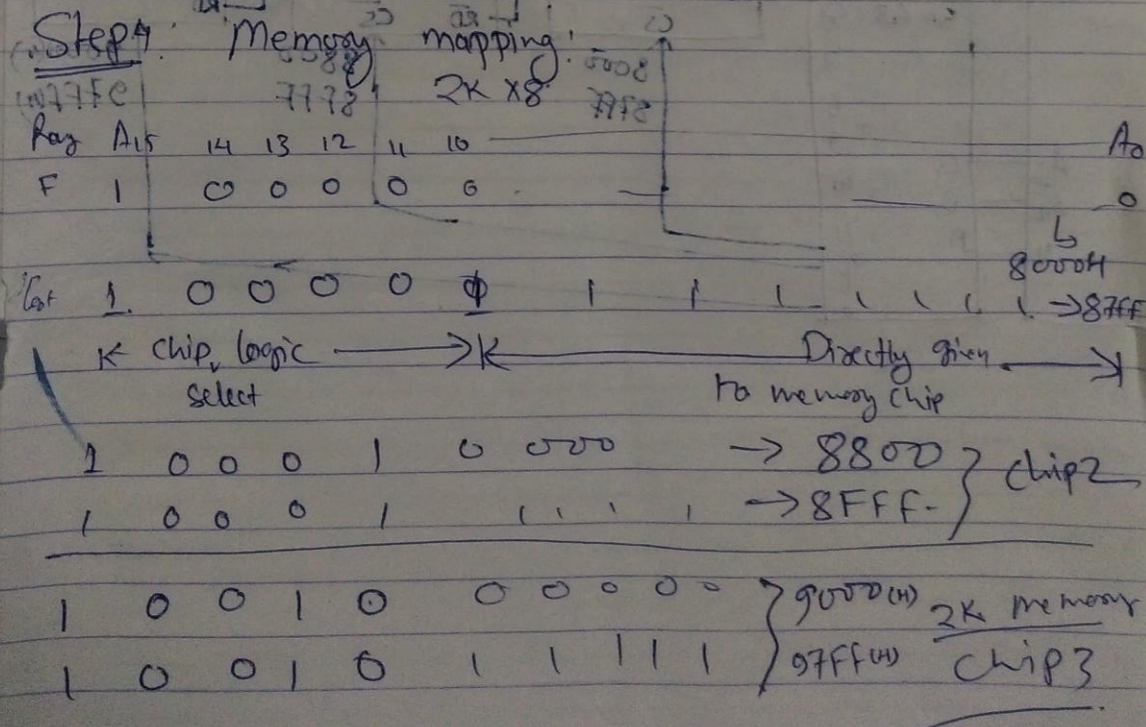
Design and interface. 6K x 8 memory to 8085 using 2K x 8 memory chips. Select starting address 8000H. Give the address range of each chip used.

Solⁿ.

Step 1: The 6K x 8 memory is to be built using 2K x 8
 → no. issues with data lines of 8 is for 6K x 8.
 $6K = 2K + 2K + 2K$.

Step 2: The address lines required for 2K chip are 11
 So A₀ to A₁₀ should be directly connected to up address bus

Step 3: Remaining lines A₁₁ to A₁₅ will be used to generate chip select signal for all 3 - 2K chips are used.



Bit Pattern:

A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	Chip Select
1	0	0	0	0	2K x 8 1 st
1	0	0	0	1	2K x 8 2 nd
1	0	0	1	0	2K x 8 3 rd

