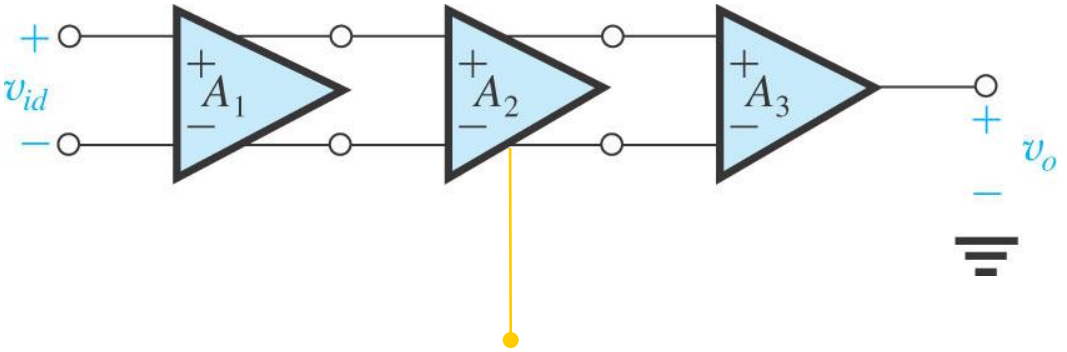
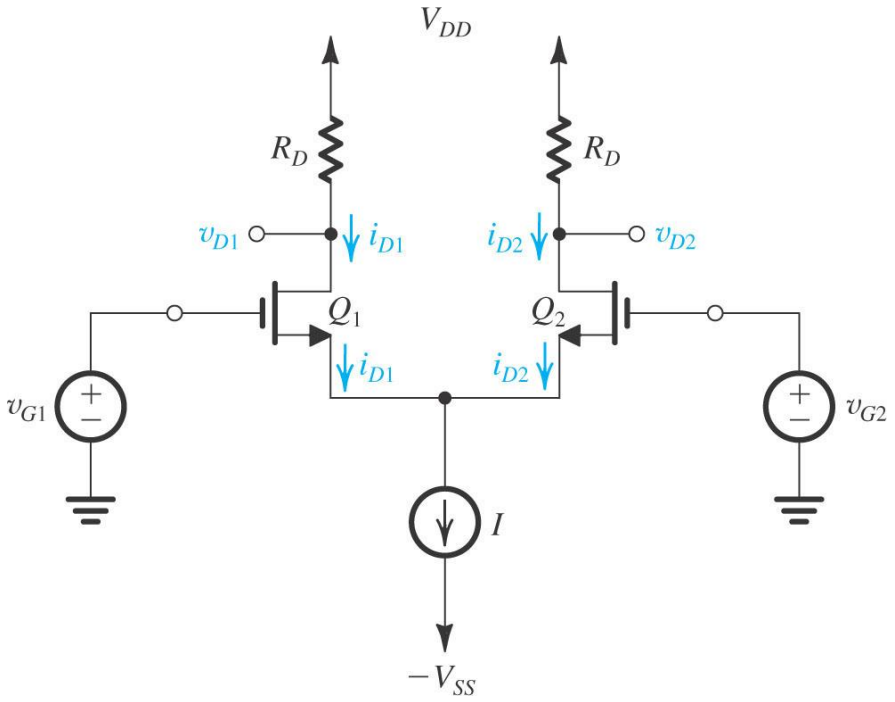
Chapter 8

Differential and Multistage Amplifiers

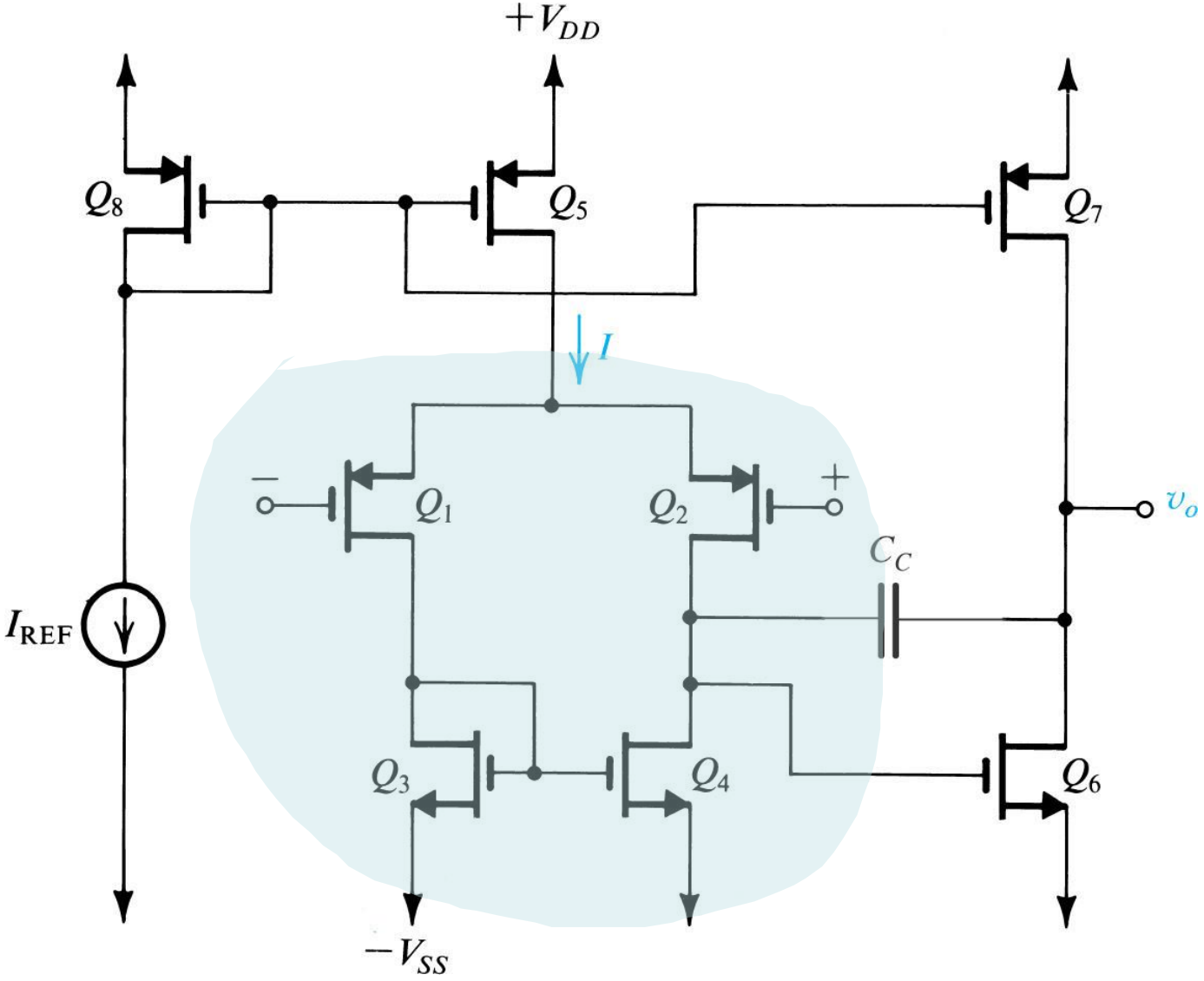




PART A: MOS Diff Pair with Passive Load

Active-Loaded Differential Pair

Two Stage Op Amp (MOSFET)



Learning Objectives

1) **MOS and the BJT differential amplifiers**: how they reject common-mode noise or interference and amplify differential signals

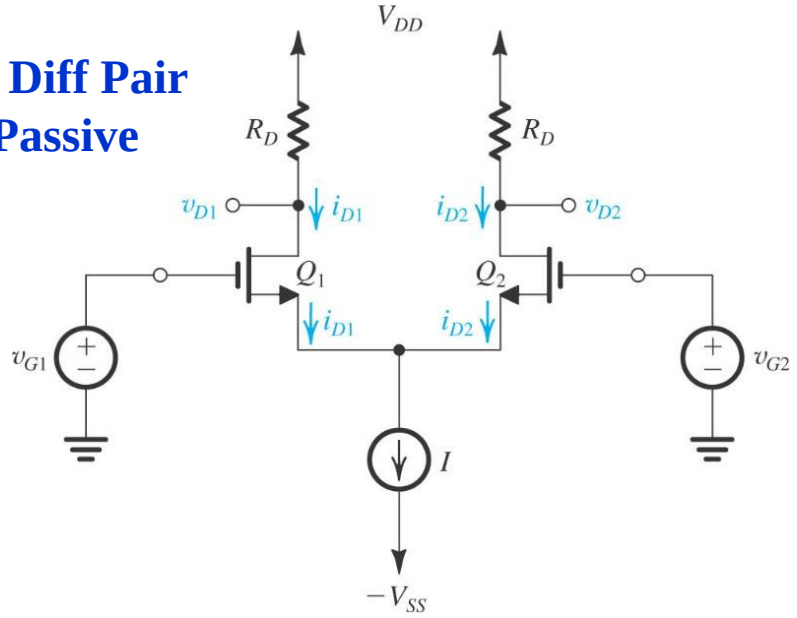
2) The analysis and design of MOS and BJT differential amplifiers: utilizing passive (resistive) loads and active (current-source) loads

3) The structure, analysis, and design of amplifiers composed of two or more stages in cascade

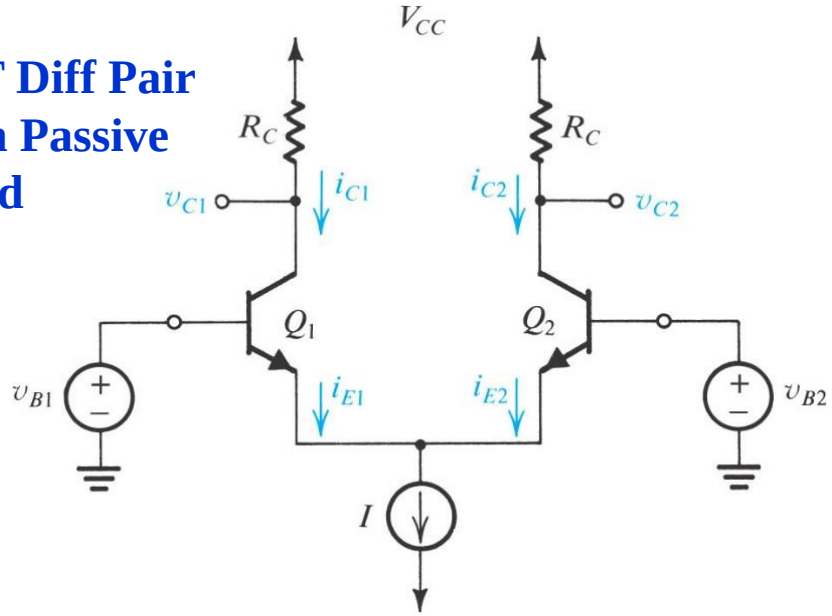
Why Differential?

- What is a **Differential Signal**?
- Differential circuits are less sensitive to noise and interference
- Differential configuration enables biasing the amplifier and coupling of amplifier stages without bypass and coupling capacitors
- Useful in IC design because of good matching between the transistors

MOS Diff Pair with Passive Load



BJT Diff Pair with Passive Load



MOS Differential Pair

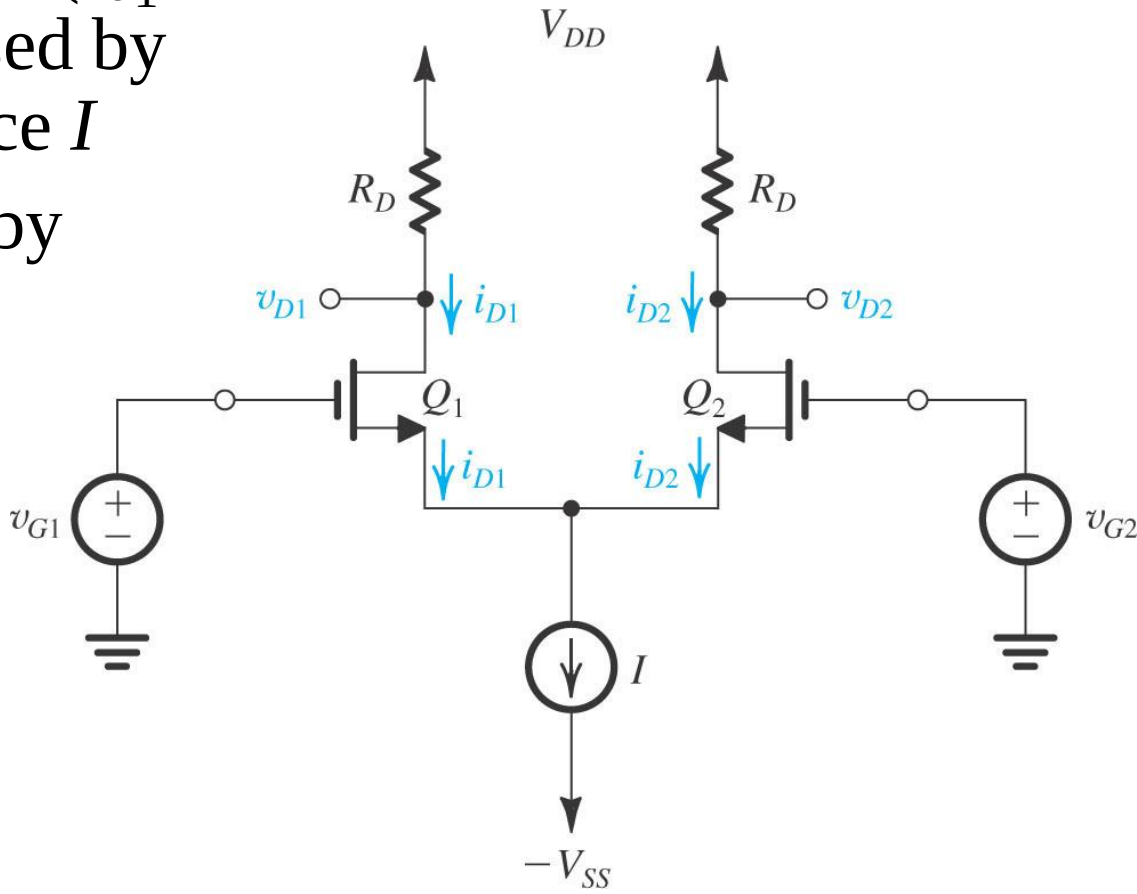
8.1. The MOS Differential Pair

MOS Differential Pair

- Two matched transistors (Q_1 and Q_2) joined and biased by a constant current source I which is implemented by current mirror

- Q_1 and Q_2 must stay in saturation

- How does the diff. pair work?



Important Parameters and Characteristics

1) Input Common-mode Range

2) Differential Input Voltage

3) Large Signal Operation

4) Small Signal Operation

5) Common-mode Rejection Ratio (CMRR)

6) Input Offset Voltage

Input Common-Mode Range

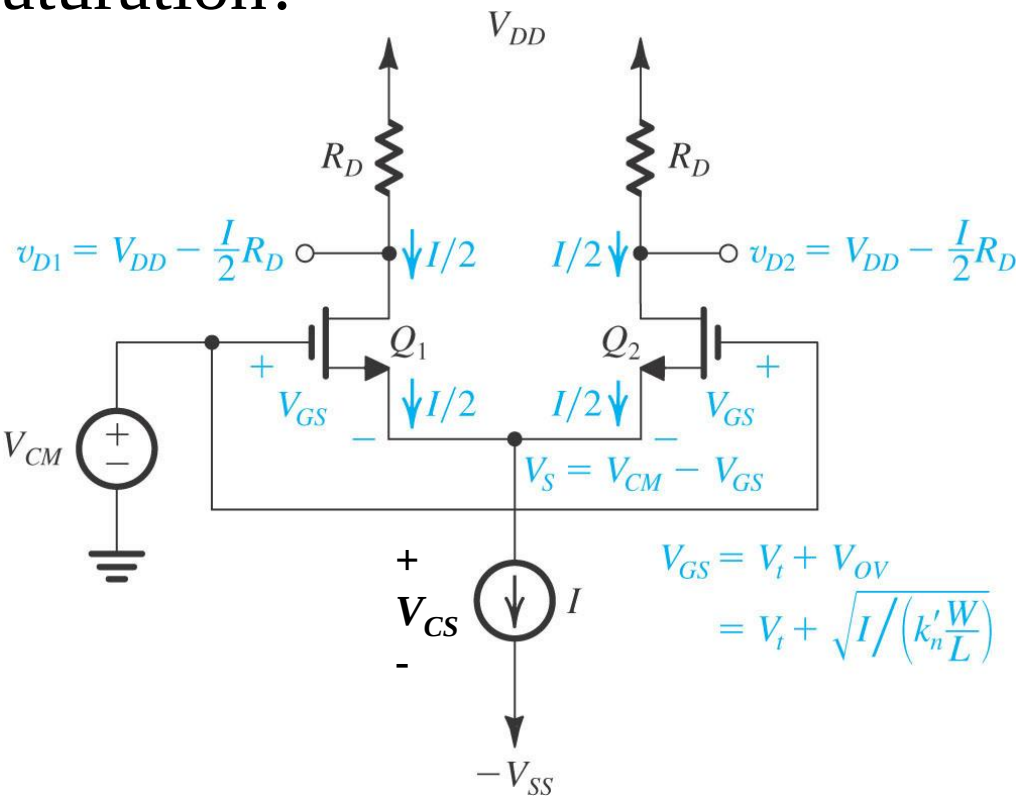
DC Common-mode voltage (V_{CM})

- What is the range of input voltage within which the transistors will stay in saturation?

- $V_{CM\_max} = V_{tn} + \underbrace{V_{DD} - 0.5IR_D}_{V_D}$

- $V_{CM\_min} = -V_{ss} + V_{cs} + \underbrace{V_{tn} + V_{ov}}_{V_{GS}}$

Min voltage need to keep the current mirror in saturation



Differential Input Voltage

Differential Input Voltage (V_{id})

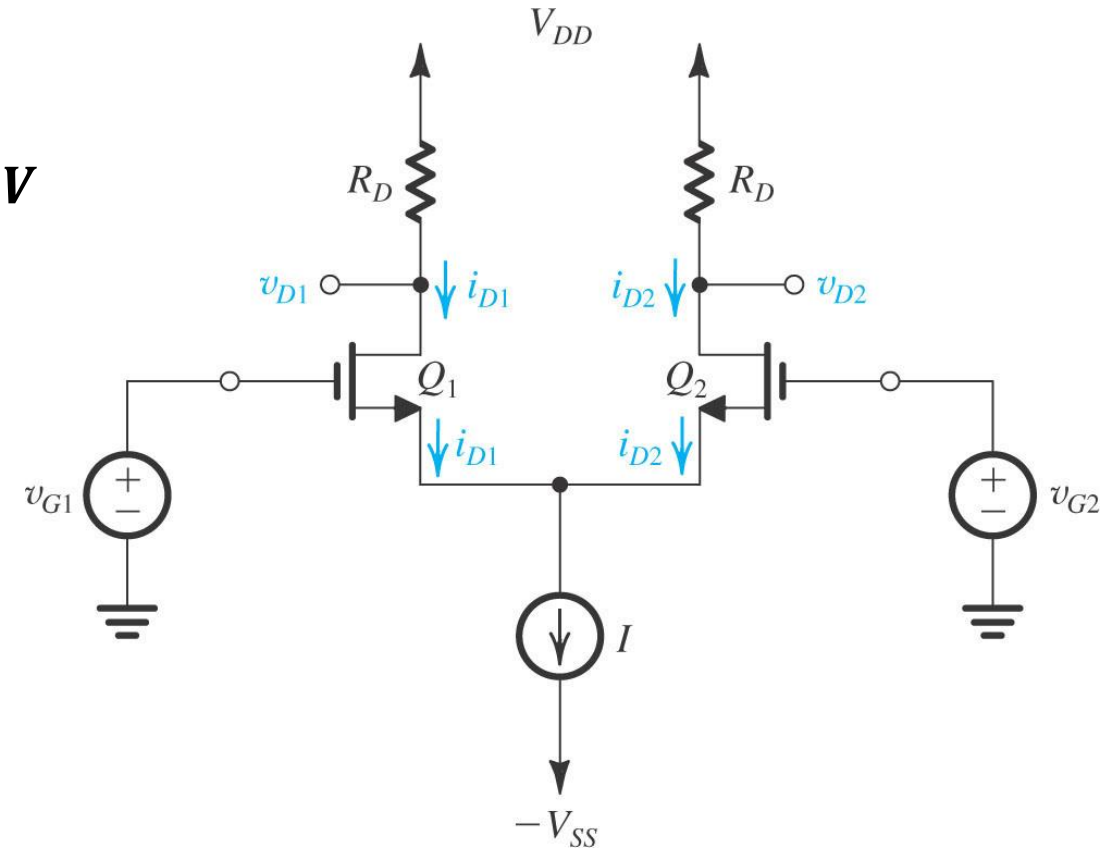
- Both Q_1 and Q_2 in saturation

- $V_{id} = V_{GS1} - V_{GS2}$

$$-\sqrt{2}V_{OV} < V_{id} < \sqrt{2}V_{OV}$$

$i_{D2}=I$, Q1 is off

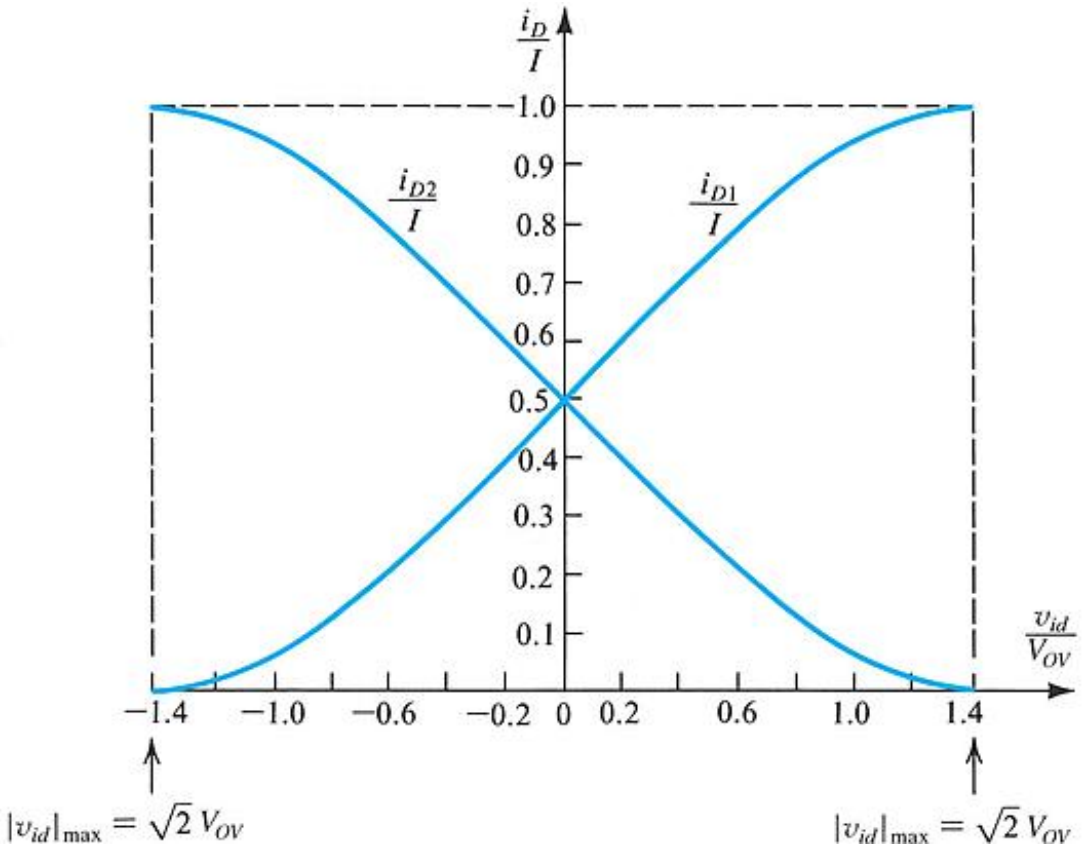
$i_{D1}=I$, Q2 is off



Large Signal Operation

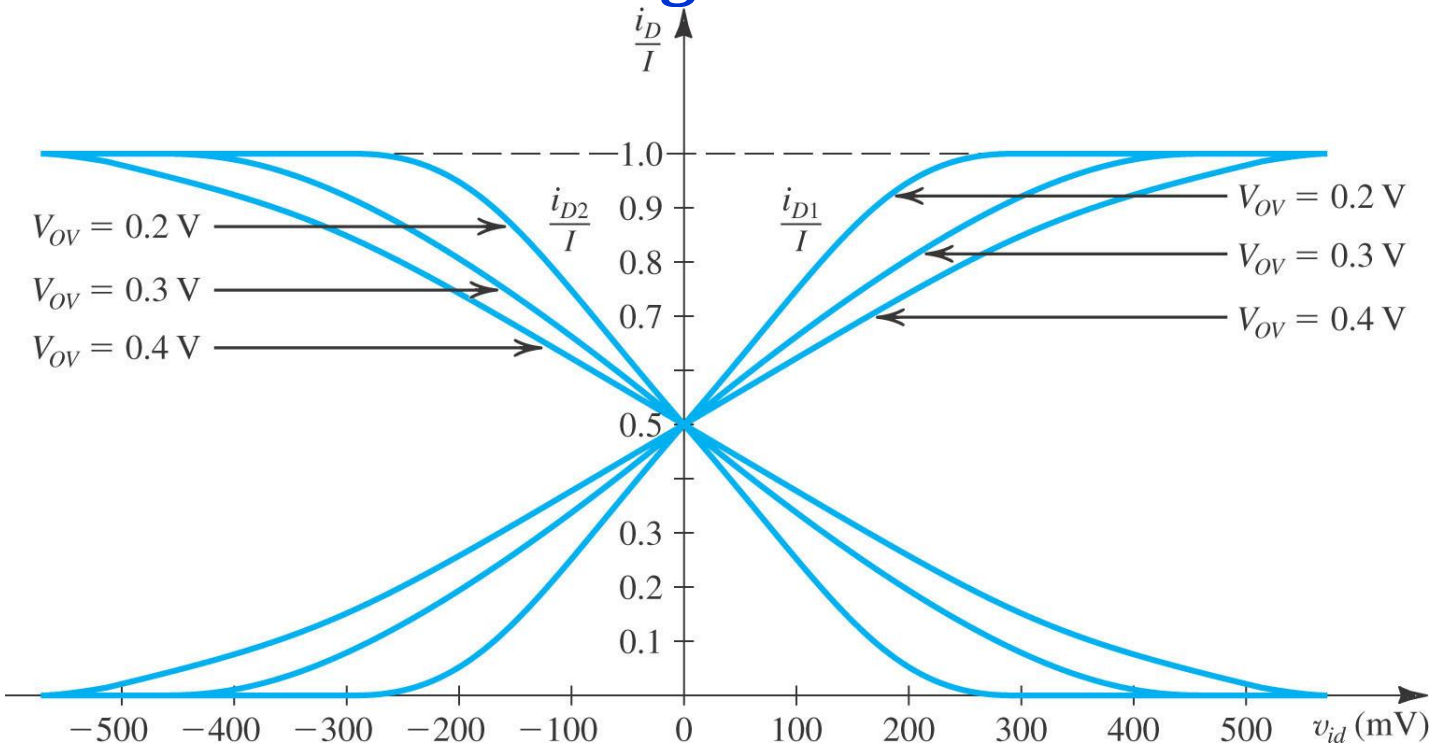
Current Steering

- Where should we operate the diff pair?
- $i_{D1} = \frac{I}{2} + \left(\frac{I}{V_{ov}}\right)\left(\frac{V_{id}}{2}\right)$
- $i_{D2} = \frac{I}{2} - \left(\frac{I}{V_{ov}}\right)\left(\frac{V_{id}}{2}\right)$



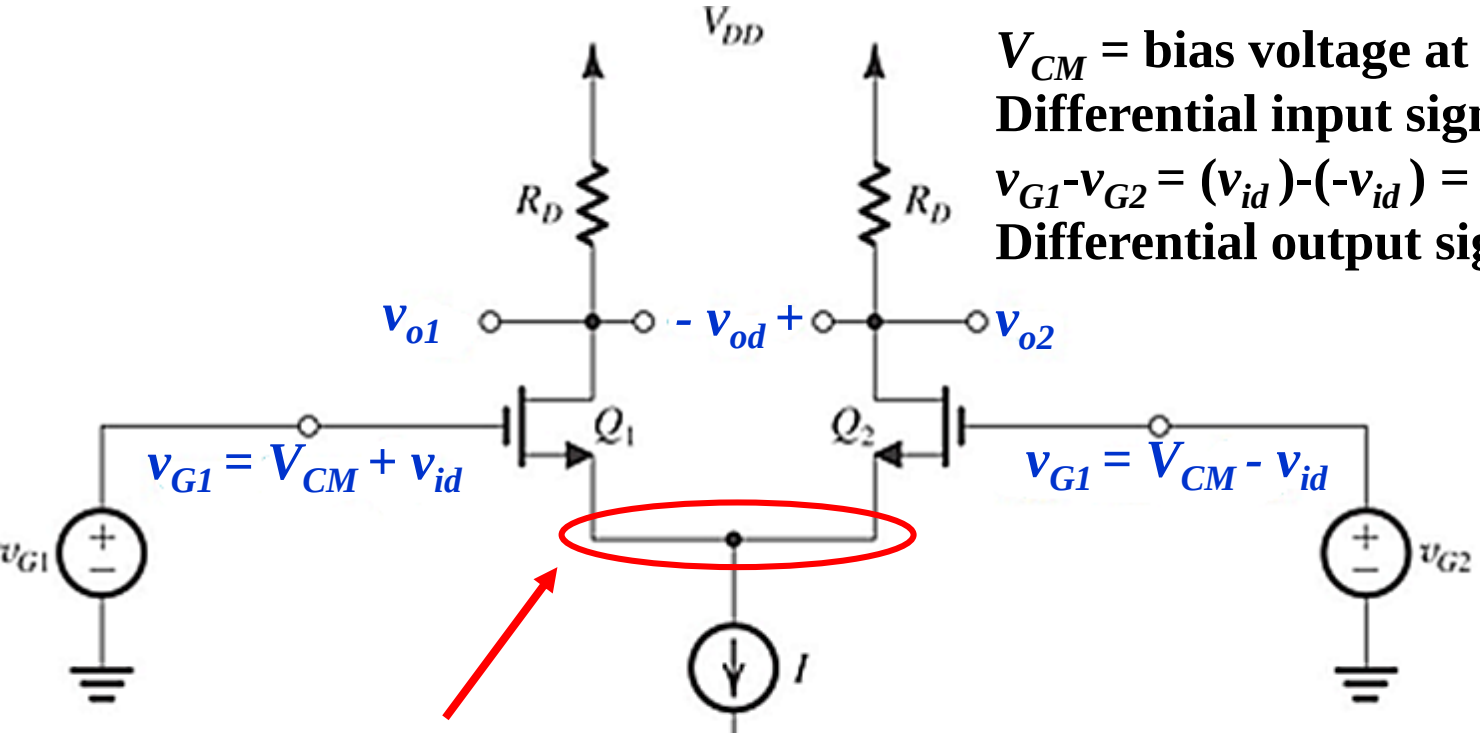
Large Signal Operation

How to increase linear range?



- V_{OV} increases: Gain will decrease, Linearity will increase
- V_{OV} decreases: Gain will increase, Linearity will decrease
- Can increase the bias current to increase g_m and gain

Small-Signal Operation



V_{CM} = bias voltage at the gate or noise

Differential input signal =

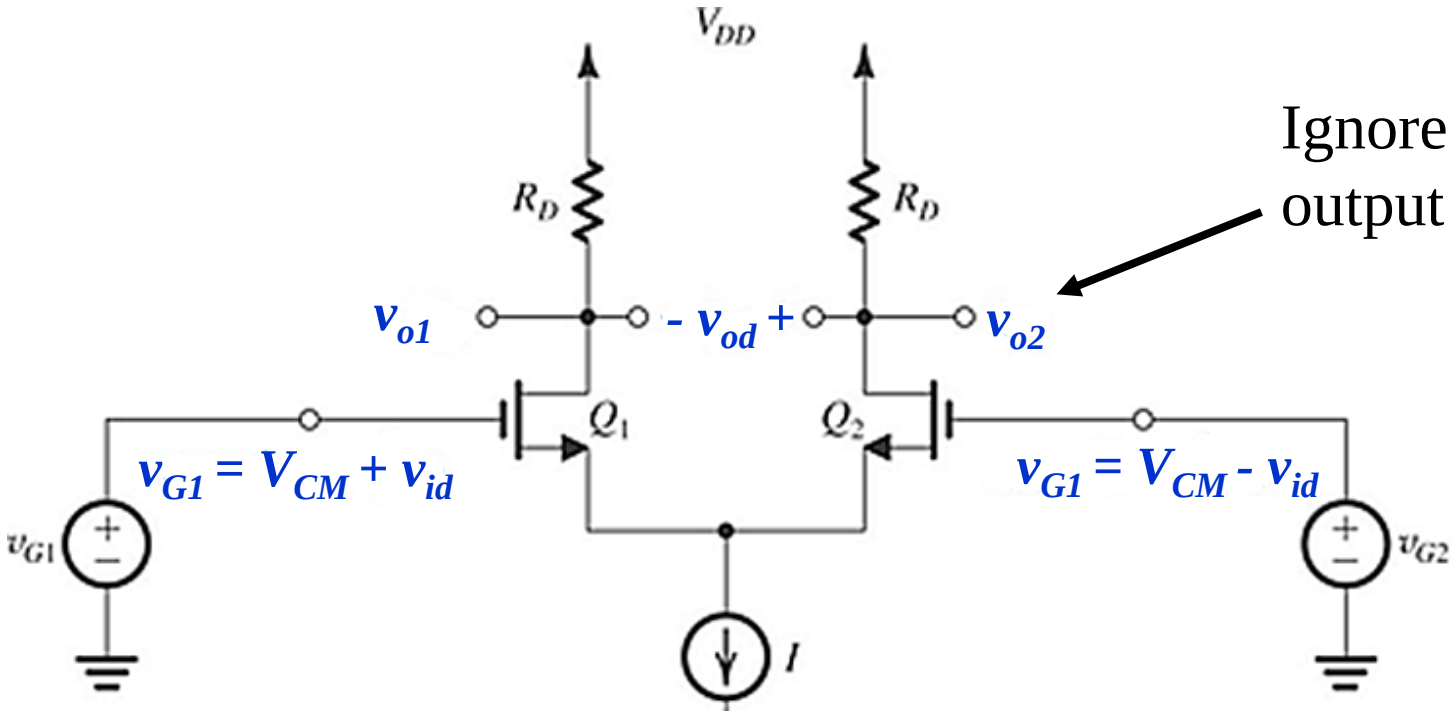
v_{G1}-v_{G2} = (v_{id})-(-v_{id}) = 2v_{id}

Differential output signal = v_{od}=v_{o2} - v_{o1}

Virtual ground at the source

- AC ground
- Q_1 and Q_2 are perfectly matched and are in saturation
- Truly differential input signal
- Eliminates need for large bypass capacitor

Differential Gain, A_d



Ignore DC at the output for now

Differential Gain= 2 x single stage gain

- If the input differential voltage = $v_{id} - (-v_{id}) = 2v_{id}$ then
- Output voltages: $v_{o1} = -g_m R_D (v_{id})$, $v_{o2} = -g_m R_D (-v_{id}) = g_m R_D (v_{id})$
- Output differential voltage $v_{od} = v_{o2} - v_{o1} = 2\, v_{id}\, g_m R_D$
- **Differential gain**=$A_d = |v_{od} / v_{id}| = 2\, g_m R_D$
- **Differential gain**=$A_d = |v_{od} / v_{id}| = g_m R_D$ (if input diff. voltage= $v_{id}/2 - (-v_{id}/2) = v_{id}$ Note: book assumes this input diff. voltage)

Common-Mode Gain, A_{cm}

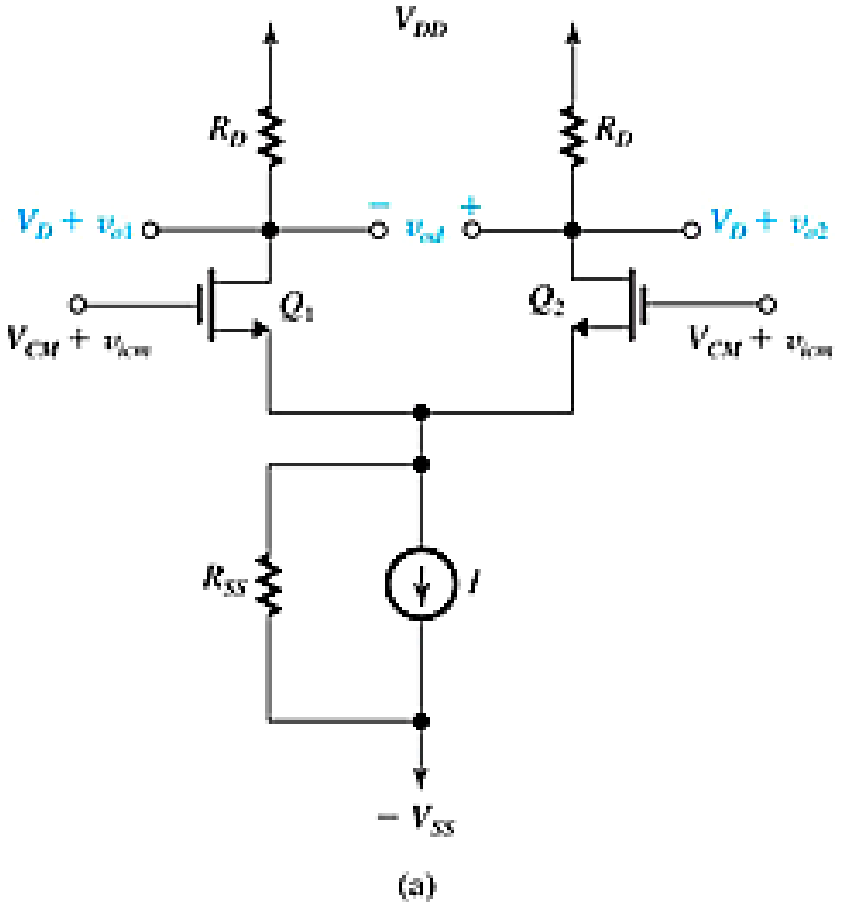
Mismatches amplify noise

- Mismatch in R_D

$$A_{cm} = \frac{v_{od}}{v_{icm}} = \frac{\Delta R_D}{-2R_{SS}}$$

- Mismatch in g_m

$$A_{cm} = \frac{v_{od}}{v_{icm}} = \frac{\Delta g_m R_D}{1 + 2g_m R_{SS}}$$



Common-mode gain A_{cm} is unwanted and should be minimized

Common-Mode Rejection Ratio (CMRR)

CMRR: Figure-of-merit for noise rejection

$$CMRR(dB) = 20log_{10}\left|\frac{A_d}{A_{cm}}\right|$$

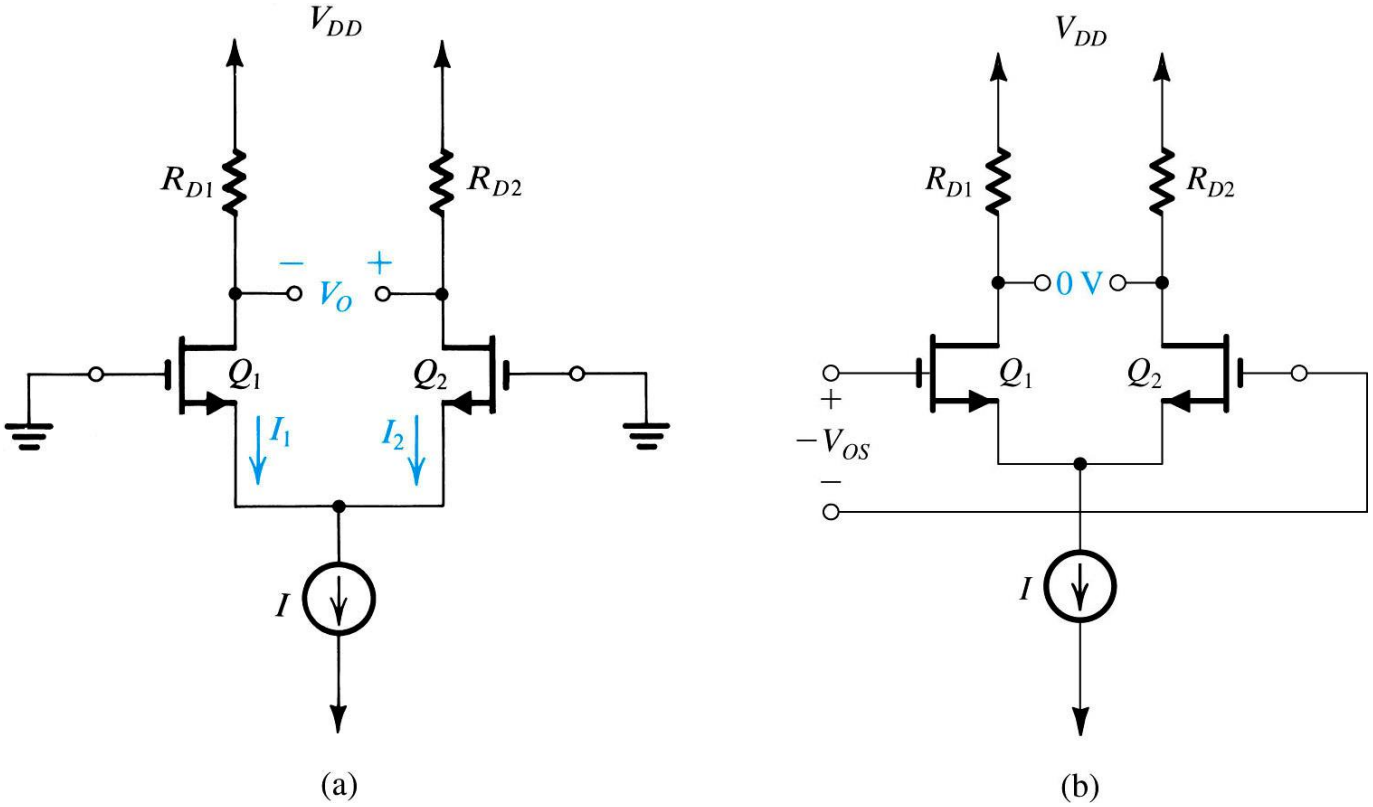
How to increase CMRR (or reduce noise amplification)?

- Increase R_{SS} (output resistance of Current Mirror)
- Q_1 and Q_2 should be perfectly matched (g_m values match)
- R_D values (or output resistances of the active load) should be perfectly matched

Input Offset Voltage

Device mismatches cause a finite dc voltage at the output

$$V_{OS} = \sqrt{\left(\frac{V_{OV}}{2}\frac{\Delta R_D}{R_D}\right)^2 + \left(\frac{V_{OV}}{2}\frac{\Delta(W/L)}{W/L}\right)^2 + (\Delta V_t)^2}$$



Apply a small voltage of opposite polarity to cancel the offset

List of Problems

MOS Diff Pair

p8.2: input common mode range of PMOS differential amplifier

ex8.4 MOS diff pair: differential gain

ex8.7 (simulate and verify) MOS diff pair: CMRR

p8.15: design of MOS differential amplifier