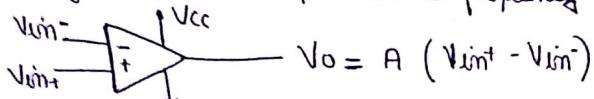


8/1/19

DC gain \rightarrow when input has no frequency



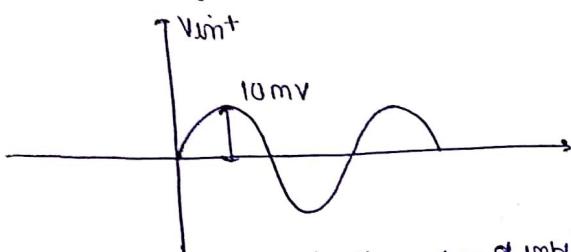
OPAMP \rightarrow Analog or digital device ??

Let $V_{cc} = 5V \Rightarrow V_{out}$ cannot be greater than 5V

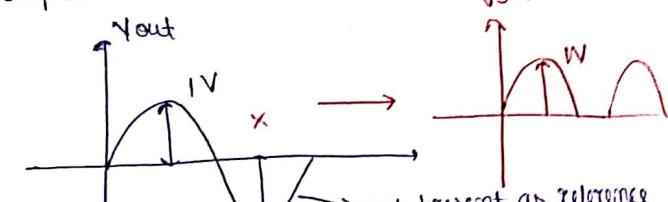
$$V_{in-} = 0$$

$$A = 100$$

Now give sinusoidal waveform of amp 1mV at V_{in+}

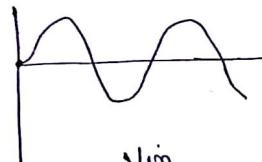


Ques what should be the value of input so that output is not distorted?

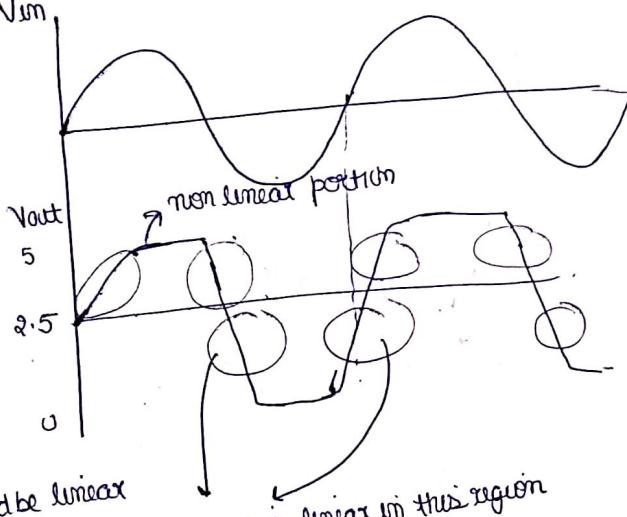


not present as reference voltage has lower limit '0' V. It would be correct if lower limit was $-V_{cc}$

If V_{out} starts from ± 5 then it can go ± 5 above & ± 5 below to get 5Vpp



$5V = A \times x$
 $5V = 100 \times x$
 $x = 50 \text{ mV}$
 V_{in} should be less than 50mV
so that distortion does not occur
as $A = 10^4 \Rightarrow x = 0.5 \text{ mV}$ (input range)
OPAMP acts as amplifier only for
small range else it acts as
comparator.



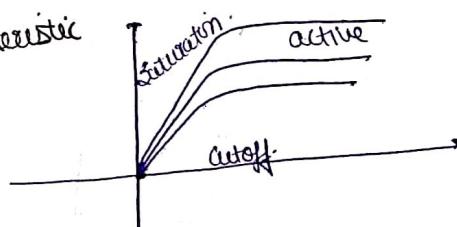
Ques Linearity and non-linearity?

- 1st property of amplifier is that it should be linear
here we know the input & the output.

Oscillators \rightarrow Non linear

Filters \rightarrow Linear in passband and in other non linear

BJT \rightarrow VI characteristic



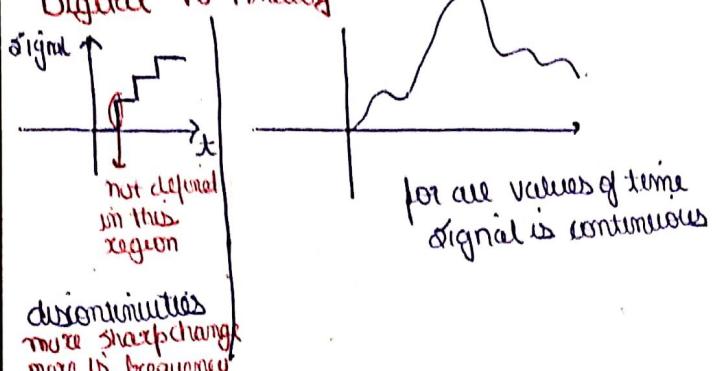
$V_{out} = A V_{in}$
linear & stable

Every system works only for a range of input.

Feedback is very important for stability. opamp's are used with -ve feedback.

System won't be able to respond for lower side (it requires some min input) as well as higher side.

Digital vs Analog



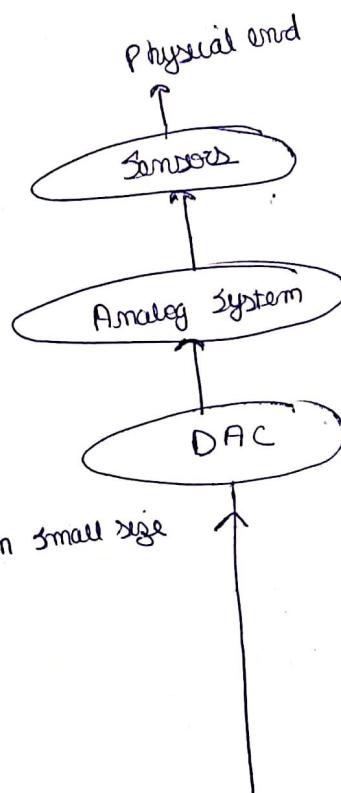
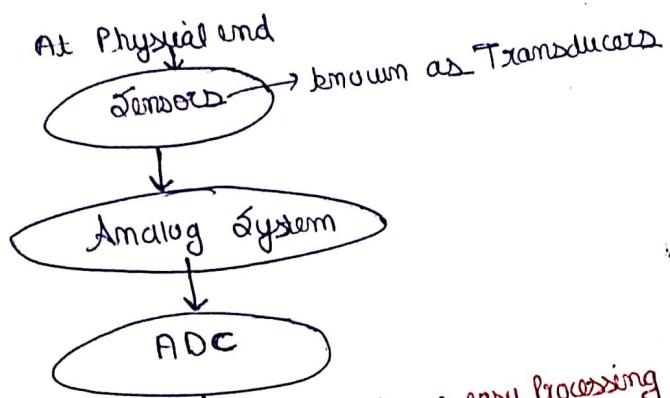
Ques Where do we need Digital and Analog Systems

All the information available around us - temperature, humidity etc are analog.

To communicate with our surrounding we need Analog System.

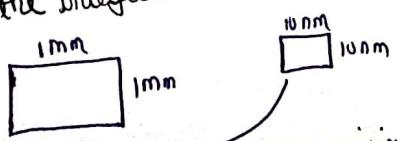
To perform processing we require digital system.

For Preprocessing analog systems are important

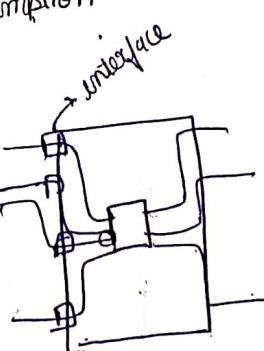


- easy processing
- huge chunk of data can be stored in small size
- as stored so can be reused
- power saving
- robust
- compatible
- smart

These two systems need to be interfaced properly.
More is the integration lesser will be the Power consumption



around 10 billion transistors on this chip



Integration

- ① Power
- ② Area
- ③ Complexity
- ④ Noise
- ⑤ Cost
- ⑥ Speed

$$\frac{dV}{dt} = \frac{i}{C}$$

either increase $i \rightarrow$ but it will increase power consumption

or decrease $C \rightarrow$ decrease area (d is 3rd dimension won't affect)

Transistor \rightarrow lower dimension one will be faster as parasitic capacitance will be low
i.e. A load \rightarrow C goes \rightarrow $\frac{dV}{dt}$ more \rightarrow speed more

10/1/19

Digital, miniaturization of analog is required to deal with digital
 popular digital circuits are memory

$$1KB \rightarrow 2^{10} \text{ bits}$$

$$1MB \rightarrow 2^{20} \text{ bits}$$

Integration impo. When blocks repeat.

Transistor dimensions will become $\sqrt{2} \cdot \text{dim}$ \rightarrow Area $\frac{1}{2}$ over 18 months

e.g. 180 nm, technology node

length of channel
 or min pitch / in general

Boundary \rightarrow Semiconductor industry forming IC's.
 with shrinkage of size performance gets affected.

$$\frac{dV}{dt} = \frac{i}{C}$$

$$C = \frac{\pi \epsilon_0}{d} \quad n = l \times w$$

$n \rightarrow$ unaffected

so as $n \uparrow, C \uparrow \rightarrow$ speed \uparrow (i constant)
 Transistor size $\downarrow \rightarrow$ speed \uparrow $\rightarrow V_{DD} \downarrow$

Static Power \rightarrow when constant current flows
 dynamic " \rightarrow due to charging & discharging of capacitor

$$P_D = C V_{DD}^2$$

To produce digital data, Analog box is required on same platform that is why NLSJ comes

To get same performance with miniaturization
 as size \downarrow , controlling parameters \downarrow

We use sensor because it is cheapest but cannot sense all physical entities.
 We are searching for sensors that could be embedded in chips and power consumption is less.

Q&A

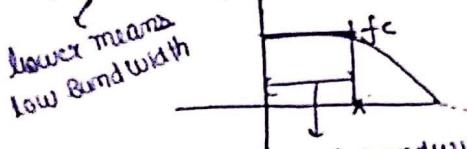
MOSFET → Cheap, compatible towards digital VLSI, Blueprint taken (Photolithography)
 vs BJT
 → leakage current 10^{-6}
 Power dissipation
 but in BJT there
 is some current
 in base)

↓
 its cost depends
 on no. of masks/
 blueprints)
 less than that of
 BJT.

In Analog Domain

Speed of BJT more as in MOSFET no. of intercapacitance are more.. almost every node is associated with capacitor ($\approx 10^{-15} \text{ F}$)

cutoff frequency of MOSFET < BJT

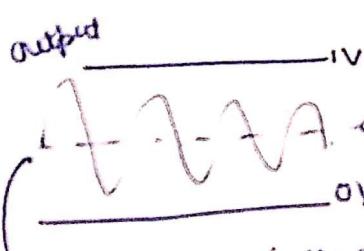


This bandwidth of BJT is higher \Rightarrow we can achieve higher speed as can work with higher frequency.

Gain → small signal
 large signal

we put sys in state where maximum efficiency can be achieved.

Q points



+ve small signal
 -ve small signal

(large signal), biasing state, Q point (in BJT)

QP set here initially so that equal prob. of moving in both directions of signal

will be distorted.

usually small signal \rightarrow AC signal \rightarrow frequency changes

(gain etc. parameters are for these)

System state must be constant and on that small signals are applied which are then amplified etc.

Small signal val gain = $g_m R_{out}$

Transconductance

equivalent model.

We replace mosfet with equivalent model.

$$g_m = \frac{i_c}{V_T} \quad (\text{mosfet})$$

g_m of BJT

$$V_T = 26 \text{ mV}$$

$$\text{g}_m = \frac{I_o}{V_T}$$

$$V_T < V_{\text{in}}$$

$$\text{g}_m \text{ BJT} > \text{g}_m \text{ MOSFET}$$

~~BJT~~ Speed more, gain more, less noise than MOSFET, Bandwidth more

Parameters of Analog design

- # Cost
- # speed (B.W) ↑
- # Power ↓
- # Noise ↓
- # Gain ↑
- # Linearity (Gain should be constant for all inputs) ↑
- # I/p & O/p impedance
- # Supply → increases swing but also increases power dissipation also
- # Swinging (min & max) ↑ fixed for technology node
- # Swinging should be wider

g_m of MOSFET

$$V_T = 26 \text{ mV at } 300\text{K}$$

$$V_{\text{in}} \rightarrow V_{\text{out}}$$

$$\text{g}_m = \frac{I_o}{V_{\text{in}}}$$

if 90% area taken by digital then analog takes 5% only
So area not a concern in Analog.

keep amplifier in mind

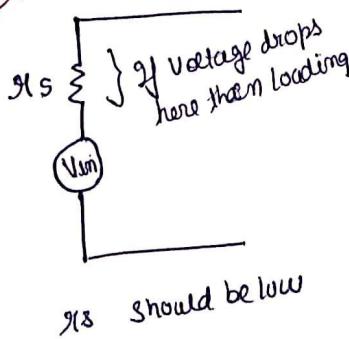
Amplifiers should have power amplification
in microphone battery amplifies power

$$\text{Small signal power gain} = \frac{V_{\text{out}} I_{\text{out}}}{V_{\text{in}} I_{\text{in}}}$$

4 different ...
V-I ~~transconductance~~
I/p Imp ∞
O/p Imp ∞



For voltage source eq circuit

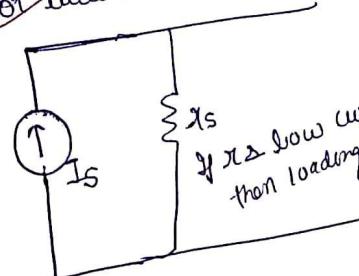


r_s should be low

$$\text{but if } r_{\text{out}} = 0 \Rightarrow g_{\text{out}} = 0$$

$$g_{\text{out}} = g_m R_{\text{out}}$$

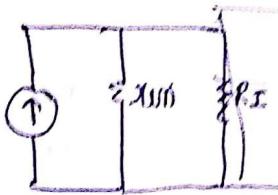
current amp:
I-V
0
0
For current source eq circuit



When Voltage as Input \rightarrow Input impedance ∞
So that V_{in} transfers completely

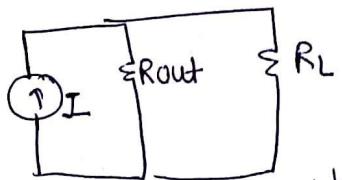
(Gm must be high in present)

When Current as I/P \rightarrow Input Impedance should be 0



O/P Impedance (now amplifier becomes source)

Amp with O/P as voltage, $R_{out} = 0$



when O/P is current, R_{out} should be ∞ so that I is available for R_L completely.

V·I \rightarrow Transconductance amplifier best as $g_{mi} \propto 2 \cdot R_{out} \rightarrow g_{mi} \rightarrow \infty$

16/11/19

FETs (Field Effect Transistor)

most of the programmable IC's are digital IC

we make connections
and not circuits

• ASIC's \rightarrow putting, wiring, connecting every single transistor

Application specific IC

• Semi custom IC's \rightarrow

• Fully custom IC's \rightarrow Designing everything

• Programmable IC's \rightarrow

1

NIMOS

Source emitting storage

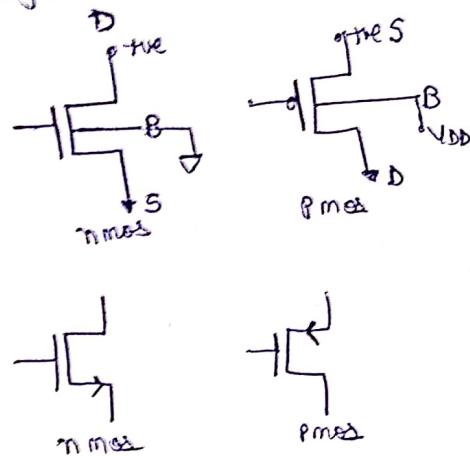
Drain accepts or draws charge.

Here Main Vol = ground

Source low Vol

Drain high Vol

more layer → more masked → more cost

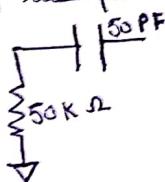


Normal doping $\sim 10^{15}-18$ atom/cm³ → doping higher

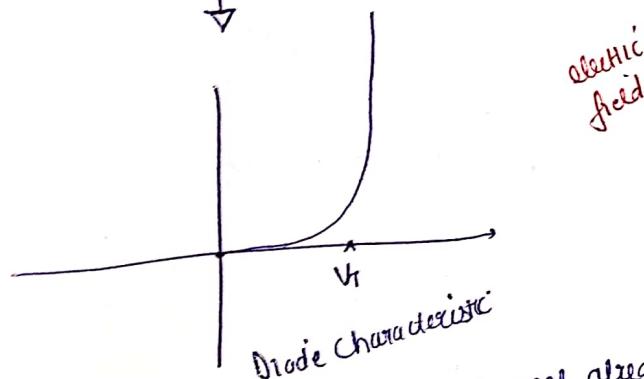
than this denoted by + sign

- None of the junction must be forward biased
- we need to put ESD on IC to protect it from damage
- electric discharge due to heavy current inside.

Our body has few $10\text{ k}\Omega$ of Resistance for eg $50\text{ K}\Omega$



we keep gets complete we experience discharge



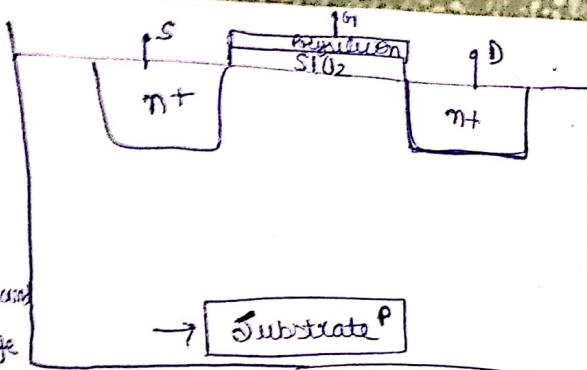
$$E_f = \frac{dV_{ds}}{dL} \rightarrow \begin{matrix} \text{Voltage} \\ \text{Length of Channel} \end{matrix}$$

→ mean life time
→ mean free path
 e^- won't survive in depection region

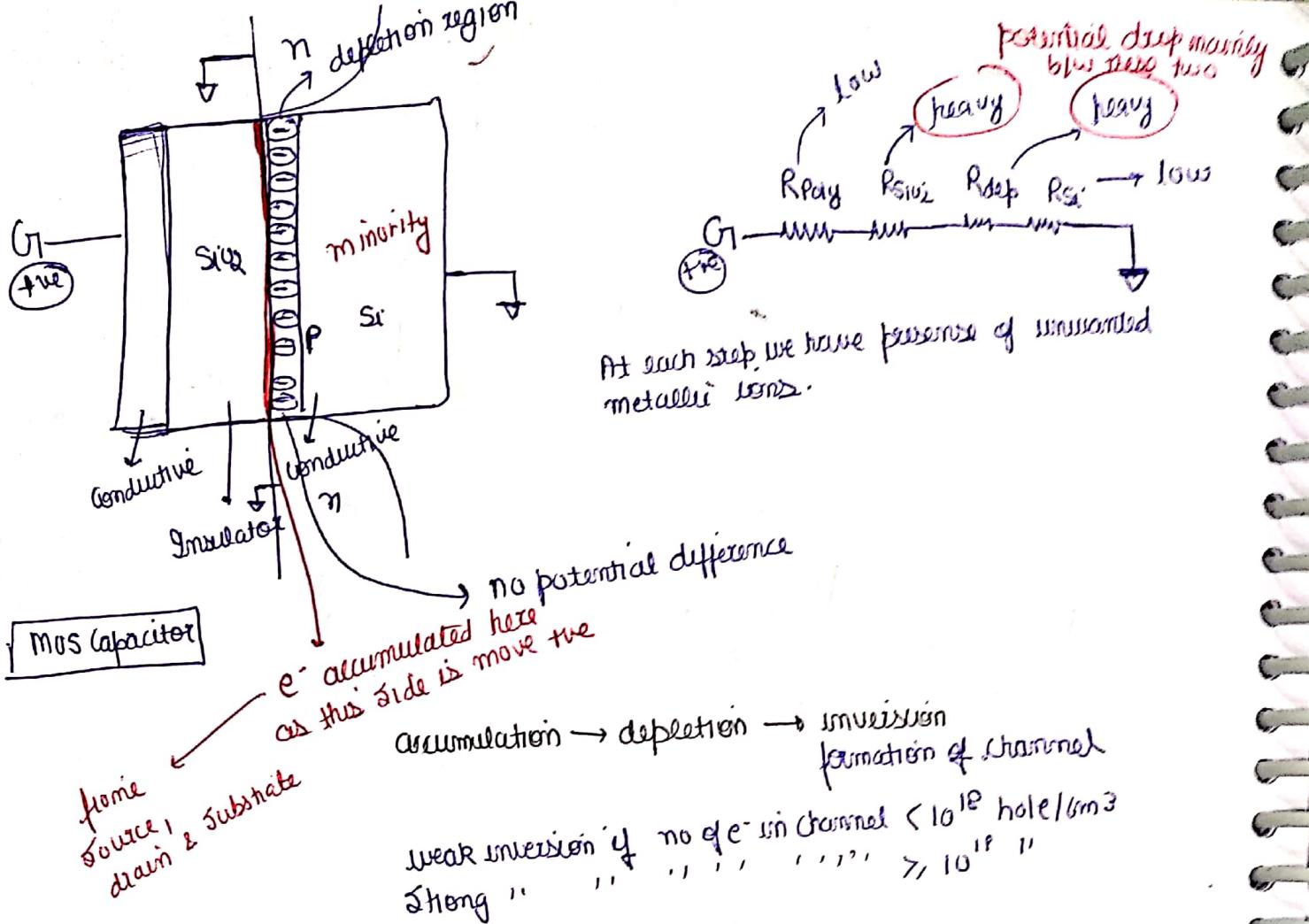
Depletion Type MOSFET → channel already present
Enhancement → Channel needs to be created

Accumulation → Polysilicon can be considered as metal as it is heavily doped
Poly silicon because metal will melt due to high temperature in above layers.

Robust Strong as compared to Al



MOSFET is identical



density density equal to bulk \rightarrow strong inversion
 Threshold Voltage $\rightarrow V_T$ required such that density of e⁻ in channel \neq density of holes in bulk.

drop in depletion region \rightarrow surface potential

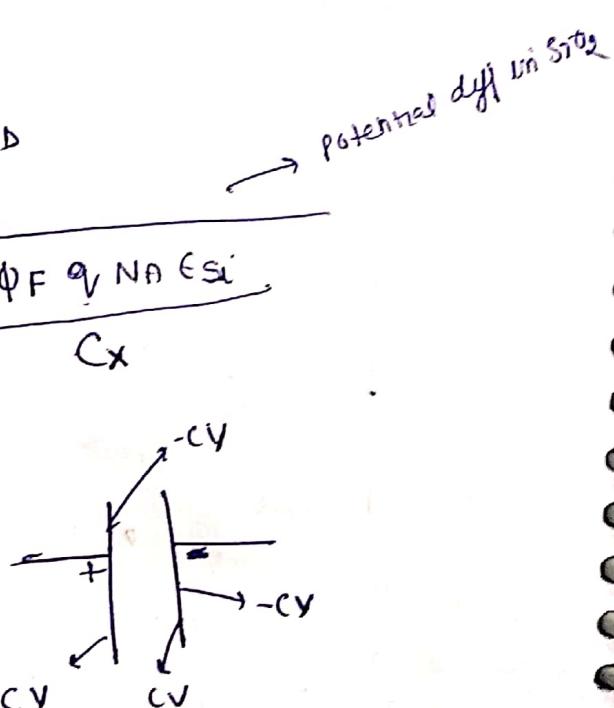
$$V_D = \frac{KT}{q} \ln \frac{NA ND}{n_i^2}$$

at $V_T, NA = ND$

$$V_T = \underbrace{\left(\frac{KT}{q} \ln \left(\frac{NA}{n_i} \right) \right)}_{\text{across depletion}} \phi_F + \frac{\sqrt{2\phi_F q N_A \epsilon_{Si}}}{C_x}$$

$$V_T = 2\phi_F + \frac{\sqrt{2\phi_F q N_A \epsilon_{Si}}}{C_x}$$

$$C = WL C_{ox}$$

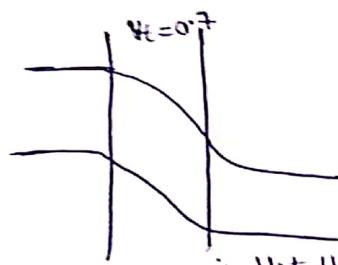


At interface there will be mix up of Si's $\text{SiO}_2 = \text{SiO}_x$ (rough surface) \rightarrow unwanted bonds.

1 impurity terms when 10^{12} Si carbures.

$$V_{th} = \underbrace{\alpha \Phi_F}_{\text{Si}} + \underbrace{\frac{\sqrt{2qN_A\Phi_F\varepsilon_{Si}}}{C_{ox}}}_{\text{SiO}_2} + \underbrace{\frac{\Phi_{ext} +}{C_{ox}}}_{\text{unwanted charges}} + V_{fb}$$

When P & N contact they have diff. work functions they exchange charges to achieve equilibrium



To make it flat we need flatband (V_{fb}) potential

17/1/19

- 1) Higher is the doping (substrate) higher is the V_{th}
- 2) on $\uparrow T$, charges will release energy and less holes can recombine as lattice vibrate so they are to be swept out

$T \uparrow \rightarrow V_{th} \uparrow$

$C_{ox} \rightarrow$ per unit area capacitance

$$C_{ox} = \frac{\epsilon_{SiO_2}}{t_{ox}}$$

more is the thickness of oxide layer, weaker will be electric field

$$E = \frac{V}{d}$$

$$V_{th} \propto t_{ox}$$

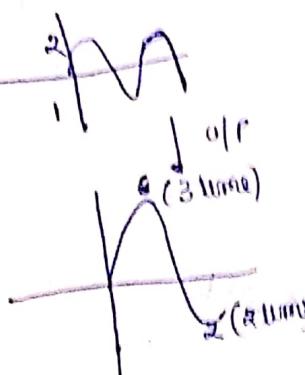
$$V_{th} \propto T$$

$$V_{th} \propto \text{doping}$$

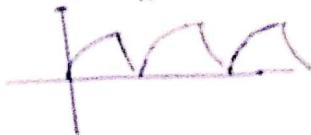
Threshold Voltage will derive many parameters that are supposed to be constant. So V_{th} must be constant.

If for example gain is not constant then signal properties will change.

Square wave made of odd harmonics (infinite)



$$\text{Signal} = A \sin \omega t + B \sin 3\omega t + C \sin 5\omega t + D \sin 7\omega t$$



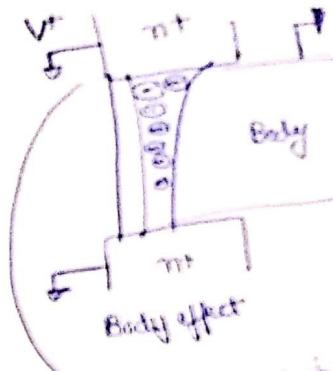
Square wave is formed by odd harmonics

Body effect
Now if Voltage is applied to Drain, it will attract e^- from inversion layer (from where e^- come)

$V_D \rightarrow$ inversion layer charge + depletion layer charge (constant)
constant To maintain total charge depletion layer charge

→ To get back inversion layer
① Intrinsic V_{DS} (gate potential) is constant
Depletion region boundary (near periphery when channel length is less)
Now when $V_D=0$, $V_S=0$, $V_G=V$
new depletion region will increase than due to that reason
depletion region already does of creating depletion layer.

Body effect $\uparrow V_{th}$
Depletion region boundary $\uparrow V_{th}$



- here n is at high voltage,
- p is ground
- so depletion region ↑
- as more field

In case of Body effect

$$V_{DS} = V_{thp} + Y \left(\sqrt{2\phi_F + V_{SEL}} - \sqrt{2\phi_F} \right)$$

Hot e^- effect
When channel length L, E_F , mobility, carrier energy E (collide with lattice)
 \pm Ox hole traps. So e^- can get trapped in this, then will take out charge due to that time when inversion layer is formed e^- 's already passed so lost work $\rightarrow V_{th}$.

in p channel, V_{thp}

Current Equation

$$I_{DS} = \frac{Q}{t} = \frac{CV}{t} = \frac{Cox WL V}{t} = \frac{Cox WL}{Aox t} \left(\frac{V_G - V_{th}}{L} - \frac{(V_D + B)}{L} \right)$$

emitting charge drift

$$M_{EDS} = V_{drift} = \frac{L}{t} = \frac{W}{L} \frac{V_{DS}}{L}$$

$$\frac{1}{t} = \frac{W}{L^2} \frac{V_{DS}}{L}$$

$$I_{DS} = \mu_n (oxW) \frac{L}{L} \left(V_{GS} - V_S + V_S + V_{TH} - \frac{V_D + V_S}{2} \right) V_{DS}$$

$$I_{DS} = \mu_n (oxW) \frac{L}{L} \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS}$$

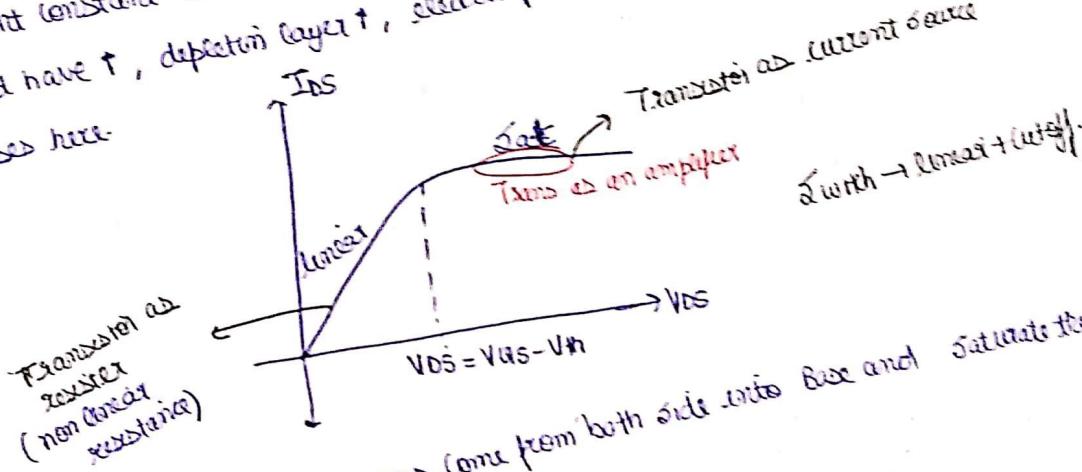
$V_{GS} > V_{TH}$
channel
is present
 $V_{DS} < V_{GS} - V_{TH}$

$$I_{DS} \propto \frac{W}{L}$$

$$I_{DS} \propto \mu_n \text{ (mobility)}$$

V_{DS} cannot be -ve because otherwise drain & source will get interchanged.

As $V_{DS} \uparrow$ and V_{GS} constant \rightarrow channel length will reduce.
 If Now current constant because if it would have \downarrow , depletion region \downarrow , channel will form
 If current would have \uparrow , depletion layer \uparrow , electric field $\uparrow \Rightarrow$ tunneling effect
 So current ceases here



g_m BJT when both forward bias, then charges come from both side into base and saturates there.
 \hookrightarrow switch \rightarrow saturation + cutoff.

$$V_{DS} > V_{GS} - V_{TH}$$

$$I_{\text{saturation}} = \frac{\mu_n (oxW)}{L^2} (V_{GS} - V_{TH})^2$$

$$I \propto \frac{W}{L}$$

in digital VLSI we choose $L_{min} \Rightarrow Cap \uparrow \Rightarrow$ speed high
 \hookrightarrow geometry less, we can put many blocks over a few area.

g_m analog VLSI area is not concern so we will change both W & L .

When $V_{GS} < V_{TH} \rightarrow$ transistor behaves like BJT
 diffusion comes into picture

$$I_{DS, \text{sub}} = I_0 e^{\frac{V_{GS} - (k-1)V_{DS}}{VT}}$$

$$\left(1 - e^{\frac{V_{DS}}{V_T}} \right)$$

Intrinsic Voltage

I very less

22/1/19

Voltage	I_{DS}	
1) $V_{GS} = 0$	0	→ off
2) $0 < V_{GS} < V_{th}$	$e^{\frac{V_{GS} - (K-1)V_{DS}}{V_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right)$	→ Subthreshold
3) $V_{GS} \geq V_{th} \& V_{DS} < V_{GS} - V_{th}$	$\frac{Un Cox W}{L} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) V_{DS}$	→ Linear / resistive
4) $V_{GS} \geq V_{th} \& V_{DS} \geq V_{GS} - V_{th}$	$\frac{Un Cox W}{2L} (V_{GS} - V_{th})^2$	→ Sat

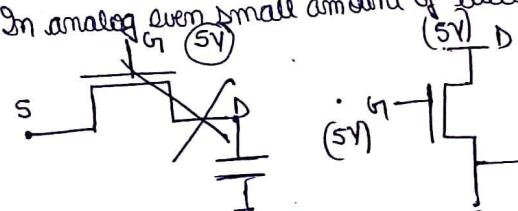
③ $V_{GS} - V_{th} \gg \frac{V_{DS}}{2}$

$$I_{DS} \approx \frac{Un Cox W}{L} (V_{GS} - V_{th}) V_{DS} = \beta (V_{GS} - V_{th}) V_{DS}$$

$$I_{DS} (\text{linear}) = \frac{1}{\beta (V_{GS} - V_{th})}$$

④ In saturation region, transistor is used as amplifier.

In analog even small amount of current will affect.



$V_{th} = 1V$
 $V_{GS} = 4V \rightarrow$ will reach to 5V in case of analog

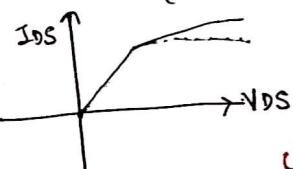
Channel length modulation

where $V_{DS} = V_{GS} - V_{th}$

channel increase $\Rightarrow L \downarrow$, width remains same, $R \uparrow$, current slightly \uparrow

$$R = \frac{PL}{A}$$

$$I_{DS, \text{sat}} = \frac{Un Cox W}{(L - \Delta L)} (V_{GS} - V_{th})^2$$



But in saturation region $R \rightarrow \infty$
 We need to balance it

Sheet channel effect

$$I_{DS, \text{sat}} = \frac{Un Cox W}{L (1 - \frac{\Delta L}{L})} (V_{GS} - V_{th})^2$$

$$I_{DS} = \frac{Un Cox W}{L} (V_{GS} - V_{th})^2 (1 + \frac{\Delta L}{L})$$

$$I_{DS} = \frac{Un Cox W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$$

$$\frac{\Delta L}{L} \propto V_{DS}$$

$$\frac{\Delta L}{L} = \lambda V_{DS}$$

channel length modulation factor

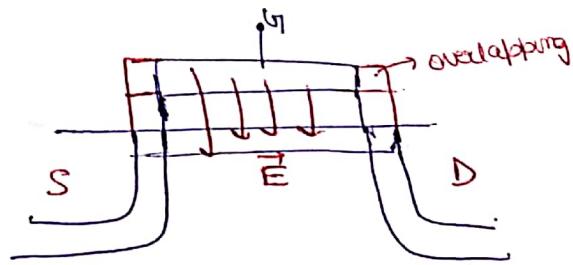
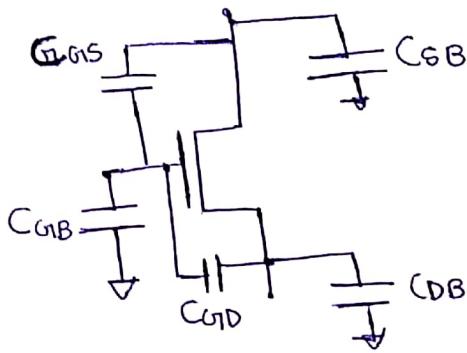
$$R_{DS, \text{sat}} = \frac{1}{I_{DS} \lambda}$$

I_{DS} strongly related to V_{GS}
 and weakly dependent on V_{DS} in saturation.

Ques What happens if V_{DS} is further?

Ans Tunneling effect and e⁻ will enter drain with high velocity \Rightarrow high kinetic energy
 \rightarrow collision \rightarrow Avalanche Breakdown
 \rightarrow flooding will occur. It will damage device

Whenever there will be p-n junction there will be capacitor



For system to be stable o/p should converge at $t \rightarrow \infty$
Poles in LHS only

$$\frac{A}{s+a} = Ae^{-at}$$

Poles corresponds to delay. If there is delay in system there will be pole.

A ————— B
I/P O/P
I/P becomes zero at some frequency
every additional path will lead to zero o/p
↓
b/w I/P & o/p
will cause equal o/p
as sense in main path

Amplifiers

Gain of amplifier = Output Resistance \times Trans Conductance = g_m

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$$

Rate of Change of o/p current with respect to I/P Voltage

Small change in gate voltage causes large change in current $I_{DS} = \frac{\mu n C_{oxW}}{2L} (V_{GS} - V_{th})^2$

| exponential relation Powerful than square |

$$\textcircled{Q} m = \beta (V_{GS} - V_{th})$$

$$I_{DS} = \frac{\beta}{2} (V_{GS} - V_{th})^2$$

$$V_{DS\text{ sat}} = V_{GS} - V_{th} = \sqrt{\frac{2I_{DS}}{\beta}}$$

$$\frac{\partial I_{DS}}{\partial V_{GS}} = \beta (V_{GS} - V_{th})$$

minimum voltage required to have current in saturation

$$g_m = \sqrt{2\beta I_{DS}} = \frac{2I_{DS}}{V_{GS} - V_{th}}$$

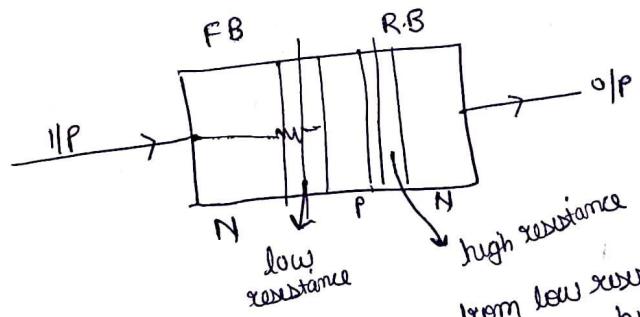
$$\beta = \frac{2I_{DS}}{(V_{GS} - V_{th})^2}$$

When β is fixed it will follow linear relation with $V_{GS} - V_{th}$

Amplifier

I/P at Gate
O/P at drain

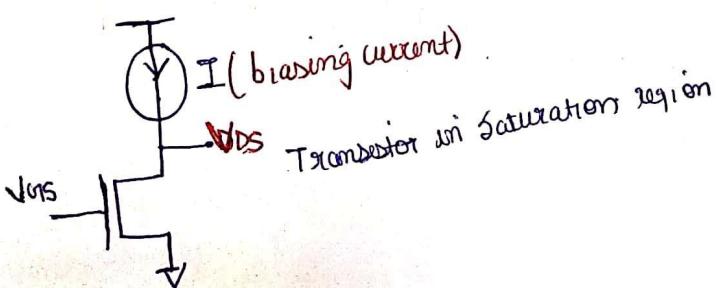
Requirement for amplification \rightarrow 1st junction forward bias
2nd " reverse bias



Constant current moves from low resistance to high resistance which will lead to low voltage to high voltage \Rightarrow gain
 $V_{out} > V_{in}$ for constant current

$$I_{DS} = \frac{\beta}{2} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$

Now if current is constant & we change V_{GS} . Will current be constant then?
If I_{DS} constant & we change V_{GS} then to keep I_{DS} constant V_{GS} changes with huge amount



amp \rightarrow small change in V_{GS}
will lead to large change in V_{DS}
if current constant

(*) Constant current & very high resistance all same thing

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b) Condition for PMOS:

$$I_{DS} \rightarrow I_{SD}$$

$$V_{GS} \rightarrow V_{SG}$$

$$V_{DS} \rightarrow V_{SD}$$

$$V_{thn} \rightarrow |V_{thp}|$$

$$I_{SD\text{ sat}_P} = \mu_P Cox \left(\frac{W}{L} \right)_P \left(V_{SG} - |V_{thp}| \right)^2 \left(1 + \lambda_P V_{SD} \right) \quad V > |V_{thp}| \text{ pmos}$$

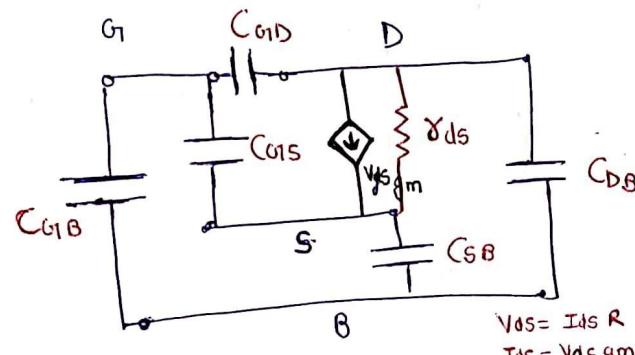
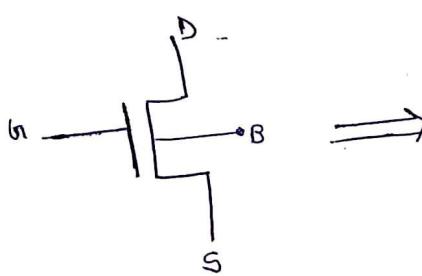
Digital are only ON & OFF devices

Analog \rightarrow To give continuous output all devices must be "on" and in saturation region.

application occurs in saturation region

To make system stable, biasing should be such that the range covers maximum saturation region

Small Signal Equivalent of MOSFET (to perform circuit analysis)



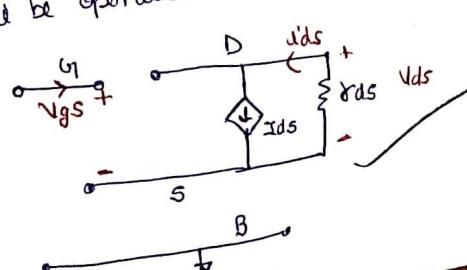
b/w gate & body \propto resistance
i.e. open circuit
no need to draw

γ_{ds} \rightarrow less when channel length is less

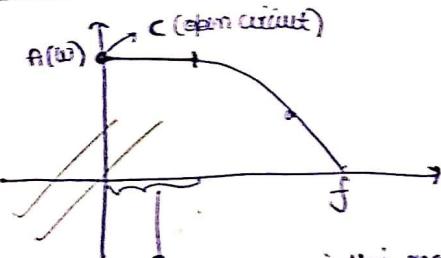
$I_{DS} \propto V_{DS}$ Current dependent \rightarrow voltage source b/w drain & source

MOSFET \rightarrow Voltage controlled current device

\approx small signal DC Gain (low frequency)
Capacitor blocks DC so for DC Capacitor must be open circuit
Capacitive inductance \propto no poles no zeros

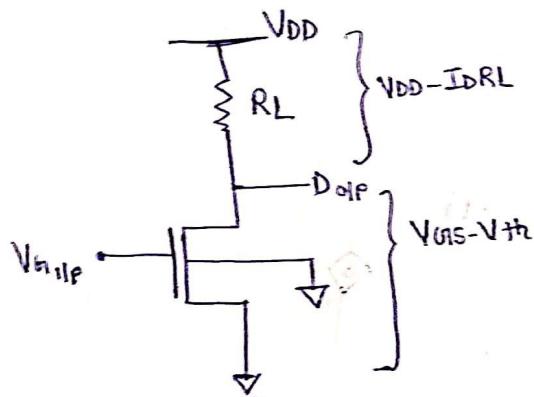


while analyzing circuits all the constant currents and voltages will be made zero.
 Voltage short circuit to ground
 Current open circuit
 i.e. assume the parameters that do not change as zero.



A constant in this region so we analyze at $f=0$
 $C_{\text{op}} = \text{open circuit}$
 $f=0 \Rightarrow \text{DC analysis}$
 as $f \uparrow \rightarrow \text{AC analysis}$

delay terms from poles, poles from R & C



For saturation $V_{GS} > V_{th}$
 $V_{DS} \gg V_{GS} - V_{th}$

Let us assume Power dissipation is given. Above this value Power should not be dissipated.

Let $V_{DD} = 2V$
 Power dissipation should not exceed 10mW
 more $I \Rightarrow$ more speed
 more $I \Rightarrow$ more power dissipation
 $I < 5\text{mA}$
 Let $I = 1\text{mA}$

For 180nm technology node

$$J_{n(\text{SI})} \rightarrow n_{\text{mes}} = 300 \mu\text{A/V}^2$$

$$P_{\text{mes}} = 60 \mu\text{W}$$

$$\text{As } V_{GS} \uparrow, I_D \uparrow \Rightarrow I_D R_L f \Rightarrow V_{DD} - I_D R_L$$

range of variation, swing should be minimum

$$V_{DD} = 2V$$

$$V_D = 1.85$$

$$V_{GS} - V_{th} = 0.5$$

V_D should be such that

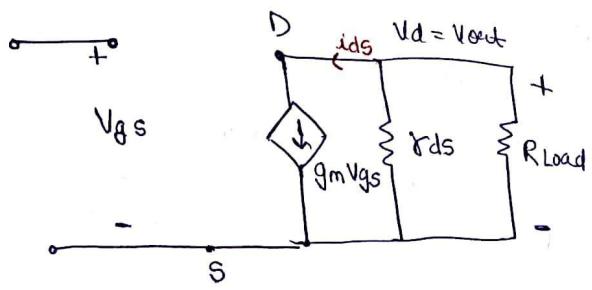
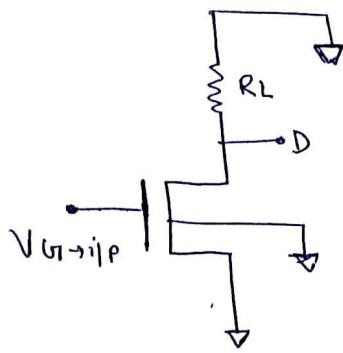
Variation is even and maximum

$$V_D = \frac{2+0.5}{2}$$

$$\begin{aligned} V_D &= \frac{1.7}{2} \\ &= 0.85 \end{aligned}$$

more $R_L \Rightarrow$ lesser will be swing

$$\begin{aligned} V_D &= \frac{2.3}{2} \\ &= 1.05 \end{aligned}$$



$$\frac{V_{out}}{V_{in}} = \frac{V_{ds}}{V_{gs}} =$$

as input ↑, output ↑ So that $V_{DS} - I_D R_{Load}$
not decrease.
out of phase

$$V_{ds} = -g_m V_{gs} \frac{r_{ds} R_{load}}{r_{ds} + R_{load}}$$

$$\frac{V_{ds}}{V_{gs}} = -g_m \frac{r_{ds} R_{load}}{r_{ds} + R_{load}}$$

$$g_{m\text{in}} = -g_m \frac{r_{ds} R_{load}}{r_{ds} + R_{load}}$$

$$r_{ds} = \frac{1}{I_D \lambda}$$

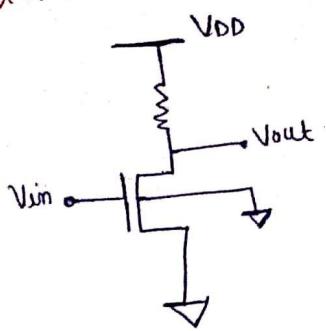
If we ↑ gain through Load (+)
it will affect swing (+)
as $I_D \uparrow$

If $g_m \uparrow \Rightarrow I \uparrow$ again swing ↑

$$A_v = -g_m (r_{ds} \parallel R_L)$$

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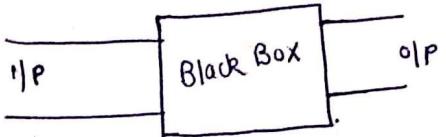
Common Source Amplifier



$$AV = -g_m (\gamma_{ds} \parallel R_{load})$$

\downarrow
X conductance

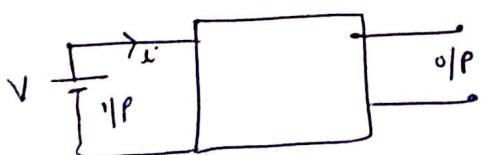
$\rightarrow R_{out}$



To find input impedance apply single voltage source at input terminal, find the current flowing in box and then find impedance

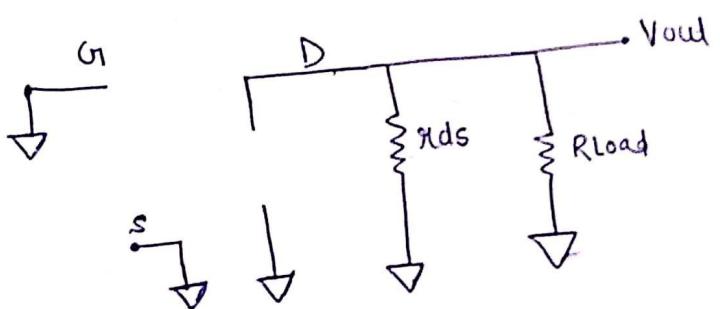
when I/P current = 0, $Z_{in} = \infty$

To avoid superposition



Small signal analysis

All voltages except V_{out} will be zero



$$V_{gs} = 0$$

$I_{ds} = V_{gs} g_m = 0 \rightarrow$ open circuit

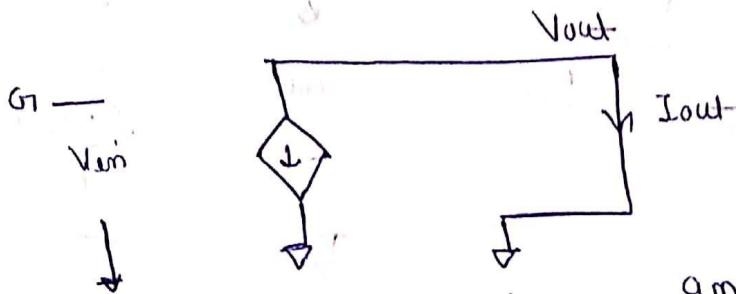
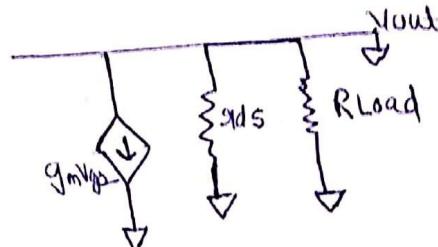
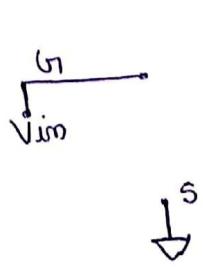
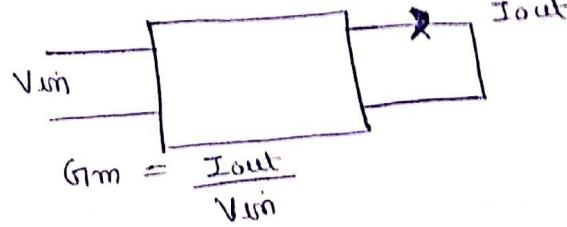
$$R_{out} = R_{load} \parallel r_{ds}$$

(R_{load} limiting gain)

Now find g_m

$$\text{as overall gain} = g_m (\text{of system}) R_{out}$$

To find Transconductance of system \rightarrow Take a black box with short output



$$I_{out} = -g_m V_{gs} = -g_m V_{in}$$

$$\frac{I_{out}}{V_{in}} = -g_m$$

unit A/Volt
gm of order mA/Volt

$$G_{m\text{out}} = G_m R_{out}$$

$$= -g_m (R_{load} \parallel r_{ds})$$

\Rightarrow input \uparrow & o/p \downarrow

Look from Drain side

$$V_{gs} = 0$$

$$R_{out} = r_{ds}$$

~~$$\frac{I + g_m V_{gs}}{r_{ds}} = V$$~~

$$g_m V_{gs} = -\frac{V}{R}$$

$$R = \frac{1}{g_m}$$

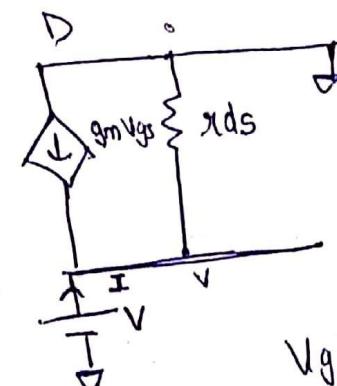
at
order of KSR

$$R_{out} = r_{ds} \parallel \frac{1}{g_m}$$

Look from Source side

$$V_T$$

$$B$$



$$V_{gs} = -V$$

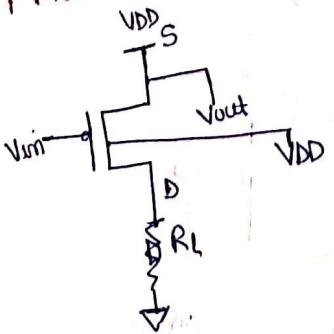
$$\frac{r_{ds}}{\frac{1}{g_m}} = \frac{r_{ds}}{1 + g_m r_{ds}}$$

$$R_{out} = \frac{g_{ds}}{M} \parallel \frac{1}{gm}$$

$\Rightarrow R_{out}$ of order $K\Omega$

From source side changing W/L voltage changes V_{GS} \rightarrow current strong function of V_{GS} so output changes heavily
less resistance

p mos based common source amplifier

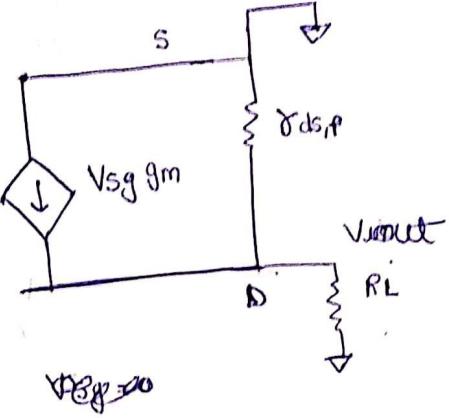


G_m

V_{in}

$\frac{V_{out}}{V_{in}}$

Small signal analysis



$$R_{out} = g_{ds} \parallel RL$$

$$V_{out} = -g_m V_{in} (RL \parallel g_{ds})$$

$$\frac{V_{out}}{V_{in}} = -g_m R_{out}$$

g_m of n mos $>$ g_m of p mos

gain is g_m dependent

How to increase gain

$$AV = -g_m R_{out} \approx -g_m R_{load}$$

(when $RL < g_{ds}$ & $RL \parallel g_{ds}$)

when only single transistor i.e. no R_{load} $\Rightarrow R_{out} = g_{ds}$
maximum gain

$$\propto \frac{\Delta L}{L}$$

$$AV = g_m g_{ds}$$

$$AV < g_m \frac{1}{\lambda I_{DS}} = \frac{g_m}{\lambda I_{DS}} \propto \frac{L}{W}$$

$$\gamma_{DS} = \frac{1}{\lambda J_{DS}} \alpha \frac{L}{W} \times \frac{L}{\Delta L}$$

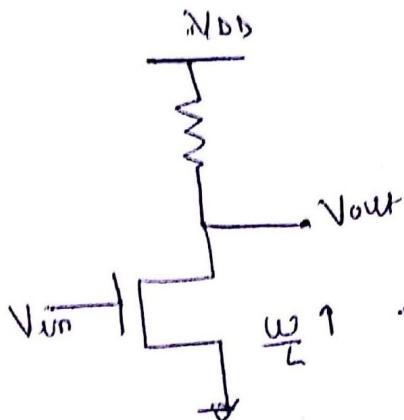
$$AV \propto \sqrt{\frac{W}{L} \times \frac{L}{W} \times \frac{L^2}{\Delta L \times W}}$$

$$AV \propto \frac{W}{L} \times \frac{L^2}{\Delta L \times W}$$

$$AV \propto \frac{L}{\Delta L}$$

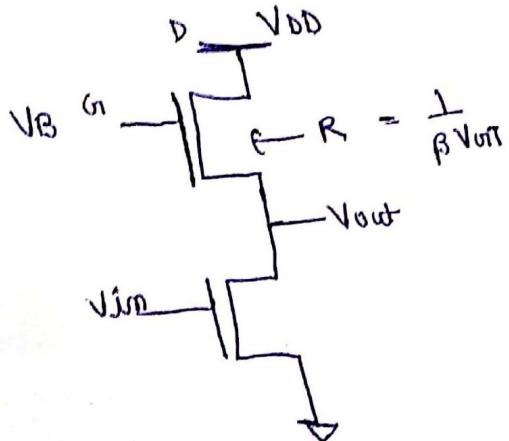
For single transmission with less no load, AV independent of W

With load \rightarrow AV dependent on W



$\Rightarrow I_{DS} \uparrow \Rightarrow$ Power dissipation $\uparrow \Rightarrow$ O/P DC Voltage \uparrow
 $\Rightarrow \beta \uparrow$
 $\text{If current changes through } V_{DS} - V_{th} \Rightarrow V_{DS} - V_{th} P \Rightarrow \text{swing} \uparrow$
 $\text{If current constant } (V_{DS}, V_m) \uparrow \Rightarrow V_{DS,dc} \uparrow$
Overall swing \uparrow

Now transistor will be used for making resistance



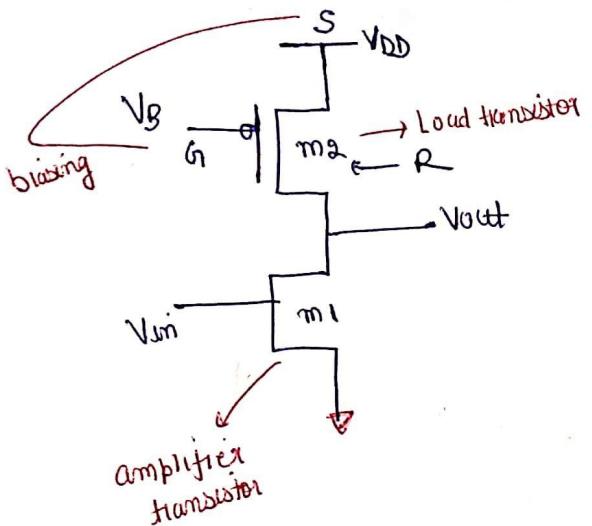
In linear region, Resistance is small

R should be constant

If V_{DS} changes, current changes, R changes ... \Rightarrow not a use

So source is o/p of above nMOS

use PMOS

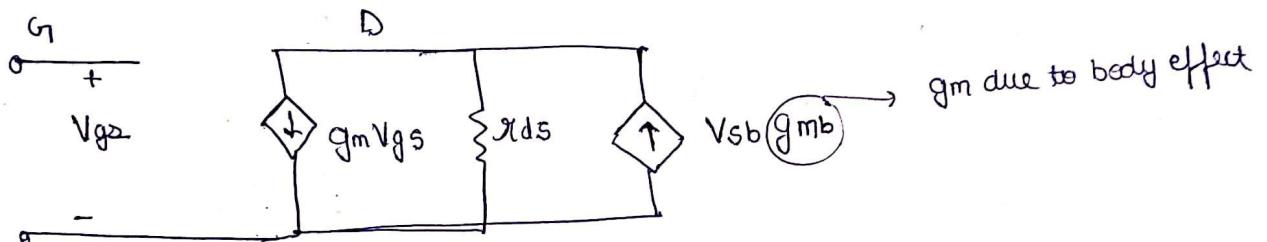


$$\text{gain} = -g_m \times (\gamma_{ds} \parallel \frac{1}{\beta_2(V_{SD} - |V_{thp}|)})$$

$$R = \frac{1}{\beta_2(V_{SD} - |V_{thp}|)}$$

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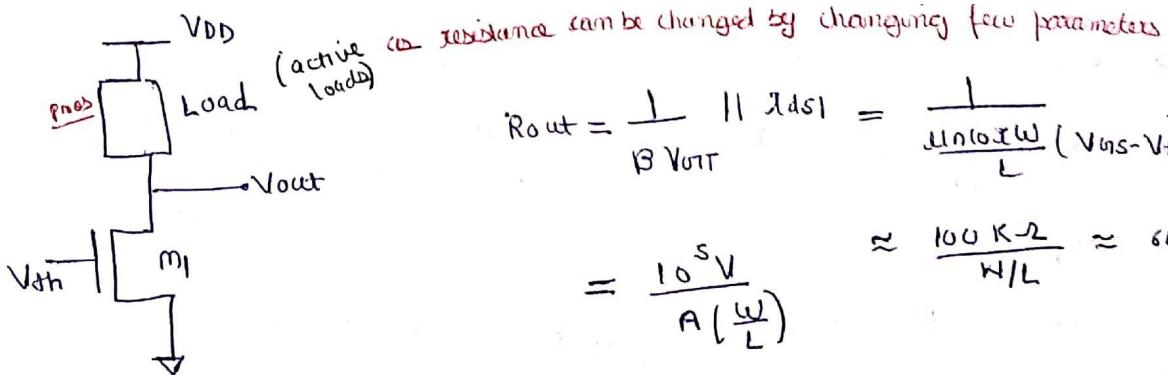
$\nabla V_{th} \uparrow \Rightarrow \text{Current} \downarrow$
 V_{th} depends on V_{SB} (n-mos) & V_{SS} (p-mos)



$$R = \frac{1}{g_m + g_{mb}} \parallel r_{ds} \approx \frac{1}{g_m + g_{mb}}$$

Overall resistance +

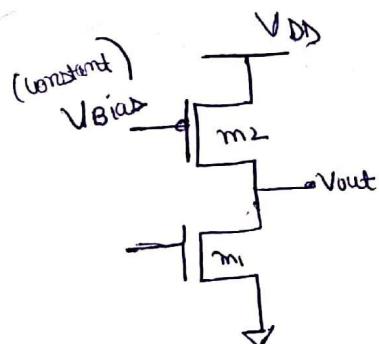
when source is no longer grounded, current flows in through source terminal and \uparrow due to which $I_{DS} \downarrow$



λ is independent of technology.

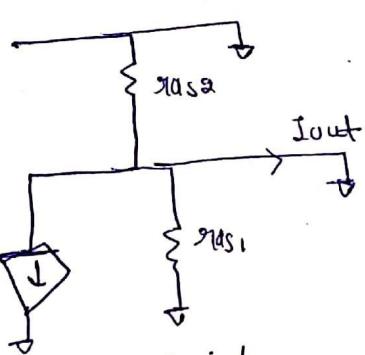
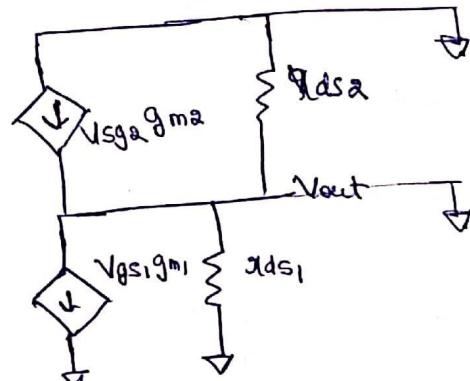
R_{out} can be increased by $\uparrow L$
but $\uparrow L$ will decrease g_m

How to implement High Resistance (load)
both transistors in saturation region



2) min channel length (L)
3) min width (W)

$$180 \text{ nm} \rightarrow \lambda = \frac{180 \text{ nm}}{2}$$



$V_S = V_{DD}$ } Both constant $\Rightarrow S_0$
 $V_g = V_B$ } grounded
in signal port

$$V_{DSat} = \sqrt{\frac{2ID}{\beta}}, \text{ when } ID \text{ is fixed}$$

$V_{SD} > V_{GS1} - V_{th}$ for PMOS
 $V_{DS} > V_{GS2} - V_{th}$ for NMOS

$$V_{DD} - V_{out} > V_{DD} - V_{Bbias} - V_{th}$$

$$V_{out} - 0 > V_{in} - V_{th}$$

$$R_{out} = \frac{1}{g_m1} \parallel \frac{1}{g_m2}$$

$$\Delta V = -g_m1 \left(\frac{1}{g_m1} \parallel \frac{1}{g_m2} \right)$$

$$V_{in} - V_{th} < V_{out} < V_{Bbias} + V_{th}$$

Output swing

$$V_{out} \leq V_B + |V_{thpl}|$$

$$min \rightarrow \sqrt{\frac{2ID}{\beta_1}} (V_{GS} - V_{thn})$$

$$\begin{aligned} max &= |V_B + V_{mpl}| \\ &= V_{DD} - (V_{DSat})_2 \\ &= V_{DD} - \left(\sqrt{\frac{2ID}{\beta_P}} \right) \end{aligned}$$

If $\beta_P \uparrow \Rightarrow max \uparrow$
 $\beta_n \uparrow \Rightarrow min \downarrow$
 $\Rightarrow swing \uparrow$ if $(W/L) \uparrow$
 $V_{DSat} \downarrow$ but overall
swing \uparrow

$$V_{DD} > V_{thn} - V_{thp}$$

Both transistors in saturation and experience high resistance

Both transistors as current source
& two current source in series
is a very bad design
as not possible
Two voltage sources can't be in parallel
" current " " " series
" current " won't be in saturation
so one of them won't be in saturation
Stability will be lost
apply feedback to make it stable.

Input swing

$$V_{in} > V_{thn}$$

$$V_{DS} > V_{GS} - V_{thn}$$

$$V_{out} > V_{in} - V_{thn}$$

$$V_{in} < V_{out} + V_{thn}$$

if V_{in} exceeds this boundary can come out of saturation

If $V_{GS} \uparrow \Rightarrow V_{DS} \downarrow \Rightarrow$ upper transistor can come out of saturation

$$V_{GS,max} \leq \sqrt{\frac{2ID}{\beta_{n1}}} + (V_{th})_n$$

$$V_{DD} - V_{DSat} > V_{in} - V_{thn}$$

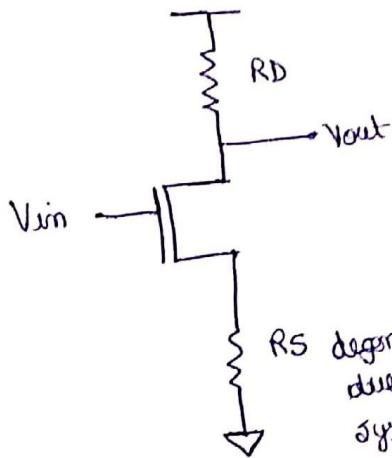
$$V_{DD} - V_{DSat} + V_{thn} > V_{in}$$

If $V_{in} \downarrow, V_{out} \uparrow \Rightarrow$ upper transistor can come out of saturation

If $V_{in} \uparrow, min$ can come out of saturation

Non linearity comes from g_m

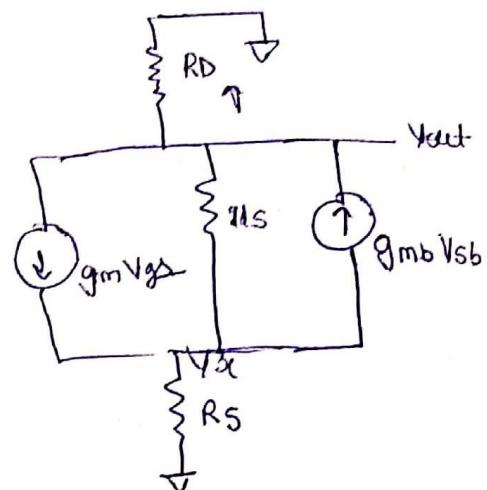
Source Degeneration (System Stabilization)



R_S degenerative resistance
due to this gain \downarrow
system tends towards stability

Whenever body effect comes, first & foremost problem
is non linearity

V_{out} is V_P & not V_{DS}



$$V_{gs} = V_{in} - V_x$$

$$V_{sb} = V_x$$

$$\frac{V_o}{R_D} \neq g_m V_{in} - g_m V_x + \frac{V_o - V_x}{g_{ds}} \equiv V_x g_{mb}$$

$$V_x = \frac{\frac{V_o}{R_D} + g_m V_{in} + \frac{V_o}{g_{ds}}}{g_m + \frac{1}{g_{ds}} + g_{mb}}$$

$$g_{ds} \text{ huge} \Rightarrow \frac{1}{g_{ds}} = 0$$

$$V_x = \frac{\frac{V_o}{R_D} + g_m V_{in}}{g_m + g_{mb}}$$

$$g_m (V_{in} - V_x) = g_m V_x + \frac{V_o}{R_S}$$

$$\frac{V_{in} g_m}{g_m + \frac{1}{R_D} + g_{mb}} = V_x$$

$$g_m = (1 - R_S g_m) g_m$$

$$\frac{V_{in} g_m}{g_m + g_{mb} + \frac{1}{R_s}} = \frac{V_o / R_D + V_{in} g_m}{g_m + g_{mb}}$$

$$A_v \approx -\frac{R_D g_m}{R_s g_m + 1} \approx -\frac{R_D g_m}{R_s g_m} = -\frac{R_D}{R_s}$$

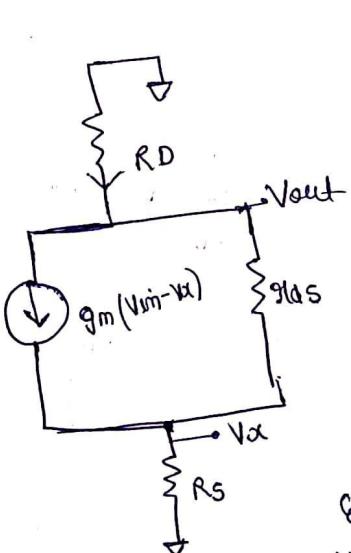
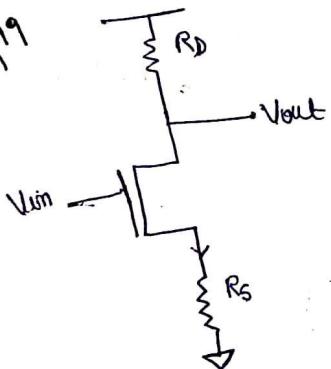
$$A_v \approx -\frac{R_D}{R_s}$$

Highly linear as independent of g_m
and A_v less.

$V_{in} \uparrow$ current \Rightarrow current $\uparrow V_x \Rightarrow V_{out} \uparrow$ ($-ve$ feedback)
This will not allow current to change much

g_m is no longer very high
and system got stable

5/2/19



V_{out}

Equate current value

$$-\frac{V_{out}}{R_D} = \frac{V_x}{R_S}$$

$$-\frac{V_{out}}{R_D} = g_m \left(V_{in} + \frac{V_{out} R_S}{R_D} \right) + \frac{V_{out} + V_{out} R_S}{R_D} \frac{1}{r_{ds}}$$

$$-\frac{V_{out}}{R_D} = g_m V_{in} + \left(\frac{g_m R_S}{R_D} + \frac{V_{out}}{r_{ds}} + \frac{1}{r_{ds}} + \frac{R_S}{R_D r_{ds}} \right) V_{out}$$

$$g_m V_{in} = -V_{out} \left(\frac{1}{R_D} + \frac{R_S}{R_D r_{ds}} + \frac{g_m R_S}{R_D} + \frac{1}{r_{ds}} \right)$$

we can neglect terms having r_{ds} in denominator

$$g_m V_{in} = -V_{out} \left(\frac{1}{R_D} + \frac{g_m R_S}{R_D} \right)$$

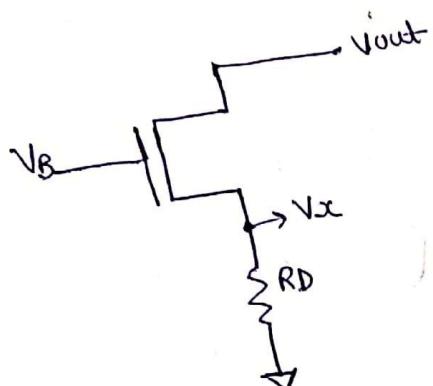
$$\frac{V_{out}}{V_{in}} = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-R_D}{\frac{1}{g_m} + R_S}$$

free from body effect
and non linearity

R_D and R_S can be implemented by transistors

$$A_v = \frac{g_{dsP}}{g_{dm}}$$

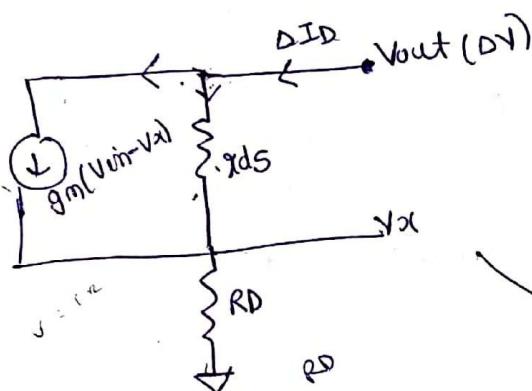
$R_D \rightarrow$ Replaced by PMOS
 $R_S \rightarrow$ Replaced by NMOS



If V_{out} is changed by ΔV find ΔV_x

$$\Delta V = \frac{\Delta I}{\text{Resistance}}$$

$$\Delta V_x = \Delta I R_D$$



$$\frac{V_x}{R_D} = \frac{V_{out}}{\Delta I_D}$$

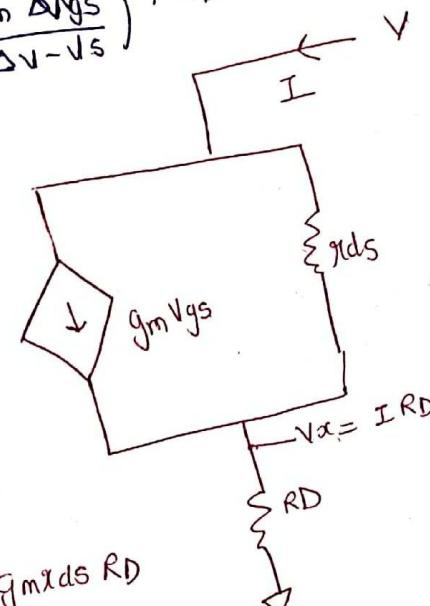
$$g_{ds} \| (g_m v_{gs}) + R_D$$

~~$$g_{ds} \| \frac{g_m \Delta I_D}{\Delta V - V_S} + R_D$$~~

~~$$\begin{aligned} & g_m V_x + g_{ds} \\ & \cancel{g_m V_x + g_{ds}} \\ & \cancel{g_m V_x + g_{ds}(\Delta V - V_x)} \\ & \cancel{g_m V_x + g_{ds}(\Delta V - V_x)} \end{aligned}$$~~

$$g_m (-I_R) + \frac{V - I_R D}{g_{ds}} = I$$

$$\frac{V}{I} = g_{ds} + R_D + g_m g_{ds} R_D$$

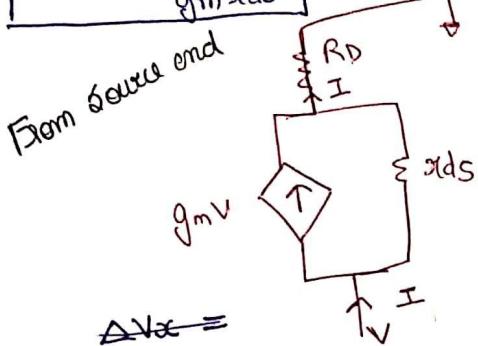


$$\Delta V_x = \Delta I R_D$$

$$= \frac{\Delta V}{\text{Resistance}}$$

$$= \frac{\Delta V R_D}{g_m R_D I_{DS}}$$

$$\Delta V_x = \frac{\Delta V}{g_m I_{DS}}$$

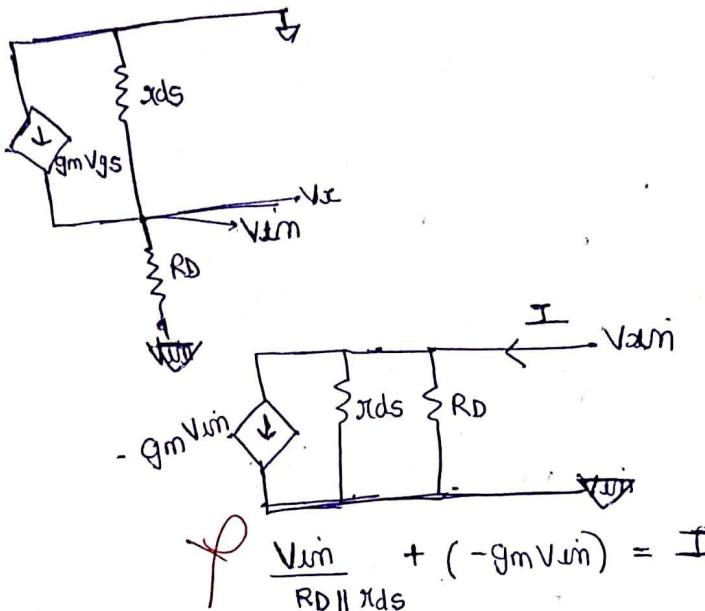


$$I = g_m V + \left(\frac{V - I R_D}{I_{DS}} \right)$$

$$\frac{V}{I} = \frac{1}{g_m} + \frac{R_D}{g_m I_{DS}}$$

From source

Resistance gain



$$V_{in} \left(-g_m + \frac{1}{R_D \parallel I_{DS}} \right) = I$$

$$\frac{V_{in}}{I} = -g_m + \frac{I_{DS} + R_D}{I_{DS} R_D}$$

$$R = \frac{I_{DS} R_D}{I_{DS} + R_D - g_m I_{DS} R_D}$$

$$R = \frac{1}{\frac{1}{R_D} + \frac{1}{I_{DS}} - g_m}$$

Limited gain because overall resistance = $R_S \parallel$ huge resistance

It limits gain

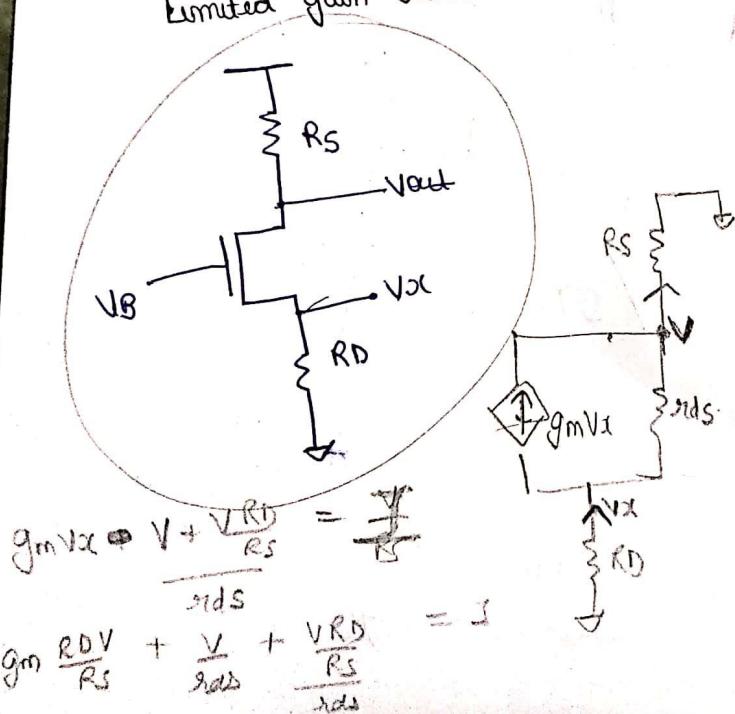
$$\frac{-R_S}{g_m + R_D}$$

$$A_V = -\frac{R_S \times g_m}{(R_D \parallel I_{DS}) g_m}$$

$$A_V = -\frac{R_S}{R_D \parallel I_{DS}}$$

$$\frac{V}{R_S} = -\frac{V_{xL}}{R_D}$$

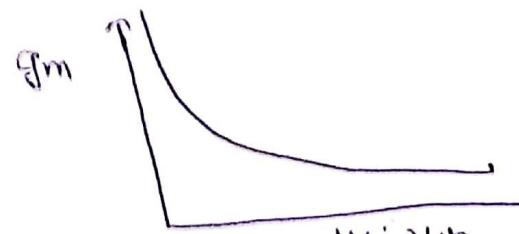
$$V_{xL} = -\frac{V_{RD}}{R_S}$$



$$g_m = \sqrt{2\beta I_D}$$

$$g_m = \beta V_{DS} \quad \left. \right\} \text{when } I_D \text{ is constant how does } g_m \text{ varies}$$

$$g_m = \frac{\partial I_D}{V_{DS}}$$



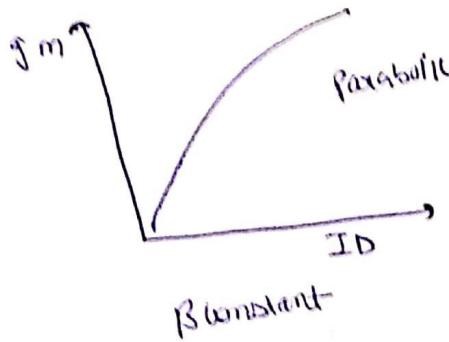
I β V_{DS}

$$I \propto \beta (V_{DS} - V_{th})^2$$

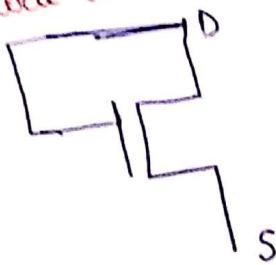
if V_{DS} changes in \uparrow linearly
 $\beta \downarrow$ with square relation to have I constant

$g_m \downarrow$ as $\beta \downarrow$ with square relation & $V_{DS} \uparrow$ linearly

III w/L constant, $I \uparrow$ linearly

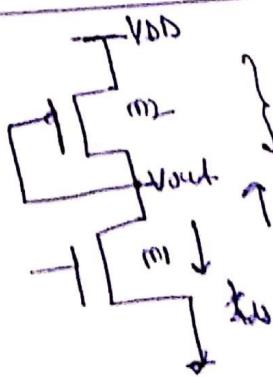


Diode Connected Load



$$V_{DS} > V_{th}$$

as $V_{DS} \uparrow$
 \sqrt{gm} changes
 current change drastically
 saturation current
 So less resistance
 $\frac{1}{gm}$



$\frac{1}{gm_p}$ low resistance
 $\frac{1}{R_D}$

$$\Delta V = g_m R_{out}$$

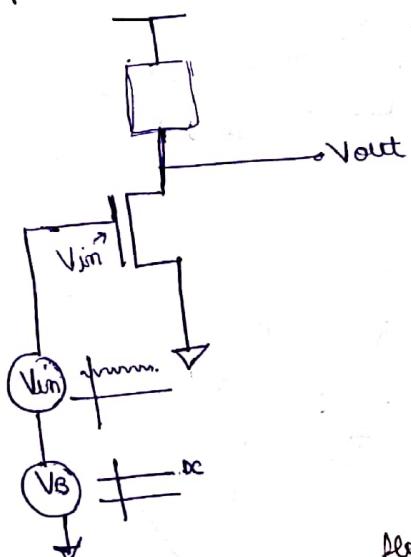
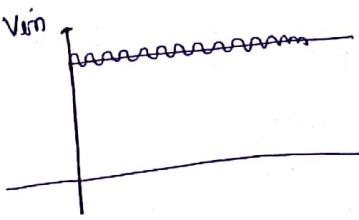
$$= \left(\frac{1}{gm_p} + \frac{1}{R_D} \right) R_{out}$$

$$= -g_m \left(\frac{1}{gm_p} + \frac{1}{R_D} \right)$$

only n_{mos} form R_{out}
 P_{nmos} is shorted
 that is first gate
 shorted with
 drain.

→ Check diode connected load impedance
 Why $\Delta V = \frac{R_D}{\text{gain}}$

6/2/19



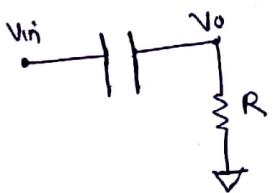
g_m BJT also capacitor is used
 so as to store DC value and
 pass the remaining variation
 (small signal),
 and thus it will not affect biasing.

g_m mosFET if external biasing not done
 then V_B (dc) can provide biasing

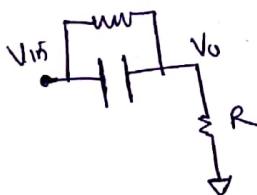
floating capacitance
 v_1 v_2
 This capacitance provides zero
 at DC

v_1
 Provides Pole
 at DC

$$\frac{V_o}{V_{in}} = \frac{R}{R + \frac{1}{j\omega C}} = \frac{\frac{R}{j\omega C}}{\frac{R}{j\omega C} + 1}$$



Zero at DC



Zero at some other value

Zeros available when more than one path present

References are also called rails

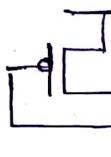
Load

$$R_D = -g_m (R_D \parallel \gamma_{ds})$$

(DC gain)

 R_S (active resistance) $\Rightarrow -g_m (R_S \parallel \gamma_{ds})$

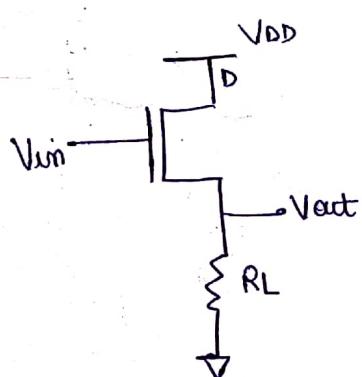
 $\Rightarrow -g_m (\gamma_{ds,p} \parallel \gamma_{ds,n})$

 Diode $\Rightarrow -g_m \left(\frac{1}{g_{mp}} \parallel \gamma_{ds,p} \parallel \gamma_{ds,n} \right)$

Source degeneration \Rightarrow

$$\frac{-R_D}{\frac{1}{g_m} + R_S} \approx \frac{-R_D}{R_S}$$

Common Source \rightarrow Common emitter
Common Drain \rightarrow Common collector

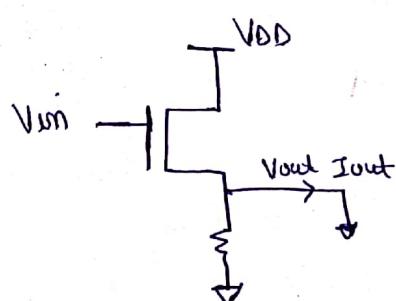


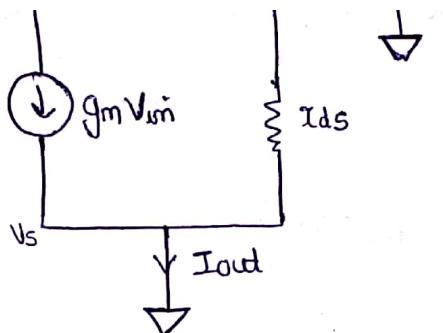
gain high when current constant
when it is not so gain
cannot be high

$$R_L \parallel \left(\frac{1}{g_m} \parallel \gamma_{ds} \right) \approx R_L \parallel \frac{1}{g_m} \approx R_L \parallel \frac{1}{(g_m + g_{mb})}$$

due to Body effect

as R_L less, and change in V_{in}





$$\frac{I_{out}}{V_{in}} = g_m$$

Drain Amplifier gain

$$A_V = \frac{g_m}{g_m + g_{mb}} \quad \text{if } R_L \rightarrow \infty$$

Source follower (or depends on source)

If $A_V = 1$ & V_{in} changes by ΔV
then V_{out} changes by ΔV

emitter follower

transconductance
amplifier to
voltage amplifier

1/p Current = 0
 $Z_{in} \rightarrow \infty$

For no loading (for voltage to voltage) Source follower

$Z_{in} \rightarrow \infty$

$Z_{out} = 0$

Voltage to current amplifier (Transconductance amplifier)

$Z_{in} \rightarrow \infty$

$Z_{out} \rightarrow \infty$

e.g. Common Source amplifier

Current to voltage (Transimpedance amplifier)

Common source amplifier followed by Source amplifier follower \Rightarrow can be used as voltage amplifier

will transfer
 ΔV by CSA with
low impedance

Problem

Non linearity due to g_m , g_{mb}
gain is 1/p dependent
driving capability poor as $g_m < 1$

$I = \frac{\beta}{2} (V_{DS} - V_{th})^2$

$$V_{in} = V_{DS} = V_{th} + V_{osat} = V_{th} + \sqrt{\frac{2ID}{\beta}}$$

Connecting RL swing \pm

$$\begin{aligned} V_{in} &= V_{DS} + IDRL \\ &= V_{th} + V_{osat} + IDRL \\ &\Rightarrow \text{"ip swing less"} \end{aligned}$$

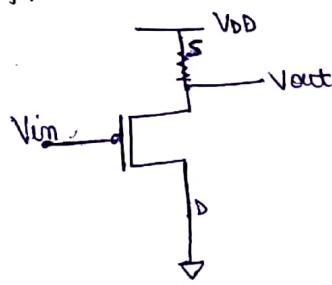
upper limit is fixed as not dependent on source.

Source follower can be used as level shifter

input gets shifted by V_{osat} value
down shifter

$$V_{in} - V_{DS} = V_2$$

How will be the pmos variant of this system



Non Linear
swing less
Cannot be used as gain circuit

$$\begin{aligned} V_{out} &= V_{in} + V_{SG} \\ V_2 &= V_{in} + V_{SG} \end{aligned}$$

up shifter

$$\begin{aligned} V_{DD} - V_{out} &= R_L I_D \\ V_{DD} - (V_{in} + V_{SG}) &= R_L \frac{\beta}{2} (V_{SG} - V_{th})^2 \end{aligned}$$

V_{SG} is itself function of current

$$i = \frac{V_{DD} - V_{in} - V_{SG}}{R_L}$$

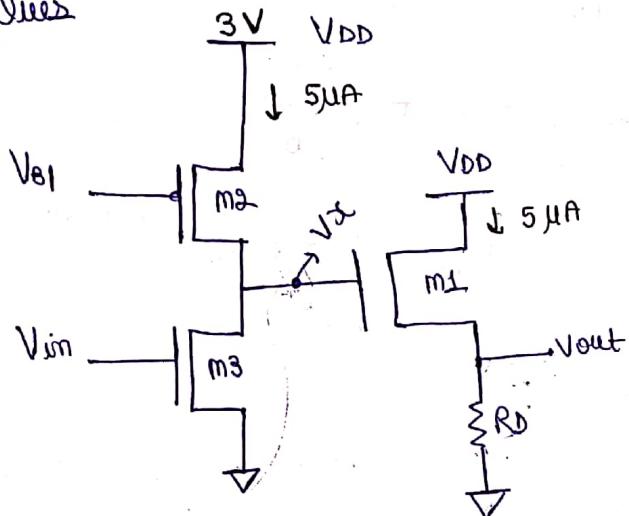
Put some value of V_{SG}

$$V_{DD} - IDRL = V_{SG} - V_{in} = 0$$

$$V_{DD} - IDRL - \left(\sqrt{\frac{2ID}{\beta}} + |V_{th}| \right) - V_{in} = 0$$

Find ID or Vin Whatever is varying

Ques



$$\lambda = \frac{0.5}{0.5} \text{ V}^{-1}$$

$$(\frac{W}{L}) = 1$$

$$V_{thp} = |V_{thn}| = 0.5$$

$$V_{min, min - max} = ?$$

$$V_{out, min - max} = ?$$

$$VDD = 3V$$

Small signal gain = ?
(DC)

$$R_D = 100k\Omega$$

$$\gamma = 0$$

no body effect

$$m_{n,ox} = 200 \mu A/V^2$$

$$m_{p,ox} = 100 \mu A/V^2$$

$$1^{\text{st}} \text{ half gain} = -g_m (\lambda_{dsn} \| \lambda_{dsp})$$

$$= -g_{m1} \left(\frac{1}{\lambda_{ID}} \| \frac{1}{\lambda_{ID}} \right)$$

$$= -\frac{g_{m1}}{2\lambda_{ID}}$$

$$= \left(\frac{1}{2 \times 0.5 V^{-1} \times 5 \times 10^{-6} A} \right) g_{m1}$$

$$= \left(\frac{10^6}{5} \right) g_{m1}$$

$$= -(200k\Omega) g_{m1}$$

\rightarrow Unfixed

$$g_{m1} = \sqrt{2BID}$$

$$= \sqrt{2 \times 200 \frac{\mu A}{V^2} \times 1 \times 5 \times 10^{-6} A}$$

$$= \sqrt{2 \times 200 \times 5 \frac{A^2}{V^2}}$$

$$= 10^{-6} \sqrt{2000} \frac{A^2}{V^2}$$

$$= 20\sqrt{5} \frac{\mu A}{V}$$

$$\approx 45 \frac{\mu A}{V}$$

$$24 \times 5 \times 10^{-6}$$

$$AV_1 = \frac{-45 \times 10^{-6} \times 2 \times 10^5}{-9}$$

2nd part

$$\frac{1}{g_m} \parallel 400\text{ k}\Omega \parallel 100\text{ k}\Omega$$

gds

$$R_{out} = \frac{\frac{1}{45\text{ }\mu\text{A}} \parallel 400\text{ k}\Omega \parallel 100\text{ k}\Omega}{\frac{10^6}{45} \parallel 400\text{ k}\Omega \parallel 100\text{ k}\Omega}$$
$$22\text{ k}\Omega \parallel 400\text{ k}\Omega \parallel 100\text{ k}\Omega$$
$$22\text{ k}\Omega \parallel 80\text{ k}\Omega$$

$$\approx 20\text{ k}\Omega$$

$$\frac{400 \times 10^3}{500} \text{ k}\Omega$$
$$\frac{80 \times 22}{102.51} \text{ k}\Omega$$

$$A_{v2} = g_m \times R_{out}$$
$$= 45\text{ }\mu\text{A} \times 20\text{ k}\Omega$$

$$\approx 0.9$$

$$\text{gain overall} = -g \times 0.9$$
$$= [-8.1]$$

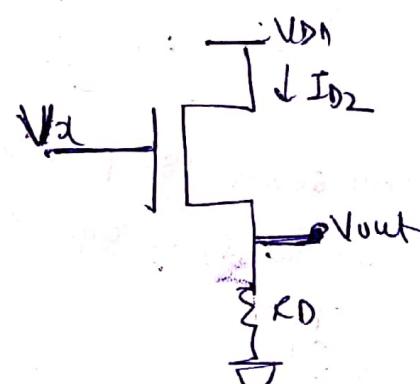
Sat Cond

$$V_{x_{min}} = V_{in} - V_{thn} = \sqrt{\frac{2ID}{B_n}}$$

$$V_{x_{max}} = V_{DD} - \sqrt{\frac{2ID}{B_P}}$$

$$V_x - V_{out} = V_{ns}$$

$$V_x = V_{out} + V_{thn} + \sqrt{\frac{2ID_2}{B_n}}$$



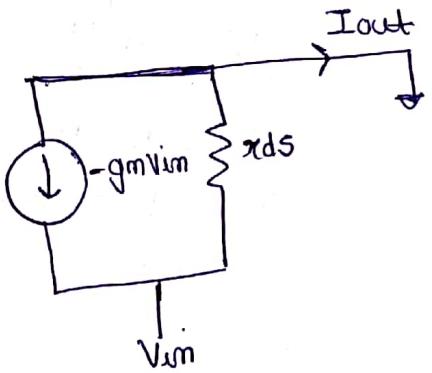
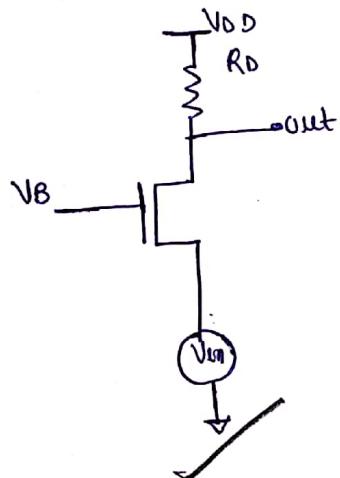
1a/2/19

Common Gate Topology

Gate Common

V_P & O/P at one of drain & source terminal
Gain will be high if O/P from drain and low when O/P from source (low impedance)

$$R_{out} = \frac{1}{g_m} || R_D$$



$$g_m V_{in} + \frac{V_{in}}{r_d.s} = I_{out}$$

$$\frac{V_{in}}{I_{out}} = \frac{1}{\frac{1}{r_d.s} + g_m}$$

$$\approx \frac{1}{g_m}$$

$$A_V = \left(\frac{1}{g_m} \right) (R_D || r_d.s)$$

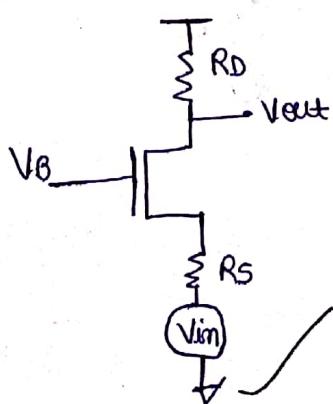
including body effect

$$A_V = g_m R_D$$

$$A_V = \frac{R_D || r_d.s}{g_m + g_{mb}}$$

$$A_V = (g_m + g_{mb}) R_D$$

g_m common source 180° phase shift, common gate 0° phase shift
 A resistance (internal) is required in series with V_{in} because without it V_{in} is not practical

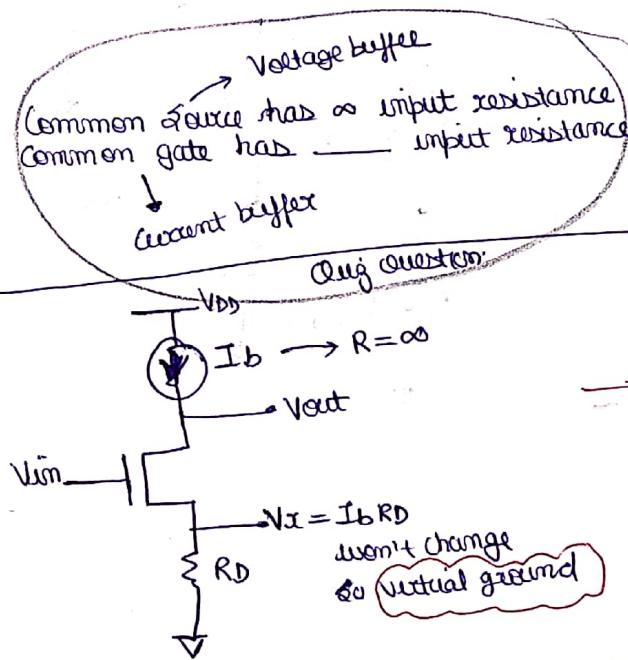


gain will be in phase unlike that of source degeneration.

$$A_V = \frac{R_D}{\frac{1}{g_m} + R_S} \approx \frac{R_D}{R_S}$$

Current amplifier
with current gain 1

Which is better common source or common gate?



$$AV = -g_m \frac{R_D}{L}$$

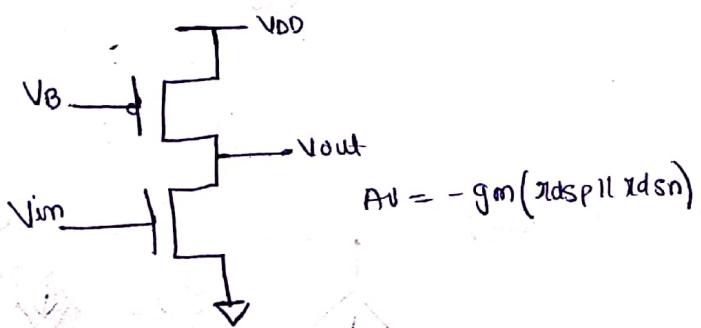
If we fix I_D How to achieve high gain??

If through R_{out} , how to achieve high R_{out} ??

If g_m changed

$$g_m \propto \sqrt{\frac{W}{L}}$$

if $\frac{W}{L}$ ↑ by 100 then g_m ↑ by 100
so not good approach.



how to ↑ this gain further

inherent gain

$$AV = -g_m \frac{R_D}{L}$$

$$\frac{R_D}{L} \propto \sqrt{\frac{L}{W}} \approx \frac{1}{L}$$

$$g_m \propto \frac{W}{L}$$

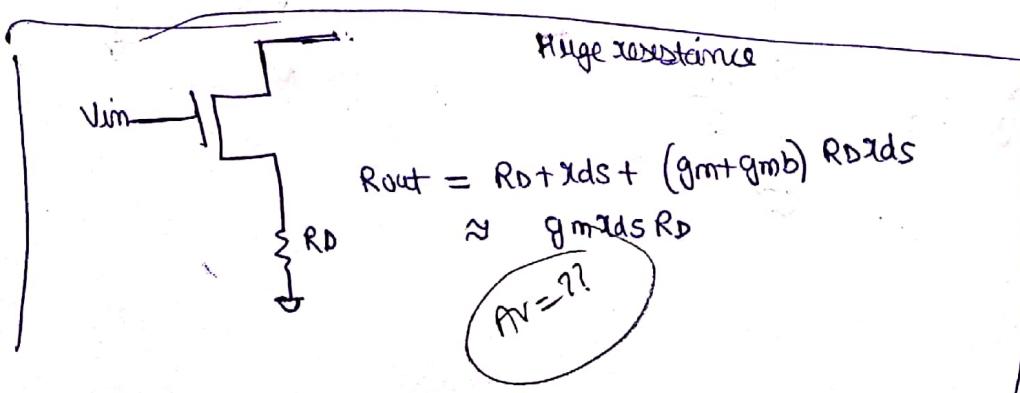
$$\frac{R_D}{L} \propto \frac{L^2}{W}$$

$$AV \propto L$$

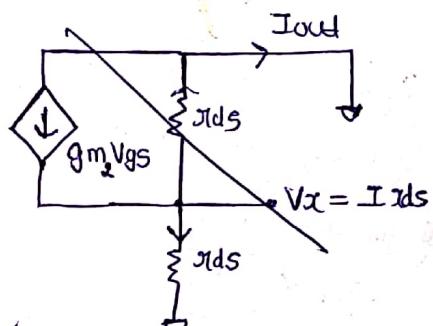
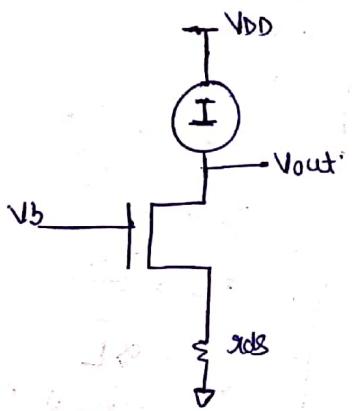
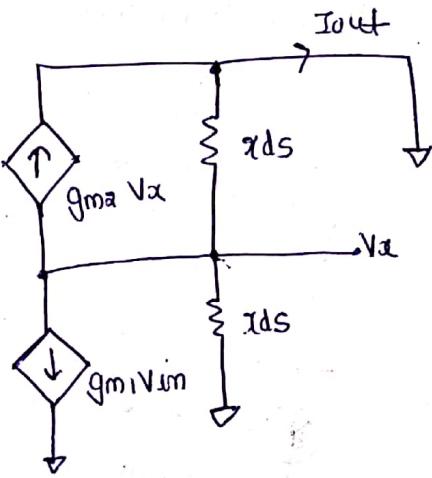
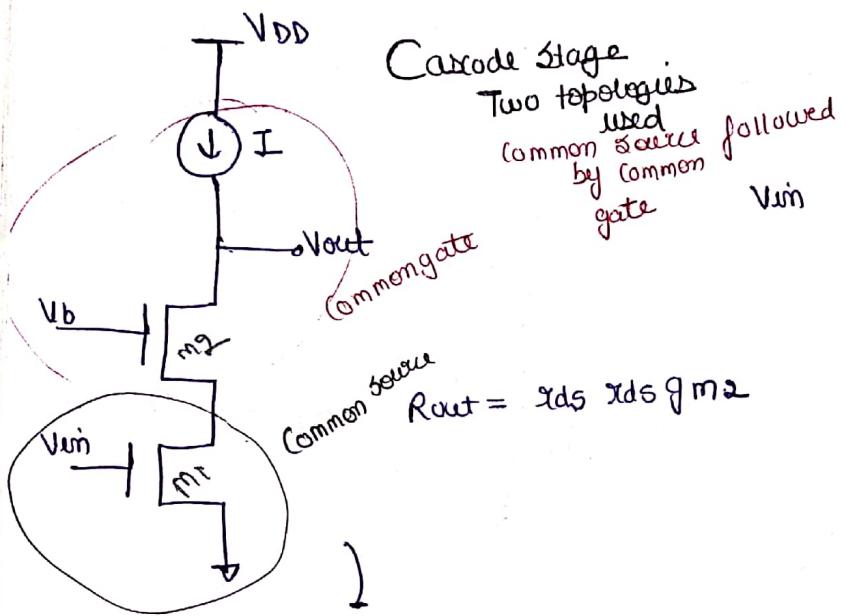
whereas if R_D present

$$g_m \propto \frac{W}{L}$$

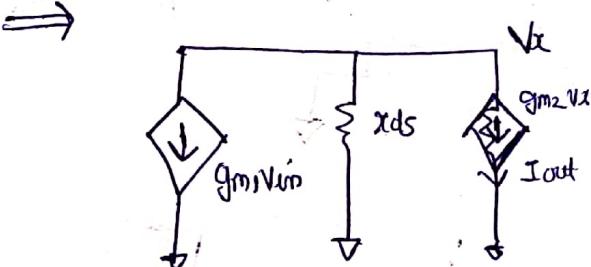
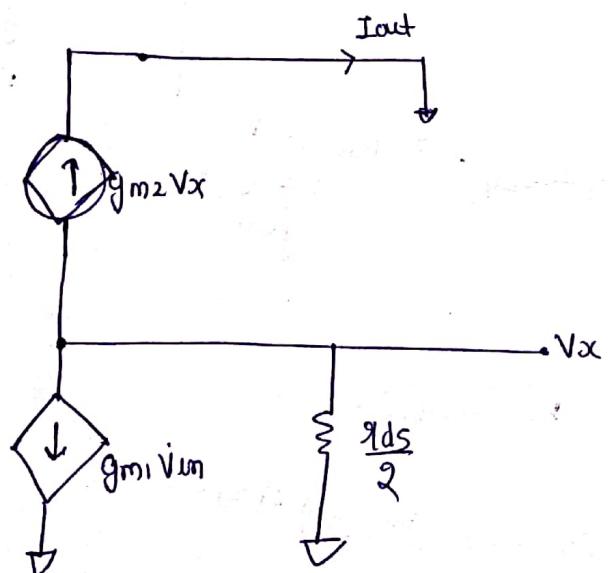
$$AV \propto W$$

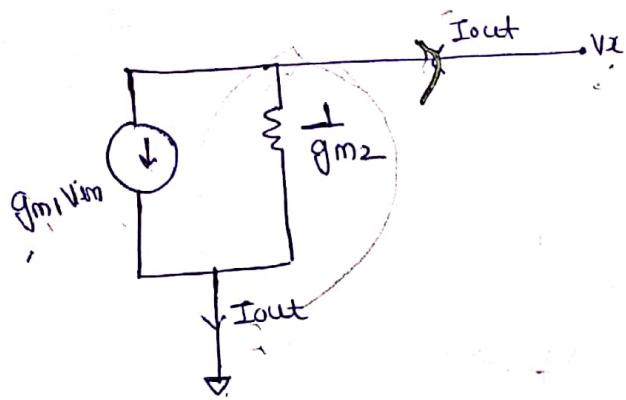


To ↑ gain further



$$I_{out} = -\frac{I_{out} r_{ds}}{r_{ds}} + g_m (-I_{out} r_{ds})$$



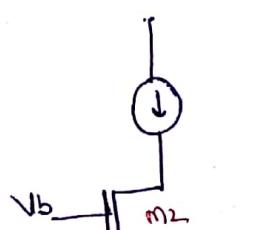


$$G_m = -g_{m1}$$

$$AV = -g_{m1} g_{m2} \chi_{ds2}$$

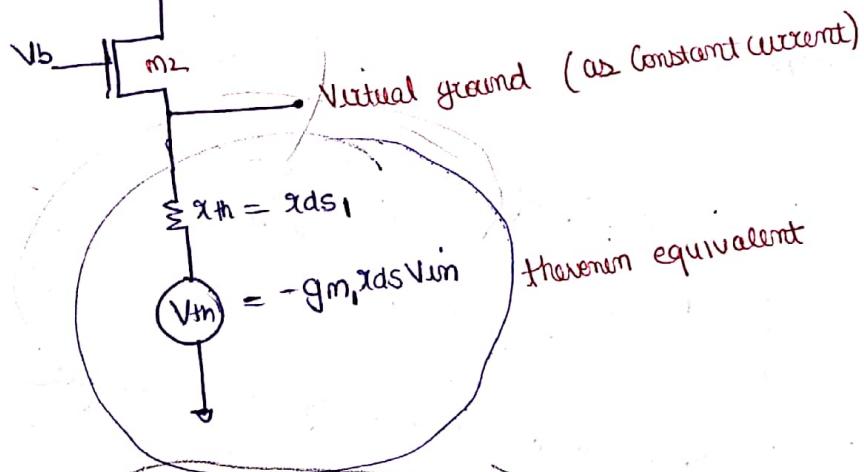
Very high gain

Another method to solve this



$$AV = \underline{g_{m2} \chi_{ds2}} \quad \text{for upper part}$$

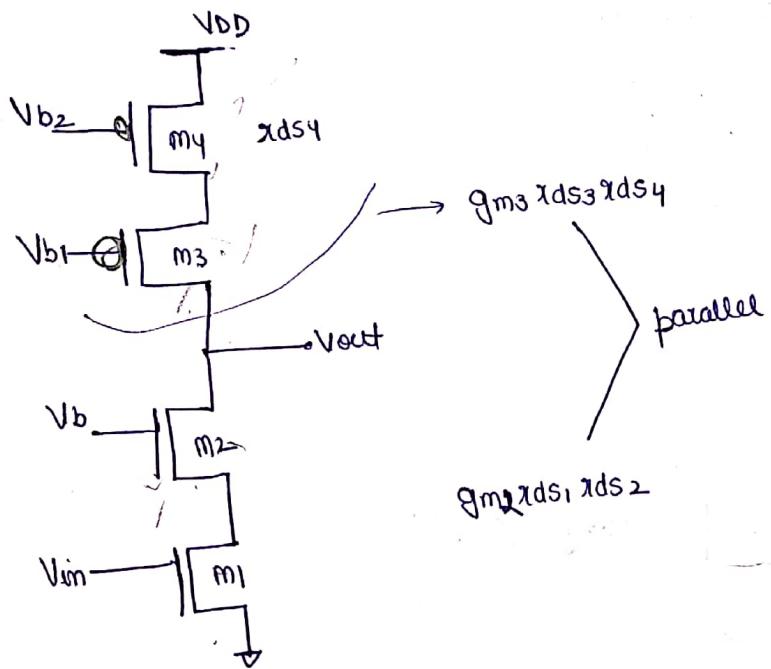
why not -ve?



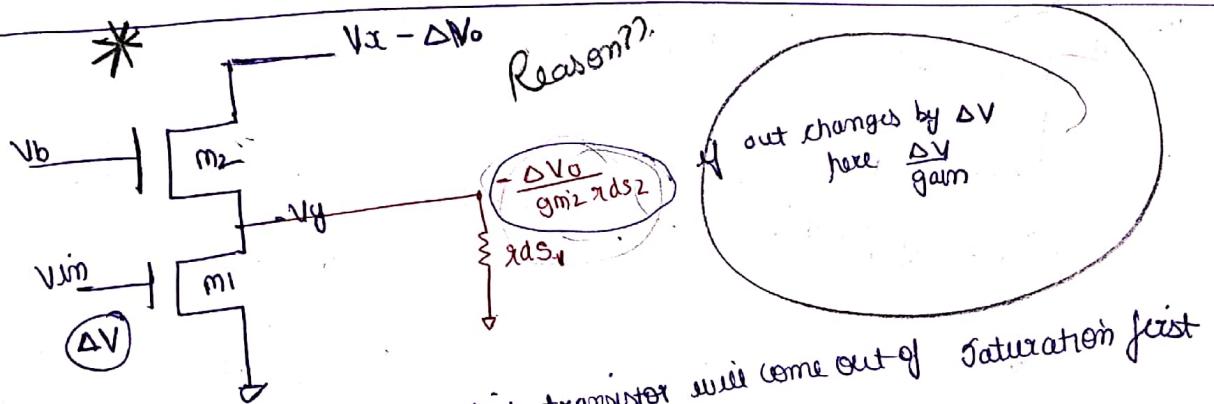
thenvenin equivalent

$$\frac{V_o}{-g_{m1} \chi_{ds1}, V_{in}} = g_{m2} \chi_{ds2}$$

$$\frac{V_o}{V_{in}} = -g_{m1} g_{m2} \chi_{ds1} \chi_{ds2}$$



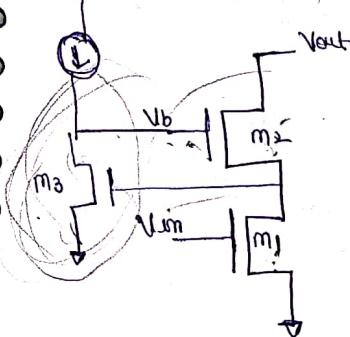
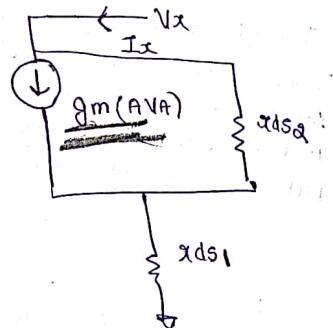
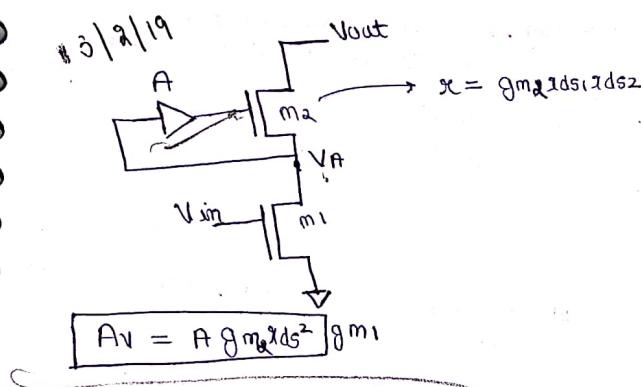
current source in series not practically possible
so circuit not realizable
gain too high



If V_{in} changes by ΔV then which transistor will come out of saturation first
Transistor out of saturation when $V_{DS} < V_{BS}$
 V_{DS} of M_2 drops more so will come out of saturation

Cascode → highest gain
→ highest impedance

3/2/19



provides gain \leftarrow Amplifier Stage
provides Rout \leftarrow Load Stage
Biasing

$$Av = gm_1 (A gm_2 r_{ds2})$$

$$= gm_1 (gm_3 r_{ds} gm_2 r_{ds2})$$

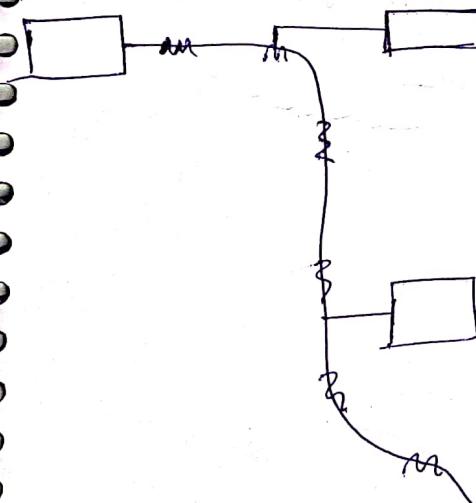
$$Av = gm_1 gm_2 gm_3 r_{ds1} r_{ds2} r_{ds3}$$

$$R = \frac{V_s}{I}$$

→ Resistance drop is different at each node
→ We cannot predict what voltage is going inside as voltage drop is unpredictable
so it is not recommended to supply voltage from external source.

all currents and voltages will be generated inside only except signals which are given at input:

To generate current & voltage externally
Biasing is studied



Once I_o is either generated internally or externally, it is further replicated. Temperature is a problem. It is not constant in real life. It would affect resistance which would further change current. But we want this reference current I_o to be constant. Till now none of circuits are completely temp independent.

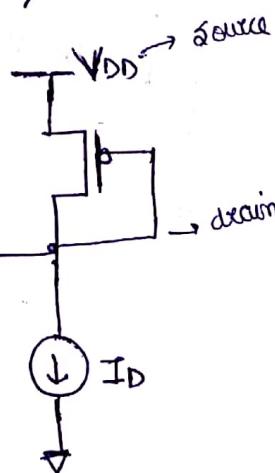
Given $V_{DD} = 1.8$. Generate 1V from it.

(if we make voltage divider using resistance
it will offer $\pm 20\%$ tolerance.
i.e. $\frac{1.8 \pm 0.7}{2}$,
huge variation)

$$V_{DS} = V_{GS} \text{ (if drain & gate sorted)}$$

$$V_{GS} = V_{DSat} + V_{Th}$$

$$V_{DD} - (V_{DSat} + V_{Th})$$



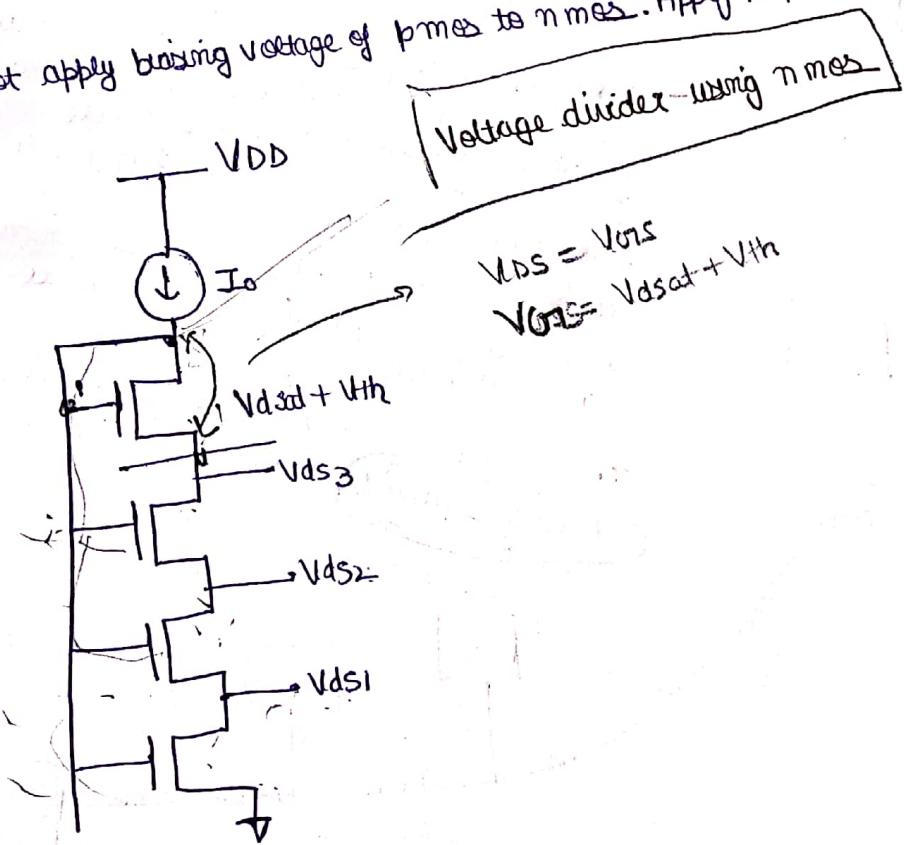
~~too~~
in saturation as D & G sorted.

Do not apply biasing voltage of pmes to nmes. Apply to pmes biasing points only.

Voltage divider using nmes

$$V_{DS} = V_{GS}$$

$$V_{GS} = V_{DSat} + V_{Th}$$

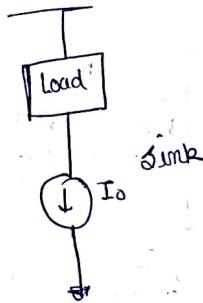
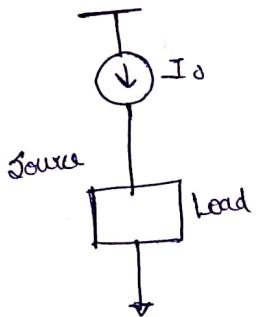


Current Source

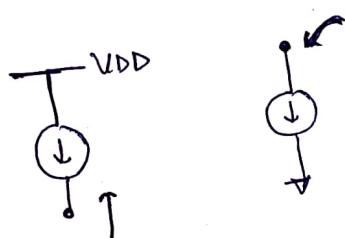
In case of Voltage no loading at gate as ∞ input impedance
but current is not applied at gate
it is applied at source or drain
so what should be properties to avoid loading
 \Rightarrow I_o generate $2I_o, 3I_o, \dots$

Current mirrors (with I_o generate $2I_o, 3I_o, \dots$)

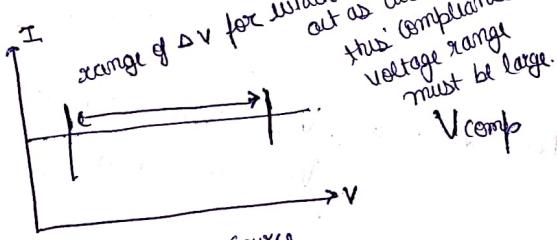
Properties of Current Source → Input impedance ∞
i.e. ~~current source~~ current source resistance $\rightarrow \infty$
 \Rightarrow Current constant



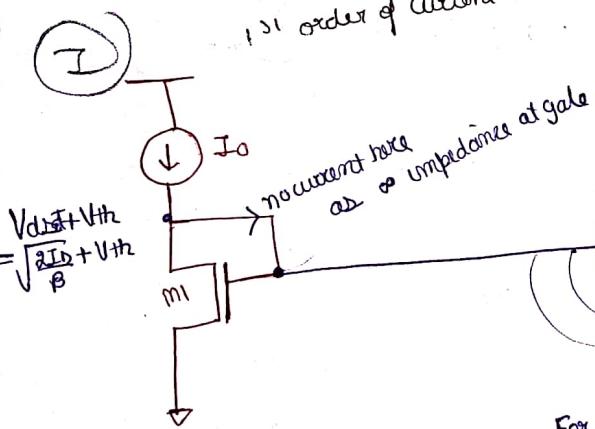
- ① $\rightarrow R \rightarrow \infty$
- ② $\rightarrow V_{comp} \rightarrow$ Range must ↑
- ③ \rightarrow mirror accuracy
(we should not get 4.5 V for 5V)



1st order of current mirror



Ideal current source



Current depends on

V_{th}

V_{DS} → same for both

V_{DS}

B

For both transistors $V_{DS} \approx 0$
current is strong function of V_{DS}

Now how to make current in $m_2 = 5I_o$
For m_2 in saturation ??

m_2 in short channel, as $V_{DS} \uparrow$, current \uparrow , seen in saturation

\uparrow Velocity \uparrow
 $V_{DS} \uparrow \Rightarrow E \uparrow \Rightarrow$ Velocity $\uparrow \Rightarrow$ Current \uparrow

$$V_{D2sat} = \mu E \\ E = \frac{V_{sat}}{d}$$

$V_{D2sat} = \mu E$
 $E = \frac{V_{sat}}{d}$

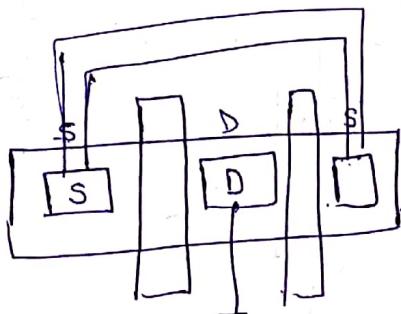
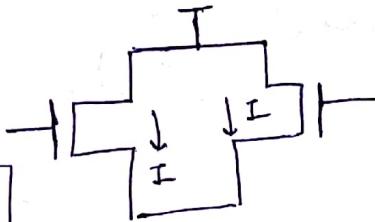
For short channel effects, Velocity saturation will occur before only

If V_{th} different, current different so we need to fix threshold voltage.

What to do, to increase current but don't change V_{th} .

→ apply transistor in parallel
→ double width

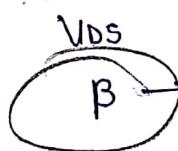
transistor in series → double length
never increase width directly as it will affect V_{th} .



draw common
both transistor in parallel.

Now we have $V_{ds} \rightarrow$ same for both

$V_{th} \rightarrow$ constant



V_{ds} → keep some done.
mirror not accurate as V_{ds} not same for both so slight change in current.
as x_{ds} not so much high

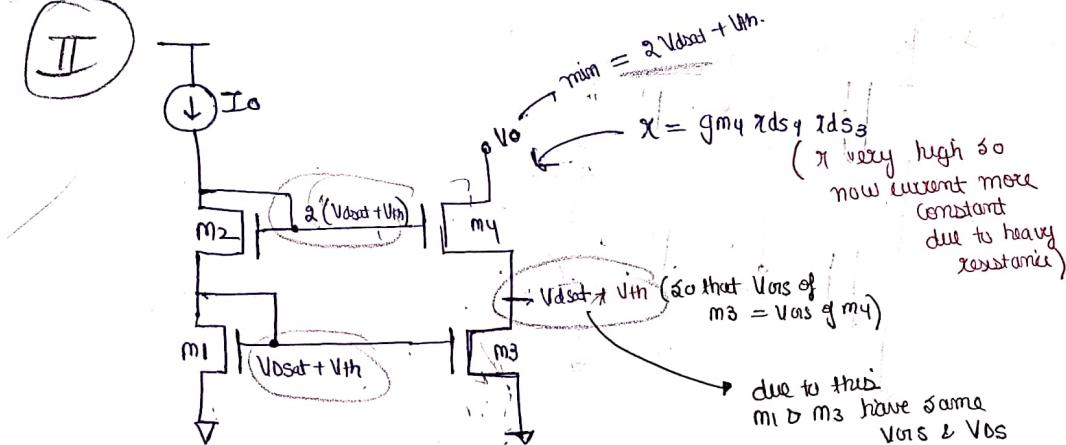
mirror → $V_{ds1} \neq V_{ds2}$

$x_{out} \rightarrow x_{ds}$

V_c range →

2nd Variant of Current mirror

(II)



Same current in m_1 & m_2 so V_{ds} same for both.

$$V_{ds} \text{ for } m_1 = V_{dsat} + V_{th}$$

$$\begin{aligned} V_o &> V_{th} - V_{th} \\ V_o &> 2V_{dsat} + 2V_{th} - V_{th} \\ V_o &> 2V_{dsat} + V_{th} \end{aligned}$$

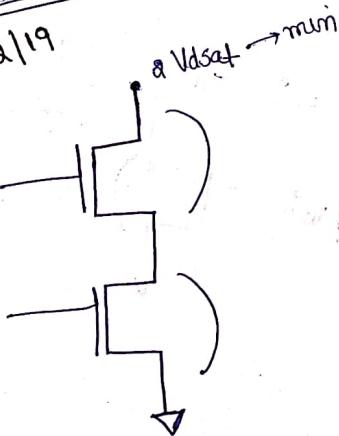
m_4 comes out of saturation first
So if m_4 in Sat $\Rightarrow m_3$ definitely in saturation

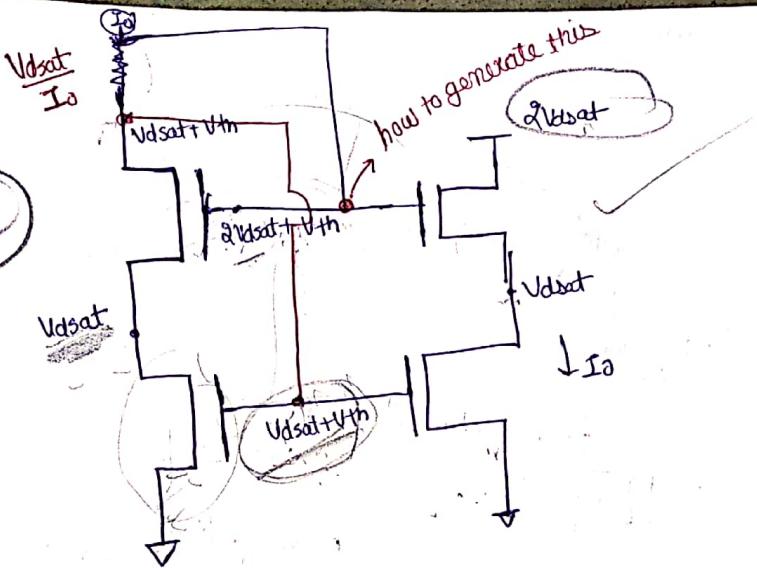
take $V_{dsat} = 200 \text{ mV}$, $V_{th} = 0.6$

here range 0-6
previously 1-8
 V_c range has decreased

- ① huge resistance
- ② exact replica
- ③ we are losing in terms of Complementary range.

14/2/19



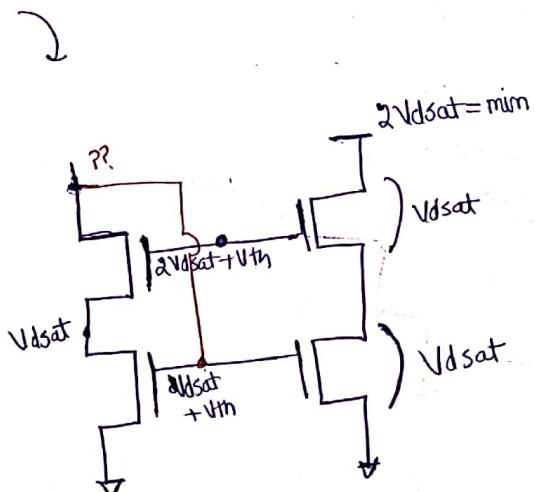


A device with $\frac{1}{4}$ th time scaling will generate $\alpha V_{dsat} + V_{th}$

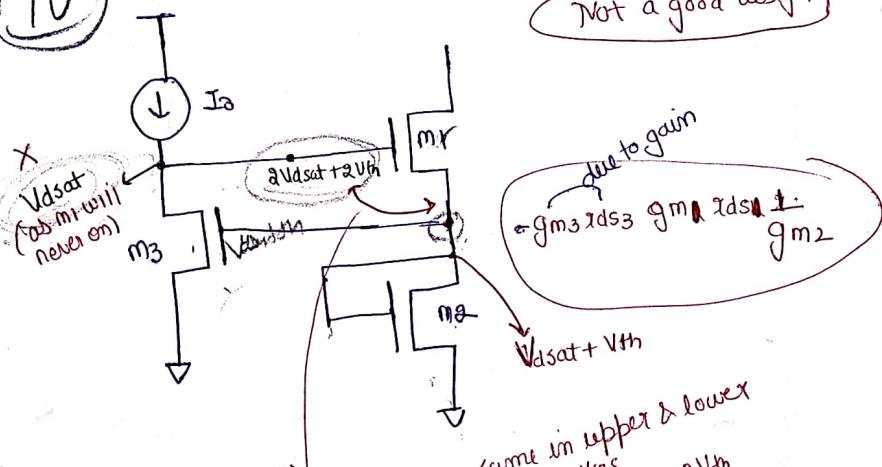
$$R = \sqrt{\frac{2ID}{\beta}} = \sqrt{\frac{2IDL}{W}} = \frac{2IDL}{W}$$

$$V_{dsat}' = \sqrt{\frac{2IDL'}{w'}} = \sqrt{\frac{1}{4}W} = \frac{1}{2}V_{dsat}$$

Compliance Voltage ↑
resistance ↑
 V_{gs} Same for both
 V_{ds}



IV

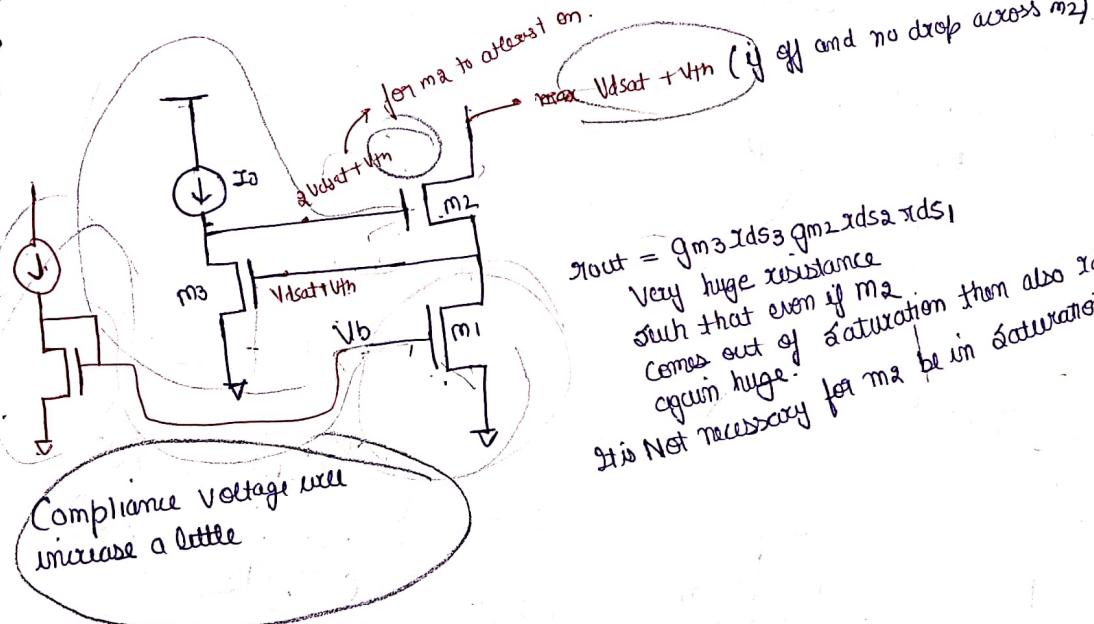


Not a good design

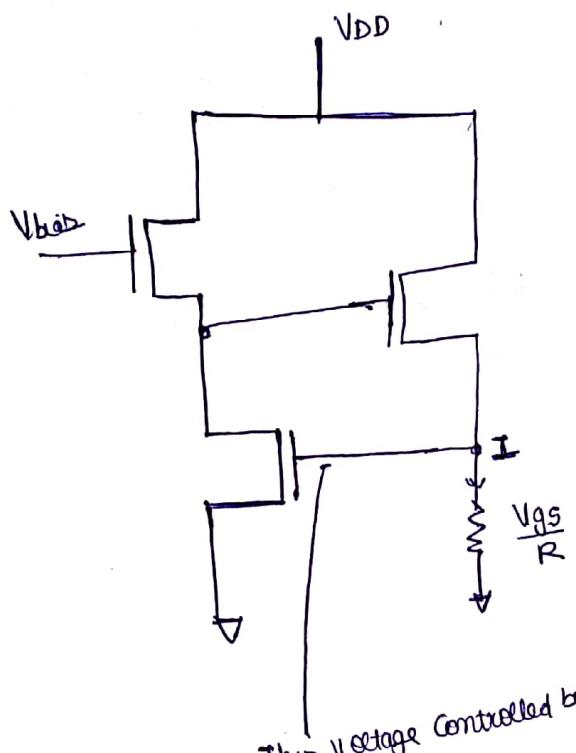
$$\text{due to gain} \approx g_{m3} r_{ds3} g_{m1} r_{ds1} \frac{1}{g_{m2}}$$

$$V_{dsat} + V_{th}$$

To keep current same in upper & lower both I should have same V_{ds}
for this V_m for upper = $2V_{dsat} + 2V_{th}$
but it is very huge voltage.



$r_{out} = g_{m3} r_{ds3} g_{m2} r_{ds2} r_{ds1}$
Very huge resistance
such that even if m_2 comes out of saturation then also $r_{out} = g_m r_{ds}^2$
again huge.
It is not necessary for m_2 to be in saturation



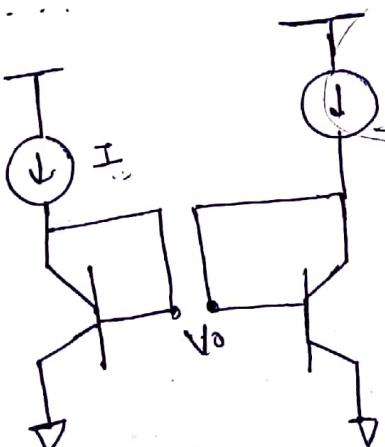
Thus voltage controlled by V_{bias} and this further controls Voltage drop across R

metal
With \uparrow in temperature, vibrations \uparrow in a lattice, \uparrow of prob of collision \uparrow , Velocity \downarrow , $R \uparrow$
semicon
With \uparrow in temp, Resistance \uparrow (for some time). After this it behaves as metal until $R \uparrow$



But we want temperature free voltage.

Bandgap . . .



$$I = I_0 \left(e^{\frac{V_{BE1}}{kT}} - 1 \right) \quad \text{--- (1)}$$

$$nI = I_0 \left(e^{\frac{V_{BE2}}{kT}} - 1 \right) \quad \text{--- (2)}$$

$$n I_0 e^{\frac{V_{BE1}}{kT}} = I_0 e^{\frac{V_{BE2}}{kT}}$$

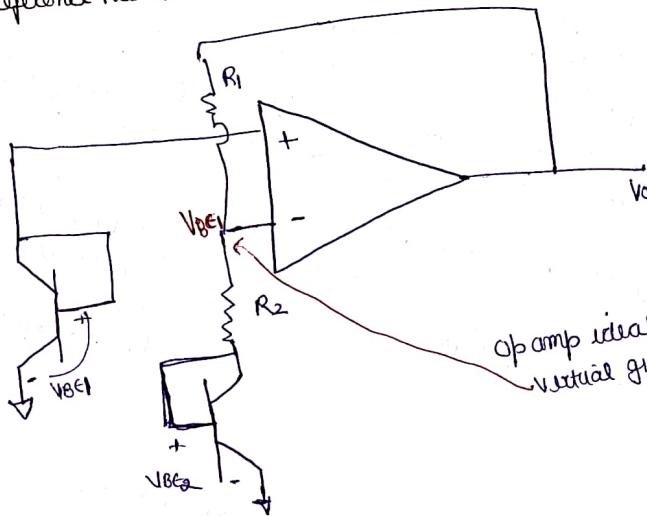
$$n = e^{\frac{V_{BE2} - V_{BE1}}{kT}}$$

$$V_T \ln(n) = V_{BE2} - V_{BE1}$$

$$\frac{kT}{q} \ln(n) = V_{BE2} - V_{BE1}$$

q

V_{BE} have -ve coefficient w.r.t Temp.
 But $(V_{BE2} - V_{BE1})$ has +ve coefficient
 With help of these two constant coefficient can be generated
 Band gap reference ~~Resistance~~ Circuit



op-amp ideal, -ve feedback thru
 virtual ground

$$\frac{V_o - V_{BG1}}{R_1} = \frac{V_{BE1} - V_{BE2}}{R_2}$$

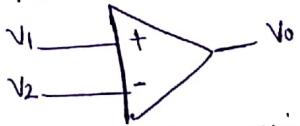
$$V_o = \frac{R_1}{R_2} \left(\frac{R_2 V_{BG1}}{R_1} + \frac{V_{BE1} - V_{BE2}}{R_2} \right)$$

$$V_o = V_{BG1} + \frac{R_1}{R_2} (V_{BG1} - V_{BE2})$$

Temp coeff -ve
 & itself function
 of Temp

19/2/19

Differential Amplifier



Applies difference
b/w two input

So called differential amplifier

$$V_0 = (V_1 - V_2) A \rightarrow \text{small signal open loop gain}$$

like offset, distortion
like offset, component of noise

Why $(V_1 - V_2)$ is important?

- ① Will cancel out correlated component of noise
- ② Carry out various functionality

When noise at V_1 & at V_2 are highly non-correlated then we take Power of noise.

When noise non-correlated and we are doing $V_1 - V_2$ then Power of noise gets added at o/p.

If $A \rightarrow 10^6 = 20 \log(10^6) \text{ dB} = 120 \text{ dB}$
very huge
 $80 \text{ dB} \rightarrow 100 \text{ dB}$ is also very high

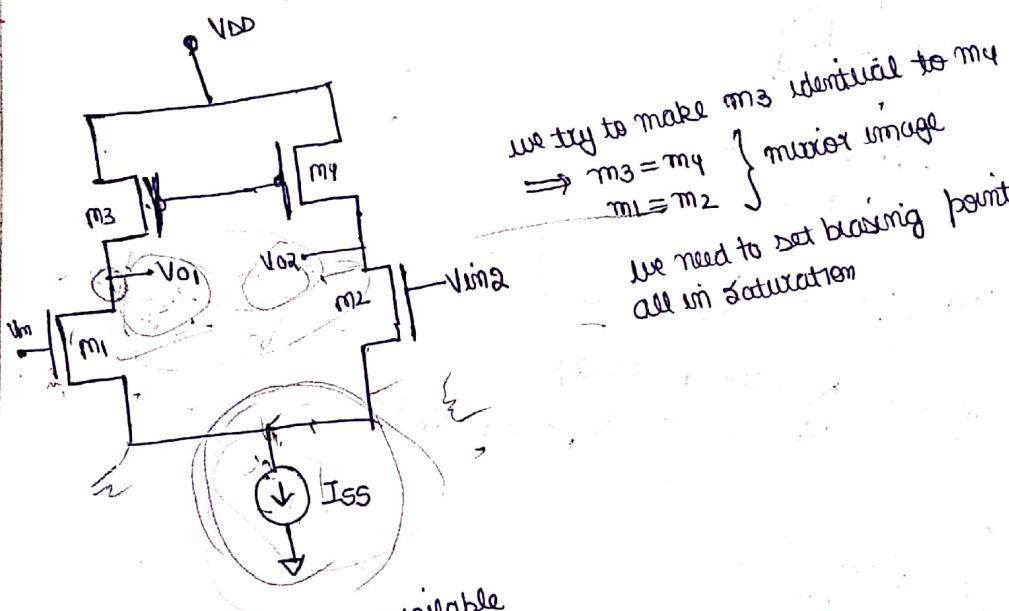
$$\text{Gain} \approx 100 \text{ dB}$$

$$B.W = 500 \text{ MHz}$$

Input impedance $\rightarrow \infty$, R_{in}

Output $\rightarrow \infty$

Power dissipation $\rightarrow \infty$



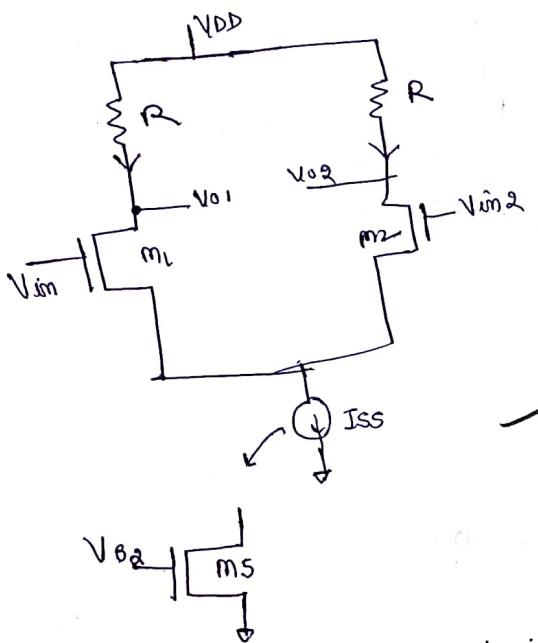
O/P offset when we are available
with same output with no input
i.e. $V_1 - V_2 = 0$

\Rightarrow (divide offset by gain) \rightarrow input offset
and apply its reverse at input

O/P offset = $V_{01} - V_{02} = V_0$

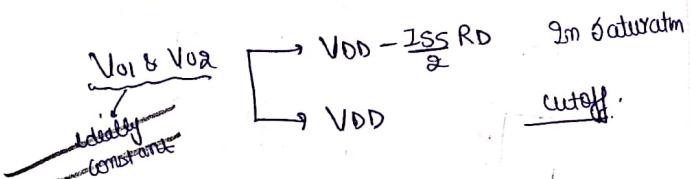
How to nullify this offset

when $V_{in1} = V_{in2} \Rightarrow V_0 = V_{01} - V_{02} = 0$, but $V_{01} \neq 0$, $V_{02} \neq 0$
such that transistor in saturation



$$V_{o1} = V_{o2} = V_{DD} - \frac{I_{ss} R_D}{2}$$

V_{o1} & V_{o2} do not change until transistor is in saturation as I_{ss} is constant current.



Find V_{in} min & max so that transistors remain in saturation

When $V_{in} \uparrow$, V_{o1} to keep V_{o1} same as current ideal, $V_S \uparrow \Rightarrow V_{BS}$ remains same
but now $V_{DS} \downarrow$

$$V_{DS} > V_{GS} - V_{th}$$

$$V_D > V_{G1} - V_{th}$$

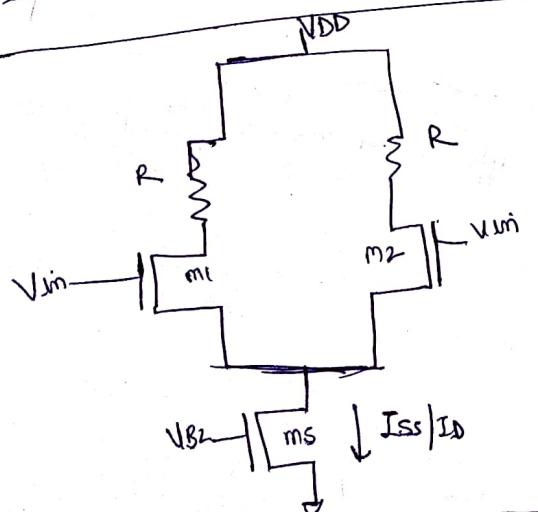
$$V_{DD} - \frac{I_{ss} R_D}{2} > V_{G1} - V_{th}$$

$$V_{G1} < V_{DD} + V_{th} - \frac{I_{ss} R_D}{2}$$

max value of V_{o1}

When $V_{in} \downarrow \Rightarrow V_S \downarrow$
 $\Rightarrow V_{BS}$ constant
 $\Rightarrow V_{DS} \uparrow$

as it is ideal case so
 V_{in} can go down upto zero



\propto less when L more

$\propto \frac{\Delta L}{L} V_{DS}$

$$V_{o1} < V_{DD} + V_{th} - \frac{I_{ss} R_D}{2}$$

Now if $V_{in} \downarrow$

for V_{BS} V_{BS} constant but now its
 $V_{DS} \downarrow$ so can come out of saturation

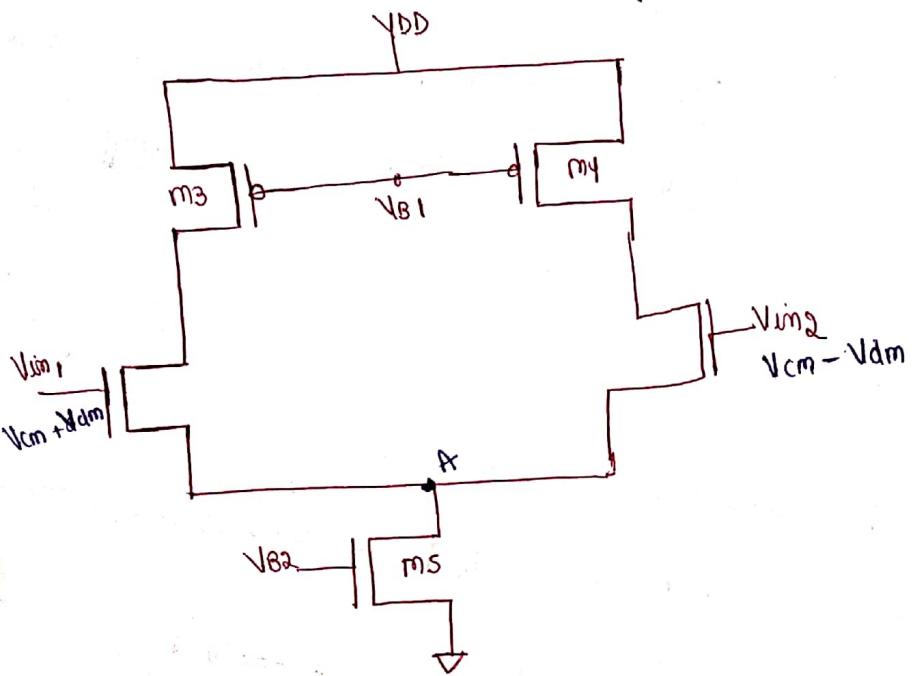
$$\begin{aligned} V_{in \min} &= V_{GS1} + V_{DS1} \\ &= \frac{\alpha I_{ss}}{2} + V_{th1} + \sqrt{\frac{2 I_{ss}}{\beta_1}} \end{aligned}$$

$$V_{in \ min} = \sqrt{\frac{I_D}{\beta_1}} + V_{in \ n} \sqrt{\frac{2 I_{ss}}{\beta_1}}$$

$V_{O1 \ max} \rightarrow V_{DD}$

$$V_{O1 \ min} = V_{DSAT1} + V_{DSAT5} = \sqrt{\frac{I_D}{B_1}} + \sqrt{\frac{2I_D}{B_5}}$$

Folding Structure



$$V_{in1} = \frac{V_{in1} + V_{in1}}{2} + \frac{V_{in2} - V_{in2}}{2}$$

$$V_{in1} = \frac{V_{in1} + V_{in2}}{2} + \frac{V_{in1} - V_{in2}}{2}$$

$$V_{in2} = \underbrace{\frac{V_{in1} + V_{in2}}{2}}_{V_{cm} \text{ (common mode)}} + \frac{V_{in2} - V_{in1}}{2}$$

differential mode signal

What will the o/p corresponding to V_{cm}

$\rightarrow V_o = 0 \ \& \ V_{O1} = V_{O2} \text{ for } V_{cm}$

$V_{O1} - V_{O2}$ will add up.

Corresponding to V_{dm} , V_{O1} & V_{O2} are opposite so their difference $V_{O1} - V_{O2}$ will add up.

$$\frac{1}{g_m} \parallel g_{ds} \rightarrow \frac{1}{g_m} + \frac{1}{g_{ds}} = \frac{1}{2g_m} \rightarrow \text{gain} = \frac{g_m}{2g_m} = \frac{1}{2}$$

If V_{in} decreases by $\Delta V \rightarrow m_s$ increases by $\frac{\Delta V}{2}$
 $m_s \rightarrow V_{in}$ same, V_{DS} change slightly \Rightarrow Current same
 \therefore that $V_{DS} \uparrow$ as $V_{in} \uparrow$ for m_1

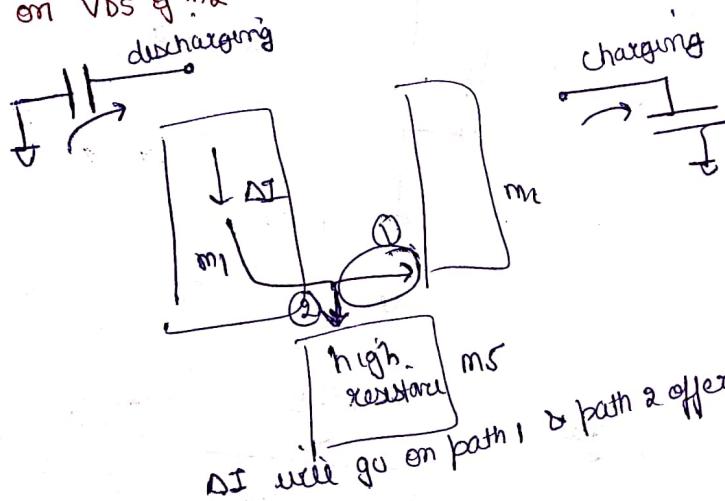
V_{o1} should \uparrow

forma, $V_{in} \uparrow$ as $V_s \uparrow \rightarrow V_{DS} \text{ should } \uparrow \Rightarrow V_{o2} \uparrow$

$\Rightarrow V_{o2} \uparrow, V_{o1} \uparrow$

\Rightarrow difference \uparrow

m_s with constant current stage is very impo. due to this change in V_{in} is reflected on V_{DS} of m_2 also thereby $\uparrow V_{o1} - V_{o2}$.



Q1/2/19
 above circuits are balanced op & balanced differential

$V_{cm} \rightarrow$ dc input
 $V_{dm} \rightarrow$ differential input
 Corresponding to $V_{dm} \rightarrow \frac{\Delta V}{2} \uparrow$
 $-V_{dm} \rightarrow \frac{\Delta V}{2} \downarrow$

Point A virtually short

$$\text{Let } V_{in1} = V_{in} + \Delta V$$

$$V_{in2} = V_{in} - \Delta V$$

Find V_{o1} & V_{o2} individually

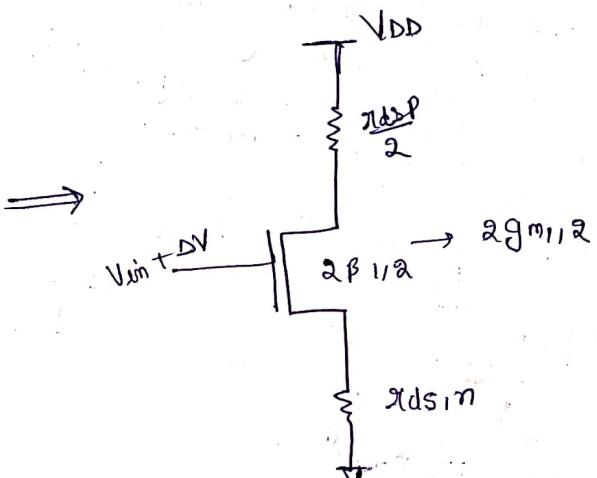
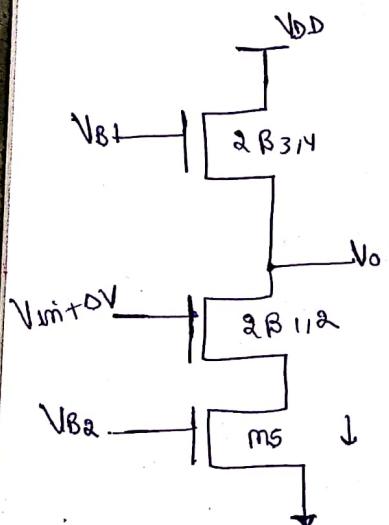
$V_{o1} = V_{o2}$ as both sides identical

i.e. V_{o1} & V_{o2} shorted

i.e. even if resistance is applied in between no current flows

m_3 & m_4 in parallel $\rightarrow 2I \Rightarrow 2\beta$

m_1 & m_2 in parallel $\rightarrow 2I \Rightarrow 2\beta$



$$\text{gain} = \frac{-g_{dss}^p}{\frac{1}{2} + g_{dss}^s}$$

$$\frac{2g_{m1,2}}{g_{dss,5}}$$

$$\Delta V_o = \frac{-g_{dss}^p g_{m1,2} \Delta V_{in}}{1 + 2g_{m1,2} g_{dss}^s}$$

should be zero for this reason
then only AC change will occur

cannot decrease this because otherwise gain will decrease

$$A_{cm} = 0 \quad (\text{when input same})$$

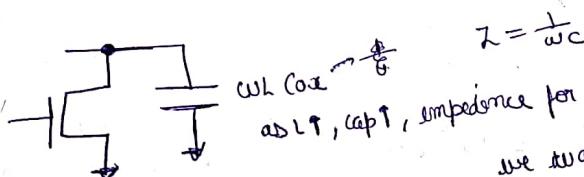
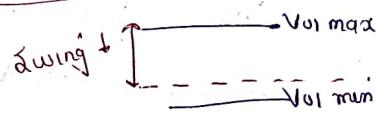
Common mode gain

as we increase L to increase g_{DS} then $V_{DSat} = \sqrt{\frac{2ID}{\beta}} \uparrow$ I_D constant

$$V_{O1 \min} = V_{DSat} + V_{DS}$$

Increasing length directly is not a solution
Apply cascading

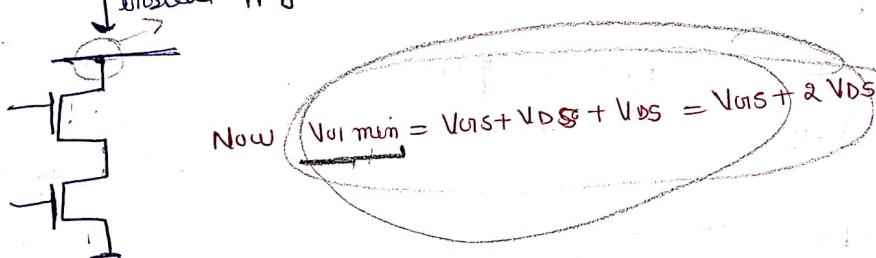
due to this ΔV_{DS} decreases ??



$Z = \frac{1}{\omega C}$
as $L \uparrow$, cap \uparrow , impedance for a particular $\omega \downarrow$

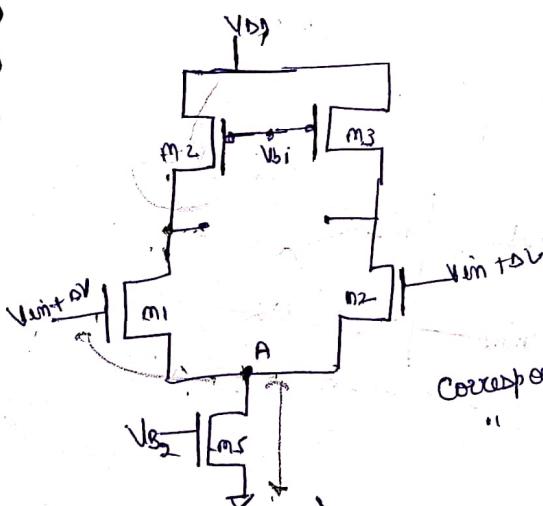
we want impedance to be ∞ and not low

instead apply



Now

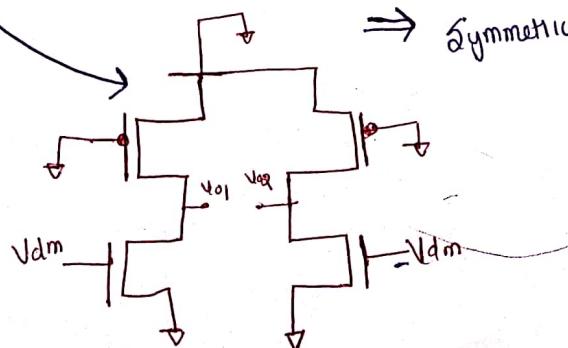
$$V_{O1 \min} = V_{DSat} + V_{DS} + V_{DS} = V_{DSat} + 2V_{DS}$$



Corresponding to V_{cm} to DC, A is virtually ground

" to V_{dm} also A is virtually ground
as m_1 causes $\rightarrow \frac{\Delta V}{2} \uparrow$
 m_2 causes $\rightarrow \frac{\Delta V}{2} \uparrow$ } overall zero

\Rightarrow Symmetry (and A exactly ground)



$$V_{o1} = -g_{m1,2} \left(\frac{r_{ds3,4}}{r_{ds1,2}} \parallel r_{ds1,2} \right) V_{dm}$$

$$V_{o2} = g_{m1,2} \left(\frac{r_{ds3,4}}{r_{ds1,2}} \parallel r_{ds1,2} \right) V_{dm}$$

$$V_{o1} - V_{o2} = -2 V_{dm} g_m \left(\frac{r_{ds1,2}}{r_{ds1,2} \parallel r_{ds3,4}} \right)$$

$$\frac{V_{o1} - V_{o2}}{V_{in1} - V_{in2}} = -g_m \left(\frac{r_{ds1,2}}{r_{ds1,2} \parallel r_{ds3,4}} \right)$$

$$g_m = \sqrt{2 I_D \beta} = \sqrt{\frac{2 \times 50 \times 10 \times 10^{-6}}{2}} = 10^{-2} \sqrt{10}$$

for $\beta = 10$
 $I_D = 50 \mu A$

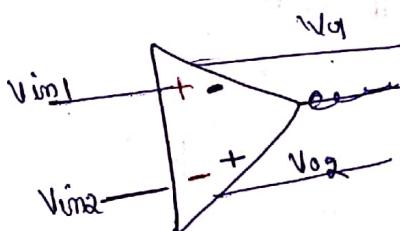
$$\lambda = 0.01$$

$$r_{ds} = \frac{1}{\lambda I_D/2} = \frac{2 \times 10^6}{0.5} = 4 \times 10^6$$

current through
each is $\frac{I_D}{2}$

$$A = \sqrt{2 \times 25 \times 10^{-6} \times 10} \left(\frac{r_{ds}}{2} \right)$$

$$= \sqrt{2 \times 25 \times 10^{-6} \times 10} \left(\frac{10^6}{2 \times 0.01 \times \frac{50}{2}} \right)$$

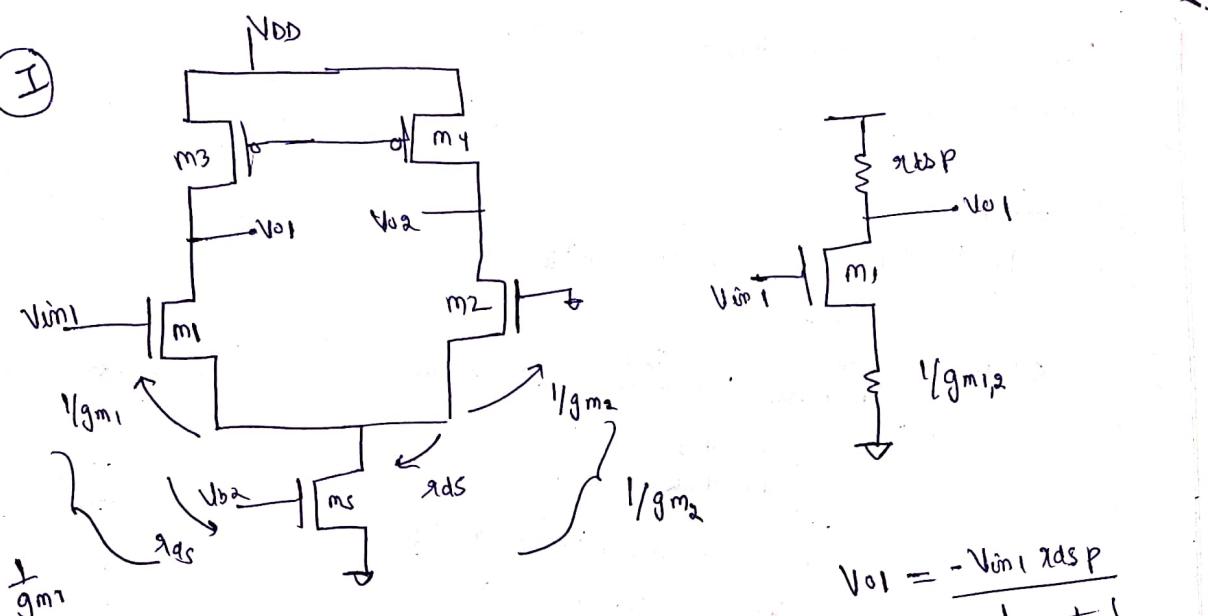


$V_{o2} \rightarrow$ in terms of V_{in1} in phase

$V_{o1} \rightarrow$ in terms of V_{in2} in phase

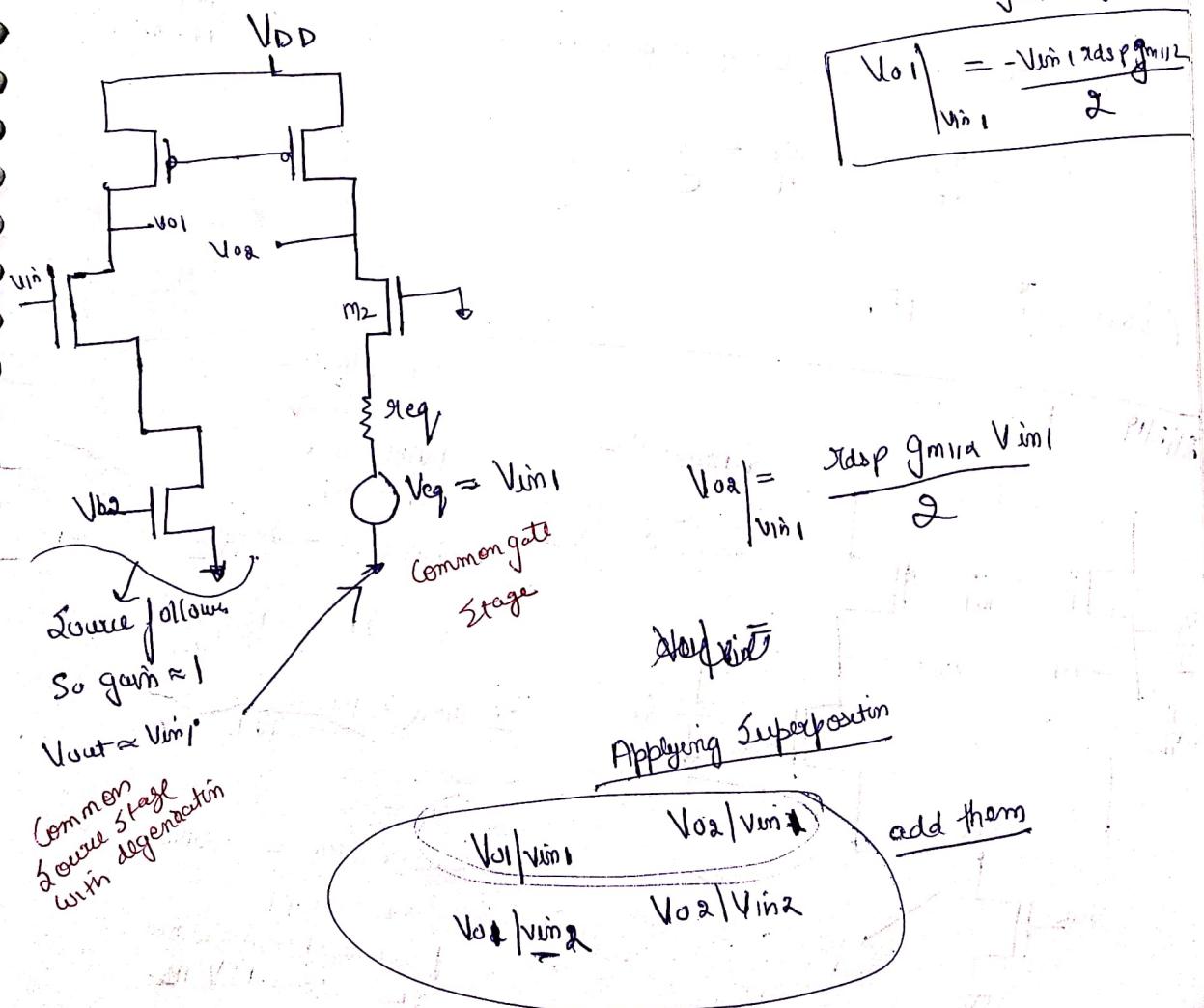
$V_{o2} \rightarrow$ out of phase in terms of V_{in2}

(I)



$$V_{o1} = \frac{-V_{in1} g_{dsP}}{1 + \frac{g_{m12}}{g_{m12}}}$$

$$V_{o1} = -\frac{V_{in1} g_{dsP} g_{m12}}{2}$$



$$\frac{V_{O1} - V_{O2}}{V_{in1} - V_{in2}} = g_m m_{1,2} \tau_{ds1,2}$$

$$d = \frac{FL^3}{12J_2}$$

Case II $V_{in1} = 0$

Find V_{O1}/V_{in2} , V_{O2}/V_{in2}

$$CMRR = \frac{A_{dm}}{A_{cm, dm}} \rightarrow \infty \text{ should be, i.e. we want } A_{cm, db} \text{ to be zero.}$$

$$Adm \rightarrow \frac{V_{O1} - V_{O2}}{V_{in1} - V_{in2}}$$

$A_{cm, dm} \rightarrow$ input individual op differential

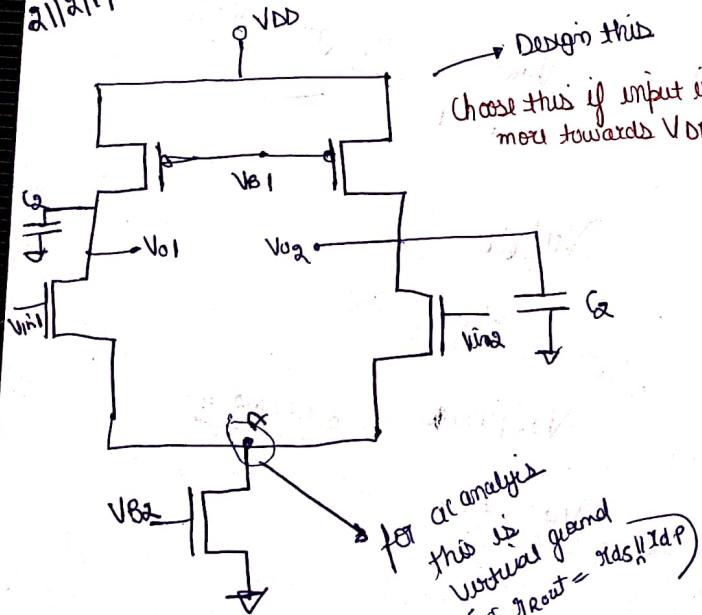
$\frac{V_{O1} - V_{O2}}{V_{in1}}$	$\frac{V_{O1} - V_{O2}}{V_{in2}}$??
-----------------------------------	-----------------------------------	----

slew rate \rightarrow maximum rate of change of V_o with respect to time $= \left| \frac{dV}{dt} \right|_{max}$

$$i = C \frac{dV}{dt} \Rightarrow \frac{dV}{dt} = \frac{i}{C}$$

(Load of CRO $\rightarrow 50 \text{ pF}$)

21/2/19 Read CMOS Drawing



Design this
choose this if input is
more towards VDD

Specifications

$$V_{DD} = 3.3 \text{ V}$$

$$|V_{th}| = 0.6$$

$$\lambda = 0.1$$

$$(N_m(C_{ox}))n = 300 \frac{\mu\text{A}}{\text{V}^2}$$

$$(\gamma)_P = 100 \frac{\mu\text{A}}{\text{V}^2}$$

I_{CMR} (Input Common mode Range) $= 1 \text{ V to } 2.5 \text{ V}$

$O_{CMR} =$

Bandwidth (BW) $= 100 \text{ MHz}$

$$C_L = 5 \text{ pF}$$

power dissipation $= 10 \text{ mW}$
slew rate $= 10 \text{ V}/\mu\text{s}$

Now gain will change. 1st order system with one resistance & capacitance
Find 3dB bandwidth.

$$\text{Rülog} \left(\frac{1}{\sqrt{2}} \right) = -3 \text{dB}$$

$$\text{Power} \rightarrow 10^{\log(1)} \\ \text{Voltage} \rightarrow 20^{\log(1)}$$

With increase in gain BW +

$$\text{Slow rate} = \frac{du}{dt} = \frac{x}{c}, \text{ Here } c \text{ is fixed}$$

~~Since rate = $\frac{dt}{C}$~~
How much maximum current can flow through capacitor

$$g_{\text{cm}} = \frac{A}{1 + R_C j \omega}$$

$$\text{at } \omega = \frac{1}{RC}, B\omega = 3 \text{ dB}$$

keep on \uparrow m₂ Voltage such that m₂ out of Saturation

Slew rate = $\frac{I_{SS}}{2 \cdot C_L}$ (the slewrate) Volts/ μ sec

when here highest the slew rate
then at C₁ highest -ve ...
with maximum

... max rate \rightarrow Voltage \uparrow in the way

I_m device current is varied by V_{BS}

For small signals linear rate plays role

$$\text{overall flow rate} = \frac{I_{ss}}{C} \left(\frac{I_{ss}}{2}, \frac{I_{ss}}{2} \text{ in both} \right)$$

→ will give max current

$V = \frac{1}{\omega} \int \omega dt$ give min current

$$BW = \frac{1}{R_{\text{eff}} + C}$$

Higher is the current more is BW & more is speed

$$\text{Power dissipation} = I_{SS}^2 V_{DD}$$

current as beyond it PD not acceptable

$$I_{omw} = I_{SS} \times 3.3$$

$$J_{SS} \approx 3 \text{ mA}$$

$$0.5mA < I_{SS} < 3mA$$

we choose $I_{SS} = 1 \text{ mA}$
 \Rightarrow BW will little higher
 \Rightarrow slew rate high

$$1 \times 10^6 = \frac{1}{(5 \times 10^{-12})(\text{Rise})}$$

$$R_{\text{set}} = \frac{1}{5.0 \times 10^{-6}}$$

$$R_{out} = \frac{105}{5} = 21$$

$$2n^0 = \frac{1}{\lambda I} \Rightarrow I = \frac{1}{2n^0} = 0.5$$

Slew rate limit of current $\rightarrow 5 \mu\text{A}$
 $BW \rightarrow 0.5 \text{ mA}$

$V_D \rightarrow 3 \text{ mA}$

So we choose $I_{SS} = 1 \text{ mA}$ so all are satisfied.

Now $g_{out} = g_{m12} R_{out}$

g_m depend on W/L i.e. sizing of transistor.

$$g_{out} = g_{m112} \times (\lambda_{ds} \| \lambda_{ds})$$

$$= g_{m112} \times \frac{\lambda_{ds}}{2}$$

$$= g_{m112} \times \frac{1}{2 \lambda I_D}$$

$$= g_{m112} \times \frac{1}{2 \lambda \frac{I_{SS}}{2}}$$

$$= g_{m112} \times \frac{1}{\lambda I_{SS}}$$

$$= \sqrt{2 \beta_{112} I_D} \times \frac{1}{\lambda I_{SS}}$$

$$g_{out} = \sqrt{2 \beta_{112} I_{SS}} \times \frac{1}{\lambda I_{SS}}$$

$$I_{O1} = \sqrt{2 \mu_{nLOX} \frac{W}{L} \times \frac{I_{SS}}{2} \times \frac{10}{I_{SS}}}$$

$$I_W = \sqrt{300 \times 2 \times 10^{-6} \times \frac{W}{L} \times \frac{1 \times 10^{-3}}{2}} \times \frac{10}{10^{-3}} \times 10^4 \sqrt{\frac{W}{L}}$$

$$I_{O2} = \sqrt{300 \times 10^{-9}}$$

$$I_W = 10^{-4} \sqrt{300 \times 10^{-1} \times 10^4} \sqrt{\frac{W}{L}}$$

$$\frac{I_W}{\sqrt{30}} = \sqrt{\frac{W}{L}}$$

$$\frac{W}{L} = \frac{3.333}{10 \times 10^{-3}} = 333.3 \quad (\text{very huge})$$

For m_5

$V_{in \ min}$ will give V_{DSat} for m_5

$$V_{in} = V_{DSat} + V_{th} + \sqrt{\frac{2 I_{SS}}{\beta}}$$

This is β_{max}

For max value of V_{in}

V_D should be atleast such that it does not come out of saturation

$$V_{in} - V_{th} < V_D$$

$$V_{in} - V_{th} < V_{out}$$

$$V_{in} - V_{th} < V_{DD} - V_{DSat P}$$

$$V_{in} - V_{th} < V_{DD} - \sqrt{\frac{2 I_{SS}}{\beta_P}}$$

$$2.5 - 0.7 < V_{DD} - \sqrt{\frac{I_{SS}}{\beta_P}}$$

$$\sqrt{\frac{I_{SS}}{\beta_P}} > 3.3 - 1.9$$

$$\sqrt{\frac{10^{-3}}{\beta_P}} > 1.4$$

$$\frac{10^{-3}}{\beta_P} > (1.4)^2$$

$$\beta_P < \frac{10^{-3}}{1.96}$$

P mos Version

