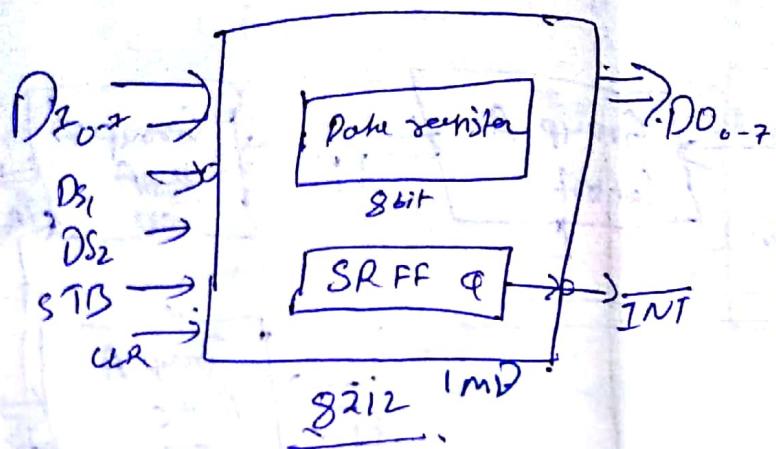
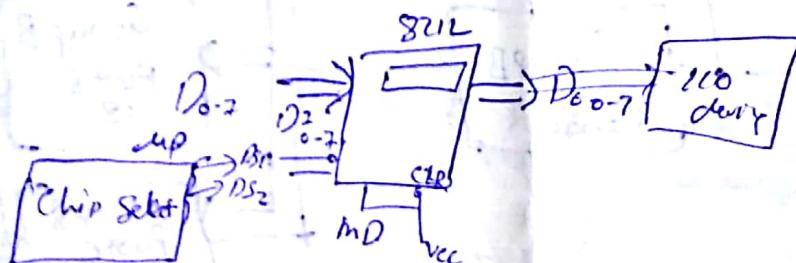


Non programmable I/O port

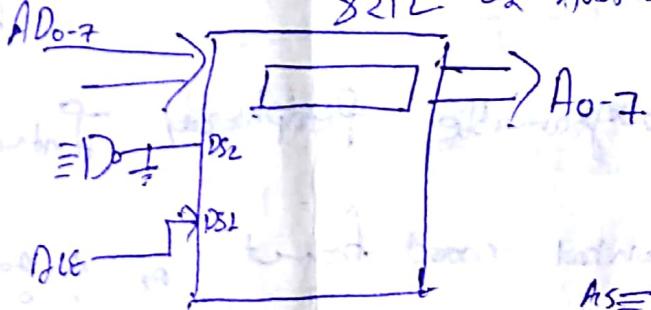


Single port device.

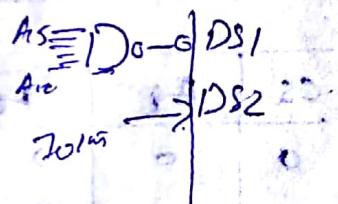
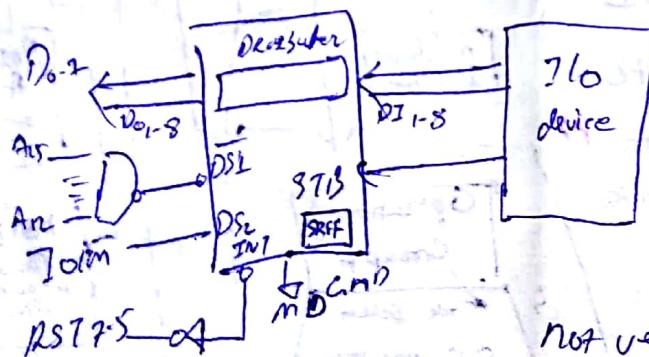
use of 8212 as o/p port



8212 as Address demultiplexing



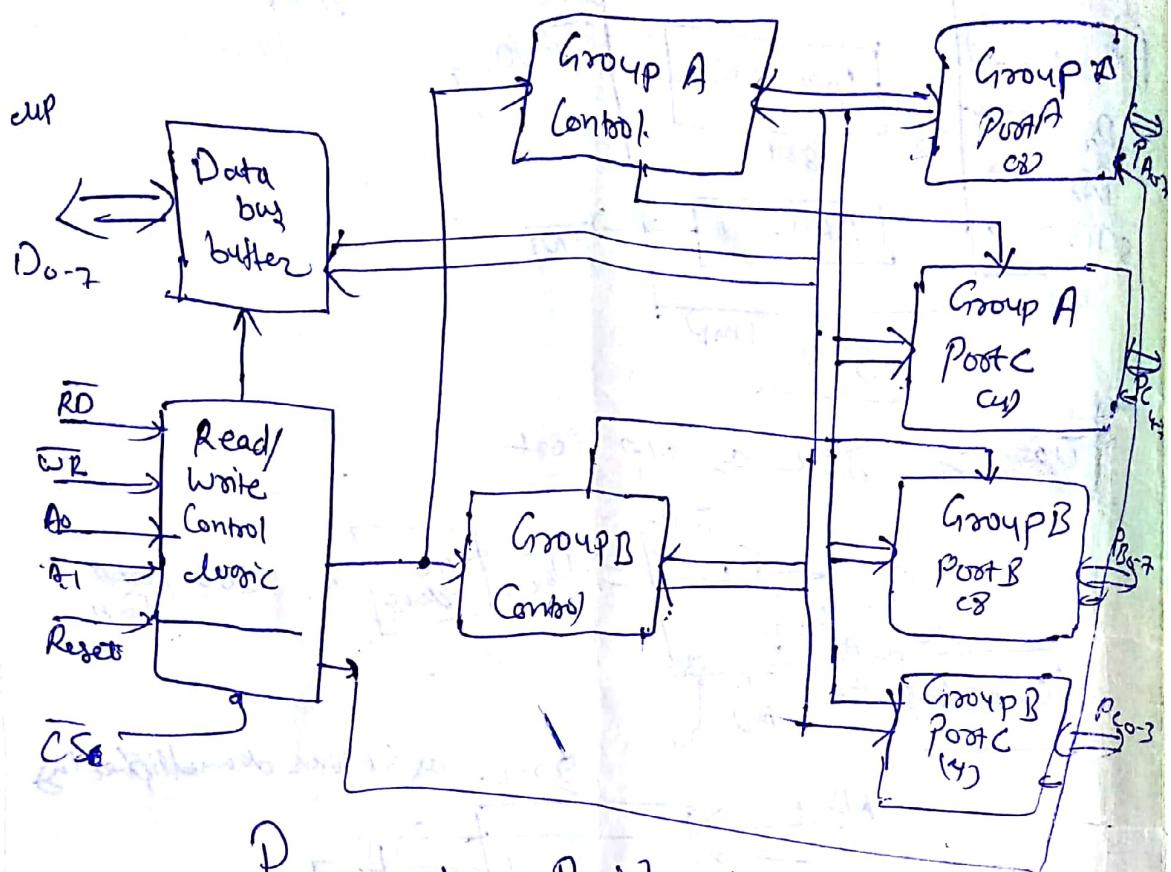
8212 as I/O Port



not very flexible device.

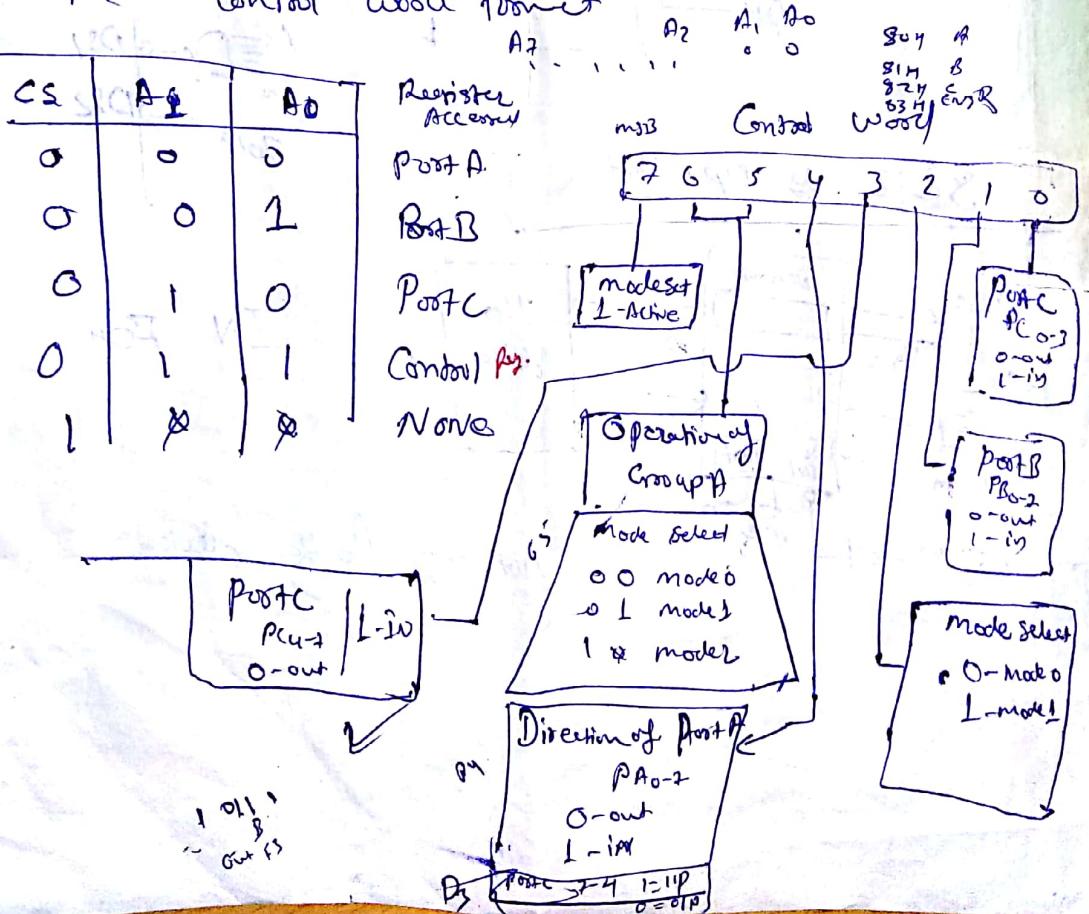
Programmable I/O port

8255A

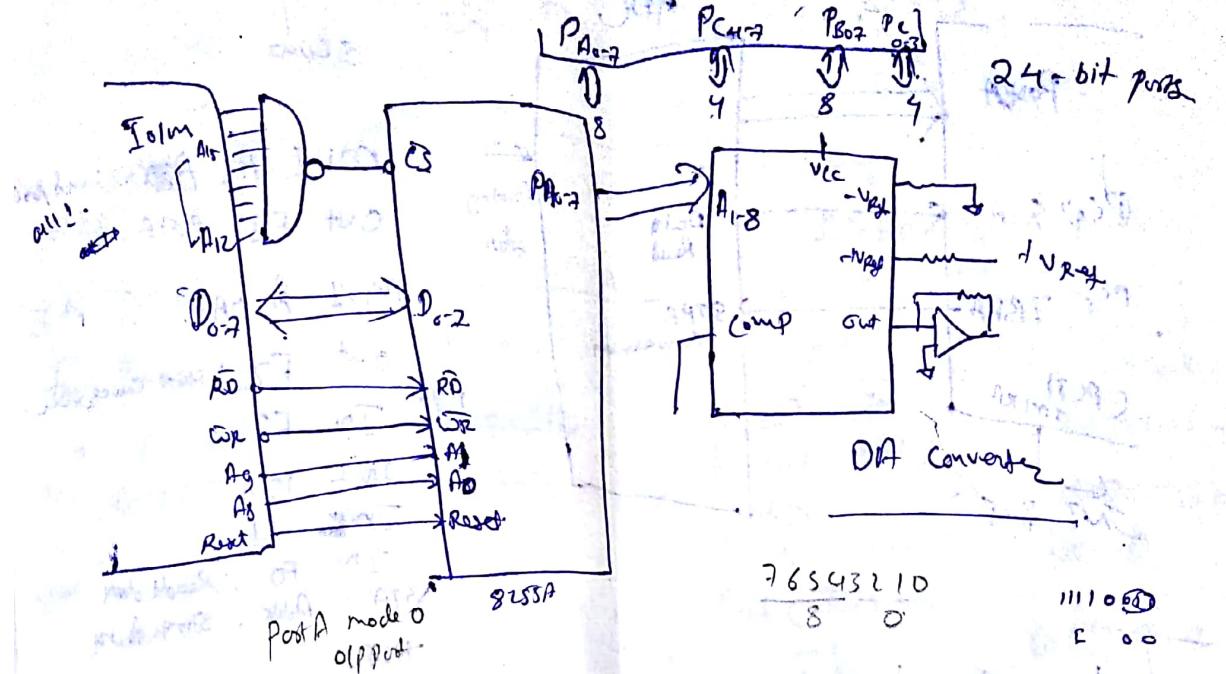


Programmable Peripheral Interface (PPI)

The Control word format



Mode 0 Simple I/O

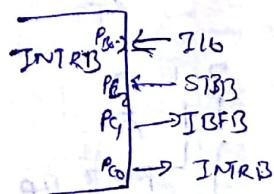
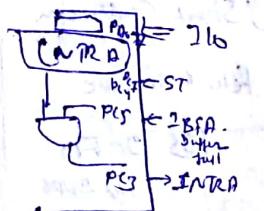


7 6 5 4 3 2 1 0
1 0 0 0

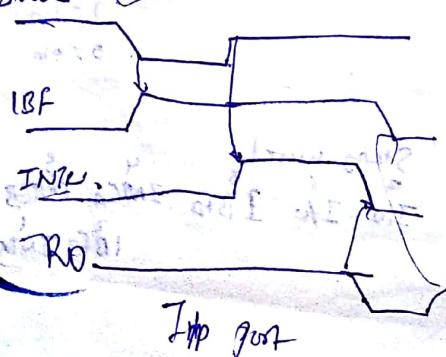
MVI A, 80H Config Port A in mode 0 & 01P port
out F3 → Configure Port A & 01P port
MVI A, Data
out F0; writes data to port A

7 6 5 4 3 2 1 0
1 0 0 0

Control word: 1011011x.



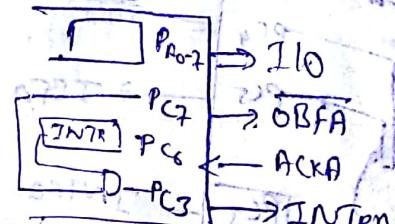
Strobe



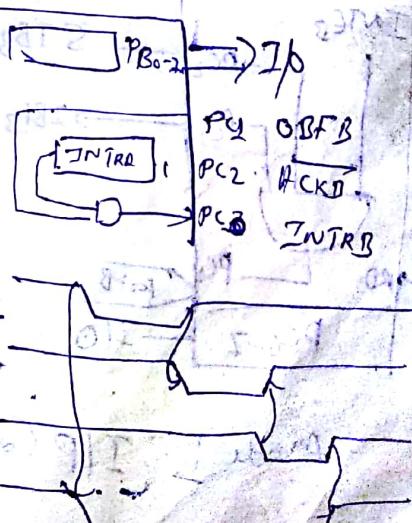
Group A:

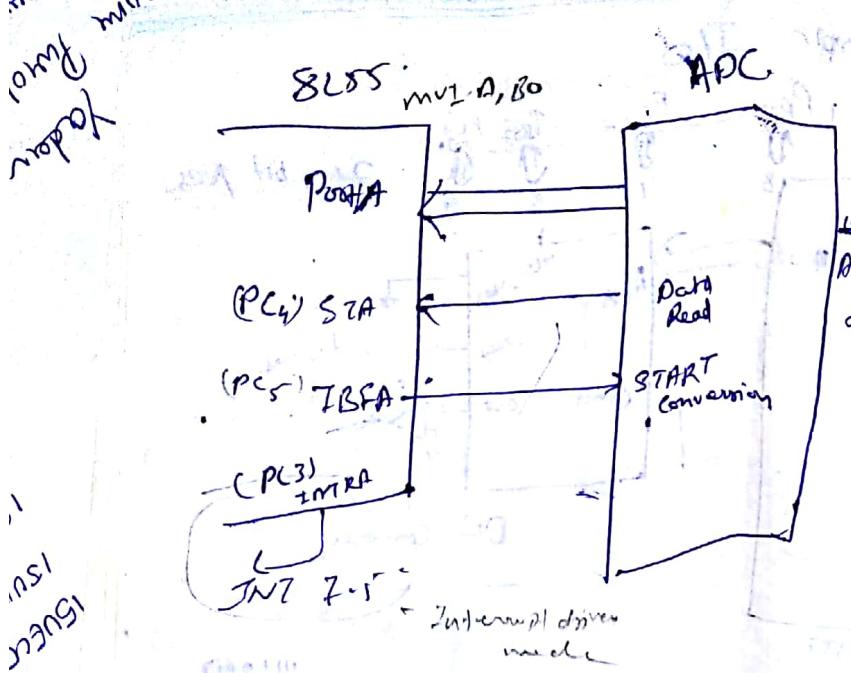
Asynchronous / Interrupt driven mode.

10 10 x 16 X



Group B





slow

M.V.I A, ~~Brown~~; ^{light brown}
out F3 post criray

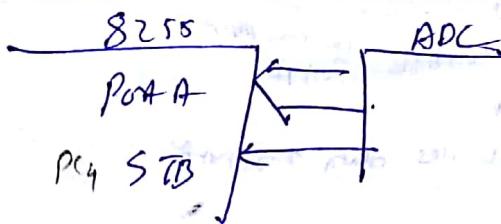
MVI A, OAH (BSR PC_(S))
out F2 ; start convergence
IN F2

L2: IN FR
ANI 10n $(PC_4)_{\text{with}} \text{BSR}$
~~JMP L1~~

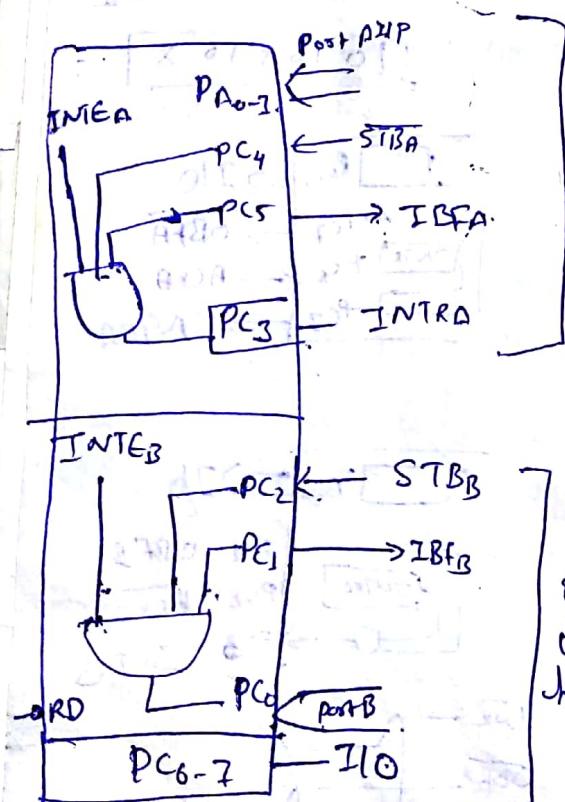
IN FO ; Recall data from
STA Addr ; Store data

HLT

Interrupt driven mode:-

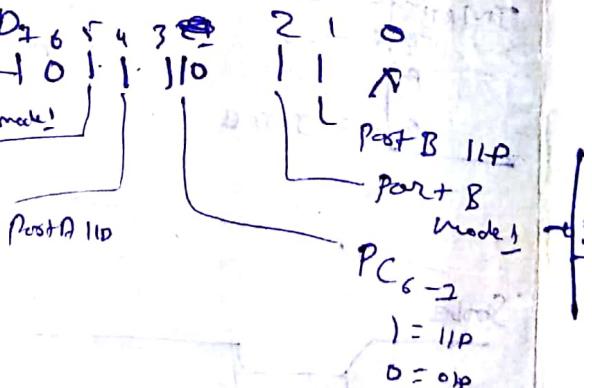
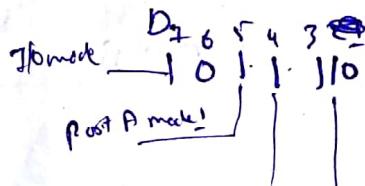


TIP Configuration



Post A win
Handshake
Signaly.

Post B
with
handshake

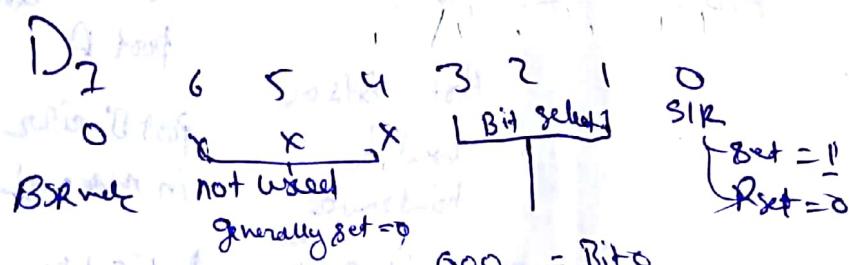


Study week!
7 6 5 4 5
I/Io I/u I/Bf_d INT_A INT_B
I/Bf_d INT_B

BSR (Bit Set / Reset) Mode:

Concerned only with 8 bits of Port C
 Set/Reset by writing an appropriate Control word in Control register. $D_7 = 0$ as BSR Control word.

it does not alter any previously transmitted Control word with bit $D_7 = 1$



if set PC ₇	0 0 0 0	1 1 1 1 = OF
reset PC ₇	0 0 0 0	1 1 1 0 = OE
Set PC ₃	0 1 1 1	0 1 1 1 = 07H

Control register address = 83H.

MVI A 0FH
 Out 83H

* written in Control register

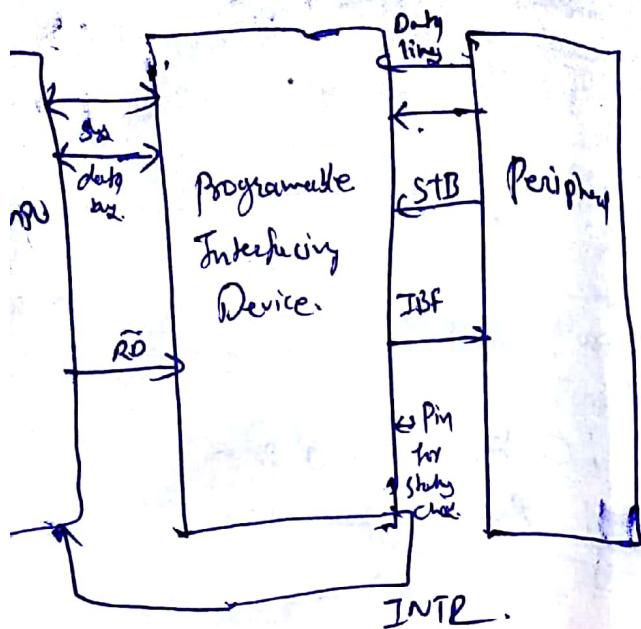
MVI A 07H
 Out 83H.

* not in Port C

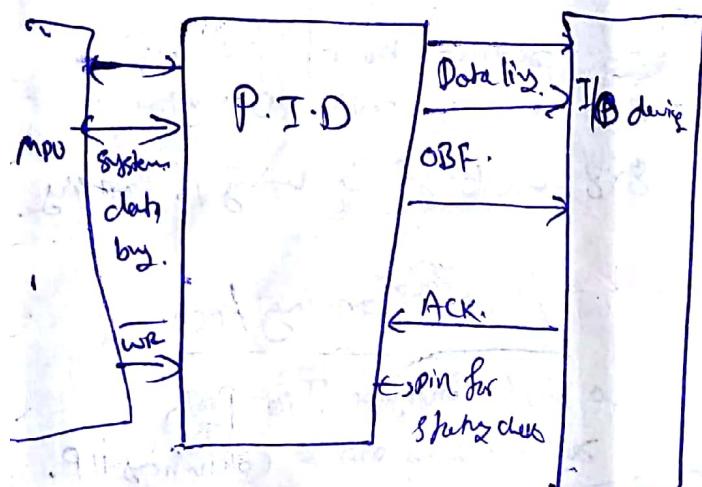
RET

* BSR. Cnt word affects only Port C
 1 bit in

* BS Cnt word does not affect the I/O module



Data I/O with handshake

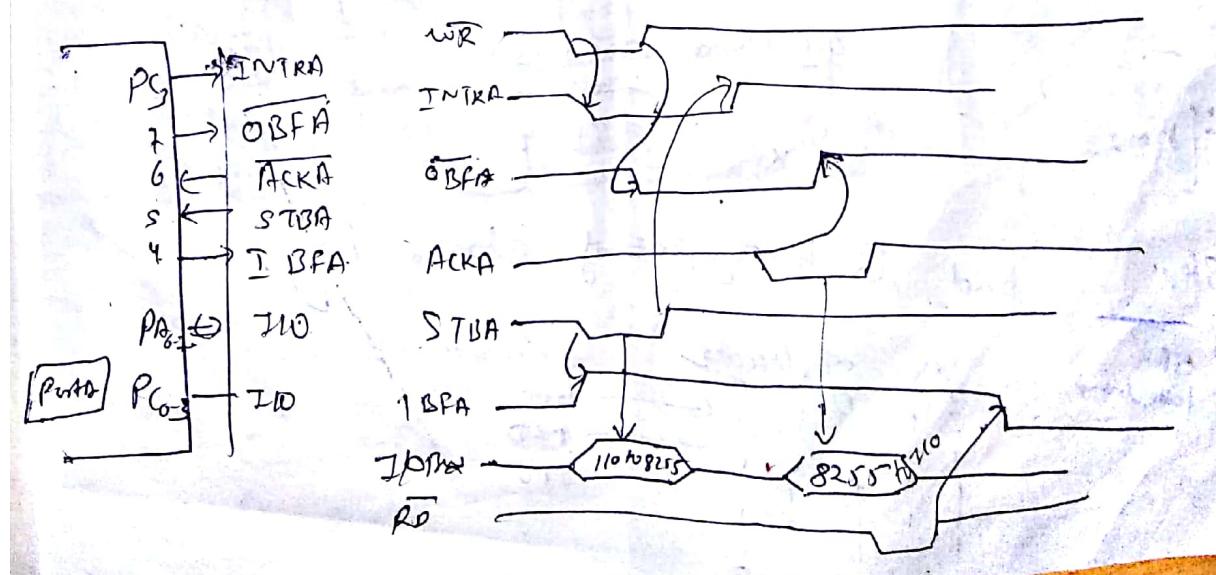


76543210
00001001

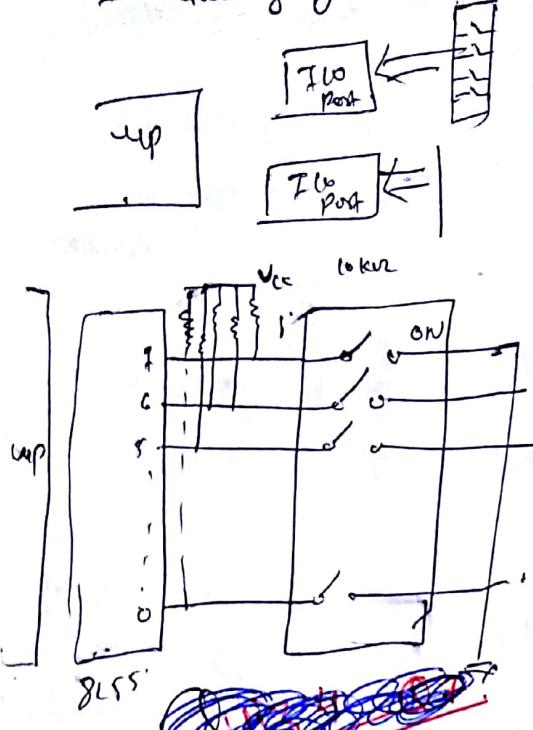
OLP with handshake.

Model 2 : standard bidirectional I/O

ctrl word 71 & xx 210

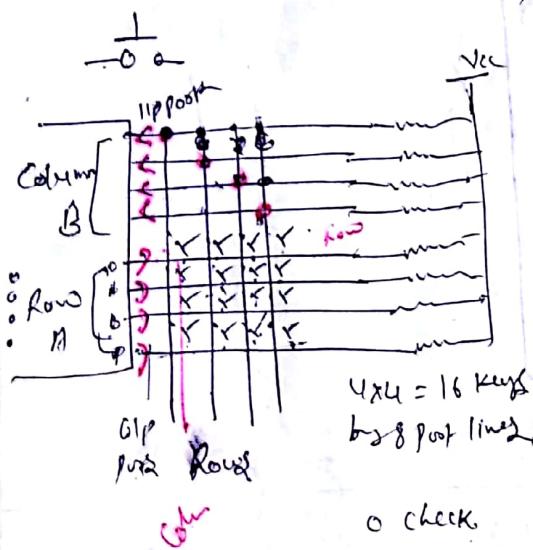


Interfacing of Switches



Configure I/O port
Read the Port value.

~~Keyboard Matrix~~



$8 \times 8 = 64$ keys by using 16 Port

Row Scanning Tech.

Step 1: Configure I/O ports
as Rows & Columns I/P.

Step 2: Check whether all keys are open.

Step 3: Check whether there is a key closure.

Step 4: Identify the closed key by row scanning

4.1 Scan row A

1	0	0	1
1	1	0	1
1	1	1	0
1	1	1	1

Find the binary part of closed key.

Steps:

either
false output

use of decoder

0	1	1	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	1

Encoded form:

000

000

010

Line reversal Technique

Step 1 Config Port A as 01P & Port B as 11P.

Column no. Port A generate all 0
Port B Read data.

Step 2 Config Port A as 01P

Port B as 11P

Row
column no.

Key bounce! → Proditive

delay generation

key depressed

key bounce

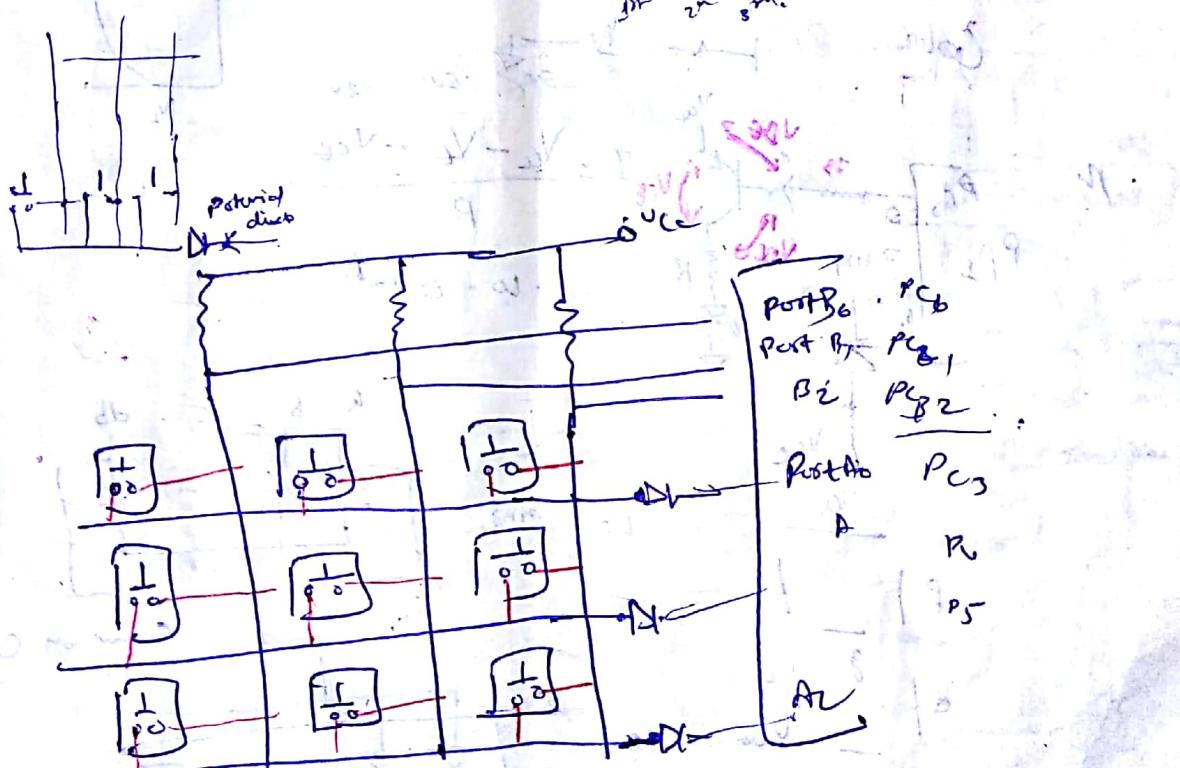
10-20 msec

Rolling If two keys pressed simultaneously

o 2 Key lockout

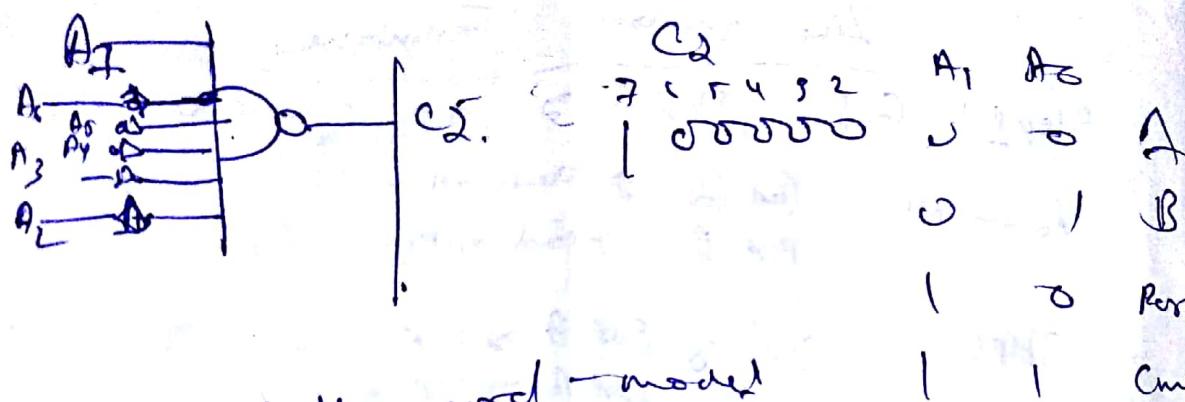
o n-key rollover

K, J, L → memory
at a time



Row horizon

Col vertical.

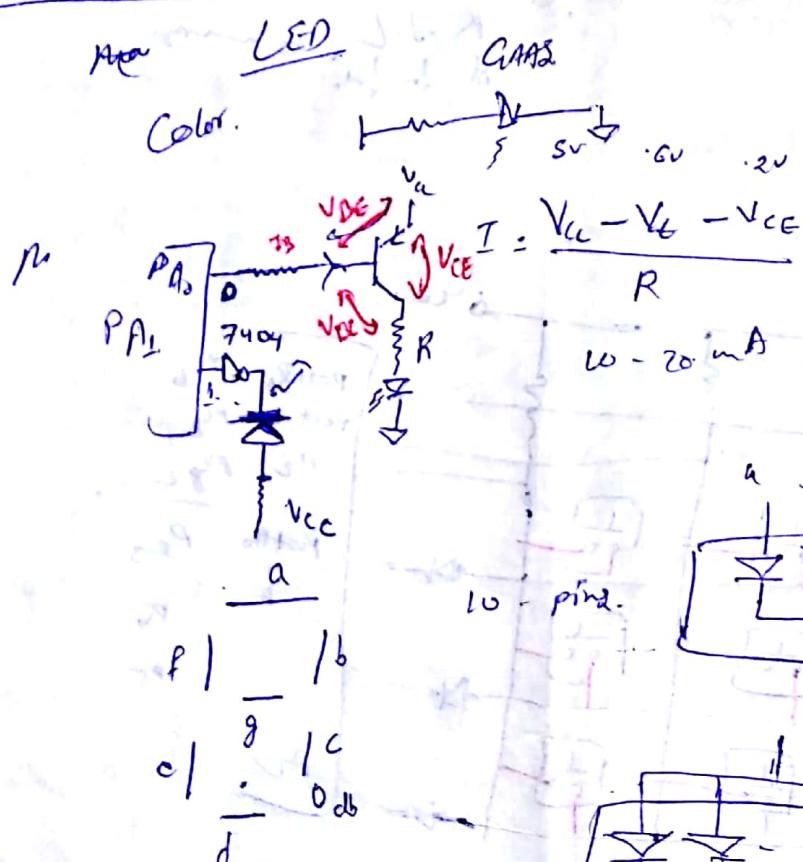


IIP Control word - mode

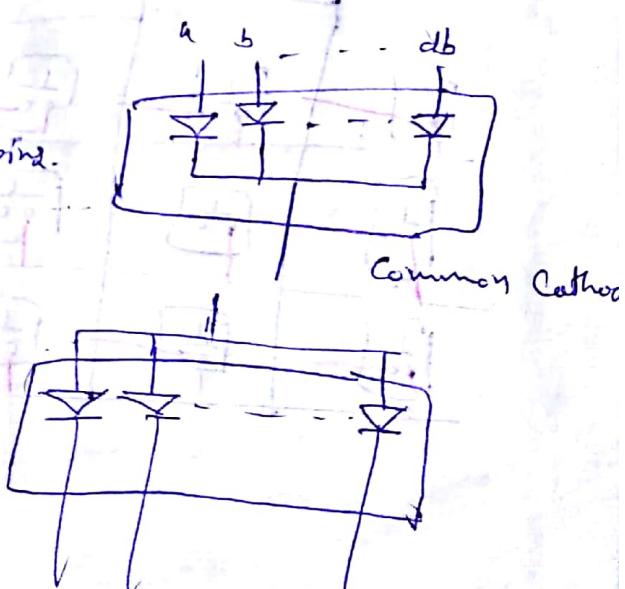
I/O I/O I_{BFA} INTEA INTRA I_{TBFB} INTEB IN

OIP Status. Word mode

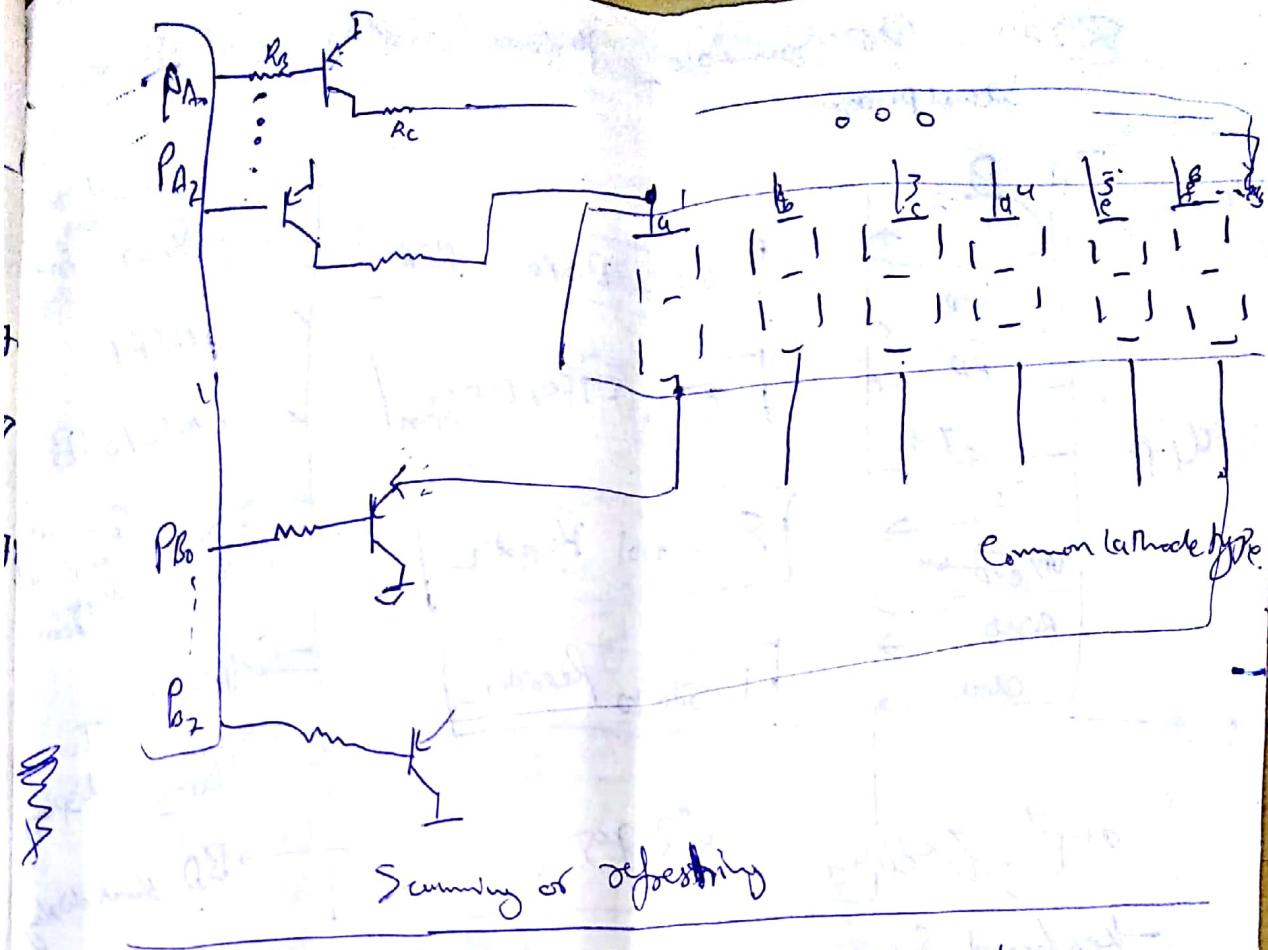
I_{BFB} INTEA I/O I/O INTRA INTEB I_{TBFB} INTEB



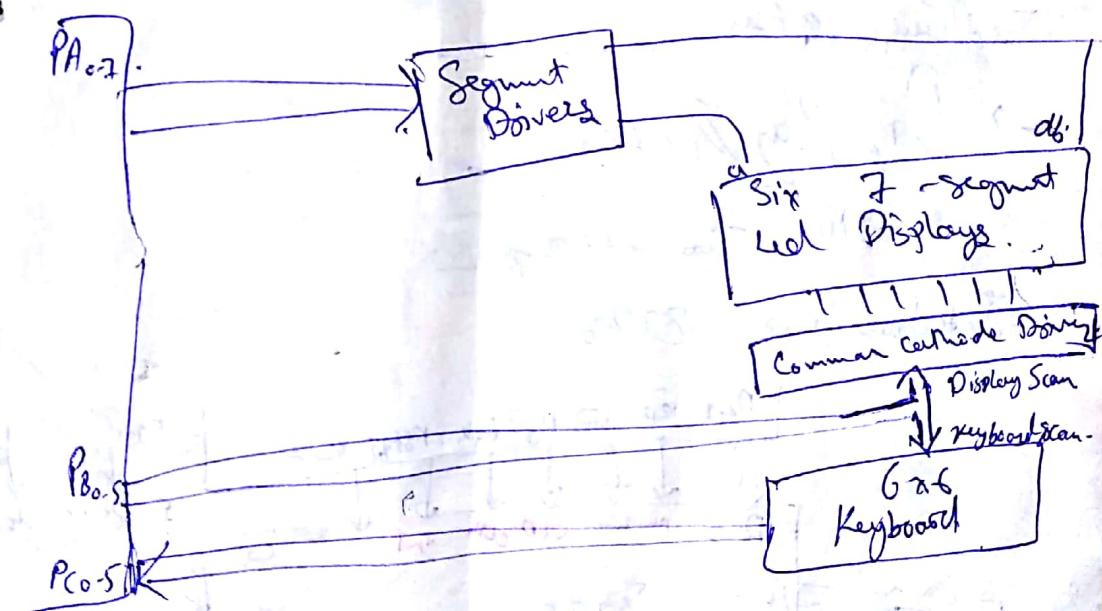
Port Gxit drive
Current for LED.



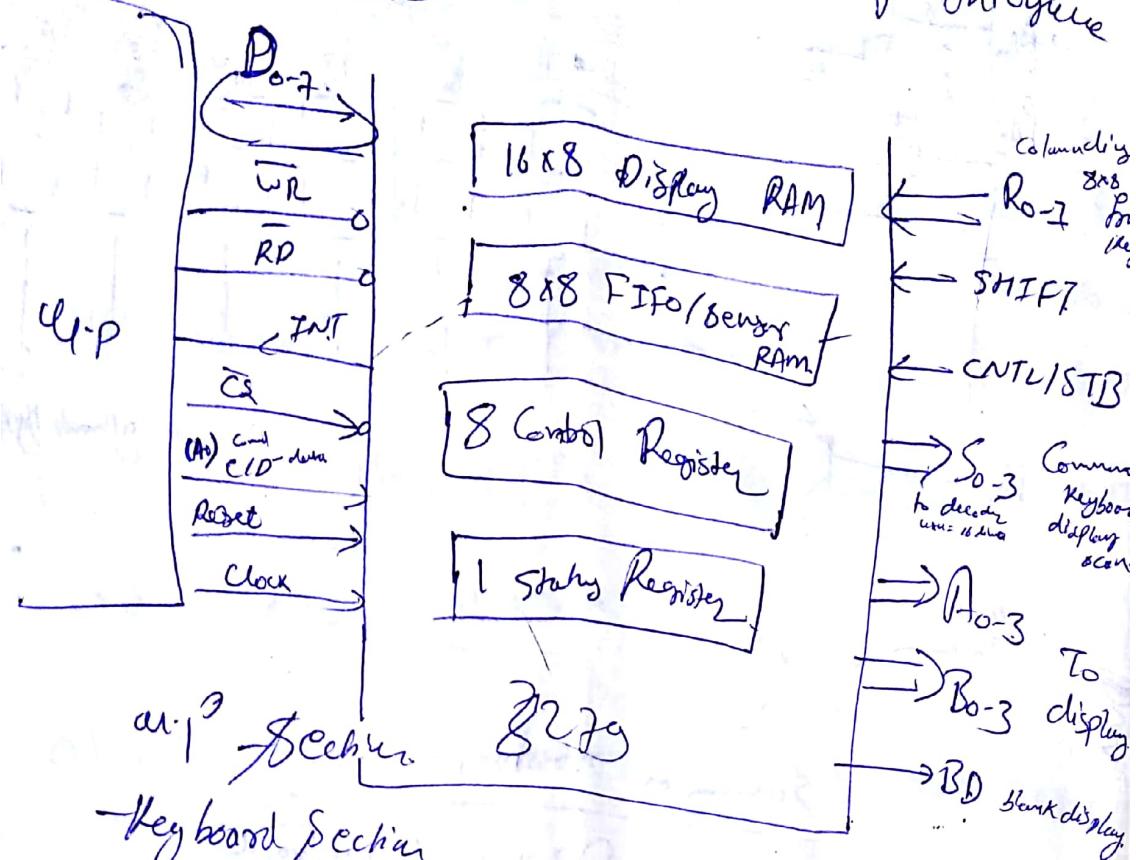
Common anode



Common Display & Keyboard



8279 Programmable Special Purpose Keyboard / display Interface



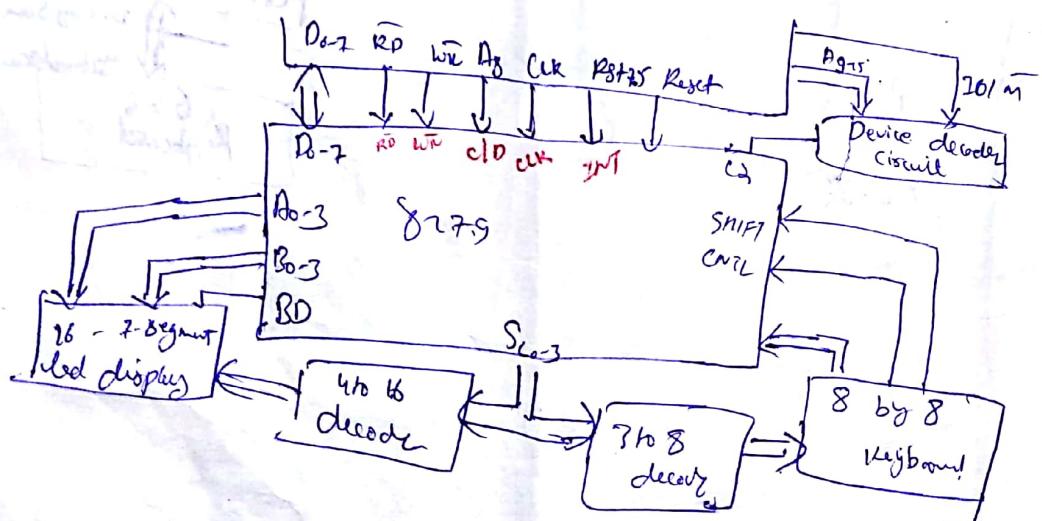
→ Keyboard Section.

→ Plan Section.

→ Display Section.

8 bit. Two 4 bit groups

Interfacing uses 8279



LCD

Power?

→ Proliferation of Portable equipment

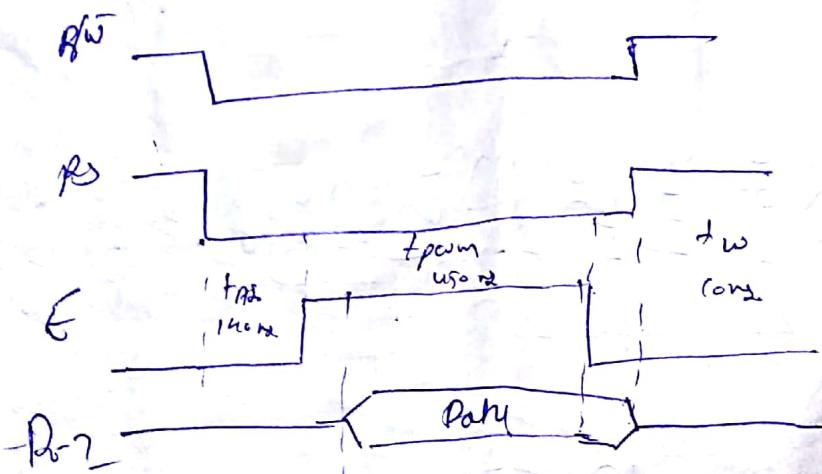
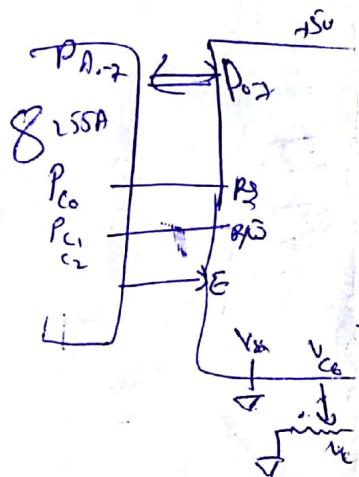
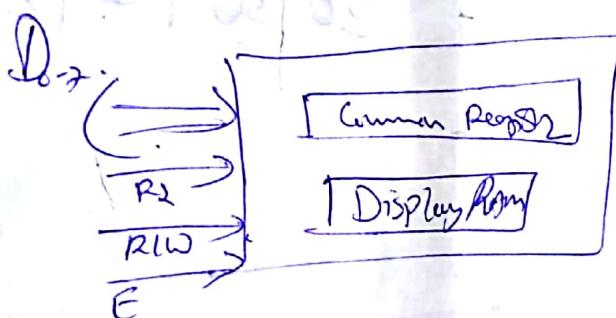
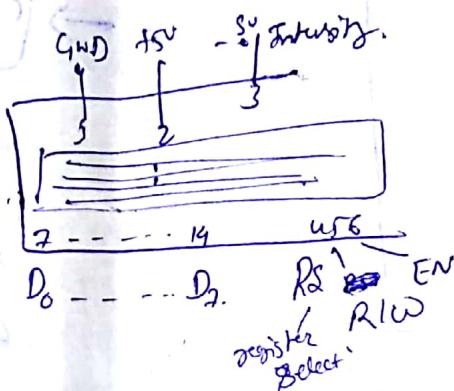
→ Declining Price. (Prices)

→ Ability to - display, Graphic.

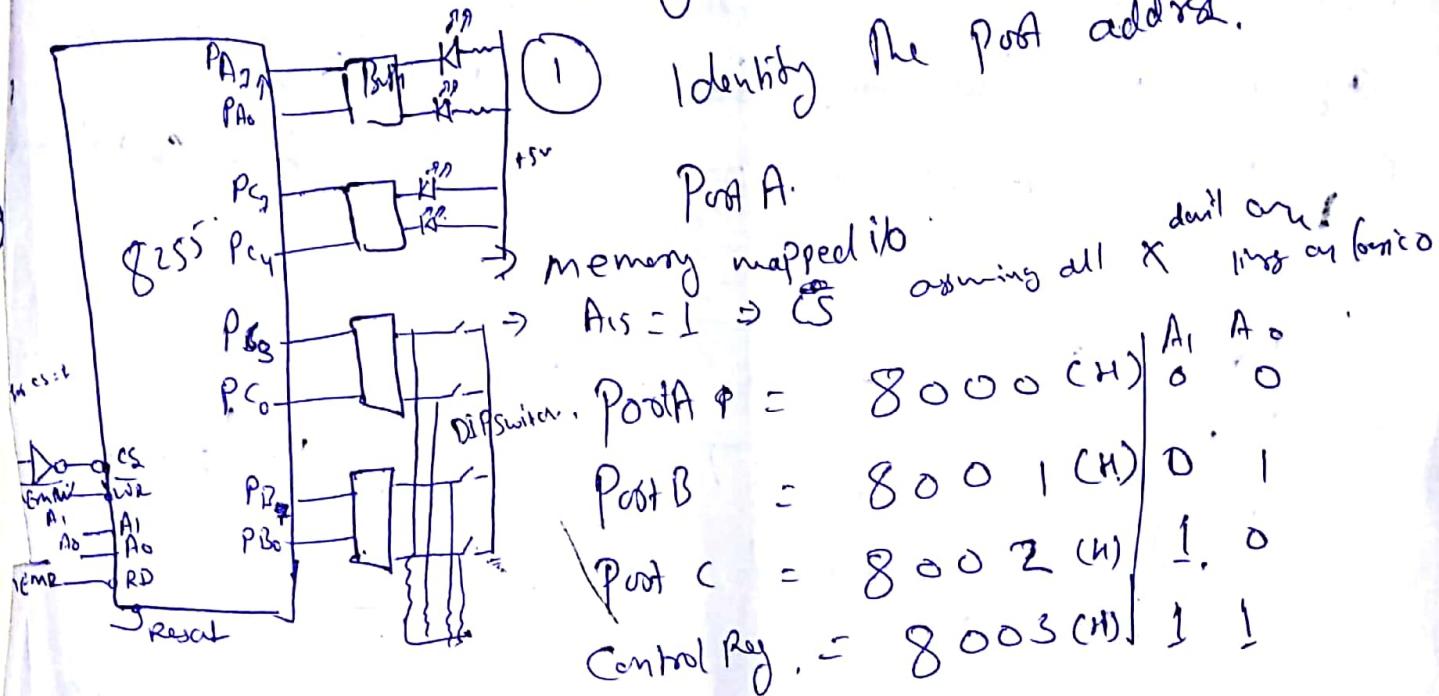
(numbered, character & graphic)

Built-in refresh Rate (Endless)

Type of Programming



- node O. Port A & B \Rightarrow two simple 8 bit I/O &
 Port C. ex. 2, 4-bit Ports.
- (1) OIP are latched.
 - (2) IIP are not latched.
 - (3) Ports do not have handshake or interrupt capability.



2. Control word for Mode O to configure Port A & Port C_O as OIP ports.
- Port A_{C_O} = OIP 1. 0 0 0 0 1 1
- Port B_{C_O} = IIP
- Prog. to read DIP Switches and display the reading from Port A to Port C_O.

```

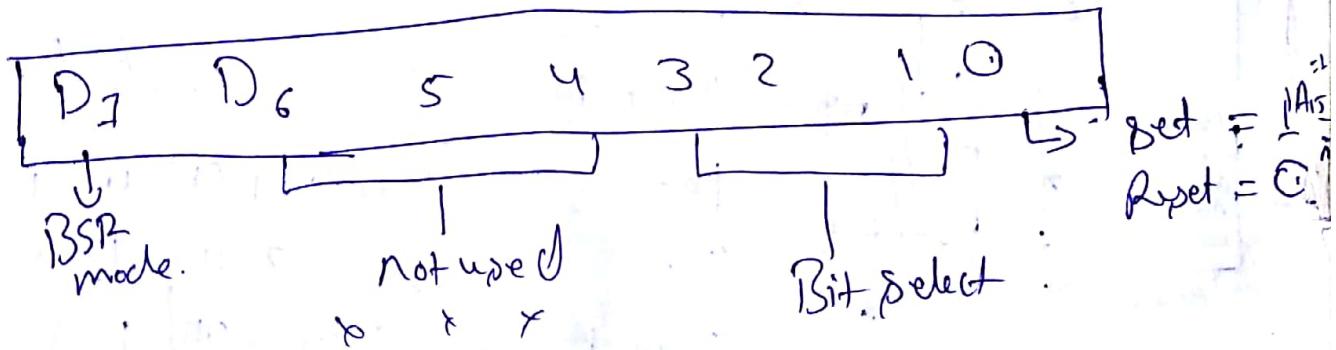
MV.L A 83
STA 8003 :- control word to initialise Port
LDA 8001 : read port B
STA 8000  $\rightarrow$  Port A
LDA 8002  $\rightarrow$  Port C
ANI 0F  $\rightarrow$  mask the upper four bits of Port C (no IIP done)
RCL | STA 8002 (H)
RCL | HLT.
    
```

BSR, C Bit Set/Reset Mode.

↳ only with eight bits of Port C, which can be set or reset by writing an appropriate Control word in Control register.

when $D_7 = 0$

$D_7 = 0$ is recognized as BSR word, and does not alter any previously transmitted Control word with $D_7 = 1$: The I/O operations of Port A & B are not affected by a BSR Control word.



Set $PC_7 \& PC_3$

& repeat them after 10ms.

000 \rightarrow Bit 0

To set PC_7

7 6 5 4 3 2 1 0

P.

O, F CH

repeat PC_7

11 1 0

~~O~~ O

Set PC_3

0111

O7 CH

Set PC_3

0110

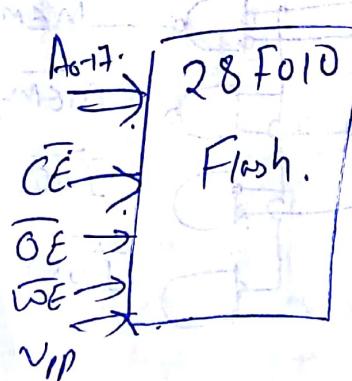
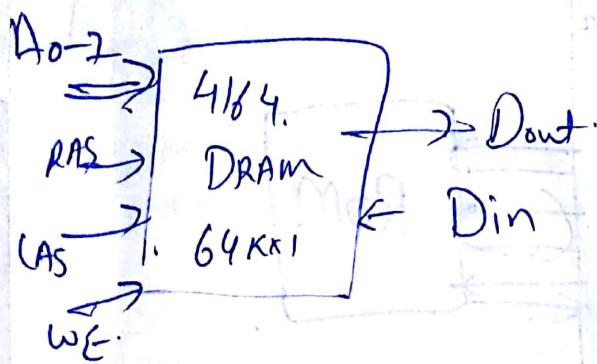
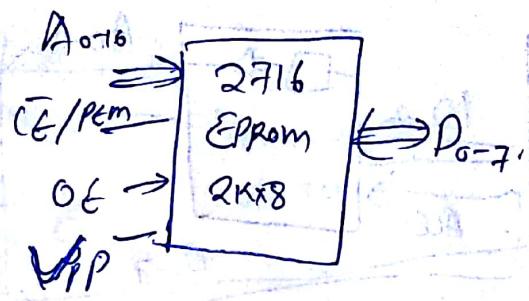
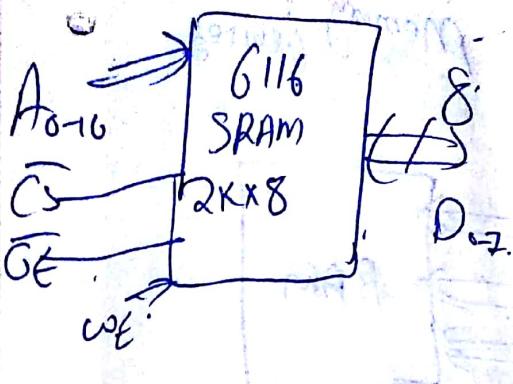
O8 CH

MVI A, 0F CH
OUT 83(CH)

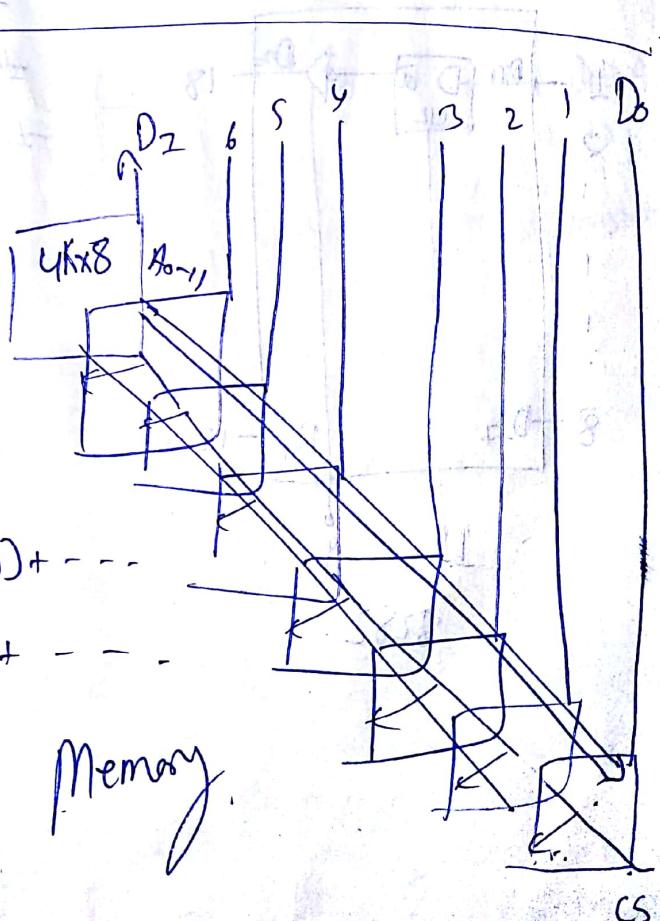
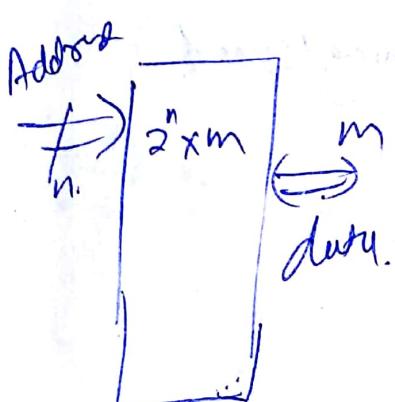
MVI A, 0E CH
OUT 83(CH)

RET/HALT

Typical organization of chips



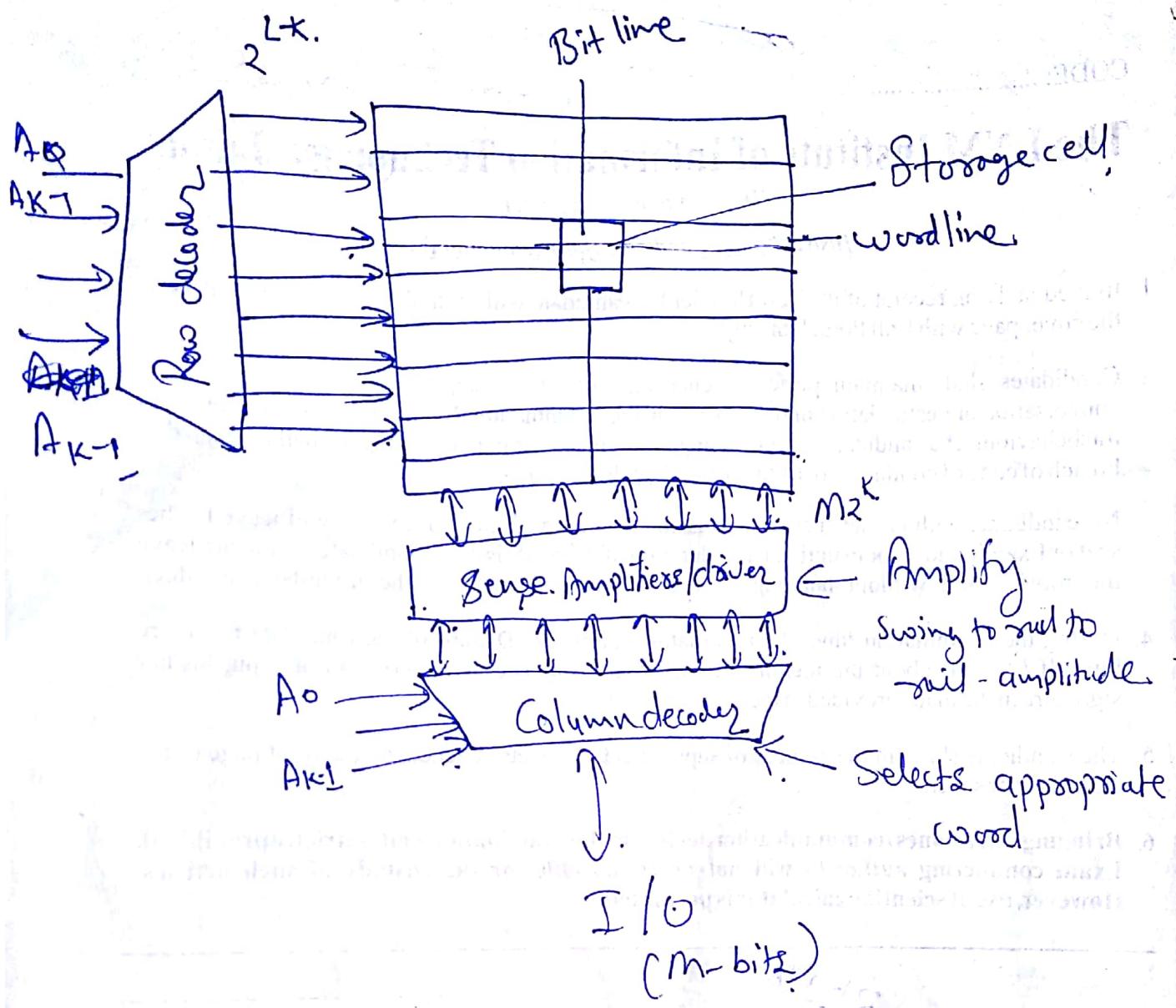
refreshing
by



$$\text{Byte} = 12(A) + 8(D) + \dots$$

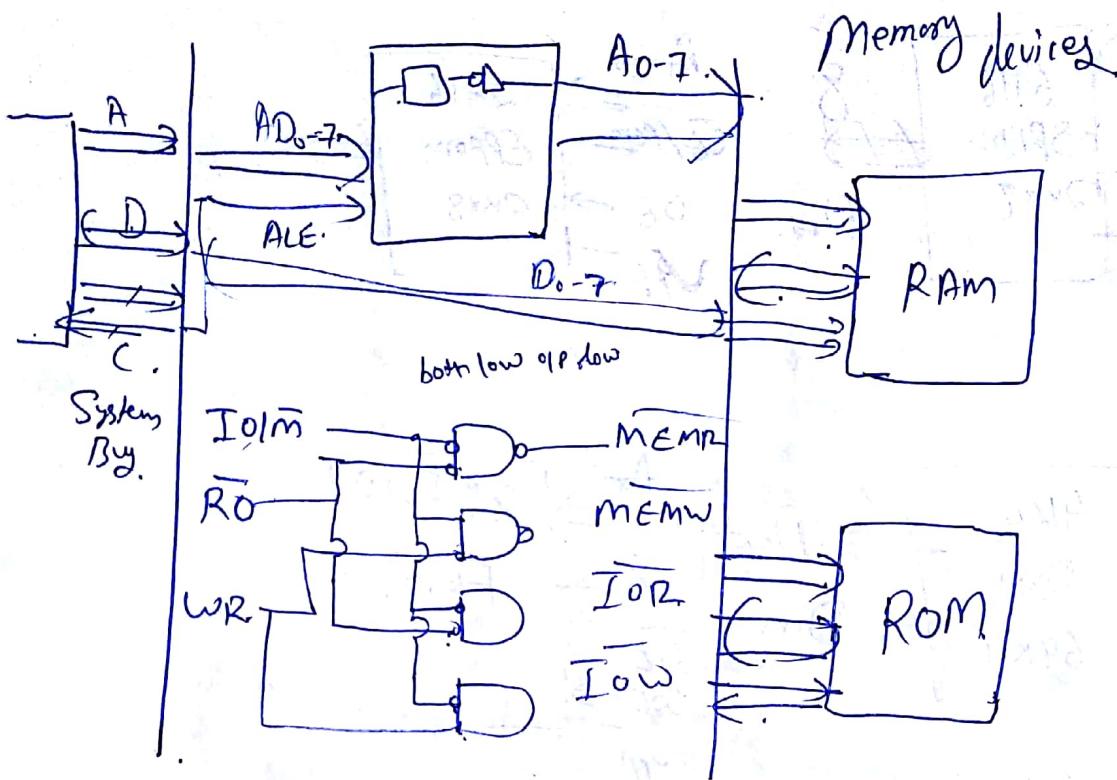
$$\text{Dit} = 12(A) + 1(D) + \dots$$

Memory.

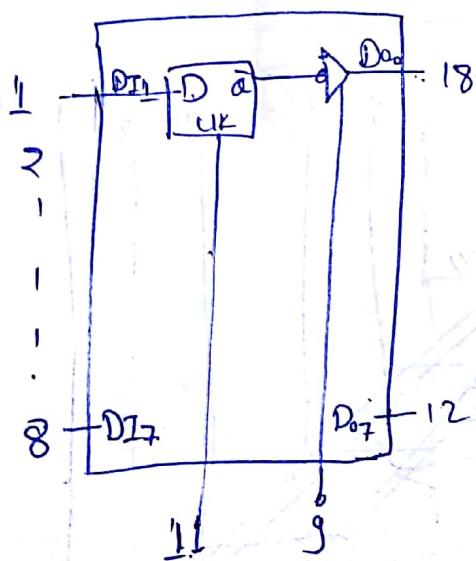


Typical Memory Organization

Incompatibilities in Memory If



→ Bus setup incompatibilities



Bus

Electrical

Timing / Speed

$$+ C_{AS} + C_{AUS} = 34\text{F}$$

$$+ C_{D1} + C_{D2} = 40$$

$$+ C_{D3} + C_{D4} = 40$$

$$+ C_{D5} + C_{D6} = 40$$

$$+ C_{D7} + C_{D8} = 40$$

$$+ C_{D9} + C_{D10} = 40$$

$$+ C_{D11} + C_{D12} = 40$$

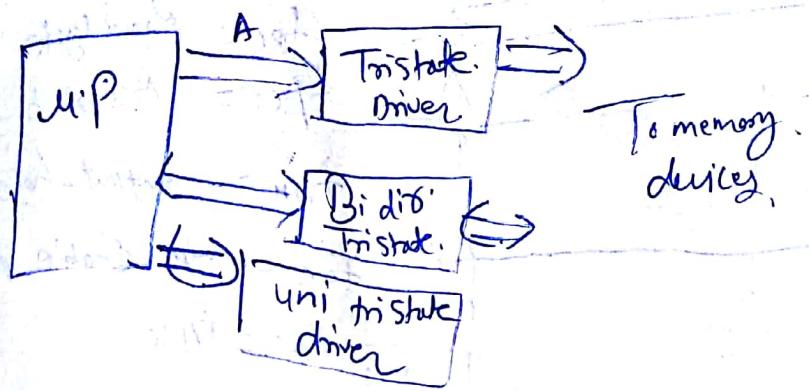
$$+ C_{D13} + C_{D14} = 40$$

$$+ C_{D15} + C_{D16} = 40$$

$$+ C_{D17} + C_{D18} = 40$$

Electrical Incompatibility

Voltage might same.
→ current driving
loop differ



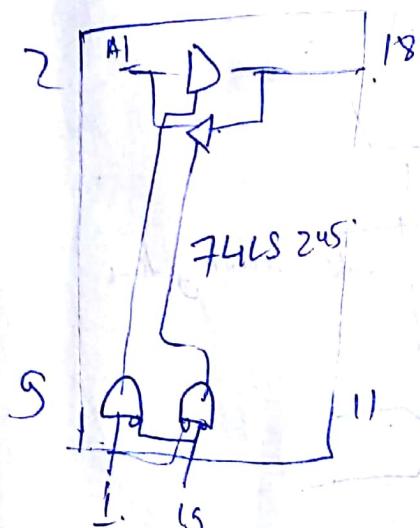
A_i \downarrow D_i
Active H/L
enable line

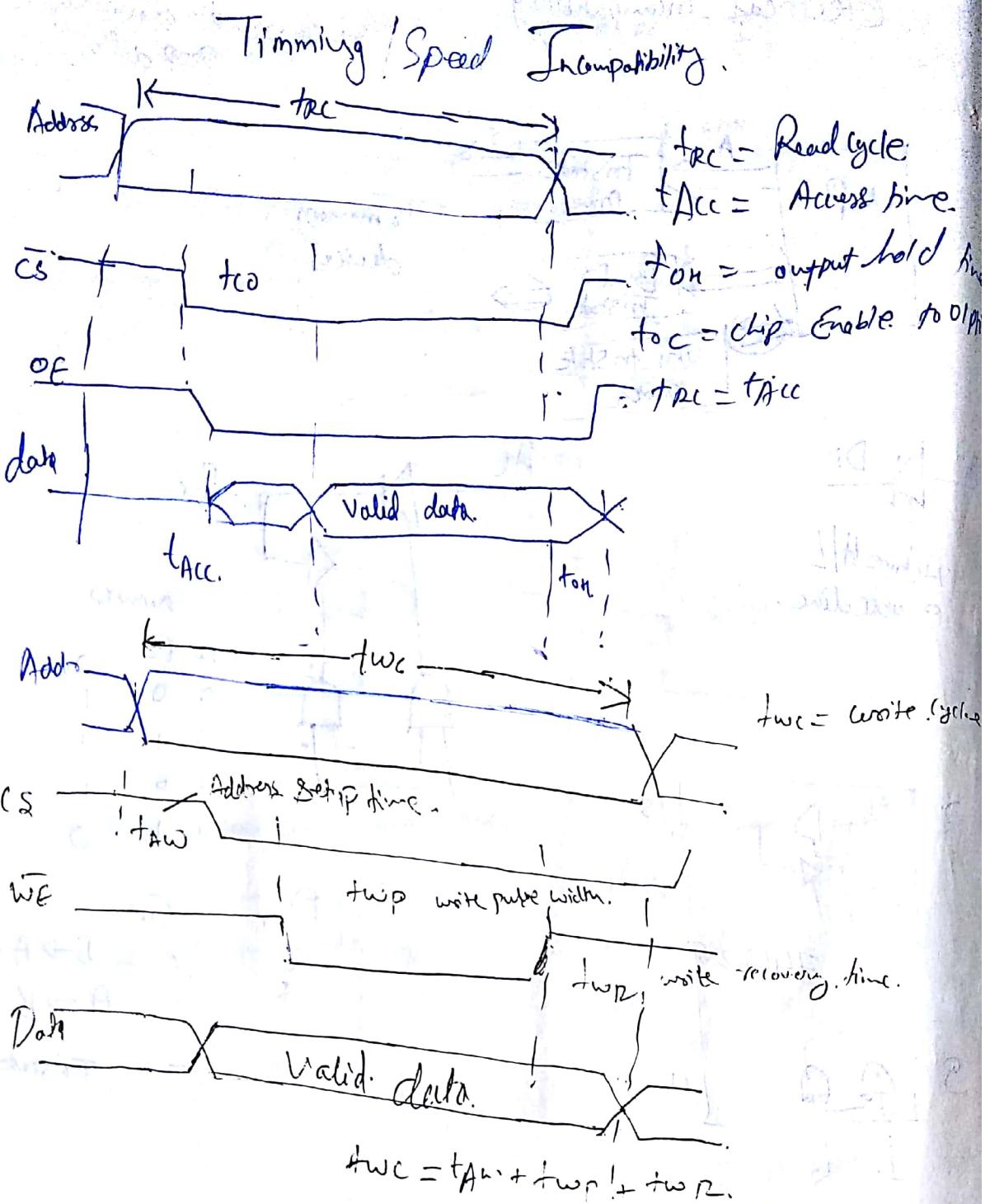
A_i \downarrow B_i

NAND

A	B
0	0
0	1
1	0
1	1

$D_{i,r}$ \downarrow E_r
 0 $\rightarrow B \rightarrow A$.
 0 $\rightarrow A \rightarrow B$.
 1 Tristate





$$t_{Ad} + t_{AS} = 225 \text{ nsec (8085)}$$

$$\text{Clock freq } T_{clock\ period} = 320 \text{ nsec}$$

$$2 \frac{1}{2} \times 320 = 800 \text{ nsec}$$

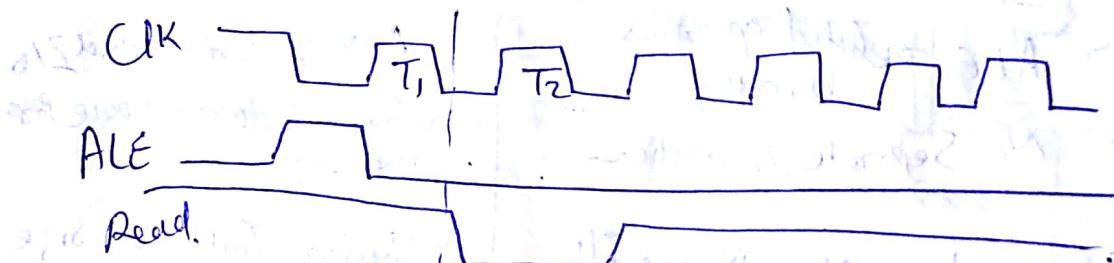
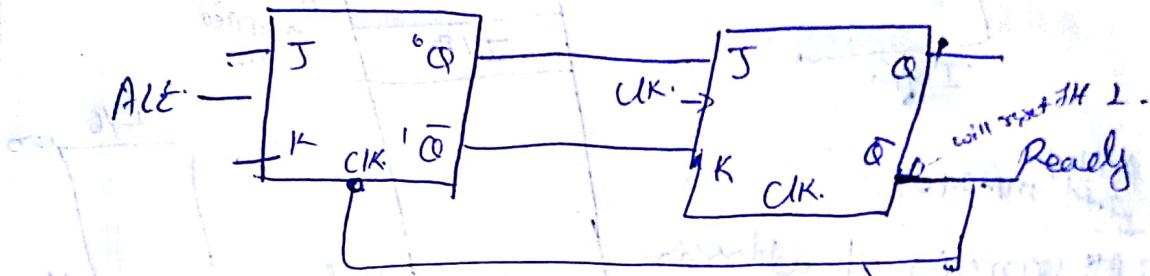
$$t_{Ad} + t_{AS} + t_{WE} = 800 \text{ nsec}$$

$$t_{WE} \leq 800 - 225 \Rightarrow 575 \text{ nsec}$$

Interfacing. Slow devices

① Slow down the freq.

② Using wait cycle.



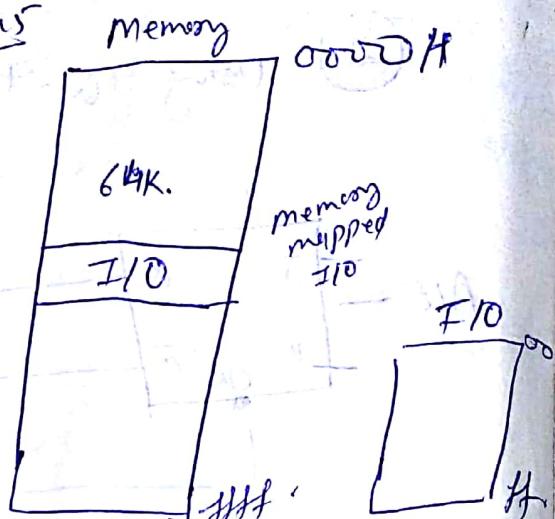
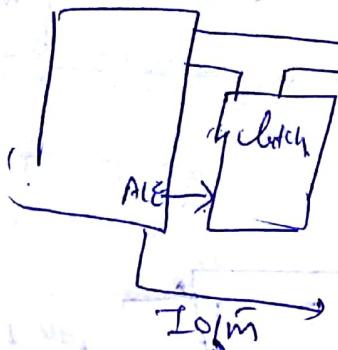
J K Q \bar{Q} $\bar{a} \bar{a}$ $a \bar{a}$

0 0 1 0 1 0

J	K	CK	Q
0	0	↑	Q_0 (clocking)
1	0	↑	1
0	1	↑	0

Q_0 toggles.

Address Space



Adv. of IMM I/O

→ Variety of address mode

→ ALE selected operations
 Directly.

→ No Separate Instruction.

dis adv Mem Mapp I/O

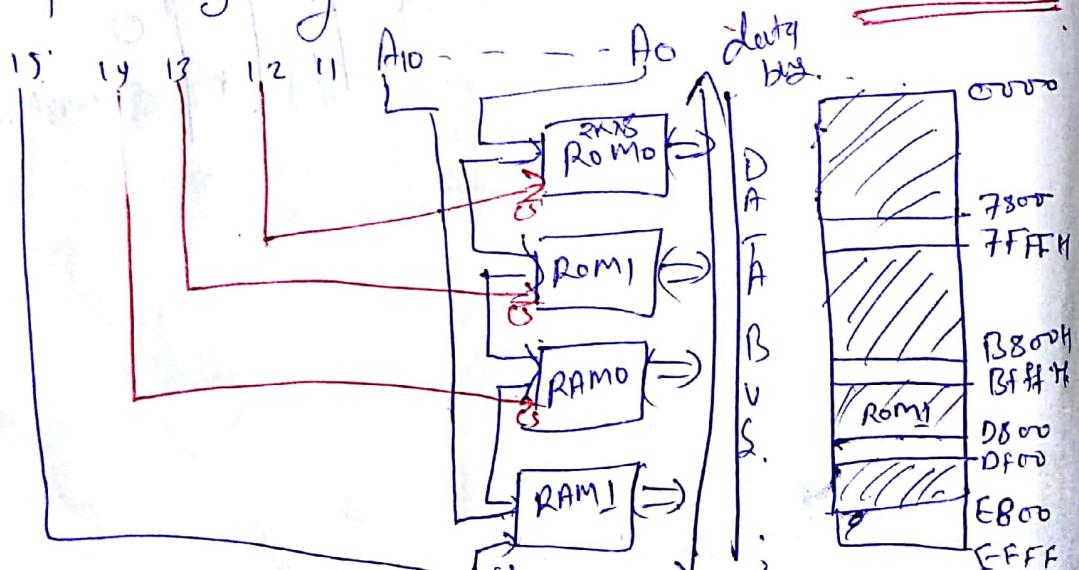
Addr Spaces occupied

Adv. of Post mapped I/O
→ Larger address space for
 memory

→ Shorter Instruction size
 Easy debugging.
→ Disadv. of Post mapped I/O
 → Extra pin is required
→ Separate Instruction.
 In/out
 (no data manipulation poss)

Partitioning of address space.

Bus contention



Partially decoded addressing.

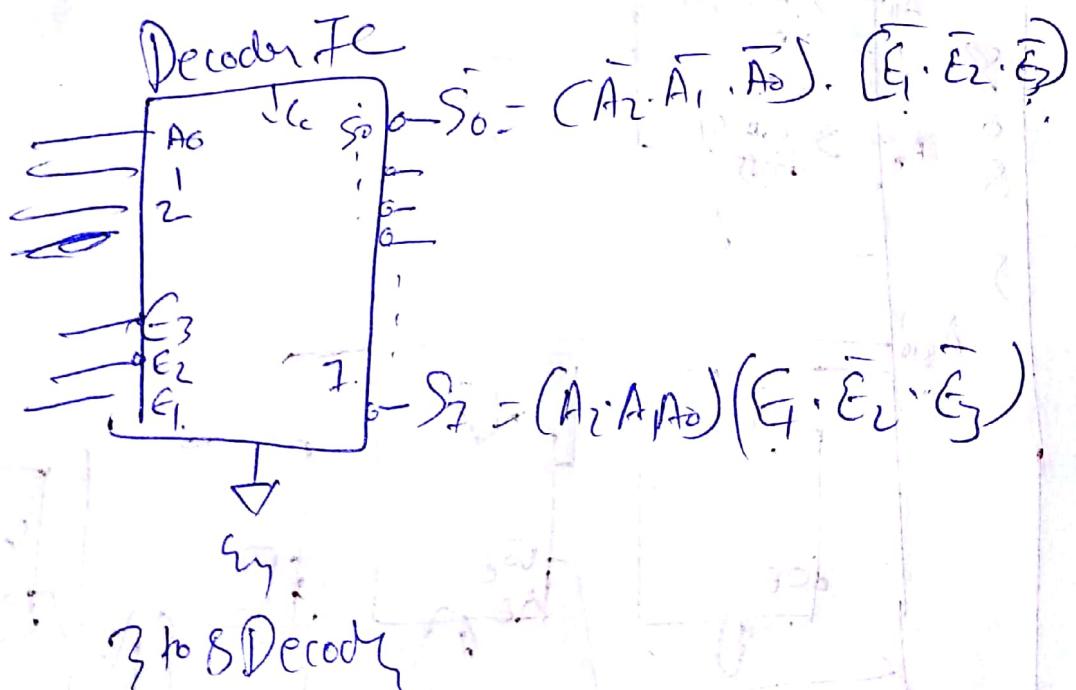
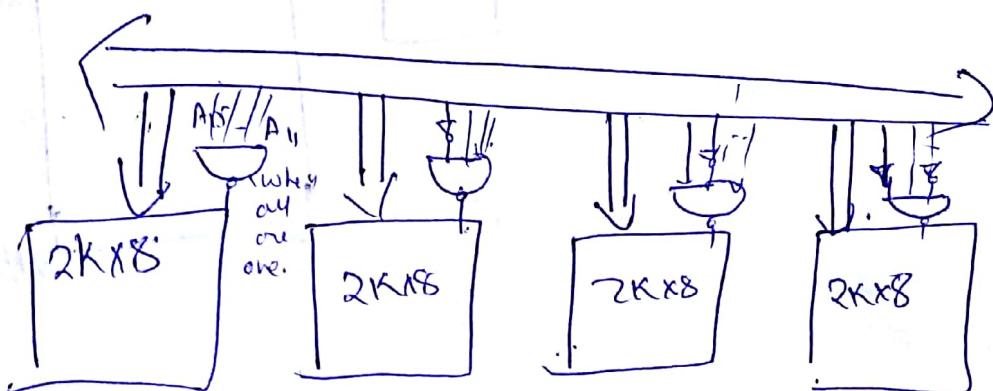
No two devices should be selected at the same time

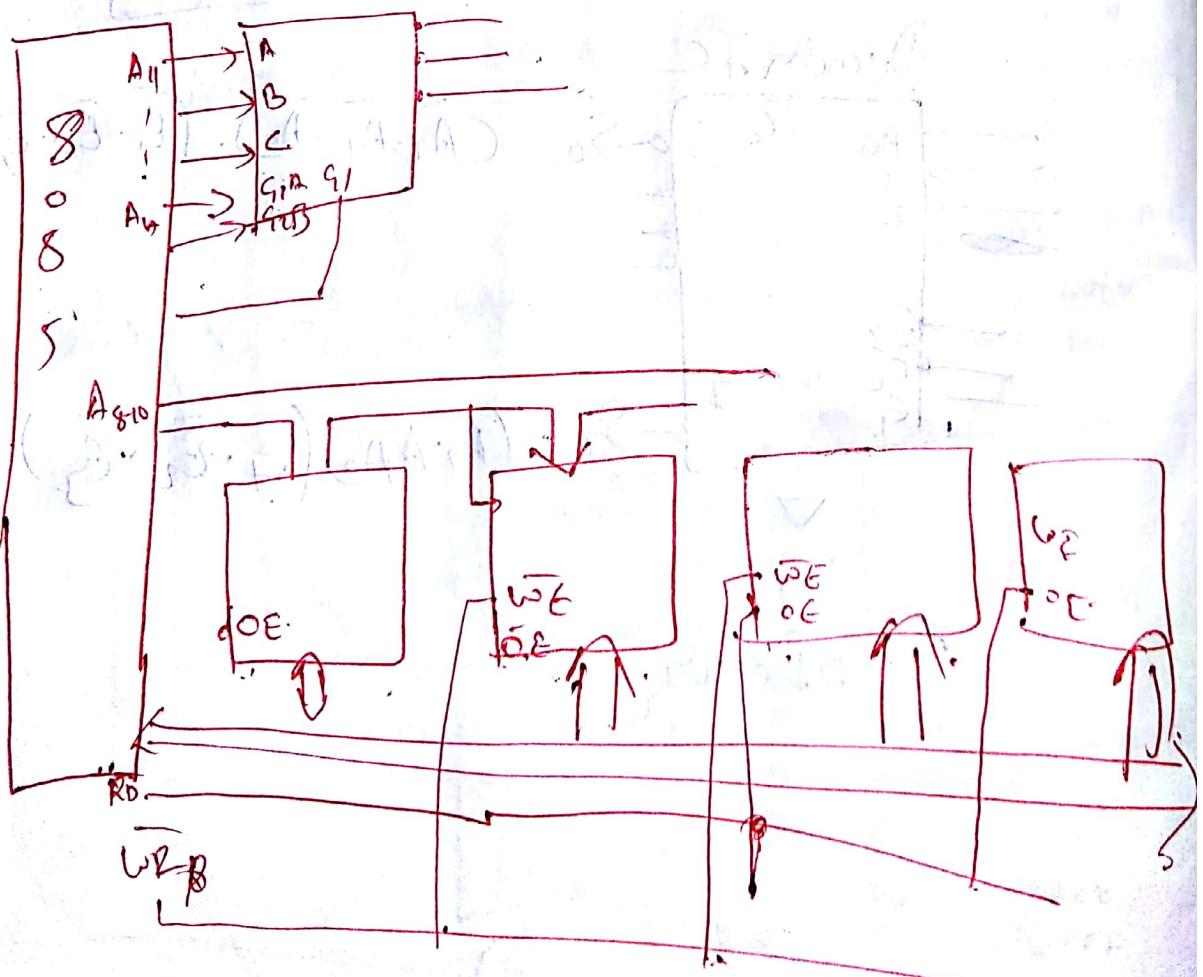
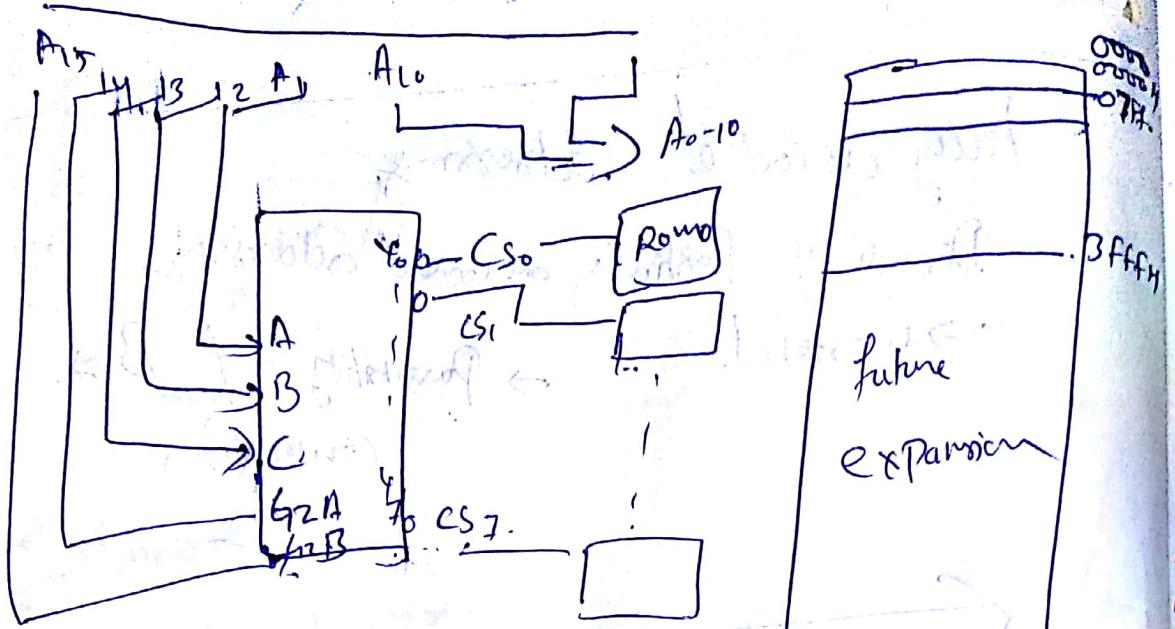
Fully decoded addressing.

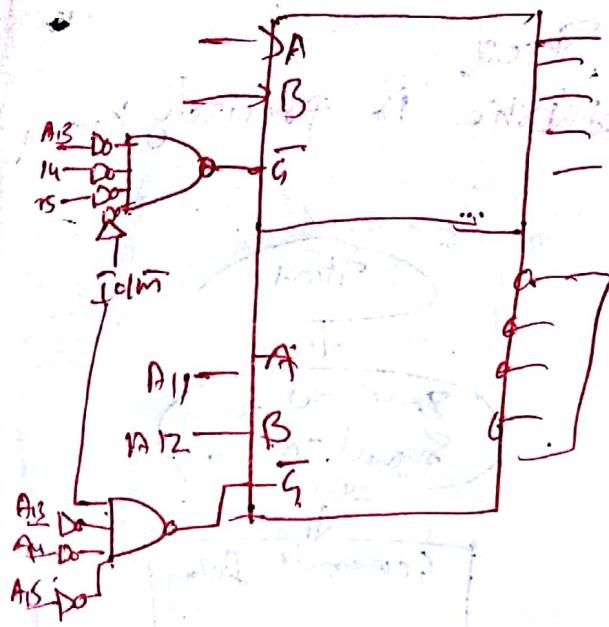
Disadv of partially decoded address

→ wasteful.

→ Possibility of Bus contention



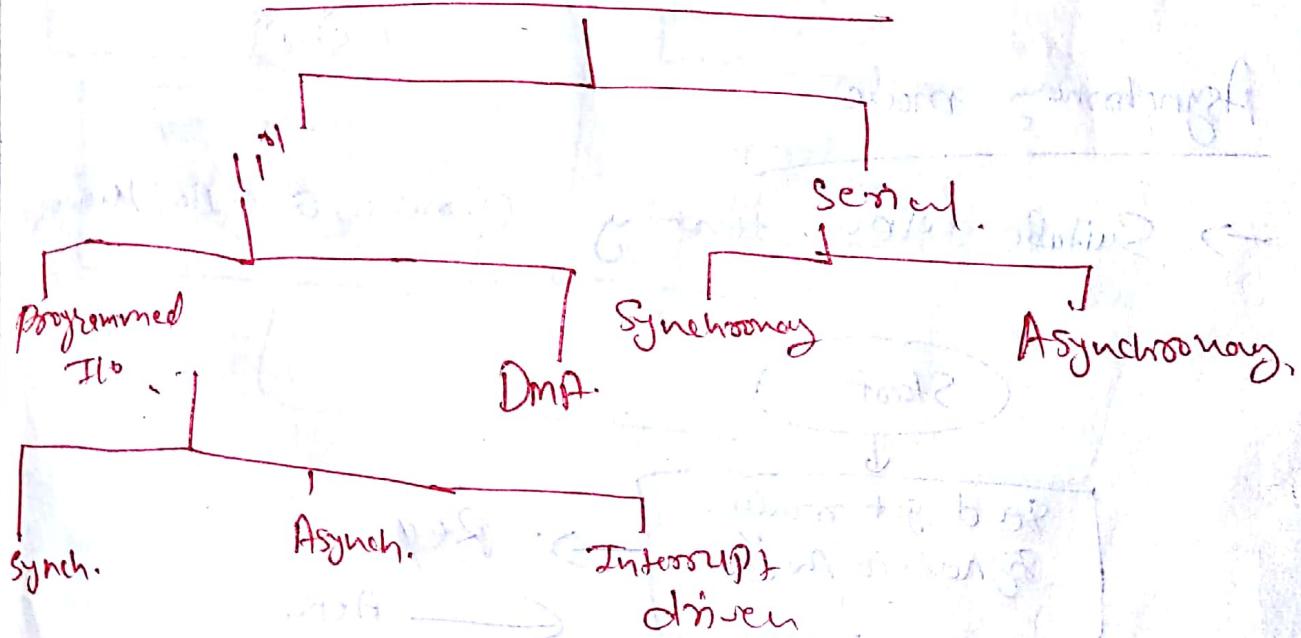




Chip Enable of Memory device.

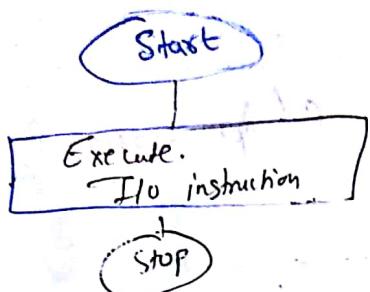
chip enable for Flopus

Modes of Data transfer



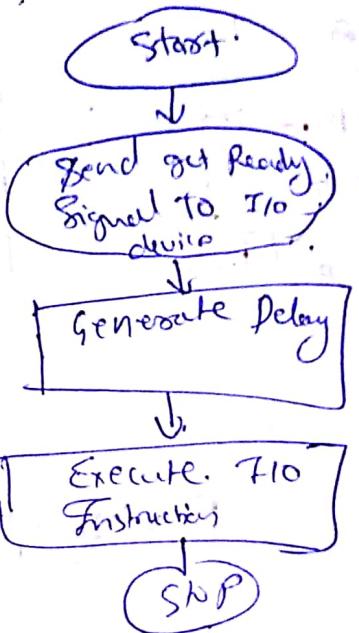
Synchrony Mode

- Compatible w.r.t Speed.
- If Speed Characteristic is precisely known



⇒ Simple.

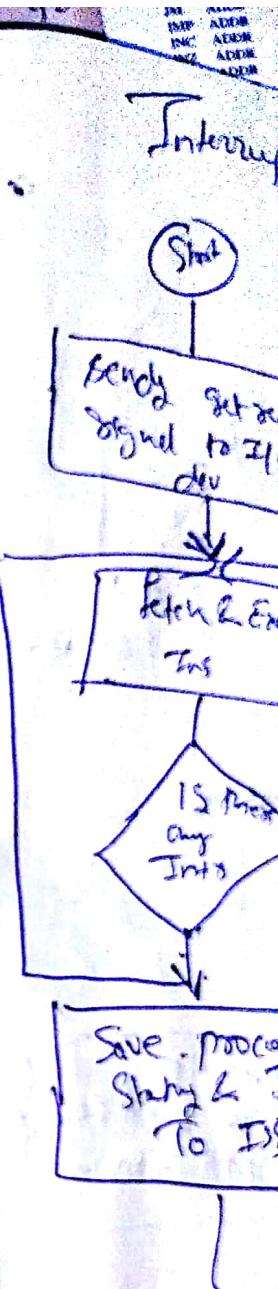
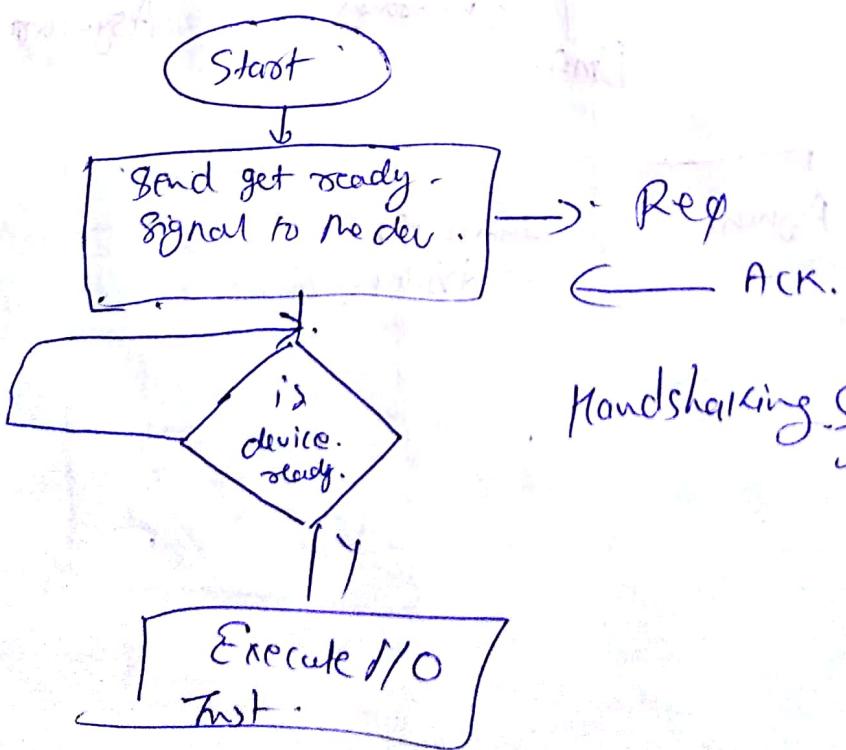
⇒ Not Suitable when
Speed char. of dev is not known



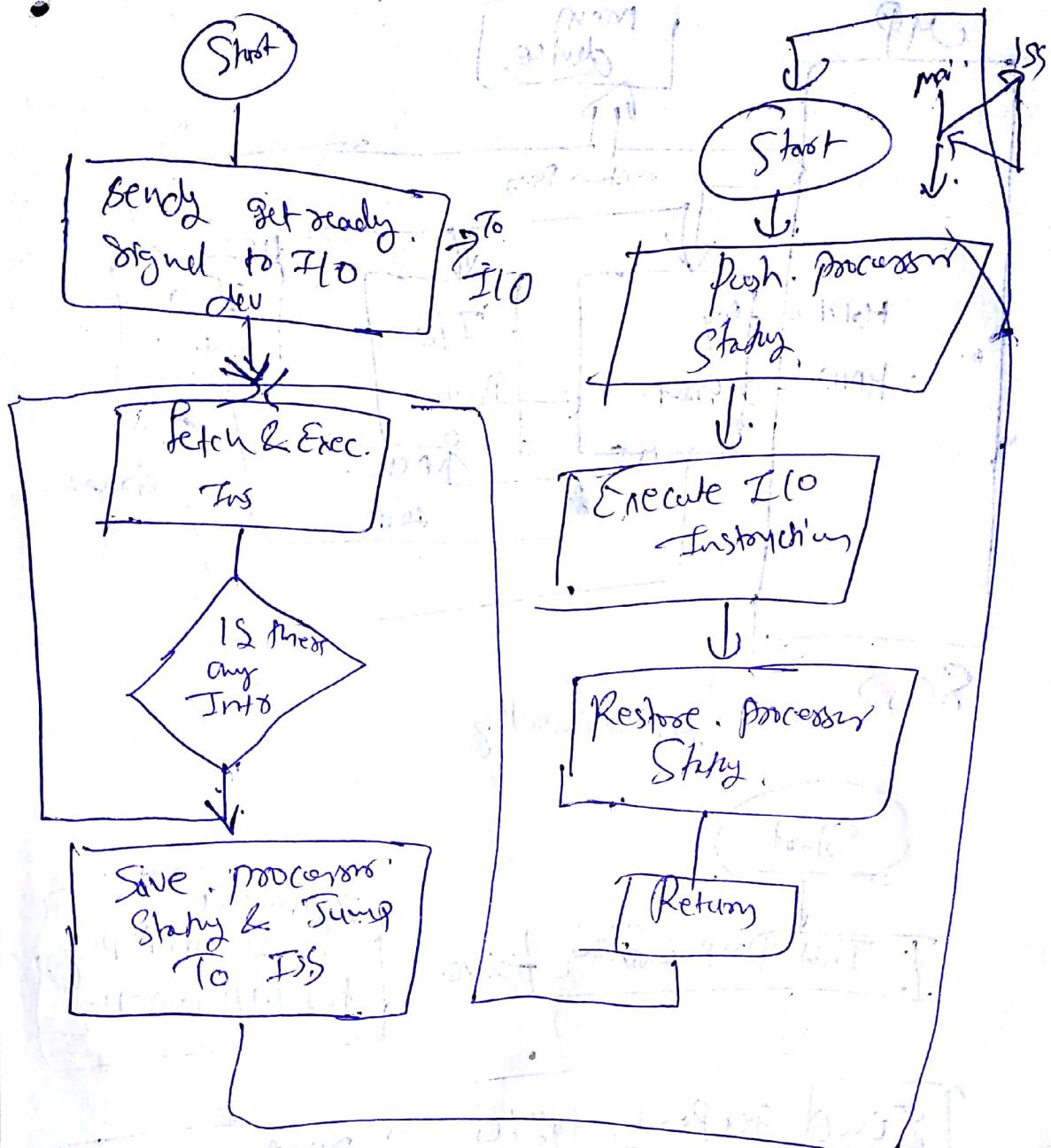
Asynchrony mode

→ Suitable when timing

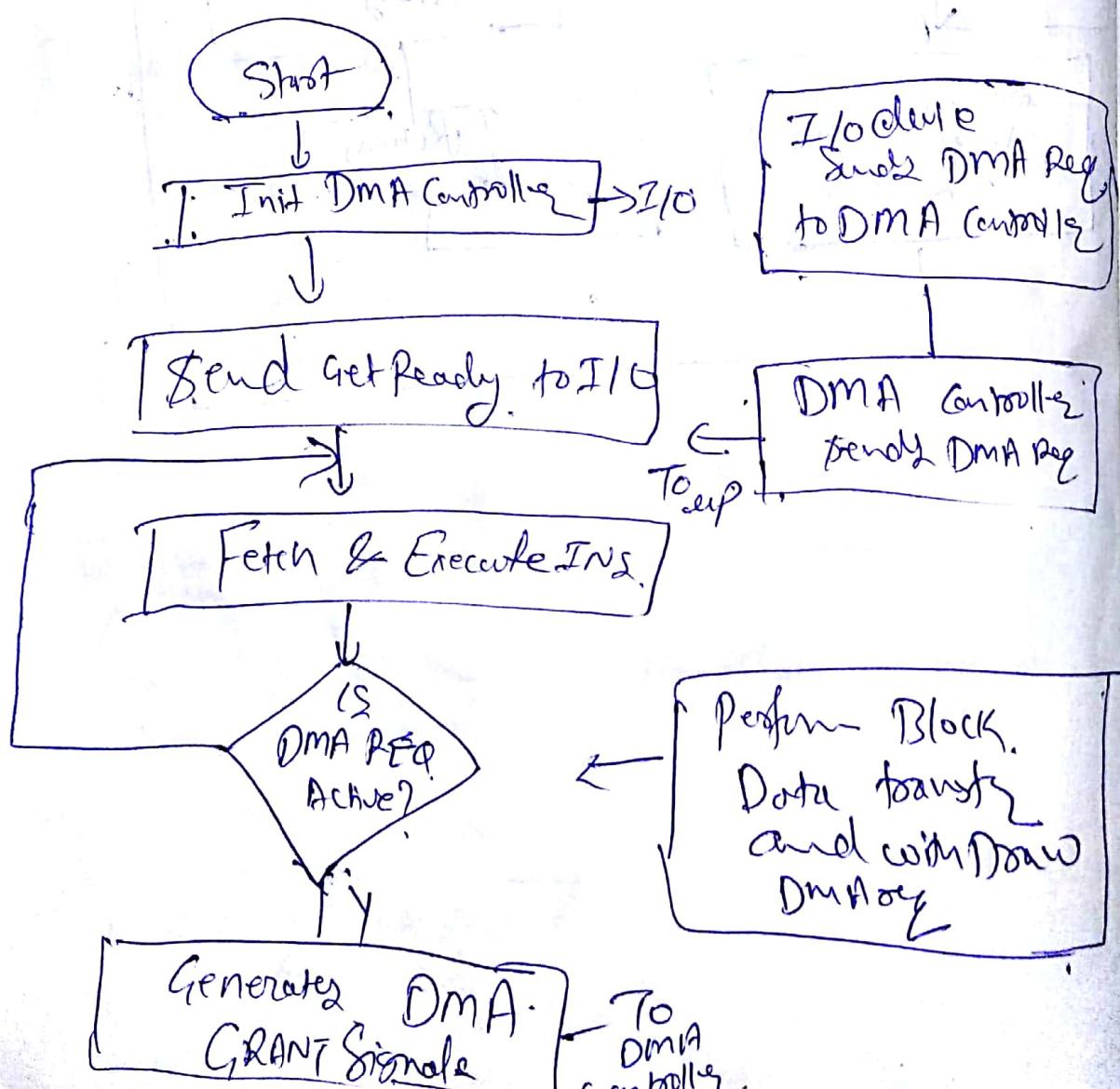
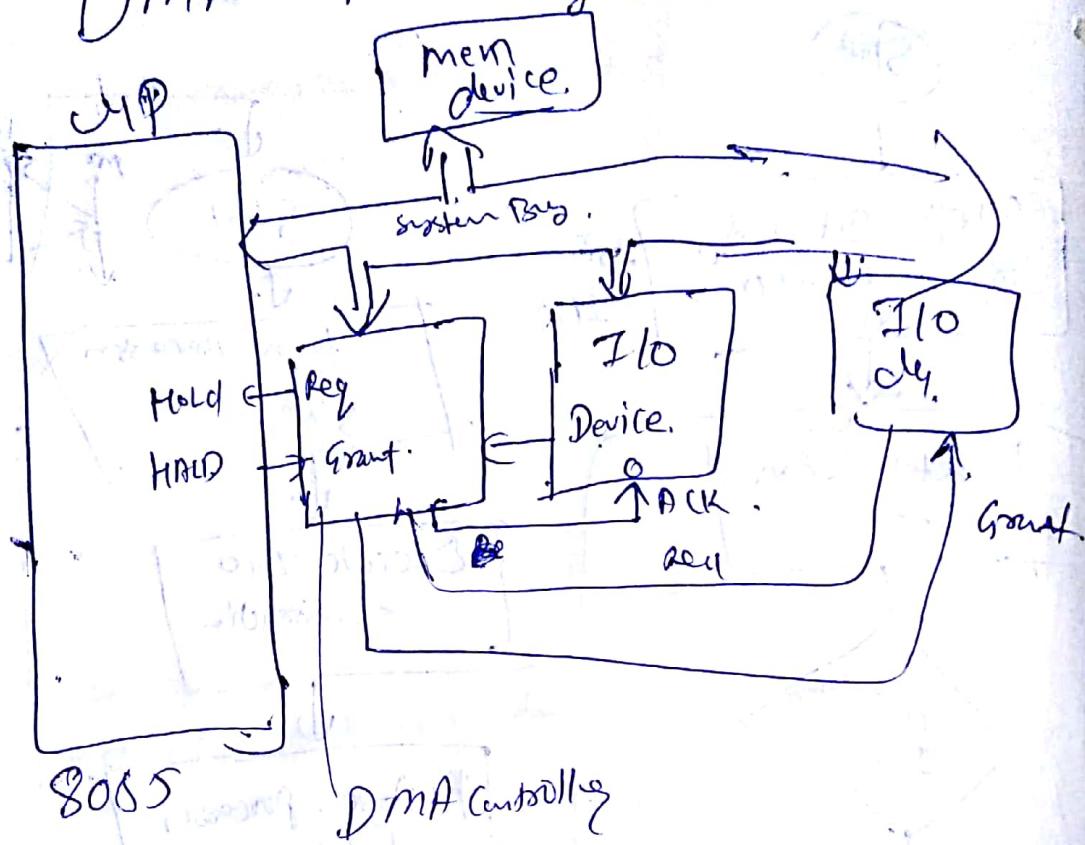
characteristics are not known



Interrupt driven mode



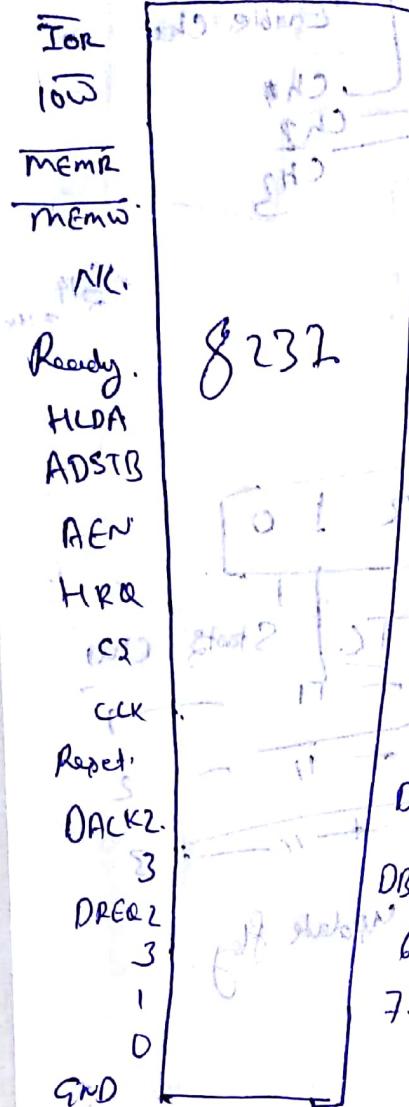
DMA Mode of DT.



DMA 8237

↳ is 110 to Processor (Slave mode)

↳ It is a data transfer processor to peripherals



A7

6

5

4

EOP

A3

2

1

0

Vcc

DB₀

1

2

3

DACK0

1

DB₅

6

7

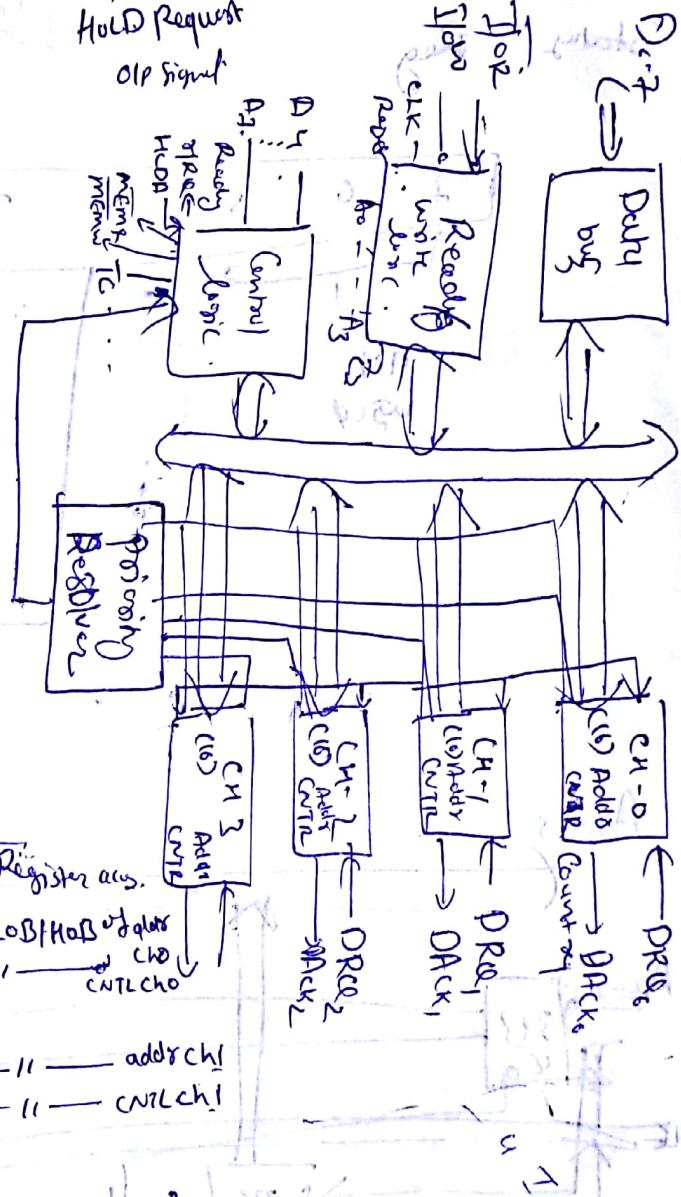
A EN

↓ Address enable.

H R Q . & H L D A .

HLD Request

OLP signal



Register acc.

Low bits of address
→ C10 CNTLCH0

addrch1
→ CNTLCH1

addrch2
→ CNTLCH2

addrch3
→ CNTLCH3

addrch4
→ CNTLCH4

addrch5
→ CNTLCH5

addrch6
→ CNTLCH6

addrch7
→ CNTLCH7

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

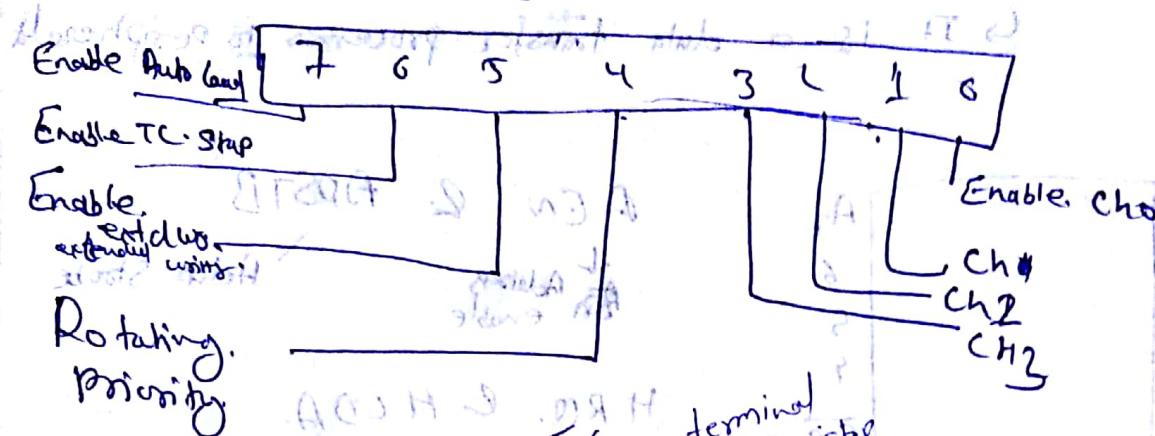
Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

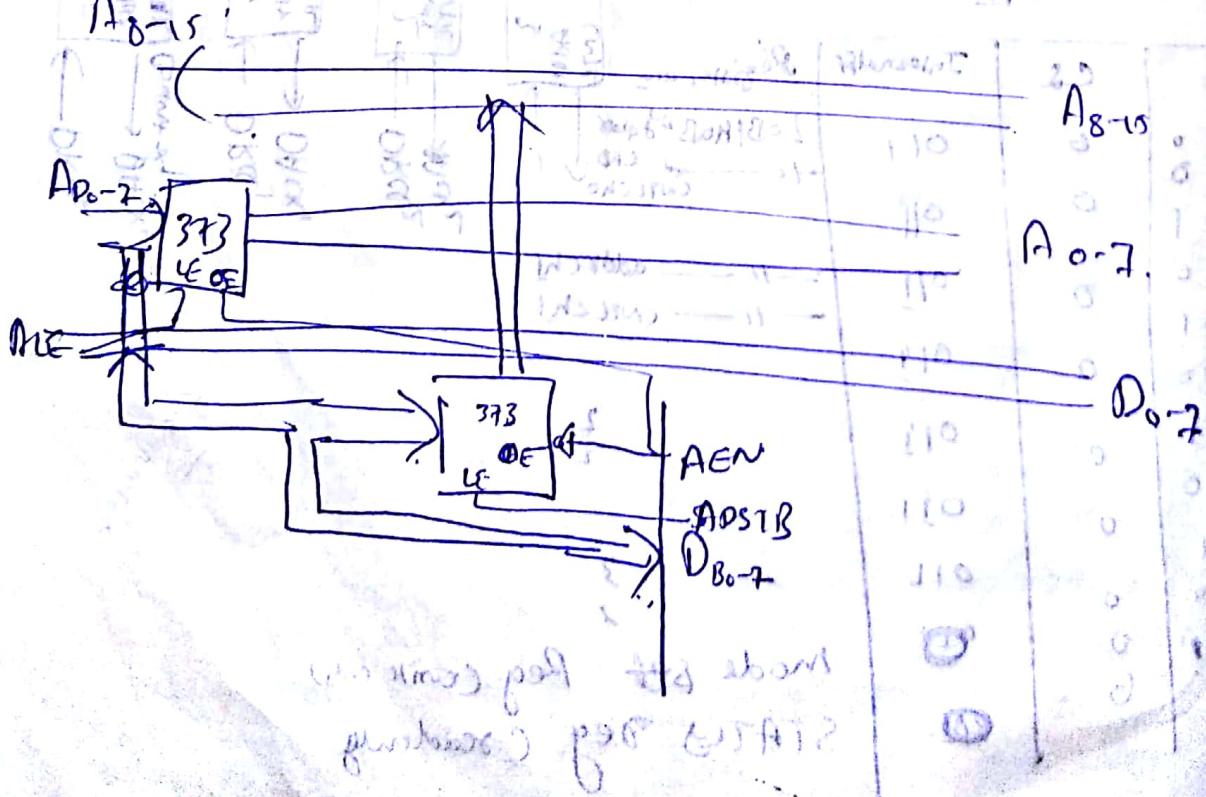
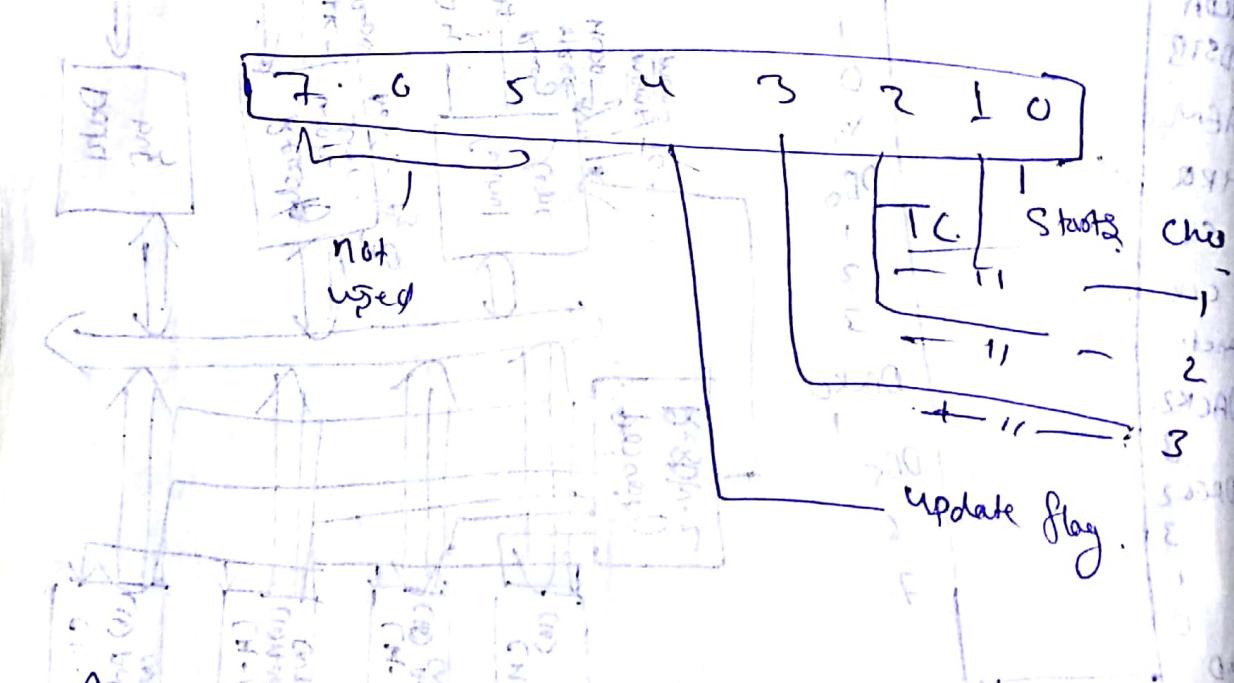
Address	C2	Internalff
A32 1 0	0	011
0 0 0 0	0	011
0 0 0 1	0	011
0 0 1 0	0	011
0 0 1 1	0	011
0 1 0 0	0	011
0 1 0 1	0	011
0 1 1 0	0	011
0 1 1 1	0	011
1 0 0 0	0	011
-1 0 0 1	0	011

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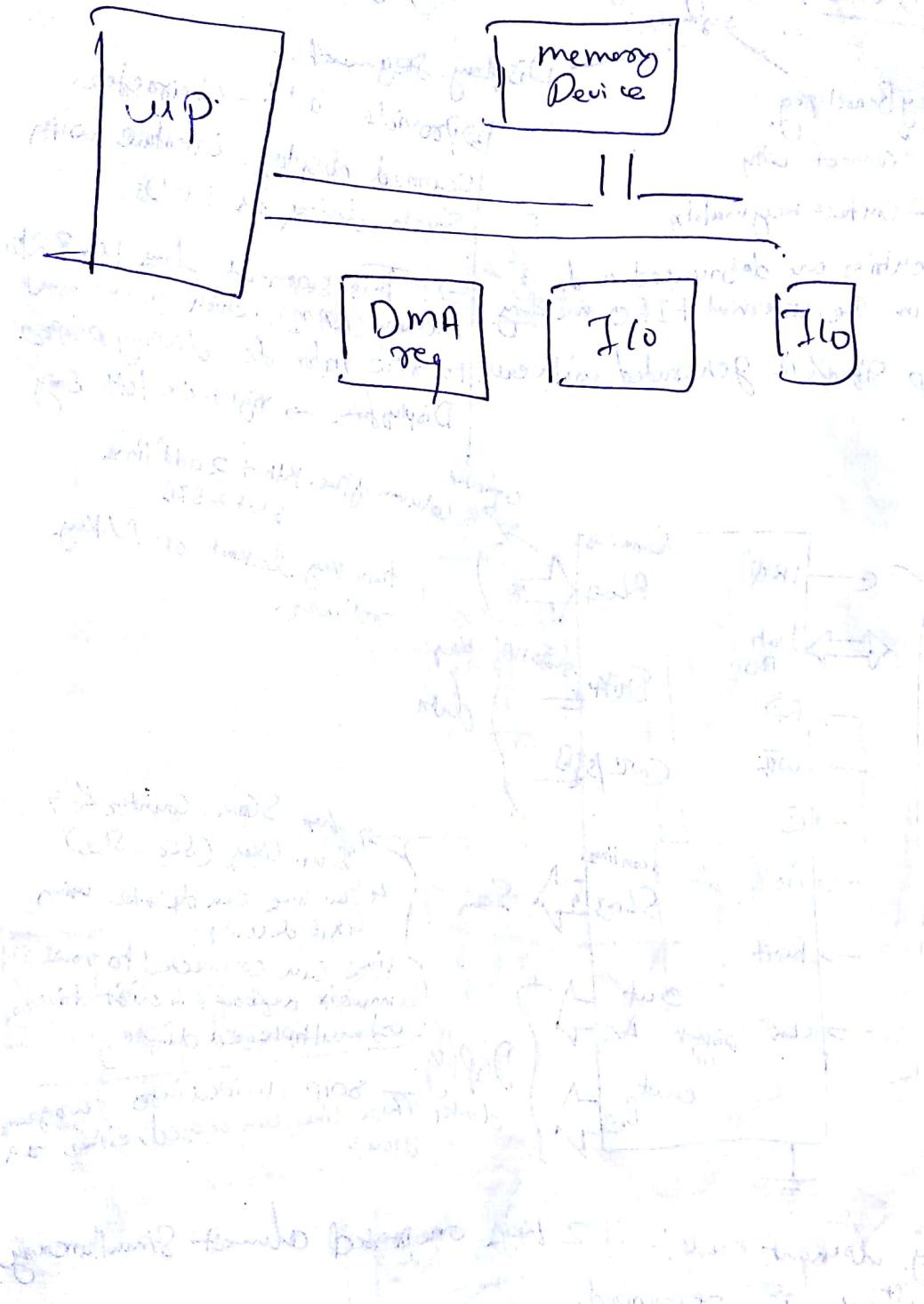
Mode Set Reg



Status Reg.



DAA	: Decimal-Adjust A	27	1/1/4	F
DAD Rp	: Add Reg. Pair to HL	00RP 1001	1/3/10	FB
DCR REG	: Decrement Reg.	00S S101	1/1/4	B
DCR M	: Decrement Mem. Contents	33	1/3/10	P
DCX Rp	: Decrement Reg. Pair	00RP 1011	1/1/6	RW
DI	: Disable Interrupt	F3	1/1/4	S
EI	: Enable Interrupt	FB	1/1/4	P
HLT	: Halt	76	1/2/5	F
IN PORT REG	: Input from 8-bit Port	DB data 00SS S100	2/3/10	FB
	: Increment Reg.			PRI



8279: Prog. Keyboard / Display Interface.

Keyboard reg.

to connect with

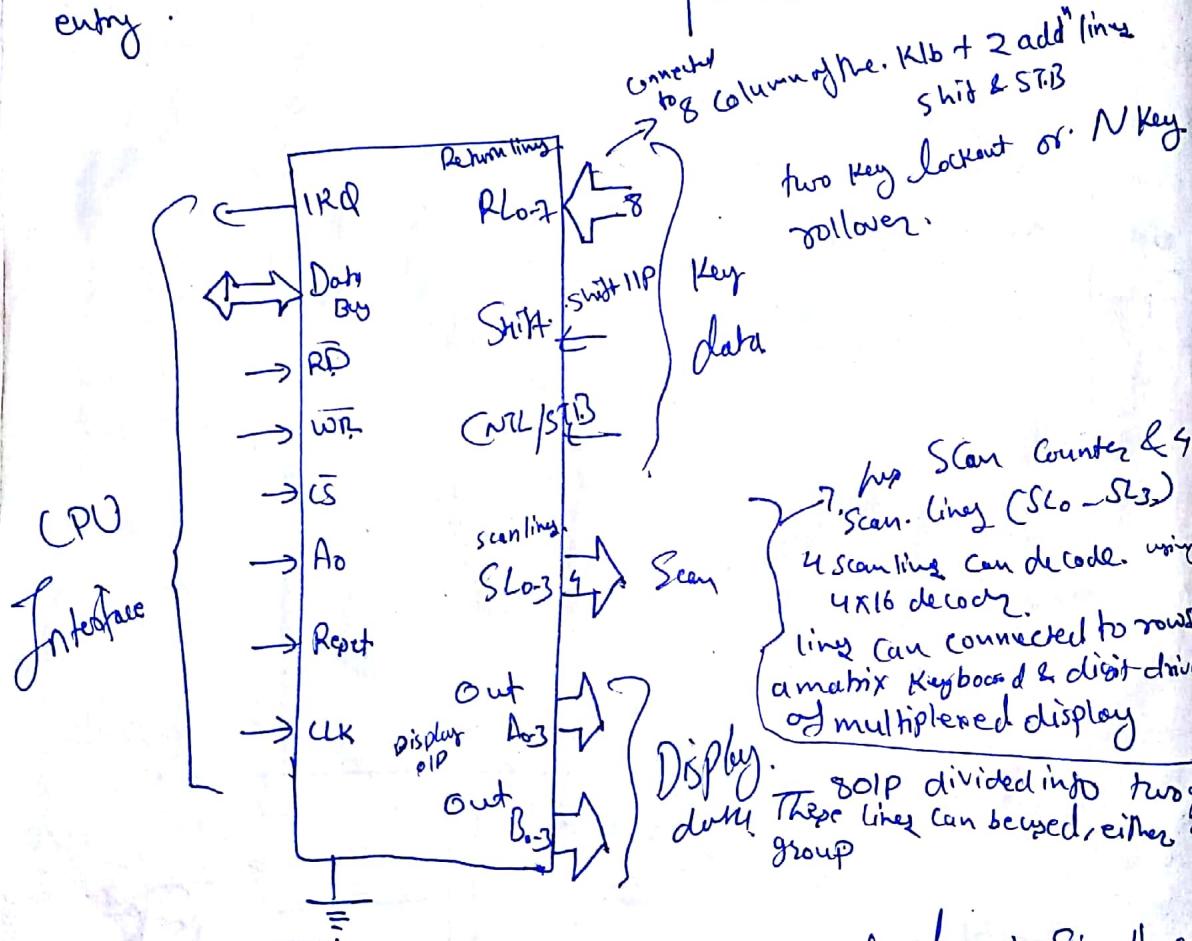
64 - Contact key matrix

Kb entries are debounced and stored in the internal FIFO memory.

& interrupt signal is generated with each entry.

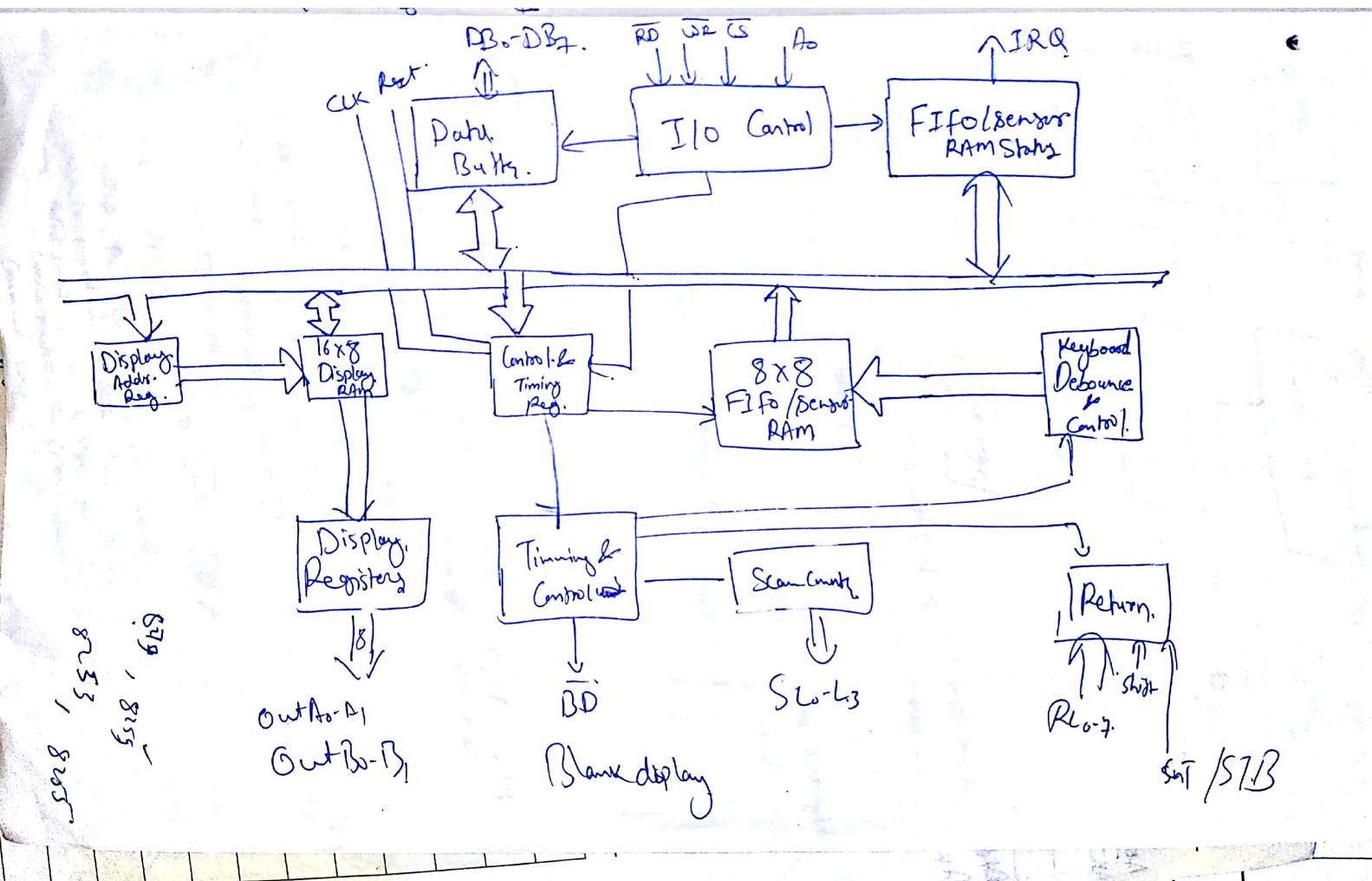
Display segment.
Provide a 16-character scanned display interface with such devices as LEDs.

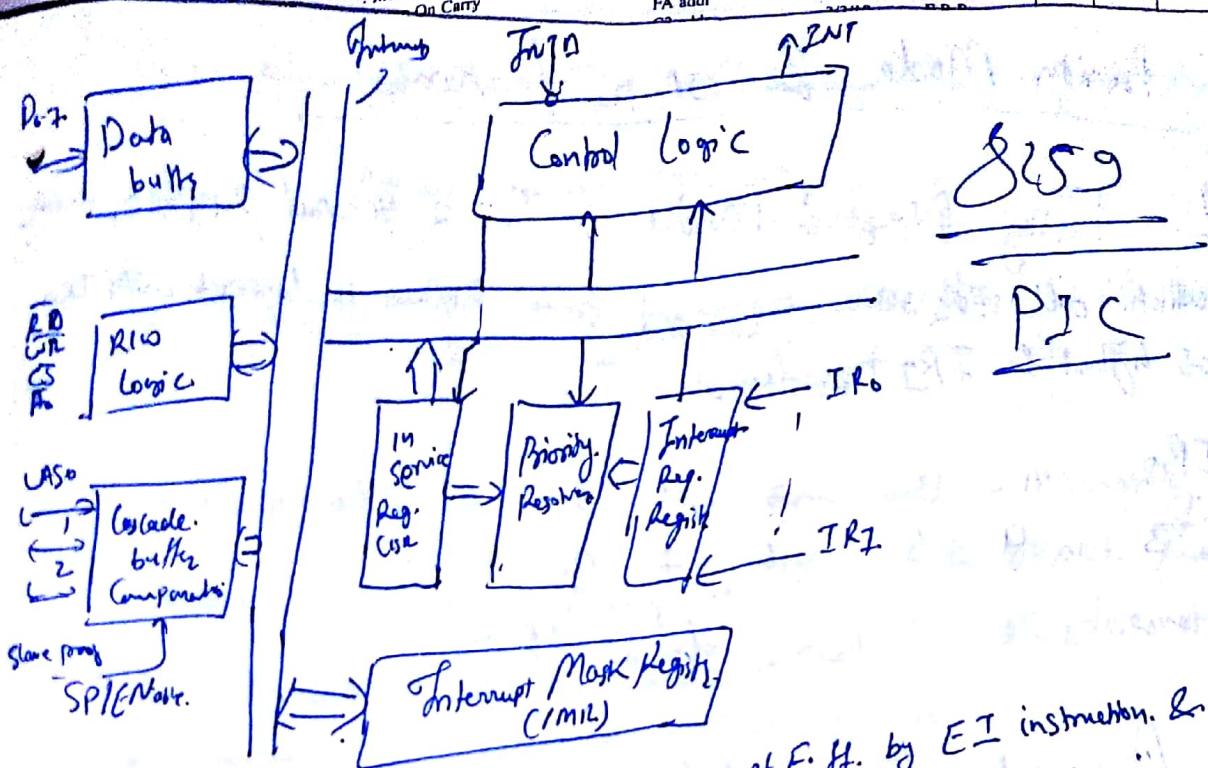
⇒ This segment has 16×8 RAM memory (RAM), which can be used to store info for display purpose.
Display from → right or left Env.



In 'two key. lockout mode':- if 2 keys are pressed almost simultaneously, only the 1st key is recognized.

In 'N-key rollover mode':- simultaneous keys are recognized & their codes are stored in internal buffer. it can also be setup so that no key. is recognized until only 1 key remain pressed.





To To Enable Interrupt \rightarrow Interrupt E. H. by EI instruction. &
8259A should be initialized by writing control words in

Control Reg.
Initialization (Command word (ICW)) \rightarrow T6 perform functions like masking interrupt, setting up status-read operation etc.
operation: Command words.

to set the proper conditions & specify RST vector address.

- ① IRR Stores the req priority resolver checks three reg. i.e. IRR, IMPR & ISR.
- ② To resolve the priority. \leftarrow Set INT high when appropriate.
- ③ MPU ack. the interrupt by sending INTA.
- ④ After INTA is received, \rightarrow appropriate ISR is set to indicate which interrupt level is being served. \leftarrow corresponding bit in IRR is reset to indicate req isn't pending.
- ⑤ Call operation. in two INTA Signals. on data bus.
- ⑥ In INTA, Run Call to B the Call M0B. The Call address is Vector bit which is placed in C0P0 during initialization.
- ⑦ During. Third INTA \rightarrow ISR is reset either AGO or EO (using command word) at end of service routine. This option is determined by initialization of command word (ICW).

Priority Mode & Other features

1. Fully Nested Mode :- This is general purpose mode in which all IRs are arranged from highest to lowest, with IR_0 as highest & IR_7 as lowest.

IR_0	1	2	3	4	5	6	7
3	4	5	6	7	0	1	2

↓ ↑
lowest highest

2. Automatic Rotation Mode :- A device after being serviced, receives the lowest priority.
e.g. IR_2 has just been serviced, it will receive the seventh priority as shown

IR_0	1	2	3	4	5	6	7
5	6	7	0	1	2	3	4

Specific Rotation Mode :- Similar to automatic

rotation mode except that the user can select any IR for lowest priority, thus fixing all prioritizing.

EI → End of Interrupt

After completion of an interrupt service, the corresponding ISR bit needs to be reset to update the information in ISR. This is called EI Command.

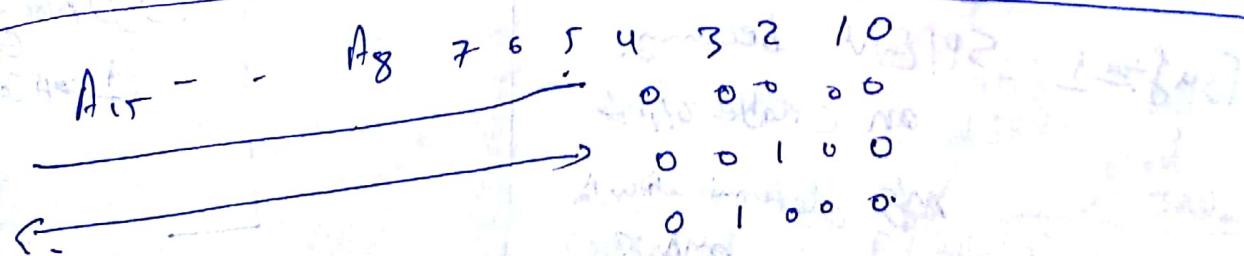
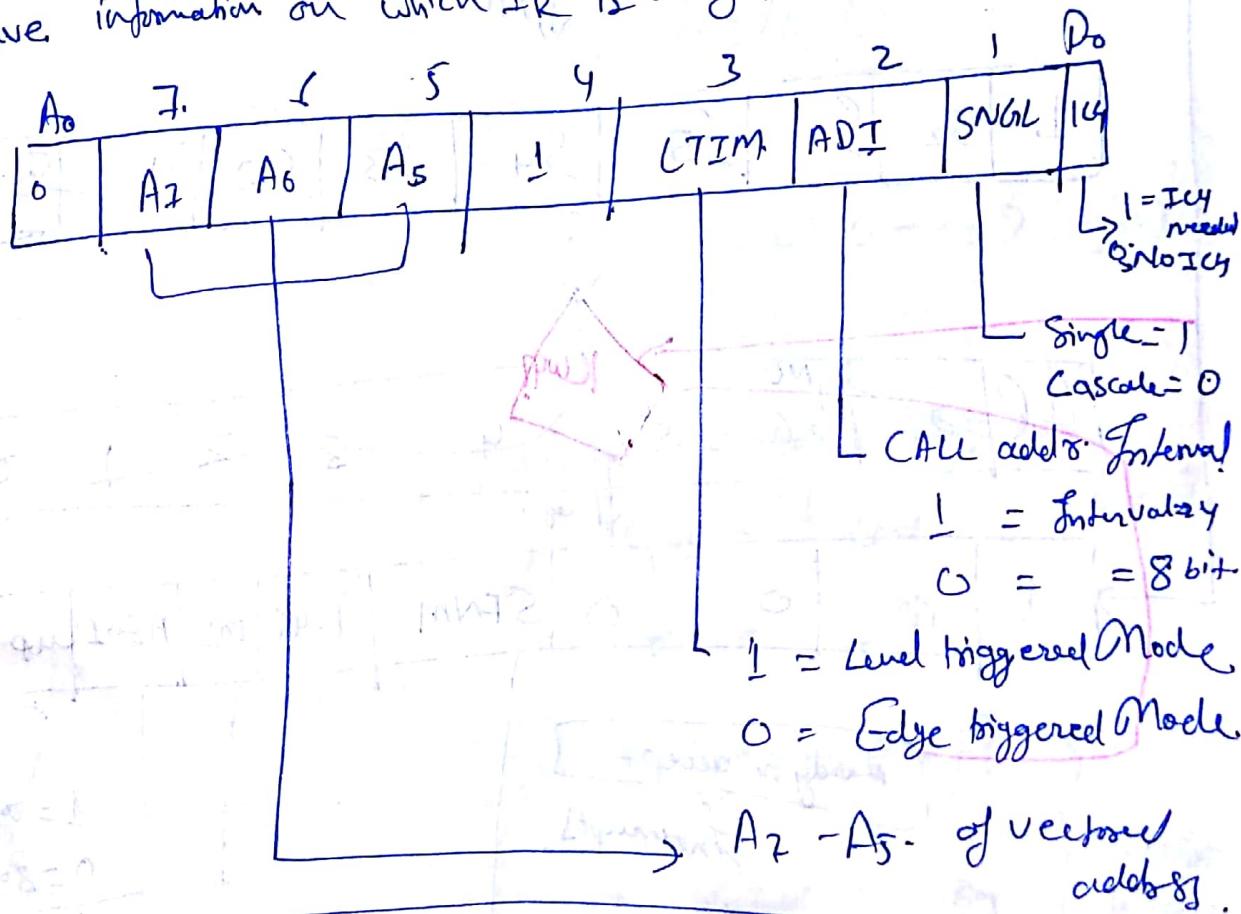
Can be issued in three formats

① Non Specific EOI Command :- it reset the

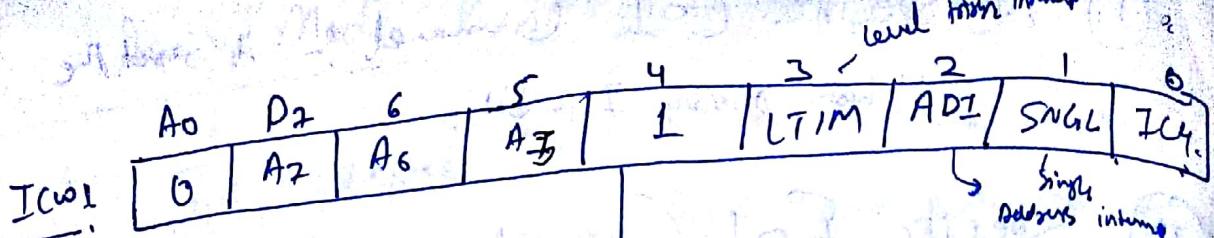
highest priority ISR bit.

② Specific EOI Command :- specifying which ISR bit to reset.

③ Automatic EOI :- no command is necessary.
During the third INTA, the ISR bit is reset. The major drawback with the mode is that the ISR does not have information on which IR is being serviced.



0000
1000



1	15	14	13	12	11	10	9	8
---	----	----	----	----	----	----	---	---

Single

NO

1	S ₇	S ₆	S ₅	S ₄	S ₃	S ₂	S ₁	S ₀
---	----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------

ICW4

Yes.

(1)	S ₇	NO	S ₄	S ₃	S ₂	S ₁	S ₀
-----	----------------	----	----------------	----------------	----------------	----------------	----------------

1	0	0	0	SFNM	B4F	m/s	AG01	up
---	---	---	---	------	-----	-----	------	----

Ready to accept
Interrupts.

Buf = 1 SP/EN becomes
an enable o/p &
m/s determination
by M/S.

$$1 = 8083 \frac{1}{8}$$

$$0 = 8085$$

\Rightarrow Normal
G0L

$1 \Rightarrow A$ G0L

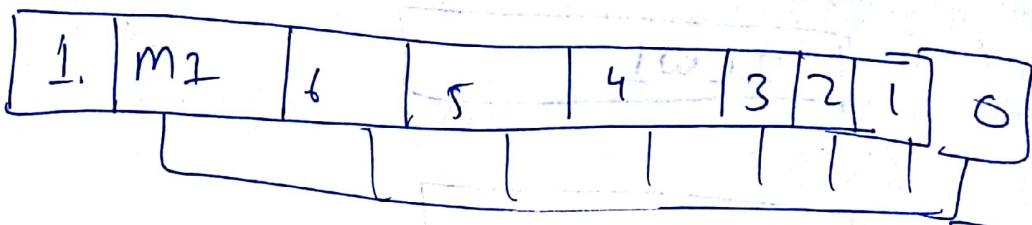
1 → Special fully
nested mode

0 = NSFNM

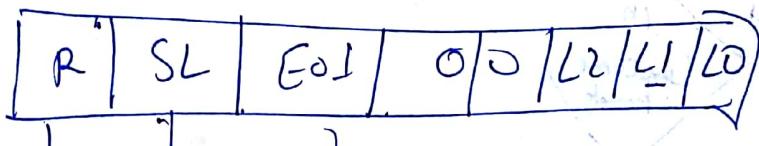
JC	ADDR	: Jump On Carry	D1 addr	3/3/7-10	FRR
DDR		: Jump On Minus	D2 addr	3/3/7-10	FRR
		: Unconditional Jump	C3 addr	3/3/10	FRR
		Carry	C2 addr	3/3/7-10	FRR

Operational Command word.

O CW → 1 Csel's & other mask bits in IPR



0



1 0 0 1

3 0 1 1

→ Non Specific EoI Command } EoI

→ Specific EoI Command }

5

→ Rotate on Non-Specific EoI Cmd

4

→ - " - AEoI (cont) } AEoI

0

→ - " - Clear }

7

→ Rotate in Specific EoI }

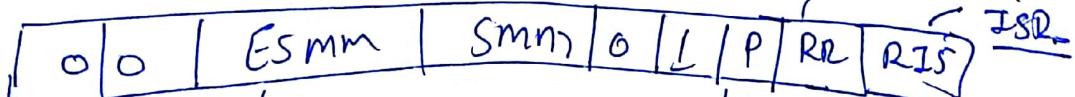
6

→ Set Priority }

2

→ Nop }

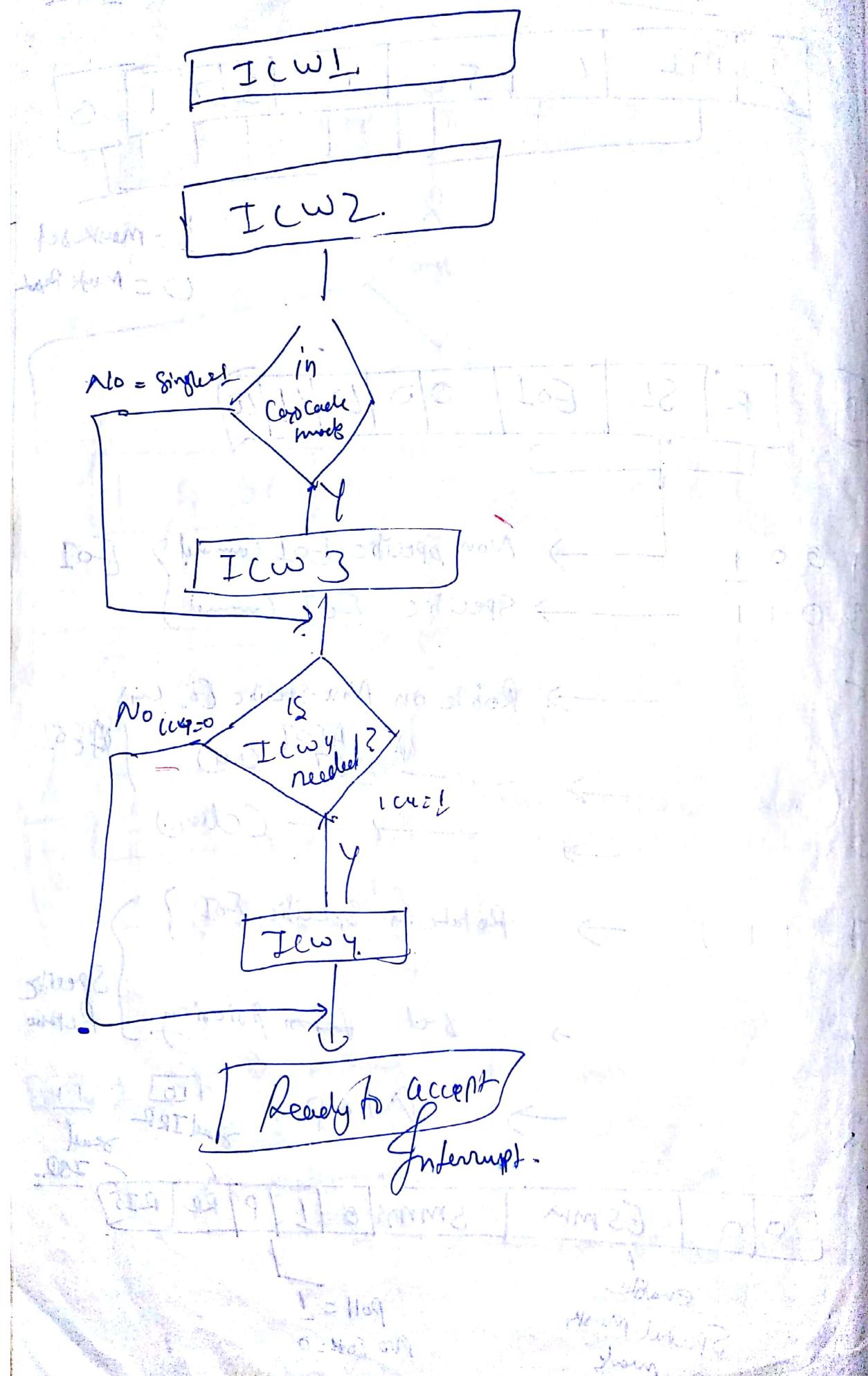
16
clear IRR
11
clear ISR



enable
Special Mask
mode

Poll = 1
Av Poll = 0

① - Ready.



Instruction		Code ¹	B/M/T ²	Machine ³ Cycles	S D ₇	Z D ₆	AC D ₄	P D ₂	CY D ₀	Flags ⁴
ACI	DATA	: Add 8-bit and CY to A	CE data	2/2/7	F R					
ADC	REG	: Add Reg. and CY to A	1000 ISSS	1/1/4	F					
ADC	M	: Add Mem. and CY to A	8E	1/2/7	F R					
ADD	REG	: Add Reg. to A	1000 OSSS	1/1/4	F					
ADD	M	: Add Mem. to A	86	1/2/7	F R					
ADI	DATA	: ADD 8-BIT TO A	C6 DATA	2/2/7	F R					
ANA	REG	: AND Reg. with A	1010 OSSS	1/1/4	F					
ANA	M	: AND Mem. with A	A6	1/2/7	F R					
ANI	DATA	: AND 8-bit with A	E6 data	2/2/7	F R					
CALL	ADDR	: Call Unconditional	CD addr	3/5/18	S R R W W					
CC	ADDR	: Call On CY	DC addr	3/5/9-18	S R R W W					
CM	ADDR	: Call On Minus	FC addr	3/5/9-18	S R R W W					
CMA		: Complement A	2F	1/1/4	F					
CMC		: Complement CY	3F	1/1/4	F					
CMP	REG	: Compare Reg. with A	1011 ISSS	1/1/4	F					
CMP	M	: Compare Mem. with A	BE	1/2/7	F R					
CNC	ADDR	: Call On No CY	D4 addr	3/5/9-18	S R R W W					
CNZ	ADDR	: Call On No Zero	C4 addr	3/5/9-18	S R R W W					
CP	ADDR	: Call On Positive	F4 addr	3/5/9-18	S R R W W					
CPE	ADDR	: Call On Parity Even	EC addr	3/5/9-18	S R R W W					
CPI	DATA	: Compare 8-bit with A	FE data	2/2/7	F R					
CPO	ADDR	: Call On Parity Odd	E4 addr	3/5/9-18	S R R W W					
CZ	ADDR	: Call On Zero	CC addr	3/5/9-18	S R R W W					

DAA		: Decimal-Adjust A	27	1/1/4	F					
DAD	Rp	: Add Reg. Pair to HL	00Rp 1001	1/3/10	F B' B					
DCR	REG	: Decrement Reg.	00SS S101	1/1/4	F					
DCR	M	: Decrement Mem. Contents	35	1/3/10	F R W					
DCX	Rp	: Decrement Reg. Pair	00Rp 1011	1/1/6	S					
DI		: Disable Interrupt	F3	1/1/4	F					
EI		: Enable Interrupt	FB	1/1/4	F					
HLT		: Halt	76	1/2/5	F B					
IN	PORT	: Input from 8-bit Port	DB data	2/3/10	F R I					
INR	REG	: Increment Reg.	00SS-S100	1/1/4	F					
INR	M	: Increment Mem. Contents	34	1/3/10	F R W					
INX	Rp	: Increment Reg. Pair	00Rp 0011	1/1/6	S					
JC	ADDR	: Jump On Carry	DA addr	3/3/7-10	F' R R					
JM	ADDR	: Jump On Minus	FA addr	3/3/7-10	F' R R					
JMP	ADDR	: Unconditional Jump	C3 addr	3/3/10	F' R R					
JNC	ADDR	: Jump On No Carry	D2 addr	3/3/7-10	F' R R					
JNZ	ADDR	: Jump On No Zero	C2 addr	3/3/7-10	F' R R					
JP	ADDR	: Jump On Positive	F2 addr	3/3/7-10	F' R R					
JPE	ADDR	: Jump On Parity Even	EA addr	3/3/7-10	F' R R					
JPO	ADDR	: Jump On Parity Odd	E2 addr	3/3/7-10	F' R R					
JZ	ADDR	: Jump On Zero	CA addr	3/3/7-10	F' R R					
LDA	ADDR	: Load A Direct	3A addr	3/4/13	F R R R					
LDAX	Rp	: Load A from M; memory address is in BC/DE	000X 1010	1/2/7	F R					

Codes¹

DDD = Binary digits identifying a destination register

SSS = Binary digits identifying a source register

B = 000, C = 001, D = 010, Memory = 110

E = 001, H = 100, L = 101, A = 111

BC = 00, HL = 10

RP = Register pair DE = 01, SP = 11

B/M/T²

B = Bytes

M = Machine cycles

T = T-states

Machine Cycles³

F = Fetch with 4 T-states

S = Fetch with 6 T-states

R = Memory Read

I = I/O Read

W = Memory Write

O = I/O Write

B = Bus Idle

Flags⁴

F = Flag is modified according to result

Z = Flag is cleared

AC = Flag is set

P = No change in flag remains in previous state

		Instruction	Code ¹	B/M/T ²	Machine Cycles ³	S D ₇	Z D ₄	AC D ₄	P D ₂	CY D ₀	Flags
LHLD	ADDR	: Load HL Direct	2A	addr	3/5/16	RRRRR					
LXI	Rp, 16-bit	: Load 16-bit in Reg. Pair	00Rp	0001 16-bit	3/3/10	RRR					
MOV	Rd,Rs	: Move from Reg. R _d to Reg. R _s	01DD	DSSS	1/1/4	F					
MOV	M,R	: Move from Reg. to Mem.	0111	0SSS	1/2/7	PW					
MOV	R,M	: Move from Mem. to Reg.	01DD	D110	1/2/7	FR					
MVI	R,DATA	: Load 8-bit in Reg.	00DD	D110 data	2/2/7	FR					
MVI	M,DATA	: Load 8-bit in Mem.	36	data	2/3/10	FRW					
NOP		: No Operation	00		1/1/4	F					
ORA	R	: OR Reg. with A	1011	0SSS	1/1/4	F					
ORA	M	: OR Mem. Contents with A	B6		1/2/7	FR					
ORI	DATA	: OR 8-bit with A	F6	data	2/2/7	FR					
OUT	PORT	: Output to 8-bit Port	D3	data	2/3/10	FRO					
PCHL		: Move HL to Program Counter	E9		1/1/6	S					
POP	Rp	: Pop Reg. Pair	11Rp	0001	1/3/10	FRR					
PUSH	Rp	: Push Reg. Pair	11Rp	0101	1/3/12	SWW					
RAL		: Rotate A Left through CY	I7		1/1/4	F					
RAR		: Rotate A Right through CY	IF		1/1/4	F					
RC		: Return On Carry	D8		1/3/6-12	SRR					
RET		: Return	C9		1/3/10	FRR					
RIM		: Read Interrupt Mask	20		1/1/4	F					
RLC		: Rotate A Left	07		1/1/4	F					
RM		: Return On Minus	F8		1/3/6-12	SRR					
RNC		: Return On No Carry	D0		1/3/6-12	SRR					
RNZ		: Return On No Zero	C0		1/3/6-12	SRR					
RP		: Return On Positive	F0		1/3/6-12	SRR					

RPE		: Return On Parity Even	E8		1/3/6-12	SRR					
RPO		: Return On Parity Odd	E0		1/3/6-12	SRR					
RRC		: Rotate A to Right	0F		1/1/4	F					
RST	N	: Restart	11XX XIII		1/3/12	SWW					
RZ		: Return On Zero	C8		1/3/6-12	SRR					
SBB	R	: Subtract Reg. from A with Borrow	1001	ISSS	1/1/4	F					
SBB	M	: Subtract Mem. Contents from A with Borrow	9E		1/2/7	FR					
SBI	DATA	: Subtract 8-bit from A	DE	data	2/2/7	FR					
SHLD	ADDR	: Store HL Direct	22	addr	3/5/16	FRRWW					
SIM		: Set Interrupt Mask	30		1/1/4	F					
SPHL		: Move HL to Stack Pointer	F9		1/1/6	S					
STA	ADDR	: Store A Direct	32	addr	3/4/13	FRRW					
STAX	Rp	: Store A in M, memory address is in BC/DE	000X	0010	1/2/7	FW					
STC		: Set Carry	37		1/1/4	F					
SUB	R	: Subtract Reg. from A	1001	0SSS	1/1/4	F					
SUB	M	: Subtract Mem. from A	96		1/2/7	FR					
SUI	DATA	: Subtract 8-bit from A	D6	data	2/2/7	FR					
XCHG		: Exchange DE with HL	EB		1/1/4	F					
XRA	R	: Exclusive OR Reg. with A	1010	ISSS	1/1/4	F					
XRA	M	: Exclusive OR Mem. with A	AE		1/2/7	FR					
XRI	DATA	: Exclusive OR 8-bit with A	EE	data	2/2/7	FR					
XTHL		: Exchange Stack with HL	E3		1/4/16	FRRWW					

Codes¹

DDD = Binary digits identifying a destination register

SSS = Binary digits identifying a source register

B = 000, C = 001, D = 010, Memory = 110

E = 001, H = 100, L = 101, A = 111

Rp = Register Pair BC = 00, HL = 10

DE = 01, SP = 11

B/M/T²

B = Bytes

M = Machine cycles

T = T-states

Machine Cycles³

F = Fetch with 4 T-states

S = Fetch with 6 T-states

R = Memory Read

J = I/O Read

W = Memory Write

O = I/O Write

B = Bus Idle

S = Sign

Z = Zero

AC = Auxiliary Carry

P = Parity

CY = Carry

Flags⁴
✓ = Flag is modified according to result
0 = Flag is cleared

1 = Flag is set

Blank = No change in flag, remains in previous state

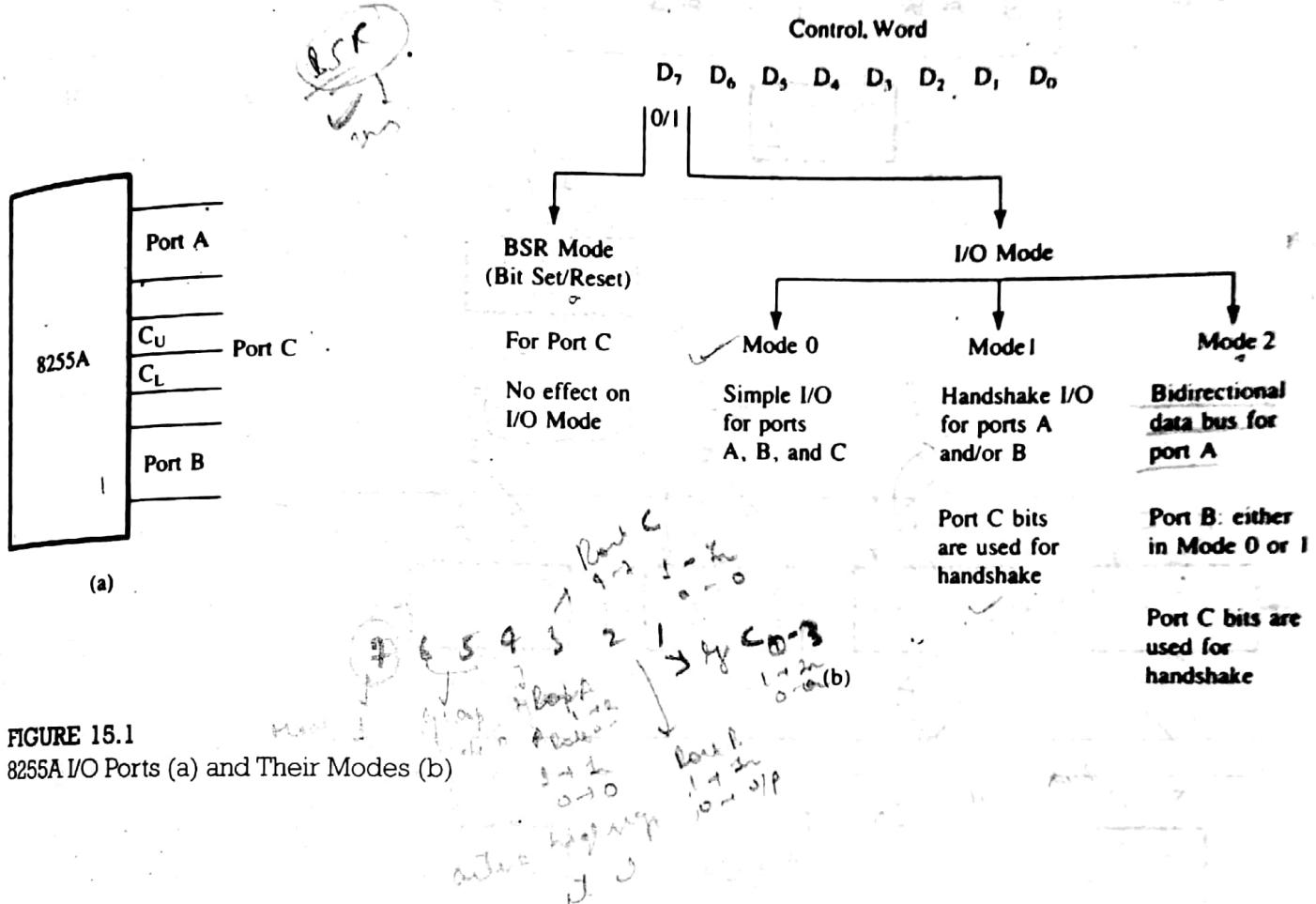


FIGURE 15.1
8255A I/O Ports (a) and Their Modes (b)

- **RESET (Reset):** This is an active high signal; it clears the control register and sets all ports in the input mode.
- **CS, A₀, and A₁:** These are device select signals. CS is connected to a decoded address, and A₀ and A₁ are generally connected to MPU address lines A₀ and A₁, respectively.

The CS signal is the master Chip Select, and A₀ and A₁ specify one of the I/O ports or the control register as given below:

CS	A ₁	A ₀	Selected
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	X	X	8255A is not selected.

As an example, the port addresses in Figure 15.3(a) are determined by the CS, A₀, and A₁ lines. The CS line goes low when A₇ = 1 and A₆ through A₂ are at logic 0. When these signals are combined with A₀ and A₁, the port addresses range from 80H to 83H, as shown in Figure 15.3(b).

INTERFACING PERIPHERALS (I/Os) AND APPLICATIONS

mode, and automatic-end-of-interrupt mode. To simplify the explanation of the 8259A, illustrative examples will not include the cascade mode or the 8086/88 mode and will be limited to modes commonly used with the 8085.

15.5.1 Block Diagram of the 8259A

Figure 15.29 shows the internal block diagram of the 8259A. It includes eight blocks: control logic, Read/Write logic, data bus buffer, three registers (IRR, ISR, and IMR), priority resolver, and cascade buffer. This diagram shows all the elements of a programmable device, plus additional blocks. The functions of some of these blocks need explanation, which is given below.

READ/WRITE LOGIC

This is a typical Read/Write control logic. When the address line A_0 is at logic 0, the controller is selected to write a command or read a status. The Chip Select logic and A_{11} determine the port address of the controller.

CONTROL LOGIC

This block has two pins: INT (Interrupt) as an output, and INTA (Interrupt Acknowledge) as an input. The INT is connected to the interrupt pin of the MPU. Whenever a valid interrupt is asserted, this signal goes high. The INTA is the Interrupt Acknowledge signal from the MPU.

INTERRUPT REGISTERS AND PRIORITY RESOLVER

The Interrupt Request Register (IRR) has eight input lines (IR_0 – IR_7) for interrupts. When these lines go high, the requests are stored in the register. The In-Service Register (ISR) stores all the levels that are currently being serviced, and the Interrupt Mask Register (IMR) stores the masking bits of the interrupt lines to be masked. The Priority Resolver (PR) examines these three registers and determines whether INT should be sent to the MPU.

CASCADE BUFFER/COMPARATOR

This block is used to expand the number of interrupt levels by cascading two or more 8259As. To simplify the discussion, this block will not be mentioned again.

15.5.2 Interrupt Operation

To implement interrupts, the Interrupt Enable flip-flop in the microprocessor should be enabled by writing the EI instruction, and the 8259A should be initialized by writing control words in the control register. The 8259A requires two types of control words: Initialization Command Words (ICWs) and Operational Command Words (OCWs). The ICWs are used to set up the proper conditions and specify RST vector addresses. The OCWs are used to perform functions such as masking interrupts, setting up status-read operations, etc. After the 8259A is initialized, the following sequence of events occurs when one or more interrupt request lines go high:

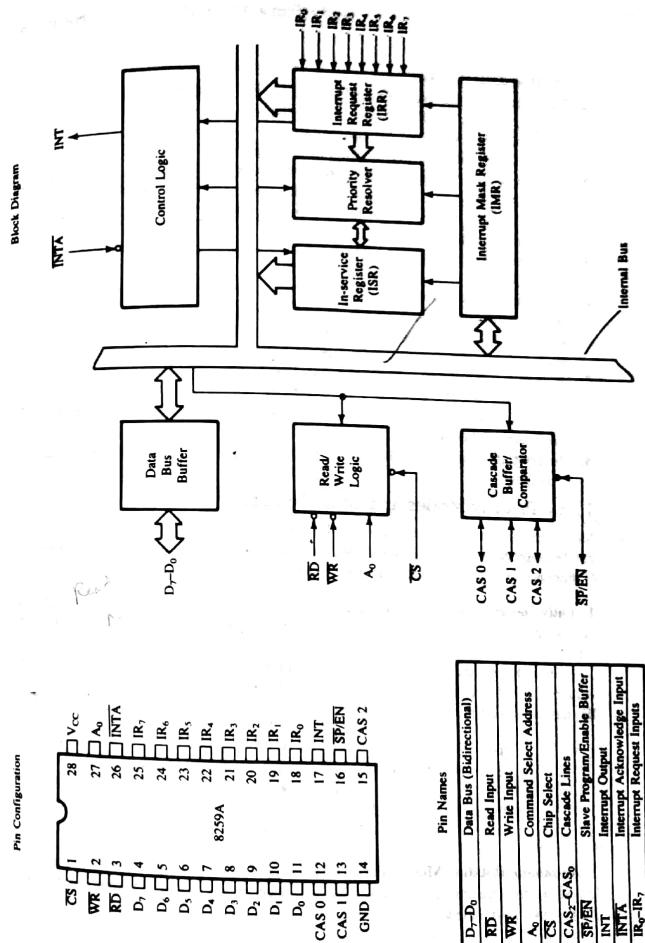


FIGURE 15.29
The 8259A: Block Diagram
SOURCE: Intel Corporation, Peripheral Components (Santa Clara, Calif.: Author, 1990), pp. 3-171, 3-172.

intel

**8237A/8237A-4/8237A-5
HIGH PERFORMANCE
PROGRAMMABLE DMA CONTROLLER**

- Enable/Disable Control of Individual DMA Requests
 - Four Independent DMA Channels
 - Independent Autoinitialization of all Channels
 - Memory-to-Memory Transfers
 - Memory Block Initialization
 - Address Increment or Decrement

- **High performance: Transfers up to 1.6M Bytes/Second with 5 MHz 8237A-5**
 - **Directly Expandable to any Number of Channels**
 - **End of Process Input for Terminating Transfers**
 - **Software DMA Requests**
 - **Independent Polarity Control for DREQ and DACK Signals**
 - **Available In EXPRESS**
 - Standard Temperature Range

The 8237A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The 8237A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The 8237A is designed to be used in conjunction with an external 8-bit address register such as the 8282. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips. The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to AutoInitialize to its original condition following an End of Process (EOP).

Each channel has a full 64K address and word count capability.

The 8237A-4 and 8237A-5 are 4 MHz and 5 MHz selected versions of the standard 3 MHz 8237A respectively.

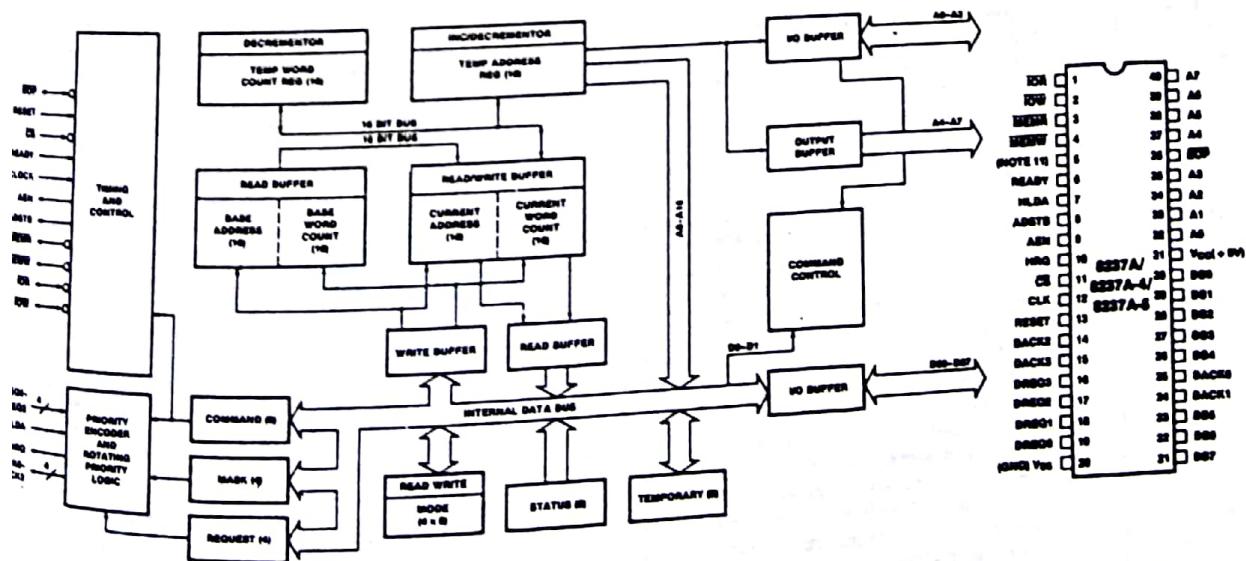


Figure 1. Block Diagram

Figure 2.
Pin Configuration

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
A4-A7	O	Address: The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
HRQ	O	Hold Request: This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes 8237A to issue the HRQ. After HRQ goes active at least one clock cycle (TCY) must occur before HLDA goes active.
DACK0-DACK3	O	DMA Acknowledge: DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.

FUNCTIONAL DESCRIPTION

The 8237A block diagram includes the major logic blocks and all of the internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks. The 8237A contains 344 bits of internal memory in the form of registers. Figure 3 lists these registers by name and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

Figure 3. 8237A Internal Registers

The 8237A contains three basic blocks of control logic. The Timing Control block generates internal timing and external control signals for the 8237A. The Program Command Control block decodes the various commands given to the 8237A by the microprocessor prior to servicing a DMA Request. It also decodes the Mode Control word used to select the type of DMA during the servicing. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

The Timing Control block derives internal timing from the clock input. In 8237A systems this input will usually

Symbol	Type	Name and Function
AEN	O	Address Enable: Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	O	Address Strobe: The active high, Address Strobe is used to strobe the upper address byte into an external latch.
MEMR	O	Memory Read: The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
MEMW	O	Memory Write: The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.

be the ϕ_2 TTL clock from an 8224 or CLK from an 8085AH or 8284A. For 8085AH-2 systems above 3.9 MHz, the 8085 CLK(OUT) does not satisfy 8237A-5 clock LOW and HIGH time requirements. In this case, an external clock should be used to drive the 8237A-5.

DMA Operation

The 8237A is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The 8237A can assume seven separate states, each composed of one full clock period. State 1 (S1) is the inactive state. It is entered when the 8237A has no valid DMA requests pending. While in S1, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State S0 (S0) is the first state of a DMA service. The 8237A has requested a hold but the processor has not yet returned an acknowledge. The 8237A may still be programmed until it receives HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the 8237A. Note that the data is transferred directly from the I/O device to memory (or vice versa) with IOR and MEMW (or MEMR and IOW) being active at the same time. The data is not read into or driven out of the 8237A in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half

REGISTER DESCRIPTION

Current Address Register — Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an EOP.

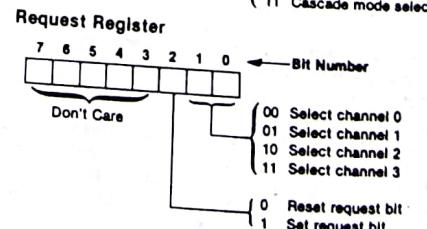
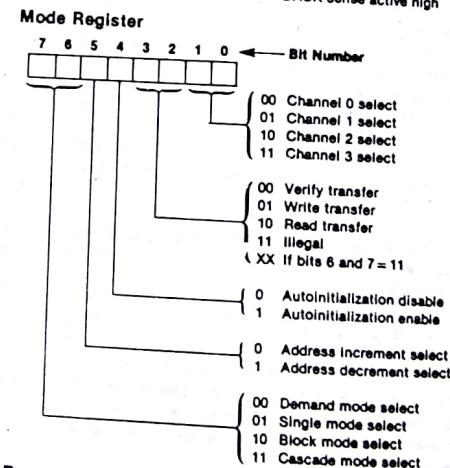
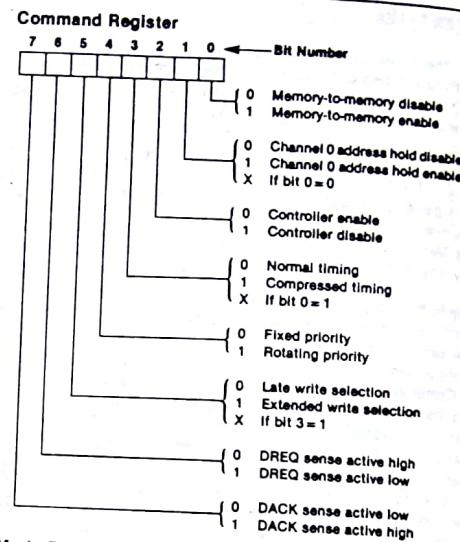
Current Word Register — Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialize can occur only when an EOP occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

Base Address and Base Word Count Registers — Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

Command Register — This 8-bit register controls the operation of the 8237A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset or a Master Clear instruction. The following table lists the function of the command bits. See Figure 6 for address coding.

Mode Register — Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

Request Register — The 8237A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are non-maskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset sepa-



rately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 5 for register address coding. In order to make a software request, the channel must be in Block Mode.

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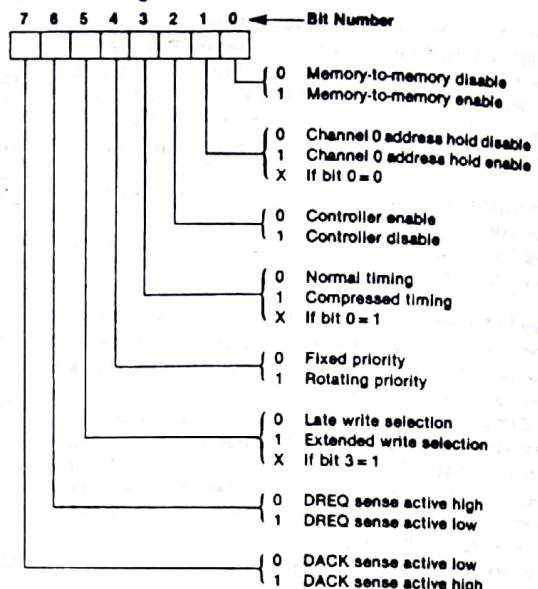
Base Address and Base Word Count Registers — Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During AutoInitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

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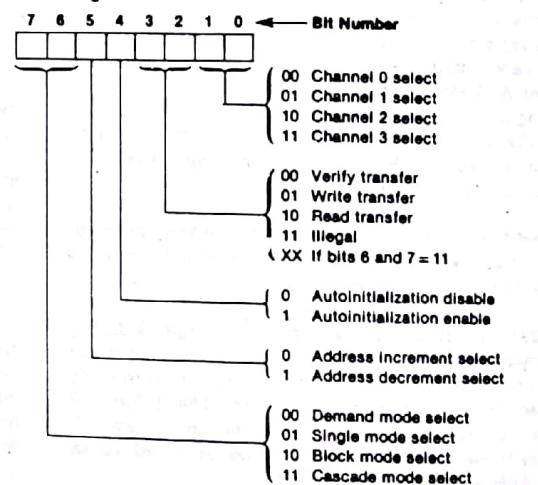
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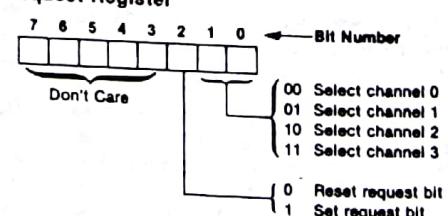
Command Register



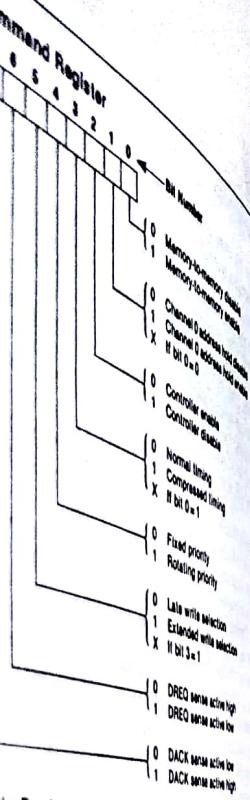
Mode Register



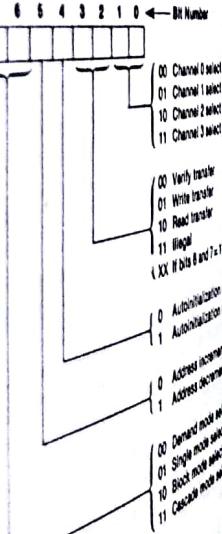
Request Register



rately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 5 for register address coding. In order to make a software request, the channel must be in Block Mode.



Mode Register

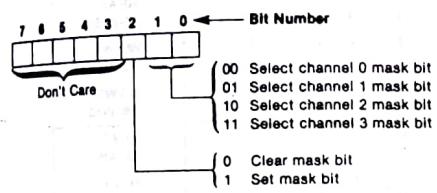


only under software control or is cleared upon power up or a Reset. To set or reset a bit, the software must be in proper form of the data word. Set request bit must be in Block Mode.

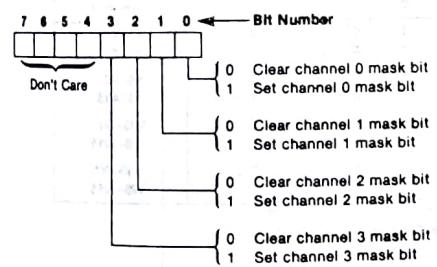
8237A/8237A-4/8237A-5



Mask Register — Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 5 for instruction addressing.



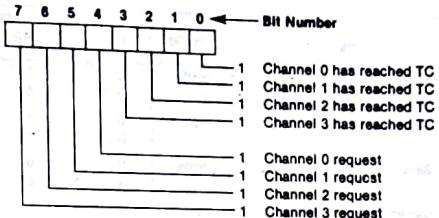
All four bits of the Mask register may also be written with a single command.



Register	Operation	Signals					
		CS	IOR	IOW	A3	A2	A1
Command	Write	0	1	0	1	0	0
Mode	Write	0	1	0	1	0	1
Request	Write	0	1	0	1	0	1
Mask	Set/Reset	0	1	0	1	0	1
Temporary	Write	0	1	0	1	1	1
Status	Read	0	0	1	1	1	0
	Read	0	0	1	1	0	1

Figure 5. Definition of Register Codes

Status Register — The Status register is available to be read out of the 8237A by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set every time a TC is reached by that channel or an external EOP is applied. These bits are cleared upon Reset and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service.



Temporary Register — The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Software Commands — These are additional special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The two software commands are:

Clear First/Last Flip-Flop: This command is executed prior to writing or reading new address or word count information to the 8237A. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers are cleared and the Mask register is set. The 8237A will enter the Idle cycle.

Clear Mask Register: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Figure 6 lists the address codes for the software commands:

Signals						Operation
A3	A2	A1	A0	IOR	IOW	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	0	1	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip-Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

Figure 6. Software Command Codes

READING THE 8259A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 (IMR)).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR.)

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0.)

The ISR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 8259A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the 8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever RD is active and AO = 1 (OCW1).

Polling overrides status read when P = 1, RR = 1 in OCW3.

EDGE AND LEVEL TRIGGERED MODES

This mode is programmed using bit 3 in ICW1.

If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM = '1', an interrupt request will be recognized by a 'high' level on IR Input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 8259A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

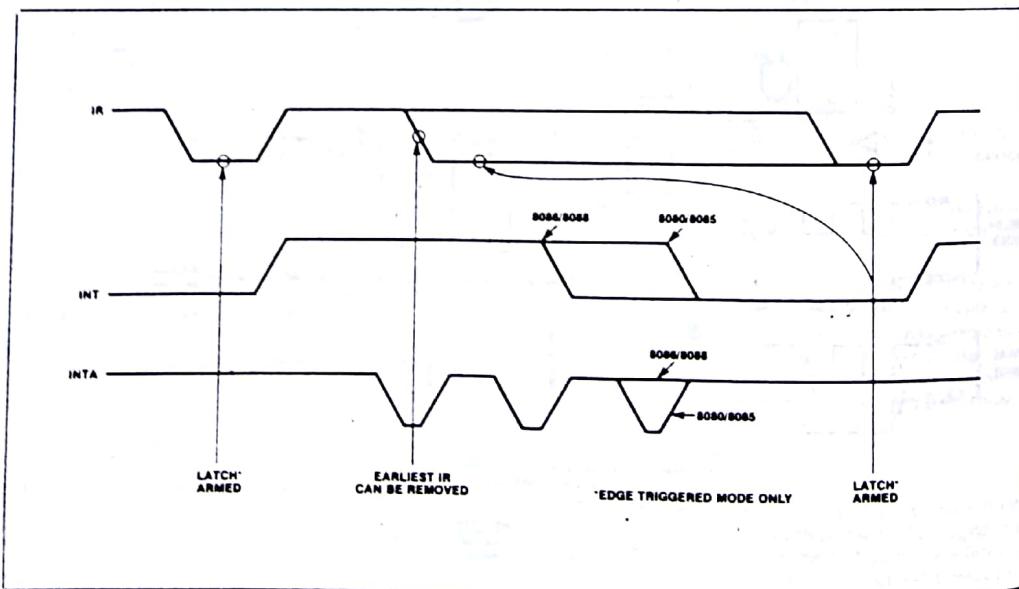


Figure 10. IR Triggering Timing Requirements

THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

- When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)
- When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

BUFFERED MODE

When the 8259A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 8259A to send an enable signal on SP/EN to enable the buffers. In this

mode, whenever the 8259A's data bus outputs are enabled, the SP/EN output becomes active.

This modification forces the use of software programming to determine whether the 8259A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

CASCADE MODE

The 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the INTA sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 8086/8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select (CS) input of each 8259A.

The cascade lines of the Master 8259A are activated only for slave inputs, non slave inputs leave the cascade line inactive (low).

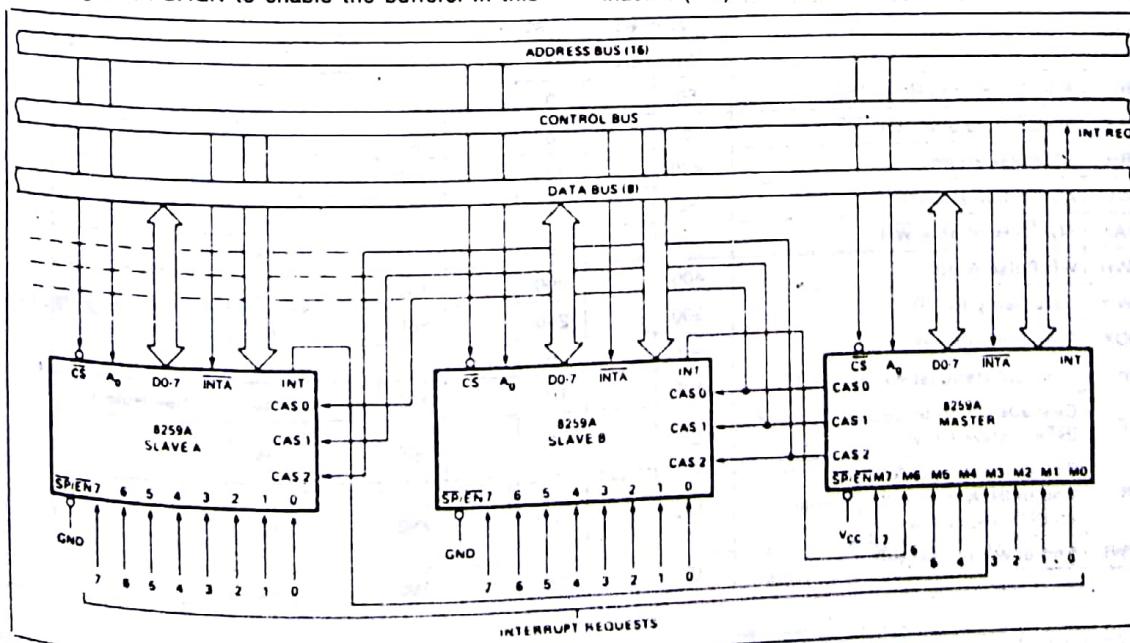


Figure 11. Cascading the 8259A

in register C. If CY = 0, the program loops back to check the next bit (D_6). The loop is repeated until 1 is found in CY, and at every iteration of the loop the key code in register C is adjusted for the next key. If more than one key is pressed, this routine ignores the low-order key. Finally, the subroutine places the key code in the accumulator and returns.

KEY DEBOUNCE

When a mechanical pushbutton key, shown in Figure 15.17(a), is pressed or released, the metal contacts of the key momentarily bounce before giving a steady-state reading, as shown in Figure 15.17(b). Therefore, it is necessary that the bouncing of the key should not be read as an input. The key bounce can be eliminated from input data by the **key debounce technique**, using either hardware or software.

Figure 15.17(c) shows a key debounce circuit. In this circuit, the outputs of the NAND gates do not change even if the key is released from position A₁. The outputs change when the key makes a contact with position B₁. When the key is connected to A₁,

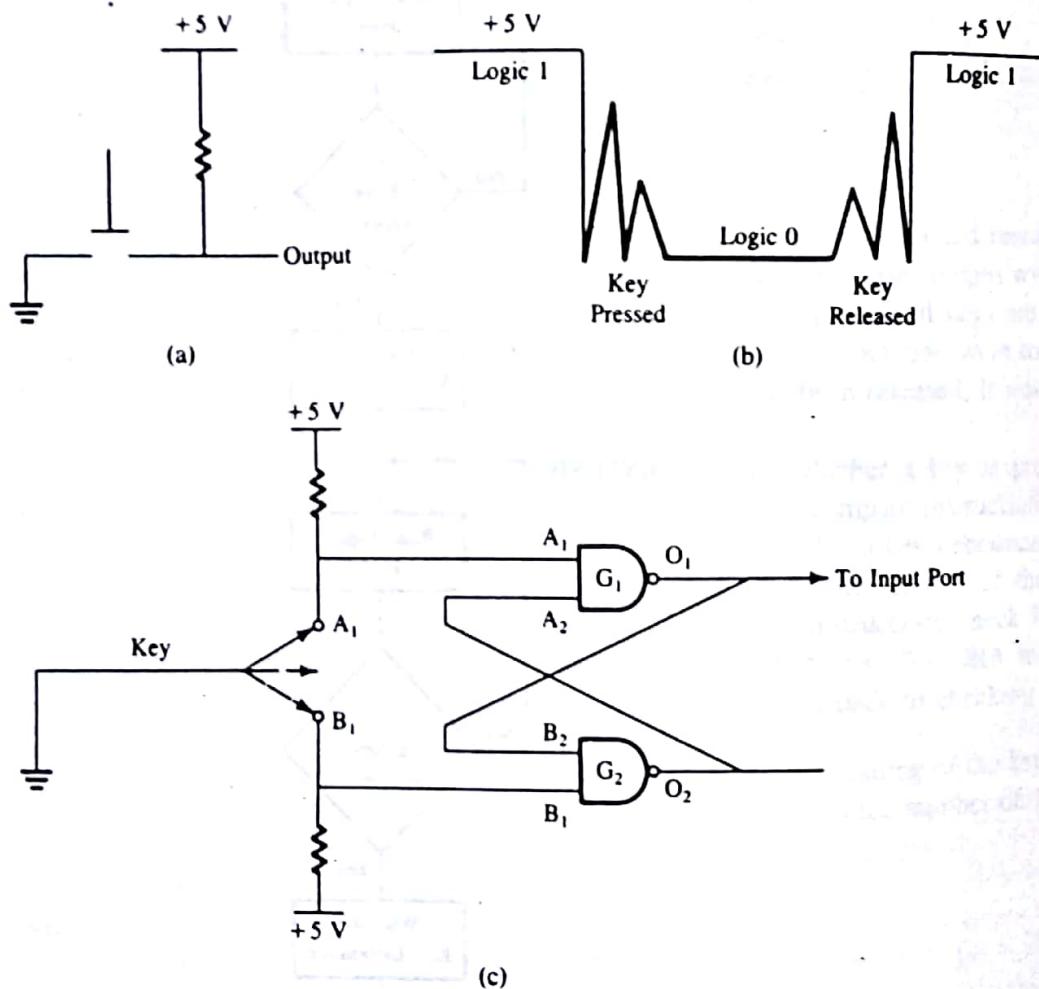


FIGURE 15.17

Pushbutton Key (a), Key Bounce (b), and Key Debounce Circuit Using NAND Gates (c)

can be used as an interrupt. The OUT remains high until a new count or a command word is loaded. Figure 15.27 also shows that the counting ($m = 5$) is temporarily stopped when the Gate is disabled ($G = 0$), and continued again when the Gate is at logic 1.

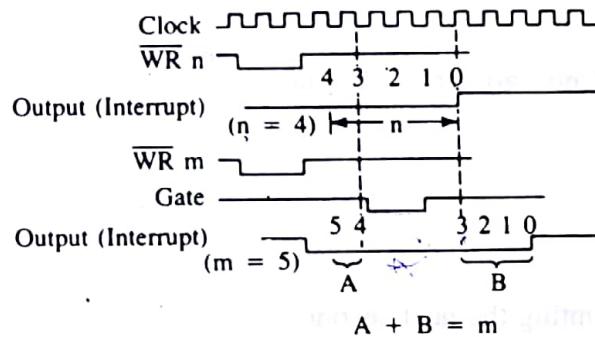
MODE 1: HARDWARE-RETRIGGERABLE ONE-SHOT

In this mode, the OUT is initially high. When the Gate is triggered, the OUT goes low, and at the end of the count, the OUT goes high again, thus generating a one-shot pulse (Figure 15.27, Mode 1).

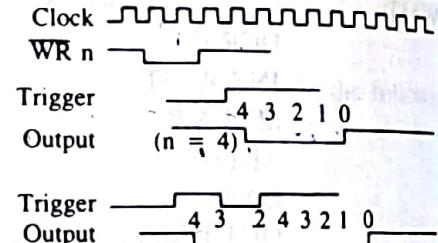
MODE 2: RATE GENERATOR

This mode is used to generate a pulse equal to the clock period at a given interval. When a count is loaded, the OUT stays high until the count reaches 1, and then the OUT goes

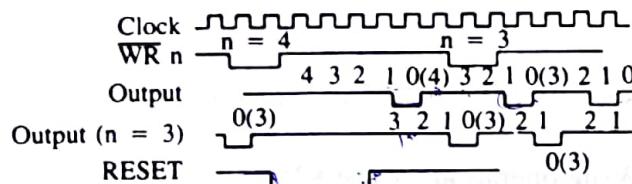
Mode 0: Interrupt on Terminal Count



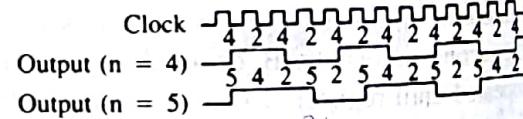
Mode 1: Programmable One-Shot



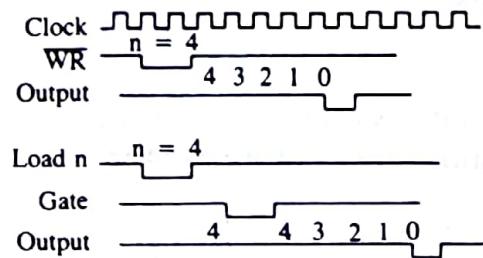
Mode 2: Rate Generator Clock



Mode 3: Square Wave Generator



Mode 4: Software Triggered Strobe



Mode 5: Hardware Triggered Strobe

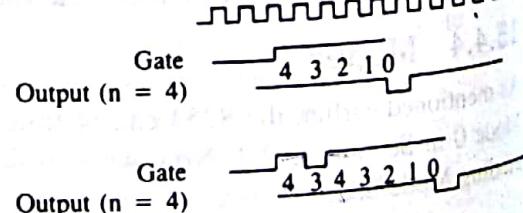


FIGURE 15.27

Six Modes of the 8254

SOURCE: Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), pp. 3-72-3-75 (adapted).

	Instruction	Code ¹	B/M/T ²	Machine ³ Cycles	S D ₇	Z D ₆	Flags ⁴			
							AC D ₄	P D ₂	CY D ₀	
ACI DATA	: Add 8-bit and CY to A	CE data	2/2/7	F R	✓	✓	✓	✓	✓	✓
ADC REG	: Add Reg. and CY to A	1000 ISSS	1/1/4	F	✓	✓	✓	✓	✓	✓
ADC M	: Add Mem. and CY to A	8E	1/2/7	F R	✓	✓	✓	✓	✓	✓
ADD REG	: Add Reg. to A	1000 OSSS	1/1/4	F	✓	✓	✓	✓	✓	✓
ADD M	: Add Mem. to A	86	1/2/7	F R	✓	✓	✓	✓	✓	✓
ADI DATA	: ADD 8-BIT TO A	C6 DATA	2/2/7	F R	✓	✓	✓	✓	✓	✓
ANA REG	: AND Reg. with A	1010 OSSS	1/1/4	F	✓	✓	✓	✓	✓	0
ANA M	: AND Mem. with A	A6	1/2/7	F R	✓	✓	✓	✓	✓	0
ANI DATA	: AND 8-bit with A	E6 data	2/2/7	F R	✓	✓	✓	✓	✓	0
CALL ADDR	: Call Unconditional	CD addr	3/5/18	S R R W W						
CC ADDR	: Call On CY	DC addr	3/5/9-18	S R R W W						
CM ADDR	: Call On Minus	FC addr	3/5/9-18	S R R W W						
CMA	: Complement A	2F	1/1/4	F						
CMC	: Complement CY	3F	1/1/4	F						
CMP REG	: Compare Reg. with A	1011 ISSS	1/1/4	F	✓	✓	✓	✓	✓	✓
CMP M	: Compare Mem. with A	BE	1/2/7	F R	✓	✓	✓	✓	✓	✓
CNC ADDR	: Call On No CY	D4 addr	3/5/9-18	S R R W W						
CNZ ADDR	: Call On No Zero	C4 addr	3/5/9-18	S R R W W						
CP ADDR	: Call On Positive	F4 addr	3/5/9-18	S R R W W						
CPE ADDR	: Call On Parity Even	EC addr	3/5/9-18	S R R W W						
CPI DATA	: Compare 8-bit with A	FE data	2/2/7	F R	✓	✓	✓	✓	✓	✓
CPO ADDR	: Call On Parity Odd	E4 addr	3/5/9-18	S R R W W						
CZ ADDR	: Call On Zero	CC addr	3/5/9-18	S R R W W						

DAA	: Decimal-Adjust A	27	1/1/4	F	✓	✓	✓	✓	✓	✓	✓
DAD Rp	: Add Reg. Pair to HL	00Rp 1001	1/3/10	F B B	✓	✓	✓	✓	✓	✓	✓
DCR REG	: Decrement Reg.	00SS S101	1/1/4	F	✓	✓	✓	✓	✓	✓	✓
DCR M	: Decrement Mem. Contents	35	1/3/10	F R W	✓	✓	✓	✓	✓	✓	✓
DCX Rp	: Decrement Reg. Pair	00Rp 1011	1/1/6	S							
DI	: Disable Interrupt	F3	1/1/4	F							
EI	: Enable Interrupt	FB	1/1/4	F							
HLT	: Halt	76	1/2/5	F B							
IN PORT	: Input from 8-bit Port	DB data	2/3/10	F R I							
INR REG	: Increment Reg.	00SS-S100	1/1/4	F	✓	✓	✓	✓	✓	✓	✓
INR M	: Increment Mem. Contents	34	1/3/10	F R W	✓	✓	✓	✓	✓	✓	✓
INX Rp	: Increment Reg. Pair	00Rp 0011	1/1/6	S							
JC ADDR	: Jump On Carry	DA addr	3/3/7-10	F R R							
JM ADDR	: Jump On Minus	FA addr	3/3/7-10	F R R							
JMP ADDR	: Unconditional Jump	C3 addr	3/3/10	F R R							
JNC ADDR	: Jump On No Carry	D2 addr	3/3/7-10	F R R							
JNZ ADDR	: Jump On No Zero	C2 addr	3/3/7-10	F R R							
JP ADDR	: Jump On Positive	F2 addr	3/3/7-10	F R R							
JPE ADDR	: Jump On Parity Even	EA addr	3/3/7-10	F R R							
JPO ADDR	: Jump On Parity Odd	E2 addr	3/3/7-10	F R R							
JZ ADDR	: Jump On Zero	CA addr	3/3/7-10	F R R							
LDA ADDR	: Load A Direct	3A addr	3/4/13	F R R R							
LDAX Rp	: Load A from M; memory address is in BC/DE	000X 1010	1/2/7	F R							

Codes¹

DDD = Binary digits identifying a destination register
 SSS = Binary digits identifying a source register
 B = 000, C = 001, D = 010, Memory = 110
 E = 001, H = 100, L = 101, A = 111
 Rp = Register Pair BC = 00, HL = 10
 DE = 01, SP = 11

B/M/T²

B = Bytes
 M = Machine cycles
 T = T-states

Machine Cycles³

F = Fetch with 4 T-states
 S = Fetch with 6 T-states
 R = Memory Read
 I = I/O Read
 W = Memory Write
 O = I/O Write
 B = Bus Idle

Flags⁴

S = Sign
 Z = Zero
 AC = Auxiliary Carry
 P = Parity
 CY = Carry
 ✓ = Flag is modified according to result
 0 = Flag is cleared
 1 = Flag is set
 Blank = No change in flag, remains in previous state

		Instruction	Code ¹	B/M/T ²	Machine ³ Cycles	S D ₇	Z D ₆	Flags ⁴ AC D ₄	P D ₂	CY D ₀
LHLD	ADDR	: Load HL Direct	2A addr	3/5/16	F R R R R					
LXI	Rp, 16-bit	: Load 16-bit in Reg. Pair	00Rp 0001 16-bit	3/3/10	F R R					
MOV	Rd,Rs	: Move from Reg. R _d to Reg. R _s	01DD DSSS	1/1/4	F					
MOV	M,R	: Move from Reg. to Mem.	0111 OSSS	1/2/7	F W					
MOV	R,M	: Move from Mem. to Reg.	01DD D110	1/2/7	F R					
MVI	R,DATA	: Load 8-bit in Reg.	00DD D110 data	2/2/7	F R					
MVI	M,DATA	: Load 8-bit in Mem.	36 data	2/3/10	F R W					
NOP		: No Operation	00	1/1/4	F					
ORA	R	: OR Reg. with A	1011 OSSS	1/1/4	F			✓ 0	✓ 0	
ORA	M	: OR Mem. Contents with A	B6	1/2/7	F R			✓ 0	✓ 0	
ORI	DATA	: OR 8-bit with A	F6 data	2/2/7	F R			✓ 0	✓ 0	
OUT	PORT	: Output to 8-bit Port	D3 data	2/3/10	F R O					
PCHL		: Move HL to Program Counter	E9	1/1/6	S					
POP	Rp	: Pop Reg. Pair	11Rp 0001	1/3/10	F R R					
PUSH	Rp	: Push Reg. Pair	11Rp 0101	1/3/12	S W W					
RAL		: Rotate A Left through CY	17	1/1/4	F					
RAR		: Rotate A Right through CY	1F	1/1/4	F					
RC		: Return On Carry	D8	1/3/6-12	S R R					
RET		: Return	C9	1/3/10	F R R					
RIM		: Read Interrupt Mask	20	1/1/4	F					
RLC		: Rotate A Left	07	1/1/4	F					
RM		: Return On Minus	F8	1/3/6-12	S R R					
RNC		: Return On No Carry	D0	1/3/6-12	S R R					
RNZ		: Return On No Zero	C0	1/3/6-12	S R R					
RP		: Return On Positive	F0	1/3/6-12	S R R					

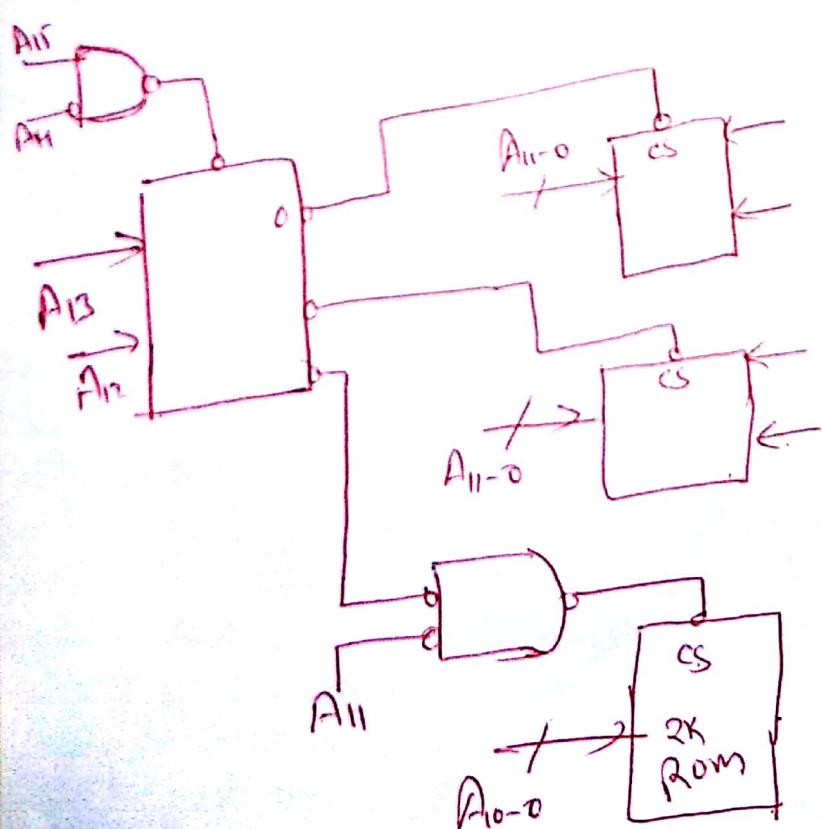
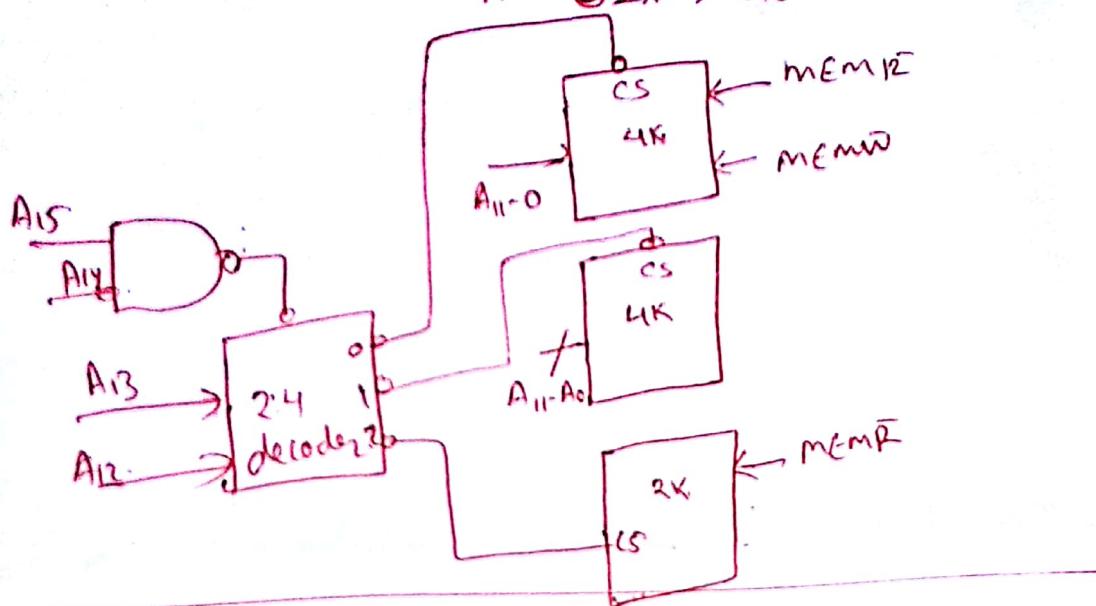
RPE		: Return On Parity Even	E8	1/3/6-12	S R R					
RPO		: Return On Parity Odd	E0	1/3/6-12	S R R					
RRC		: Rotate A to Right	0F	1/1/4	F					
RST	N	: Restart	11XX X111	1/3/12	S W W					
RZ		: Return On Zero	C8	1/3/6-12	S R R					
SBB	R	: Subtract Reg. from A with Borrow	1001 1SSS	1/1/4	F					
SBB	M	: Subtract Mem. Contents from A with Borrow	9E	1/2/7	F R					
SBI	DATA	: Subtract 8-bit from A	DE data	2/2/7	F R					
SHLD	ADDR	: Store HL Direct	22 addr	3/5/16	F R R W W					
SIM		: Set Interrupt Mask	30	1/1/4	F					
SPHL		: Move HL to Stack Pointer	F9	1/1/6	S					
STA	ADDR	: Store A Direct	32 addr	3/4/13	F R R W					
STAX	Rp	: Store A in M, memory address is in BC/DE	000X 0010	1/2/7	F W					
STC		: Set Carry	37	1/1/4	F					
SUB	R	: Subtract Reg. from A	1001 OSSS	1/1/4	F					
SUB	M	: Subtract Mem. from A	96	1/2/7	F R					
SUI	DATA	: Subtract 8-bit from A	D6 data	2/2/7	F R					
XCHG		: Exchange DE with HL	EB	1/1/4	F					
XRA	R	: Exclusive OR Reg. with A	1010 ISSS	1/1/4	F			✓ 0	✓ 0	
XRA	M	: Exclusive OR Mem. with A	AE	1/2/7	F R			✓ 0	✓ 0	
XRI	DATA	: Exclusive OR 8-bit with A	EE data	2/2/7	F R			✓ 0	✓ 0	

4K RAM - 2 | with & without foldback addressing, Starting address
 2K ROM - 1 | in 8000H

Solⁿ

- A₁₅ 14 13 12 11

1	0	00	0	0
		00		
0	1	1	1	
0	1			
1	0	0	X	A _{000H} to A _{7FFH} .
1	0	X	01	A _{800H} to A _{FffH} .



15	14	13	12	11	10
1	0	0	0	0	0
1	1	0	0	1	0
1	1	0	1	1	1
1	0	0	0	0	0
1	0	1	0	0	0
1	0	0	1	0	0
1	0	0	0	0	1