FSR → file selection Reg

INDF Reg

Indirect Reg.

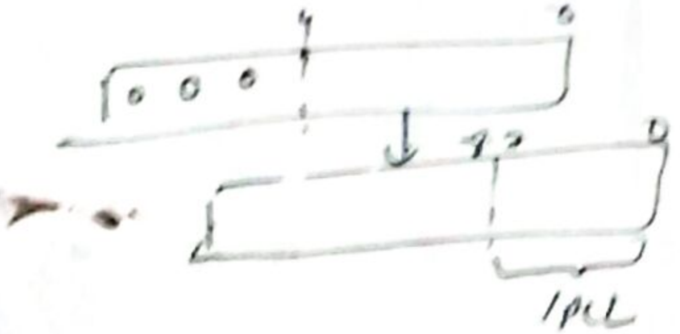
PCL → Prog. Counter low Byte
address = 02, 82H

PCLath Reg. 0A, 8A.

8 bit reg. which can be used to decide the upper 5 bits of PC.

PCLath → can be read from or written to without affecting the PC.

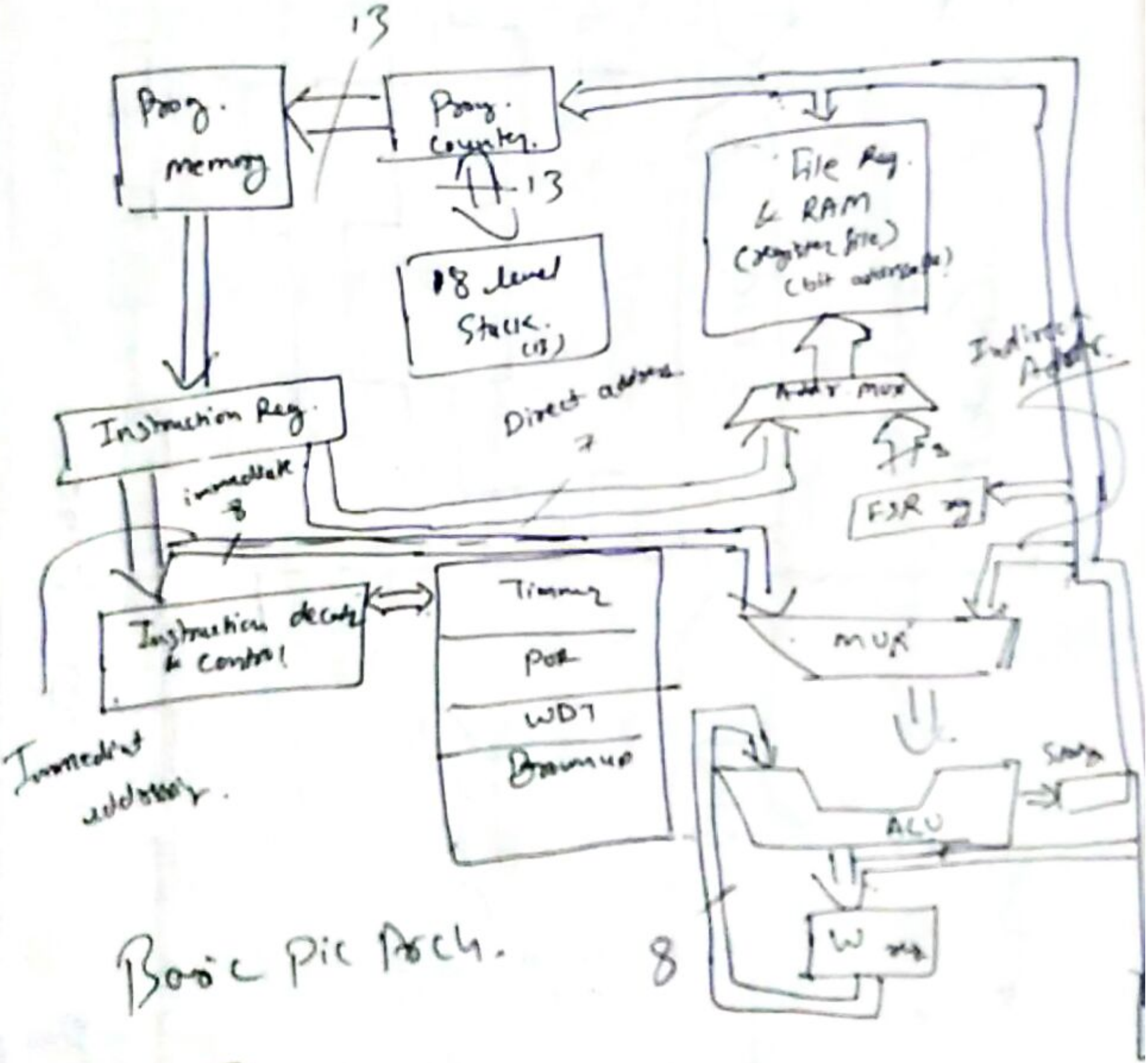
~~ꟻ~~ upper 3 bit remain zero and serve no purpose. When PCL is written to, the lower ~~FP~~ 5 bits of PCLATCH are automatically loaded to upper 5 bits of PC.



PIC Family

Packages.

8 : Pin	12C50x (12bit)	- 14bit
18 pin : -	16 C5X	(12 bit) + 14 bits
28 pin	: 16 C5X	—— " ——
40	⇒ 18F	- - -
44	- 64	17C, 18F, 24F - - - (16-bit)



Basic pic Arch.

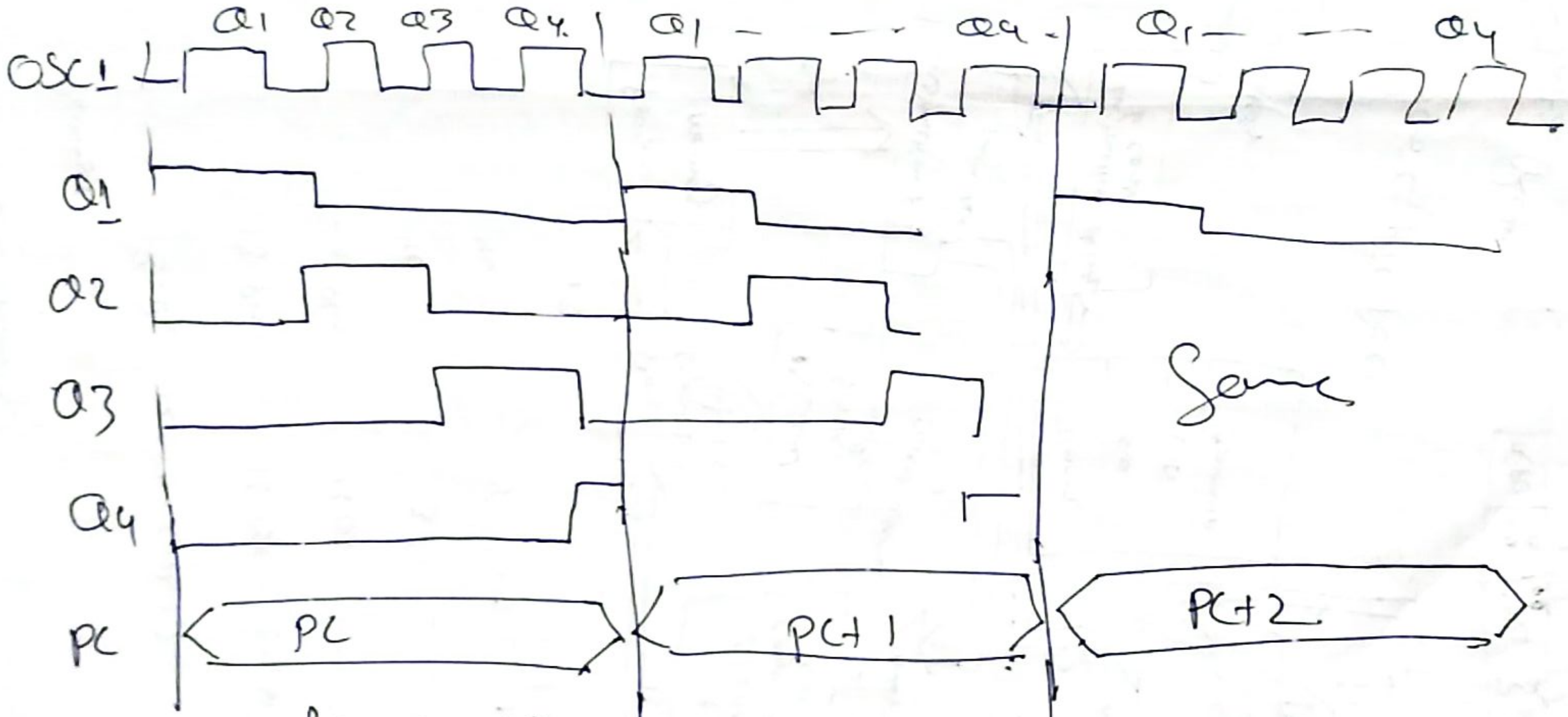
Status Reg

	RP0	NOT TO	NOT PD	Z	DC	C

Reg. bank Select

used in combination with sleep mode

A ?



Fetch Instr (P)
Execute Inst ~~p+1~~ PC-1

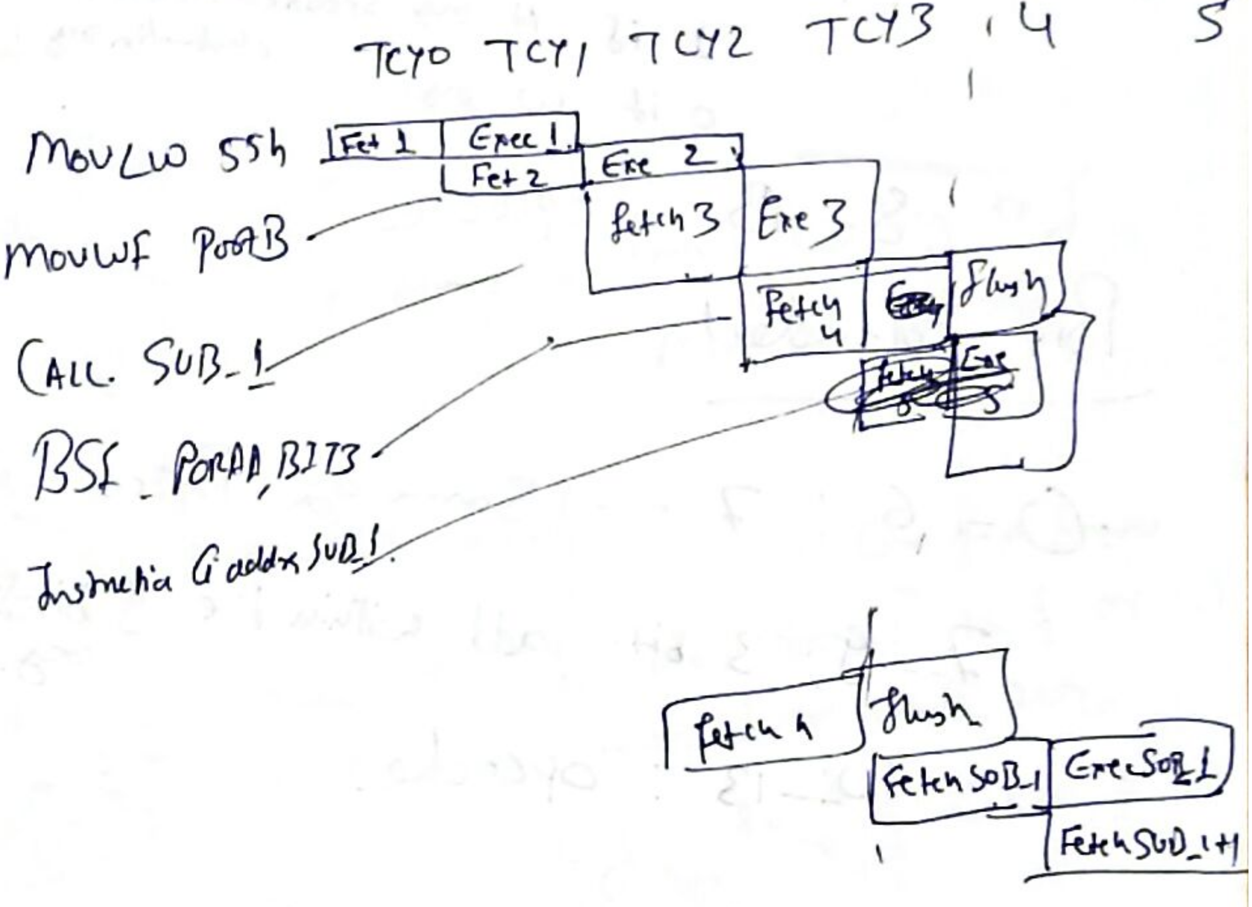
Fetch PC+1
Execute PC.

Fetc PC+2
Execute PC+1

⇒ OSC1 is divides into 4 even clocks ("Quadratures). Q1, Q2, Q3, Q4.

decoding & execution. are done b/w next Q1 &

Pipeling :-



TYCO ⇒ read MOVLW 55h.

TCY1 → executes -||- & read MOVWF PortB

TCY2 → execute MOVWF PortB & reads in Call/.--

TCY3 → execute's call & reaes BSF ---. As BSF is not the one we need or not the 1st Inst of sub prog. so it needs to be read agn

TCY4 → I-C is used in reading 1st instruction of SUB_1

TCY5 → execut 1st IC of SUB_1 & reads next.

PIC Instructing

→ 35 instruction's

→ Bit, Byte. Letoal & Control.

Byte oriented

0..6 : 7th bit is destination address.
1 if 1d reg. specified in 0 to 6th bit is destination reg.
0 if W reg.

8 – 13 : opcode

Bit oriented

: 0 – 6 : 7 -- Same as Byte

7...9 : 3 bit. add within the 8 bit file reg.

10 – 13 : opcode.

Literal and Control operation.

General.

0..7 : 8 bit. literal (immediate value)

8...13 : Opcode

Call & Goto

→ 0...10 : 11 bit. (target address or literal value)

PC=13bits → upper 2 bits of PC loaded from PCLatch<4:3>

11 : 13 opcode.

Byte : Both & Data movement.

1. addwf f, d — destination bit :- Add Contend of W with reg f if d=0 result is Stored in W else in F.

addwf 0x20, 0

2. Clrf f: Content of reg. f are cleared & Z bit is set.

eg clrf 0x30

3. movwf f.

move data from W reg to f.

movwf 0x04.

4. decfsz f, d — Conditional branch

↳ Dec f, place result in f. or W skip next instr if result is zero

e.g decfsz 0x20, 1.

high code density

8. decf f, d :- Decrement f, Place result depending on value d, effect Z flag

e.g. decf 0x30, 0

increase ~~d~~ Code density.

leteral operation (immediate)

addlw K. : add literal K to W.
e.g addlw 0x05

movlw K. ⇒ move K → W

movlw 0x21.

SWAPF :- exchage places of 4 bit nibble fields inside reg.

ALU ⇒

— MUL, DIV, Add.

Bit Manipulation. bcf ⇒ clear
bsf - set

bsf f, b set b (wher b = 0 to 7) in reg f.
e.g bsf 0x03, 5

btfsc f, b

test bit b of reg f., skip next instruction. if. bit is 0

btfsc 0x03, 2

Control instruction

1. goto K (K – 11 bit)

   Un conditional branch, literal K is loaded into PC:

   Goto there (LABEL)

2. Call K.

   Call Sum.

3. retfie. → return from interrupt service routine & re-enable interrupts.

4. Sleep → Standby mode

5. Clrwdt → cleared. WDT.

RISC.

↳ Instr with fixed length.

↳ involve reg. not memory locⁿ directly.
exe → store instr
next exe → stored it mpo.

PIC is leading archi for low end Appⁿ.

↳

8 pin → 12C.
18 → 16C
28 → 16C
40 → 18F.
44 - 68

Status Reg.

bank select.			Time out		Zero bit	digit carry or AuxC	
IRP	RP!	RP0	TO	PD	Z	DC	C.
				Power Down			Carry

↳ ALU Status.
↳ Reset Status
↳ Memory Bank.