Design and interface 6K x 8 memory to 8085 using 2K x 8 memory chips. Select starting address 8000H. Give the address range of each chip used.

Soln.

Step 1: The 6K x 8 memory is to be built using 2K x 8
→ no. issues with data lines as (8) is for 6K & 2K.
6K = 2K + 2K + 2K.

Step 2: The address lines required for 2K chip are 11
So A_0 to A_{10} should be directly connected to up address bus

Step 3: Remaining lines A_{11} to A_{15} will be used to generate Chip select signal for all 3 – 2K chips are used

Step 4: Memory mapping:

2K x 8

Reg	A_{15}	14	13	12	11	10		A_0
F	1	0	0	0	0	0		0
								↳ 8000H
Lst	1	0	0	0	0	0	1 1 1 1 1 1	→ 87FF

K chip, logic select → K → Directly given to memory chip

1 0 0 0 1 0 0 0 0 0 → 8800 } chip2
1 0 0 0 1 1 1 1 1 1 → 8FFF }

1 0 0 1 0 0 0 0 0 0 → 9000(H) } 2K memory chip3
1 0 0 1 0 1 1 1 1 1 → 97FF(H) }

Bit Pattern:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	Chip Select.
1	0	0	0	0	2K x 8 1st
1	0	0	0	1	2K x 8 2nd
1	0	0	1	0	2K x 8 3rd.