# Class 08: NMOS, Pseudo-NMOS

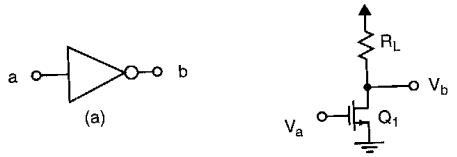
Topics:

- 02 NMOS Logic Gates
- 03 NMOS Logic Gates
- 04 Pseudo-NMOS
- 05 Pseudo-NMOS
- 06 Transistor Equivalency

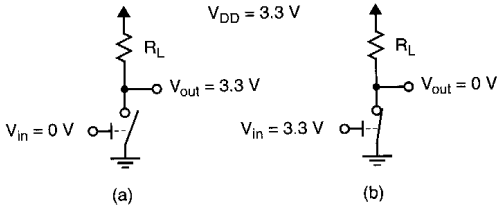
# Class 08: NMOS, Pseudo-NMOS

## NMOS (Martin c. 1)

- nMOS Inverter with resistive load



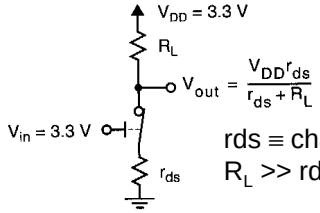

- switch level model




(a) NMOS off (b) NMOS on

want to realize resistor with a transistor

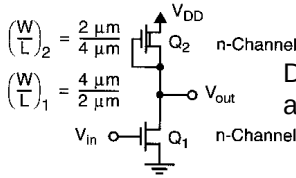
- Including transistor resistance




rds ≡ channel resistance

$R_L$ >> rds so output close to 0V

- nMOS Inverter with depletion load




n-Channel Depletion Transistor

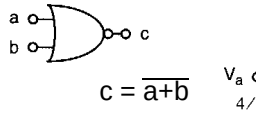
n-Channel Enhancement Transistor

Depletion nMOS, Vtn < 0

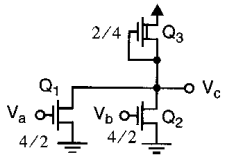
always ON for $V_{GS}$ = 0

W/L Q1 > W/L Q2 so Q1 can “pull down” Vout

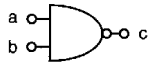
- nMOS NOR gate



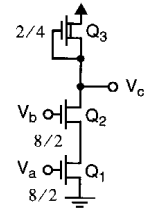

$c = \overline{a+b}$




- nMOS NAND gate



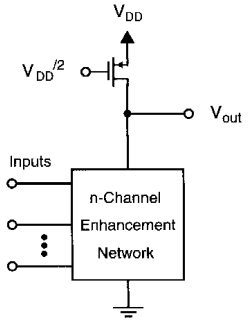

$c = \overline{ab}$



# Class 08: NMOS, Pseudo-NMOS

## NMOS (Martin c. 1)

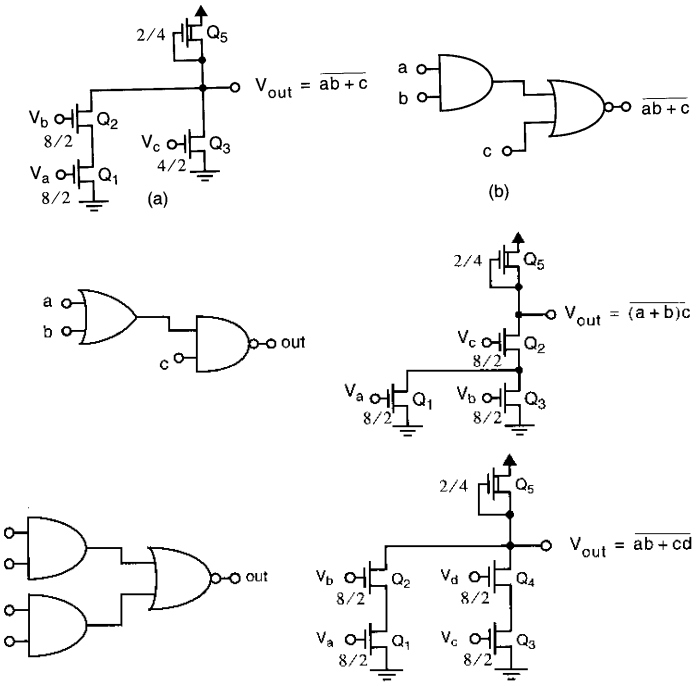
- General nMOS schematic




  - single load transistor
  - parallel and series nMOS transistor to complete the *compliment* of the desired function

    i.e., they determine when the output is low “0” rather than high “1”

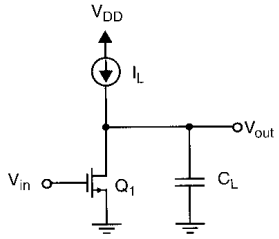
Examples: depletion-load nMOS logic



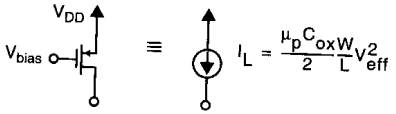
# Class 08: NMOS, Pseudo-NMOS

## Pseudo-NMOS (Martin c. 4)

•NMOS Common-Source Amplifier with current sourrce load and load capacitor




•Current-source realized with a PMOS transistor




$$I_D = \frac{\mu_p C_{ox} W}{2 L}(V_{SG} + V_{tp})^2$$

$$= \frac{\mu_p C_{ox} W}{2 L} V_{eff}^2$$

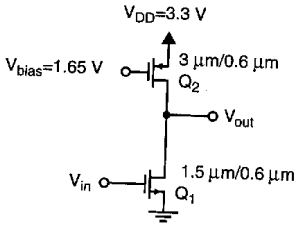
Veff = Vgs - Vt
Vds = Vgs + Vdg
at saturation, Vdg=-Vt

Valid if:
Veff = |Vds-sat| > |Vgs| - |Vtp|
-want drain at least Vt from gate

•Pseudo-NMOS inverter with PMOS load
•Choose W/L so that:

$$(W/L)_1 = \frac{(W/L)_2}{2}$$

•Choose Vbias in between VDD and ground




Q2 always on since |Vgs| > |Vtp|
Q2 in saturation if (for VDD=3.3)
|Vds| > |Veff| > |Vgs| – |Vt|
VDD – Vout > |Vgs| - |Vt|
Vout < VDD - |Vgs| + |Vt|
Vout < 1.65 + Vt < 2.45
Q1 in saturation if
Vgs = Vin > Vt
Vds > Veff > Vgs – Vt =>
Vout > Vin - Vt

•Power Dissipation:

output low (Vin is high): $P = I_L * VDD$

output high (Vin is low): $P = 0$

average static dissipation: $P = ½ * I_L * VDD$

# Class 08: NMOS, Pseudo-NMOS

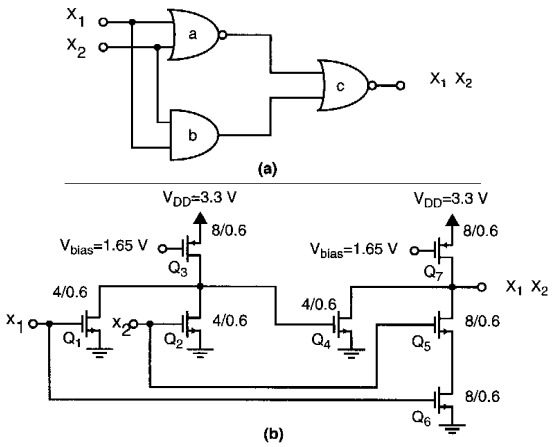
## Pseudo-NMOS (Martin c. 4)

XOR Logic in Pseudo-NMOS

$$y = x_1 \oplus x_2 = x_1\overline{x_2} + \overline{x_1}x_2 \qquad \text{remember:}$$

$$= \overline{x_1 x_2 + \overline{x_1}\,\overline{x_2}} \qquad a'+b' = (ab)'$$

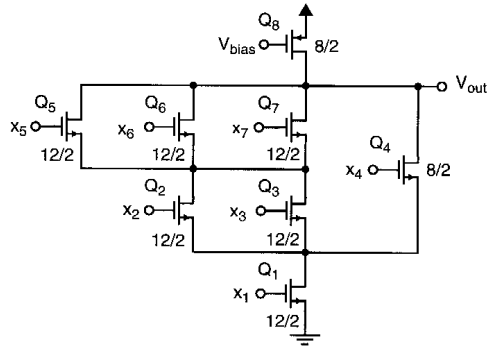
$$= \overline{x_1 x_2 + \overline{x_1 + x_2}} \qquad a'b' = (a+b)'$$




Evaluating functions from schematics

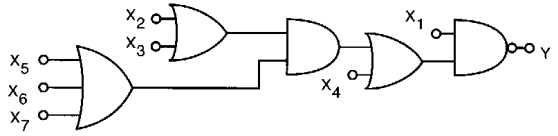
1. start with any transistor connected to ground
2. OR parallel and AND series transistors, combining all subnets in same manner
3. do again for each transistor connected to ground, and combine groups
4. take the compliment of the result

Example:




Vout' = [ x1 (x4 + (x2+x3) (x5+x6+x7) ) ]

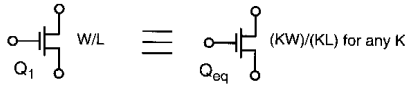
Vout = [ x1 (x4 + (x2+x3) (x5+x6+x7) ) ]'



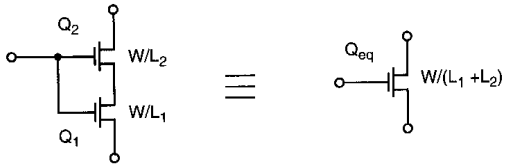
# Class 08: NMOS, Pseudo-NMOS

## Transistor Equivalency (Martin c.2, c.4)

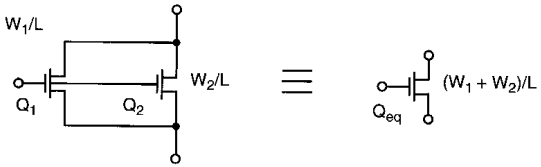
- Scaling both W and L




  - transistors act the same (to first order)
- Series Transistors

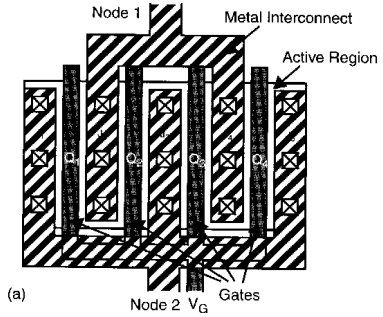



  - effectively increases L
- Parallel Transistors




  - effectively increases W

Example: Parallel Transistors



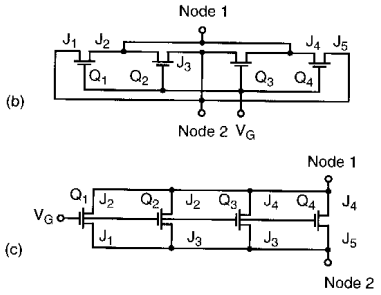




Figure 2.17: (a) layout, (b) schematic direct from layout, (c) simplified schematic