A Fully Integrated IEEE 802.15.7 Visible Light Communication Transmitter With On-Chip 8-W 85% Efficiency Boost LED Driver

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***Abstract*—This paper presents an IEEE 802.15.7 Physical Layer I (PHY-I) standard compliant visible light communication (VLC) transmitter system-on-a-chip (SoC), enabling the use of ordinary white LED lights as beacons or broadcasters for location-based applications. The mixed-signal SoC integrates a baseband digital signal processing (DSP) unit, a VLC modulator, and a switching boost LED driver with an on-chip power MOSFET. The DSP unit supports various coding schemes as well as both the on-off keying (OOK) modulation and the variable pulse-position modulation specified in the aforementioned standard. The boost LED driver is designed to power a matrix of 4 × 5 LEDs using Li-ion batteries for portable applications. The SoC simultaneously supports VLC and LED illumination with nine dimming levels. Implemented in a 0.35-μm CMOS process with 20-V devices, the SoC achieves a measured VLC data rate of up to 266 kb/s at a package error rate (PER) $< 10\%$ using a $2^{11}-1$ PRBS (pseudo random binary sequence) input. The communication distance measured is more than 2 m using no optical lens with the link efficiency of 5 nJ/bit. From an input at 3–5 V, the boost converter generates an output at 6–20 V with a 92% peak efficiency and an 8-W rating.**

***Index Terms*—Boost converter, IEEE 802.15.7, internet of Things (IoT), LED driver, system-on-a-chip, transmitter, visible light communication.**

I. Introduction

OWING to its high energy efficiency and high reliability, solid-state lighting using LEDs is being increasingly deployed for signaling, illumination and display applications. In particular, low-cost LEDs are expected to replace the existing fluorescent and incandescent lights and dominate the general illumination market in the near future [1]. Unlike other light sources, LEDs can be quickly switched ON and OFF, enabling visible light communication (VLC). As the switching frequency is high enough to achieve a reasonable data rate while the fast flickering cannot be perceived by human eyes, simultaneous illumination and VLC data transmission can be supported. Compared with conventional RF wireless communications, VLC offers several unique advantages: 1) no RF radiation and electromagnetic interference, 2) line-of-sight light propagation and high security, 3) use of unlicensed visible light spectrum with hundreds-of-THz bandwidth, and 4) compatibility with illumination infrastructure [2]. More importantly, thanks to the ubiquitous deployment of LED lights, VLC has tremendous potential to be part of the infrastructure supporting the Internet of Things (IoT).

Nowadays, most commercial white-color LED lights for illumination are implemented using a blue LED coated with a yellow phosphor layer. Due to the phosphor's slow temporal response, the LEDs exhibit modulation bandwidth typically limited to a few MHz [3] and thus high-speed data transmission is difficult to realize. For this reason, recent research is either focusing on improving the data rate for high-speed optical wireless links or utilizing the unique line-of-sight characteristic of VLC for some new applications which only require a low data rate. For the former, several simple approaches, including using a blue filter in front of the receiver to remove the slow-responding yellow-color component [4] and employing frequency-domain equalization in the LED driving circuitry to extend the effective modulation bandwidth [5], have been proposed to achieve transmission data rates over 40 Mb/s. In addition, more complicated techniques such as using discrete multi-tone modulation (DMT) [6] and carrier-less amplitude and phase modulation (CAP) [7] have been adopted to further push the data rate to 513 Mb/s and 1.1 Gb/s, respectively. In [8], novel InGaN-based resonant-cavity LEDs have been used as light source to achieve a data rate up to 100 Mb/s over 1-m distance. In [9], a multiple-input and multiple-output system using an array of micro-LEDs has demonstrated a data rate of 1 Gb/s. On the other hand, low-data-rate VLC systems, including location-based wireless broadcasting through LED lightings, signs with LED backlights and digital LED displays [10], as well as high-precision indoor positioning and navigation utilizing LED lights as location beacons [11], have demonstrated their technical advantages and superior performance over conventional solutions using RF.

Currently, most of the existing VLC prototypes are built using discrete components. A typical VLC system architecture is illustrated in Fig. 1. At the transmitter (TX) side, the VLC signal is superimposed onto the dc bias current and supplied to the LED array through a bias-T. At the receiver (RX) side, a photodetector (PD) is used to convert the optical signal into electrical current which is then amplified by a transimpedance amplifier

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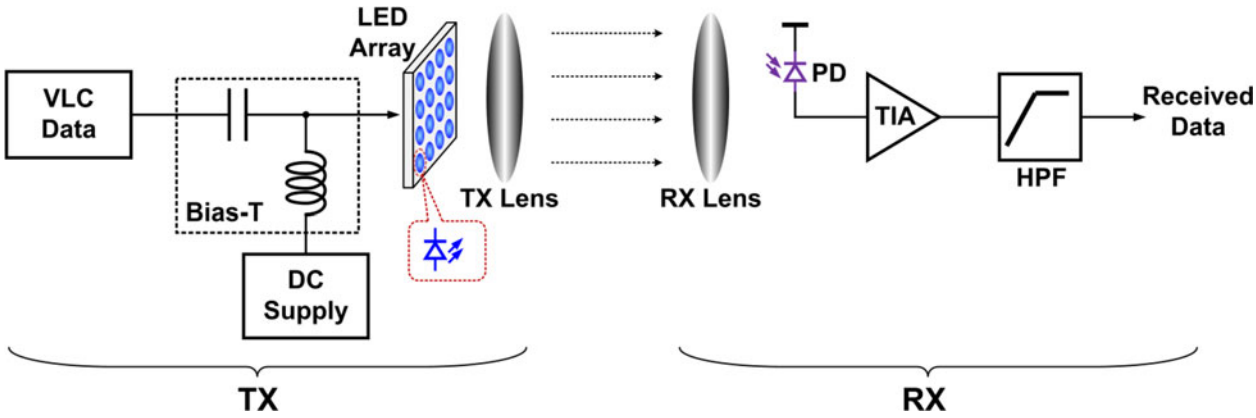

Fig. 1. Architecture of conventional VLC systems.

and passed through a high-pass filter to suppress the interference from ambient lights. Optical lenses are placed in front of the transmitter and the receiver to amplify the received optical signal. These discrete systems suffer from high cost, low reliability and large form factor. More importantly, the power consumption of dedicated VLC transmitters is prohibitively high, resulting in poor energy efficiency compared to widely-used RF wireless such as WiFi (Wireless Fidelity). Similar to other communication systems, CMOS integration could be a solution to addressing these issues, but existing VLC transmitter architectures are not suitable for on-chip implementation.

This paper describes the design and implementation details of a VLC transmitter SoC along with measured performance based on the results presented in [12]. Instead of using non-standard-based modulation and coding schemes for high data rates at the expense of short communication distances, the SoC is designed to be compliant with the IEEE 802.15.7 standard for VLC [2]. Implemented in a 0.35-μm CMOS process with 20-V high-voltage devices, the system measures a record transmission bit efficiency of 5 nJ/bit and a communication distance of more than 2 m without using any lens. Meanwhile, nine-dimming-level illumination is supported.

The paper is organized as follows. Section II briefly introduces the IEEE 802.15.7 standard and describes the proposed transmitter architecture. Section III discusses the modulation and coding schemes as well as the data flow of the baseband DSP unit. The design and circuit implementation of the VLC modulator and the LED driver are presented in Sections IV and V, respectively. Section VI describes the physical design of the SoC and shows the measurement results. Finally, the paper is summarized in Section VII.

II. System Architecture

A. IEEE 802.15.7 Standard [2]

The first release of IEEE 802.15.7 standard for wireless personal area networks using VLC was published in 2011. With multiple methods for flicker mitigation and dimming, simultaneous illumination and VLC data transmission are supported. As listed in Table I, there are three types of physical layers (PHYs) defined. PHY-I uses a single ordinary LED source and operates from 11.67 to 266.6 kb/s, targeting for low data rate applications. On the other hand, PHY-II offers much higher data rates from 1.25 to 96 Mb/s using a fast-response light source while PHY-III operates from 12 to 96 Mb/s based on color-shift keying (CSK) using multiple light sources with different colors. For each PHY, a variety of modulation and coding schemes are specified, corresponding to different data rates. This work focuses on the design and implementation of PHY-I hardware system to enable the use of ordinary white LED lights as broadcasters for location-based applications.

TABLE I
Three Physical Layers in IEEE 802.15.7 Standard

PHY Types	Modulation	Clock Rates	Data Rates
PHY-I	OOK & VPPM	200/400 kHz	11.67–266.6 kb/s
PHY-II	OOK & VPPM	≤120 MHz	1.25–96 Mb/s
PHY-III	CSK	12/24 MHz	12–96 Mb/s

TABLE II
PHY-I Operating Modes

Mod.	RLL Code	Clock Rates	RS Code	Convolutional Code	Data Rate
OOK	Manchester	200 kHz	(15,7)	1/4	11.67 kb/s
			(15,7)	1/3	24.44 kb/s
			(15,7)	2/3	48.89 kb/s
			(15,7)	none	73.3 kb/s
			none	none	100 kb/s
VPPM	4B6B	400 kHz	(15,2)	none	35.56 kb/s
			(15,4)	none	71.11 kb/s
			(15,7)	none	124.4 kb/s
			none	none	266.6 kb/s

1) PHY-I Operating Modes: The PHY-I operating modes are summarized in Table II. There are two modulation formats, on-off keying (OOK) modulation and variable pulse-position modulation (VPPM). OOK is a simple modulation in which the transmission of binary "1" and "0" is represented by turning the light ON and OFF for a specific time duration, respectively. VPPM uses the position of a pulse inside the transmission time slot to encode the information bits. For instance, a "0" transmission is

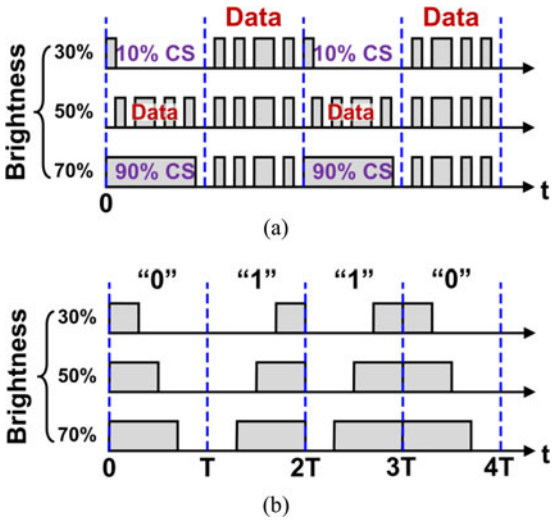

Fig. 2. Implementation of dimming: (a) OOK, and (b) VPPM.

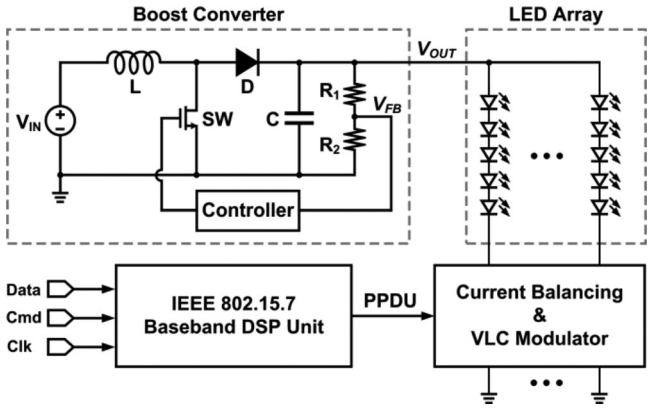

Fig. 3. System architecture of the proposed VLC transmitter.

TABLE III
BLOCK SPECIFICATION OF THE PROPOSED VLC TRANSMITTER

Building Blocks	Parameters	Values
VLC Modulator	No. of Channels	1–4
	Current Mismatch	$<1\%$
	Response Time	<125 ns
	Input Voltage	3–5 V
LED Driver	Output Voltage	6–20 V
	Max. Output Current	400 mA
	Switching Frequency	$\sim$2 MHz

indicated by sending a pulse which is aligned with the beginning of a transmission cycle, while a "1" is transmitted if the pulse is located at the cycle end. The number of consecutive 1 and 0 s is within an upper limit to mitigate flickering and to assist in clock and data recovery by using the run-length limited (RLL) codes. In OOK, the optical clock rate is 200 kHz and the Manchester coding is used for RLL codes. Forward error correction (FEC) is based on concatenated Reed-Solomon (RS) and convolutional codes. On the other hand, when operating in VPPM mode, the PHY's clock is doubled to 400 kHz and the 4B6B is used as RLL code. Only RS coding is adopted for FEC. Finally, different modulation and coding combinations result in various data rates, allowing the performance optimization according to the signal-to-noise ratio (SNR) of the VLC channel.

2) Dimming and Visibility Support: For power saving and energy efficiency improvement purposes, dimming function is supported in the standard. For OOK, dimming is performed by inserting compensation symbols (CS) into the data frame so as to maintain the required dc level according to the brightness settings. The data rate is reduced because of the less time available for data transmission. For instance, if the CS has the same period as the data, then a CS with 10% and 90% light intensity can average the overall brightness to be 30% and 70%, respectively, as illustrated in Fig. 2(a). Meanwhile, the data rate is reduced by half in both cases. As an exception, no CS needs to be added at 50% brightness, resulting in the highest data rate among all brightness settings. On the other hand, VPPM varies the pulse width in response to the requested dimming level without affecting the data rate, as illustrated in Fig. 2(b). Comparing the two dimming methods for OOK and VPPM, it can be observed that OOK allows a stable VLC transmission range at the expense of lower data rates, while VPPM provides constant data rates but its transmission range varies.

B. Proposed VLC Transmitter System

The system architecture of the proposed VLC transmitter consists of an IEEE 802.15.7 PHY-I baseband DSP unit, a VLC modulator, a dc–dc boost power converter and an LED array, as shown in Fig. 3. The DSP unit receives both data and commands from the MAC layer and performs modulation and coding as specified in the standard to generate a physical-layer data unit (PPDU). The PPDU is composed of a synchronization header for optical clock synchronization, a physical-layer header (PHR) indicating the data length and the modulation and coding scheme identifier (MCS ID), a header check sequence, and a PHY payload containing the actual data for transmission [2]. The PPDU feeds the digital input port of the VLC modulator which switches the LEDs ON/OFF to modulate their emitted light. The LED array is designed to be reconfigurable for different applications, and there can be up to 4 branches of LEDs with a maximum five LEDs in each branch. Ordinary white-color LEDs with a typical voltage drop of 2.8–3.8 V and a maximum current of 100 mA are employed here. Accordingly, the LED driver is designed to provide output of 6–20 V. Since its input is from Li-ion batteries whose output voltage is typically 3–5 V, the driver is a boost-type dc–dc power converter. Current balancing circuitry is included in the VLC modulator to equalize the output current among each LED branch and make it immune to the variations in the LED turn-on voltage. To realize VLC transmission, the LED current should respond to the digital data at a maximum modulation frequency of 400 kHz coming from the DSP unit. Furthermore, the transitions in the current waveform should be sufficiently fast to support accurate dimming in VPPM mode. Otherwise, the transition edges would contribute a considerable amount to the average dc level and thus would induce discrepancy to its desired linear variation versus the brightness settings.

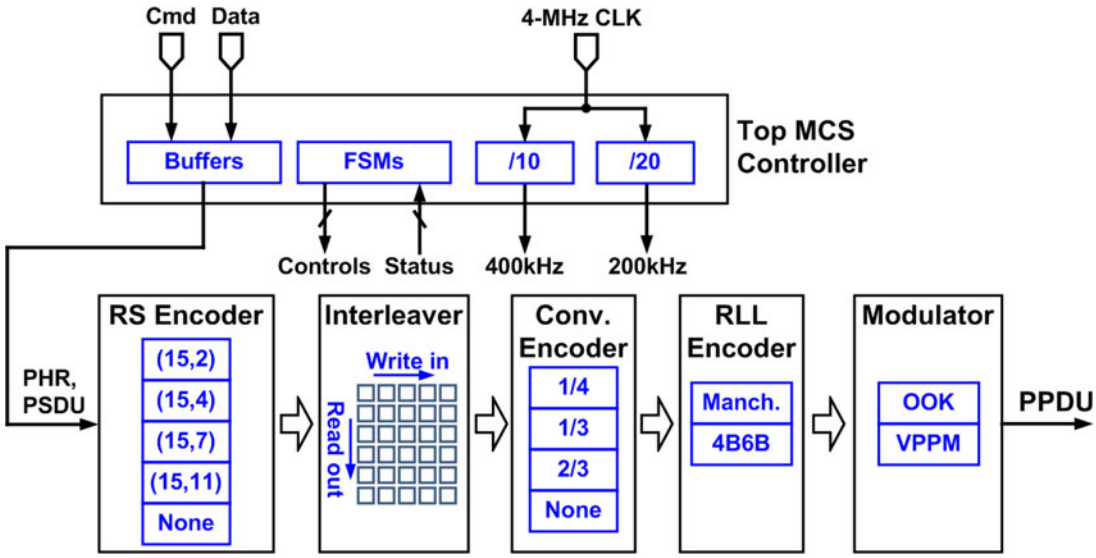

Fig. 4. Building blocks of the VLC baseband DSP unit.

As a result, for the VLC modulator, the rising and falling time of the switching is specified to be < 125 ns, which is shorter than 1/20 of the 400-kHz clock's period in VPPM, and the converter's switching frequency is optimized to around 2 MHz, as discussed later in Section V. Table III summarizes the important design parameters for both the VLC modulator and the LED driver.

III. VLC PHY-I Baseband DSP Unit

The VLC PHY-I baseband DSP unit processes the input data and command streams from the MAC layer and generates digital signal for the VLC modulator. As shown in Fig. 4, the baseband DSP unit mainly consists of an RS encoder, an interleaver, a convolutional encoder, an RLL encoder and a digital modulator. Their cooperation is coordinated by a top MCS controller. In this section, the design and implementation of each digital block will be discussed.

A. RS Encoder

An RS (n, k) code consists of k message symbols and (n–k) parity-check symbols [13]. In the IEEE 802.15.7 standard, there are four types of RS codes used as FEC outer codes, RS (15, 2), RS (15, 4), RS (15, 7), and RS (15, 11). These RS codes are all based on a finite field, Galois Field (2^4) arithmetic, which is defined by a primitive polynomial $x^4 + x + 1$. Mathematically, the generation of RS codes requires polynomial modulo operations whose direct hardware implementation is complicated and expensive. To avoid this issue, the RS encoder in this work is implemented using a structure based on linear feedback shift register (LFSR) [14] and pipelined multiplication-addition-shift operations. As an example, the implementation of the RS (15, 11) encoder is shown in Fig. 5. According to the generator polynomial $(x^4 + \alpha^{13}x^3 + \alpha^6x^2 + \alpha^3x + \alpha^{10})$, there are four multipliers with coefficients of α^{13}, α^6, α^3, and α^{10}, four stages of LFSRs, and four modulo-2 adders. As required by the Galois Field (2^4), the multipliers, the LFSRs and the adders are all 4-bit wide. Three switches are used to control the data flow. For the first 11 clock cycles of the encoding period, the switches *SW_A*1 and *SW_A*2 are closed while the switch *SW_B* is open. The 11 message symbols *M(x)* are shifted into the LFSR one by one at each clock cycle to perform modulo operation and they also feed the output directly. For the following four clock cycles, both *SW_A*1 and *SW_A*2 are open but *SW_B* is closed such that the LFSR keeps processing the loaded symbols and finally outputs the calculated remainder symbols (x^3, x^2, x^1 and x^0). To simplify the circuitry and optimize the performance, the multipliers are realized using look-up tables thanks to the fixed multiplication coefficients, while the adders are implemented

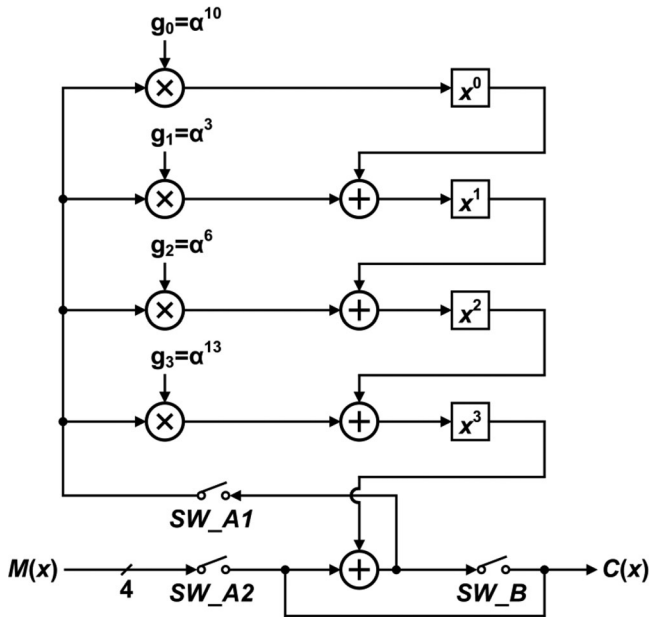

Fig. 5. Implementation of RS (15, 11) code based on LFSR.

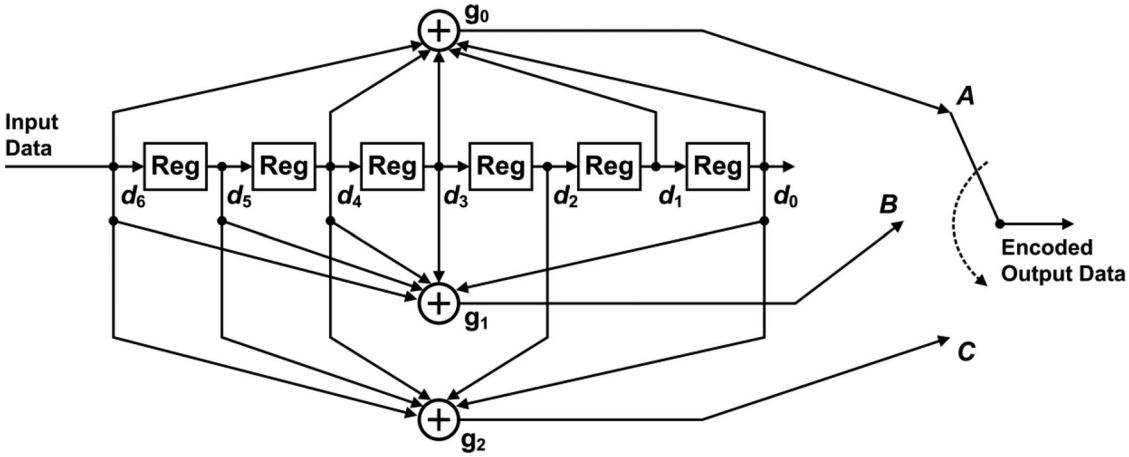

Fig. 6. Generation of the rate-1/3 mother convolutional code with constraint length of 7 and polynomial $g_0 = 133_8$, $g_1 = 171_8$ and $g_2 = 165_8$.

by 4-bit exclusive-OR gates. Furthermore, similar topologies with different stages of LFSRs and different coefficients are employed to generate the other three RS codes individually. Depending on the operating mode selected, only one of the four RS encoders is enabled at each time.

B. Convolutional Encoder

Convolutional code is used as inner code in the concatenated coding for FEC in OOK mode. As shown in Table II, there are three convolutional codes with different code rates, 1/4, 1/3, and 2/3. All of them are based on the rate-1/3 mother convolutional code with a constraint length of 7. Fig. 6 shows the generation of the mother convolutional code, where $g_0 = 133_8$, $g_1 = 171_8$ and $g_2 = 165_8$ are the generator polynomials. There are six stages of shift registers along the main data path to store the state of the encoder. Three XOR gates are used as modulo-2 adders to generate the three encoded data, *A*, *B* and *C*. Consequently, one source bit corresponds to three encoded bits, resulting in a code rate of 1/3. After that, the rate-1/4 code is obtained by puncturing two bits of the six encoded bits generated from two consecutive source bits and then duplicating the remaining bits. The rate-2/3 code is achieved similarly by discarding three out of the six encoded bits [2]. The puncturing operation doesn't cause any source data loss because of the redundancy produced by the rate-1/3 encoding. In order to terminate the encoder to an all zeros state as specified in the standard, six bits of zeros are appended to the end of the source data sequence.

C. Interleaver

An interleaver is located between the concatenated RS encoder and the convolutional encoder. As shown in Fig. 7, the interleaver consists of an array of shift registers whose height is 60-bit matched with the width of the RS codes and depth *d* is determined by the size of the data to be transmitted. Data shuffling is achieved by enabling the *LOAD* signal to load data packets horizontally and then activating the *READ* signal to read them out vertically. As a result, if a burst error appears in data transmission and the consecutive data within that period

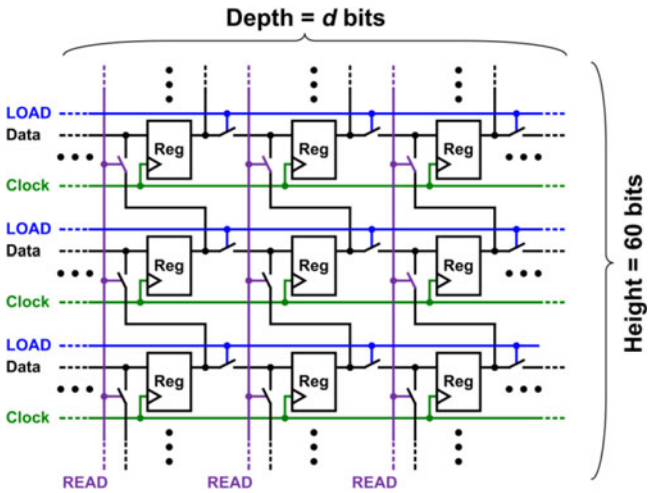

Fig. 7. Implementation of the $d \times 60$ two-direction shift register array used as interleaver.

is corrupted, the error bits will be distributed among several data packets such that each data packet will have fewer errors, increasing the probability of error correction at the receiver. At each time, only one of the two signals can be activated, which is guaranteed by the control logic.

D. RLL Encoder

The RLL encoder uses Manchester and 4B6B codes to limit the number of consecutive 1 and 0 s in OOK and VPPM operations, respectively. Manchester code represents binary data bits by transitions from one logical state to the other. The two logical states last for the same period such that the duty cycle is maintained constant. For VPPM, the 4B6B encoder maps 4-bit input data to 6-bit symbols which consist of the same number of 1 and 0 s, resulting in a constant dc level as well.

E. Digital Modulator

The digital modulator converts logical data to physical values. For OOK modulation, "0" and "1" are simply mapped to a low

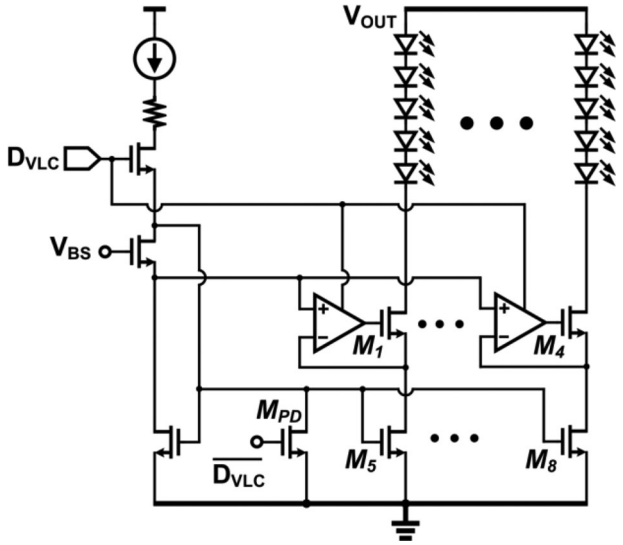

Fig. 8. Schematic of the proposed VLC modulator supporting four branches of LEDs.

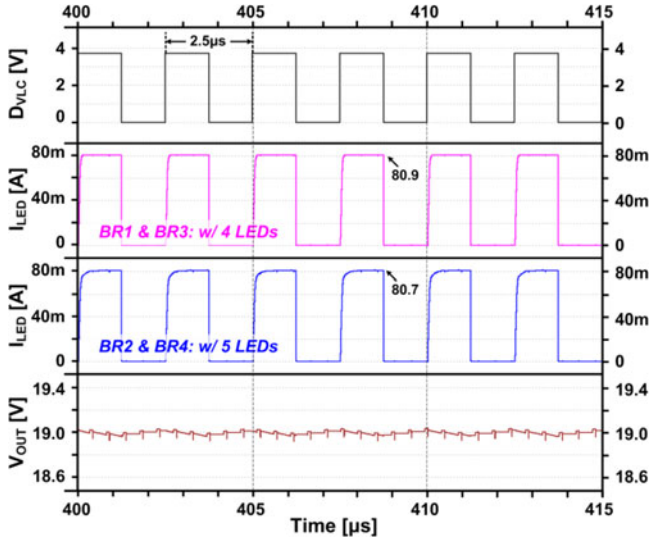

Fig. 9. Simulated transient waveforms of the VLC modulator with four or five LEDs in each branch.

voltage level and a high voltage level, respectively. As a result, no dedicated hardware is required. For VPPM, the physical value mapped from the logic "0" has a high-to-low transition and the physical value mapped from the logic "1" has a low-to-high transition, where the duty cycles are determined by the dimming settings, as shown in Fig. 2(b) discussed earlier in Section II.A-2. To support dimming control with a fine step of 10% as specified in the standard, the data period of 2.5 μs for VPPM is divided into ten identical time slots using a 4-MHz clock, which is 10 times as fast as the 400-kHz VPPM clock. The VPPM symbols representing logic "0" and "1" are then generated according to the required brightness level with their phase aligned with the 400-kHz clock.

F. MCS Controller

The MCS controller receives commands and data from MAC layer, and generates PHR and PSDU for the subsequent stages. More importantly, it coordinates the operation of each building block in PHY by monitoring their status and sending control signals to them. Two digital dividers are employed to generate the 200-kHz and the 400-kHz clocks from an external 4-MHz clock.

IV. VLC Modulator

The basic function of VLC modulator is to switch the LEDs ON/OFF according to the PPDU from the DSP unit. Meanwhile, it balances the current through the four branches of LEDs. Fig. 8 shows the schematic of the proposed VLC modulator based on a current-pulse driver in [15]. In the modulator, the regulated drain current mirror topology is employed. In the presence of LED turn-on voltage variations, the drain voltages of M_{5-8} are kept equal thanks to the feedback system composed of an op-amp driver and an NMOS (M_{1-4}). As a result, for the same gate voltage provided by the reference bias circuit, the current through the four LED branches would be equal. The digital VLC signal $D_{\rm VLC}$ is then applied to modulate the reference bias current and the current flowing through the transistors M_{5-8}. In addition, the gate of M_{5-8} is directly modulated by $\overline{D_{\rm VLC}}$ through a pull-down transistor $M_{\rm PD}$ to further speed up the turn-off time. To withstand the large voltage swing due to VLC modulation, the output transistors M_{1-4} are high-voltage NMOS (HV-NMOS) devices. The unity gain-bandwidth of the feedback loop at HV-NMOS gate nodes is designed to be ~6 MHz, which is ~15 times as high as the VPPM frequency of 400 kHz to ensure sufficiently fast transient response. In addition, the potential slow switching of the large HV-NMOS gate capacitance is avoided by shutting OFF their op-amp drivers and floating the gate nodes whenever $D_{\rm VLC}$ is low [15]. Simulations of the VLC modulator show that both the rising and falling time of the output current pulses are $<$ 100 ns for up to 100-mA per branch, which fulfills the specification in Table III. To verify the current balancing capability, transient simulations are performed. With all four branches active each of which consists of either four or five LEDs in series, the results show that the current mismatch is within 0.5 mA when the output voltage is 19 V, as plotted in Fig. 9.

V. DC–DC Boost LED Driver

A dc–dc boost power converter, depicted in Fig. 10, is designed to supply a tunable output of 6–20 V with a maximum current of 4 $\times$ 100 mA to drive an array of LEDs with up to four branches and five LEDs in series per branch. The controller circuitry and the power MOSFET are integrated on chip while the inductor, the capacitor and the Schottky diode are off chip.

As the LED current is switched ON/OFF by the VLC modulator, the load to the power converter experiences abrupt changes accordingly. In general, it takes several cycles for the converter to settle to a new state when the load varies, depending on how large the variation is. Intuitively, to obtain a modulated square

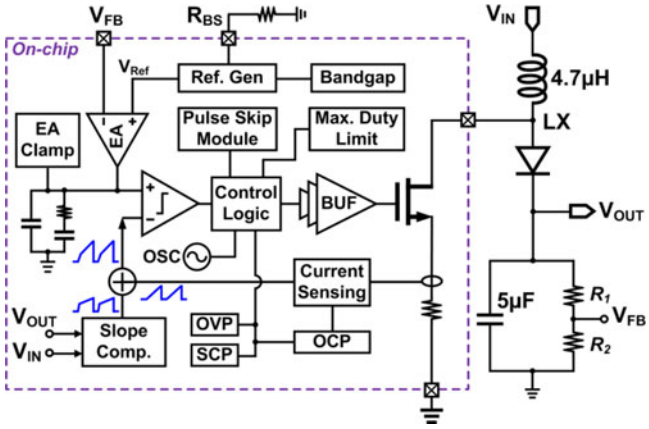

Fig. 10. Schematic of the dc–dc boost LED.

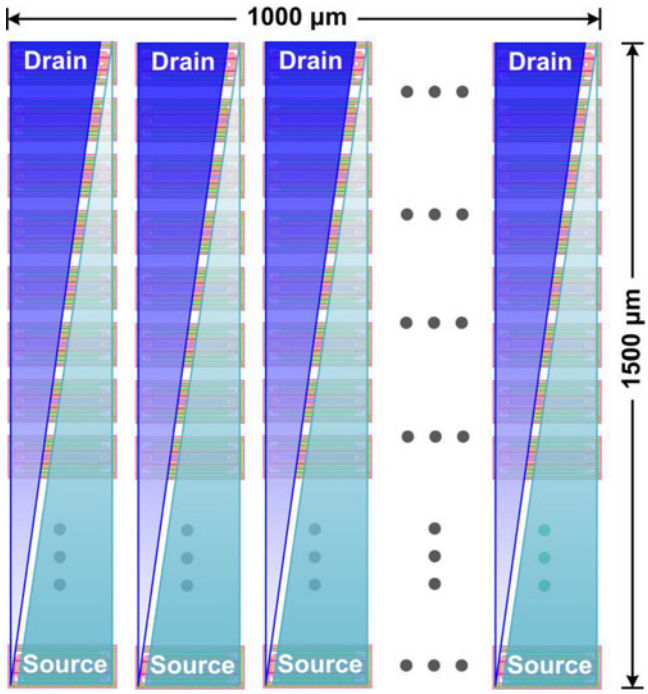

Fig. 11. Layout of the power device composed of 25 × 100 MOSFETs using Christmas-tree metal routings.

current waveform with sharp edges for VLC transmission and accurate dimming, the bandwidth of the power converter should be much higher than the VLC modulation frequency such that the settling time only occupies a negligibly small portion in each modulation period. On the contrary, if the modulation frequency is far beyond the power converter's bandwidth, the high-frequency current switching will not be responded by the closed-loop system such that no settling problem exists and the output current waveform would be approximately ideal. Therefore, in this VLC transmitter system, in order to accommodate the maximum modulation frequency of 400 kHz, the bandwidth of the power converter should be either higher than 4 MHz or lower than 40 kHz. In practice, a 4-MHz bandwidth is typically too high for a dc–dc boost converter because its required switching frequency would easily exceed 40 MHz such that the power efficiency would be significantly degraded. As a result, the bandwidth is designed to be ∼40 kHz, and the switching frequency is ∼2 MHz after optimizing the system stability.

The converter can operate in two modes: pulse skip mode under light load to ensure high efficiency, and pulse width mode (PWM) under heavy load to have a fixed switching frequency. For PWM, current-mode control with Type-II compensation is employed to guarantee the loop stability and to achieve fast response. Adaptive slope compensation by sensing the input and output voltage avoids sub-harmonic oscillations in current mode with duty ratio > 0.5. An error amplifier (EA) clamper is added to the output of the EA to limit the inrush current during start-up. An over-voltage protection with $\sim 1.2\ V_{\rm out}$ rating, an over-current protection for up to 3.5 A and a short circuit protection (SCP) are also implemented. An 8-W output power device is implemented on chip using a 100 000 μm/0.5 μm HV-NMOS. In the layout, it is arranged in a matrix of 25 × 100 small MOSFET with size of 40 μm/0.5 μm and occupies an area of ∼1.5 mm^2, as illustrated in Fig. 11. Using Christmas-tree structure, the metal routings for both the drain and the source are tapered to accommodate the current aggregation at the starting point and gradually decreasing towards the end. By doing so, a uniform current distribution is achieved and the mismatch of the voltage drops across the transistors at different locations is minimized.

The LED driver's transient response has been evaluated by simulations. In the simulation setup, an ideal switch in series with an LED branch is connected to the output of the boost converter and then a periodical digital modulation signal is applied. As shown in Fig. 12(a), when the VLC signal is 400 kHz as specified in the standard for VPPM, the current waveform is approximately ideal and the glitch at the beginning of each cycle is not a problem because of its negligibly short duration. To further verify the design considerations of the converter's bandwidth as discussed above, the VLC modulation frequency is varied from 25 to 2.5 kHz and the simulation results are summarized in Fig. 11(b) and (c), respectively. When the frequency is 2.5 kHz, the settling process lasts for ∼9% of the period in each cycle such that VLC transmission as well as accurate dimming control can be supported. However, when the modulation is at a frequency of 25 kHz, the settling process takes $>$ 30% of the period and thus would induce significant error to the brightness level under dimming.

VI. Experimental Results

The baseband DSP unit, the VLC modulator and the LED driver including power MOSFET have been integrated and fabricated in a 0.35-μm CMOS process with 20-V high-voltage devices. Fig. 13(a) shows the chip micrograph of the integrated VLC transmitter SoC. The overall area including the bonding pads is 4.0 × 2.0 mm^2, of which 1.5 × 1.5 mm^2 is occupied by the baseband with ∼37 k gate counts. For measurement, the SoC is mounted to a copper plane with a dimension of 4 × 6 mm^2 on PCB using chip-on-board with no extra heat sink, and another board is built to host an array of LEDs, as shown in Fig. 13(b)

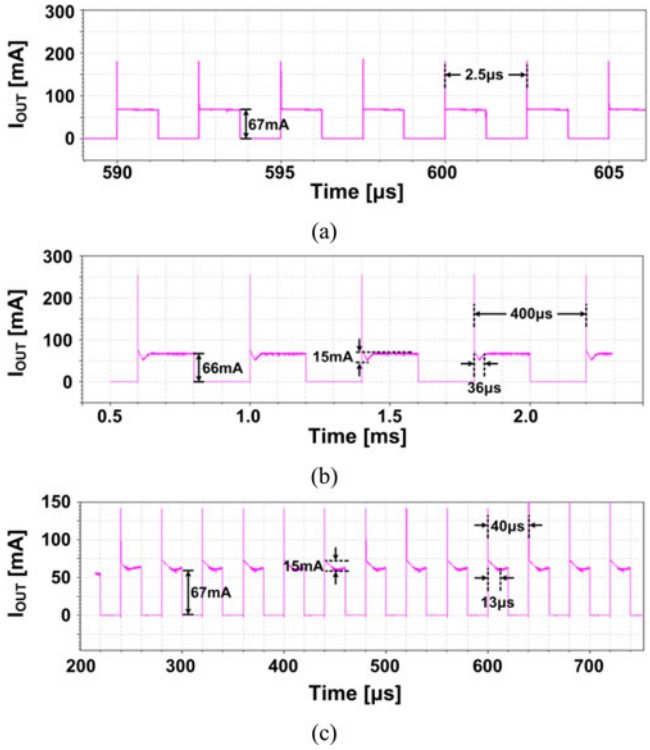

Fig. 12. Simulated transient waveforms of the LED driver with different VLC modulation frequencies: (a) 400 kHz, (b) 2.5 kHz, and (c) 25 kHz.

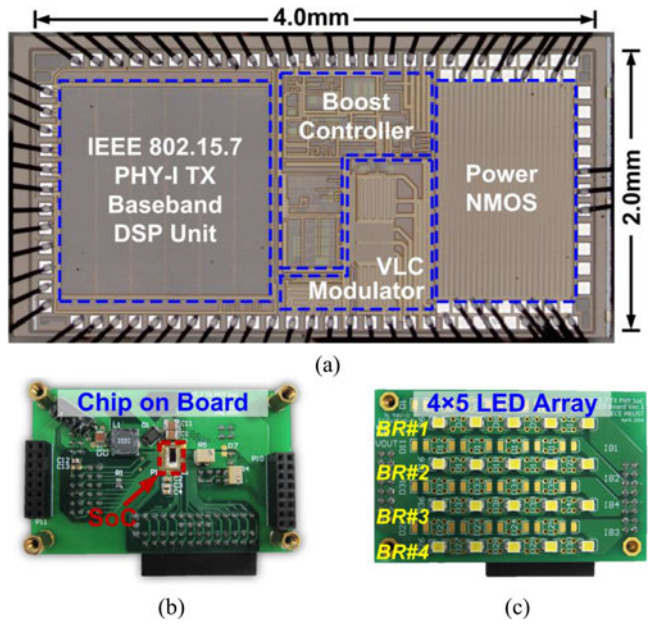

Fig. 13. (a) Chip micrograph of the integrated VLC transmitter SoC. (b) PCB with the SoC mounted using chip-on-board, and (c) PCB hosting an LED array.

and (c), respectively. The two boards are then connected together to construct a complete VLC transmitter system as depicted in Fig. 3. No optics are used at the LED array PCB.

First of all, the dc–dc boost LED driver is characterized individually. In the measurement setup, its input voltage is provided

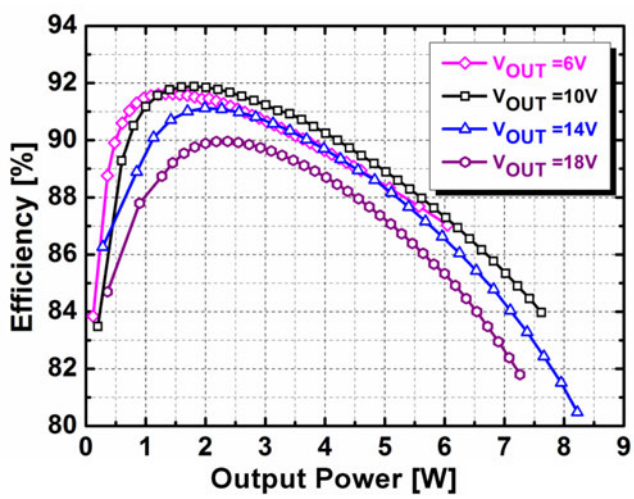

Fig. 14. Measured power efficiency of the dc–dc boost LED driver.

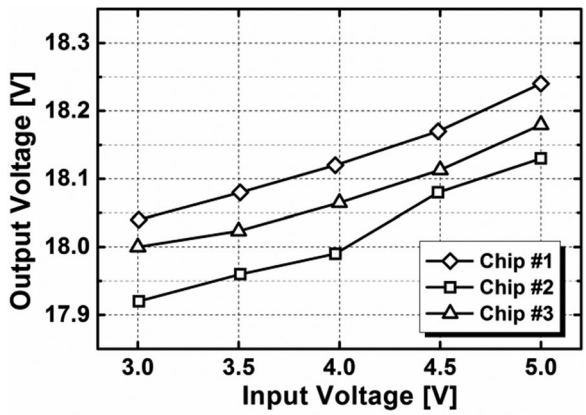

Fig. 15. Measured line regulation of the boost converter.

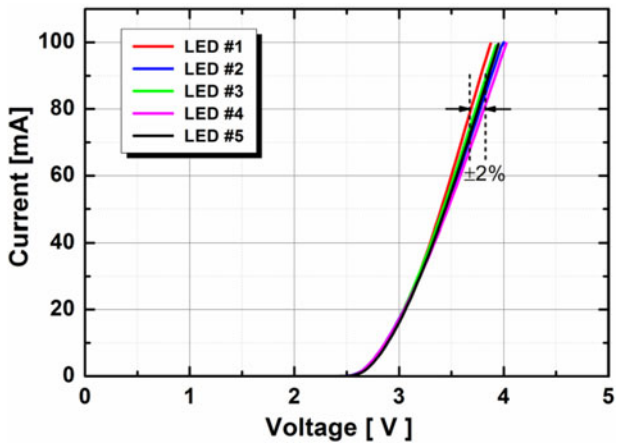

Fig. 16. Measured *I–V* characteristic of the five randomly picked ordinary white LEDs.

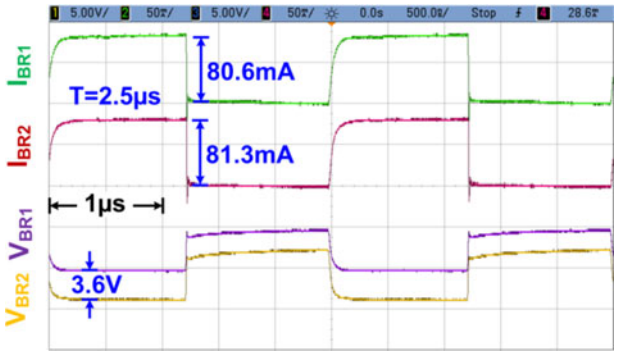

Fig. 17. Measured current and voltage drop differences with two different LED branches connected to the VLC modulator.

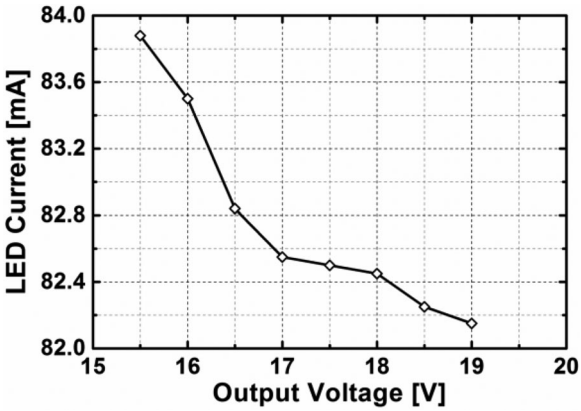

Fig. 18. Measured LED branch current versus output voltage.

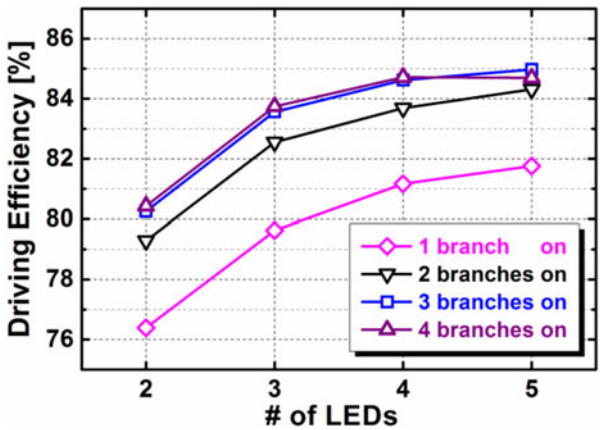

Fig. 19. Measured LED driving power efficiency.

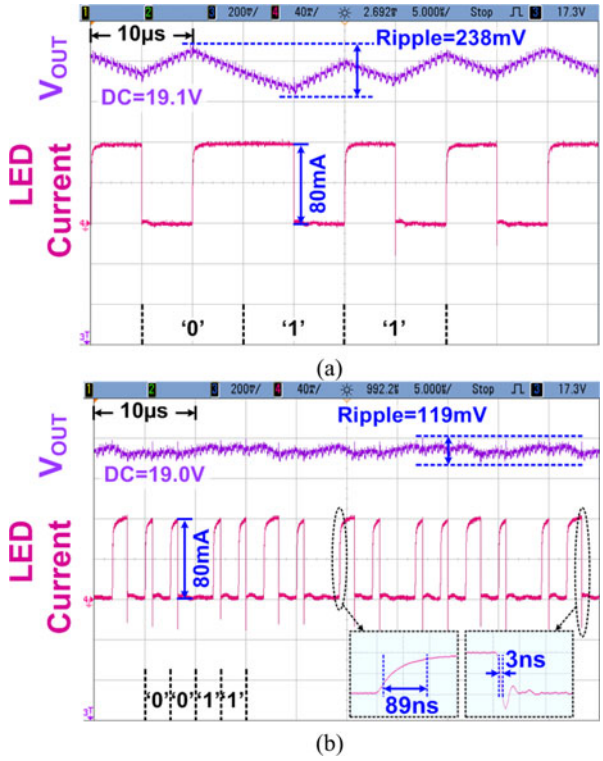

Fig. 20. Measured transient response of the VLC transmitter SoC while driving two branches of LEDs: (a) 50%-brightness OOK modulation, and (b) 30%-brightness VPPM.

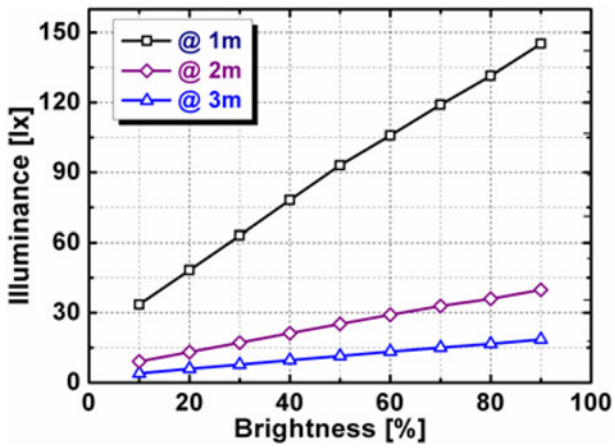

Fig. 21. Measured light intensity versus brightness settings.

by a dc voltage source (ADCMT 6244) and the output is loaded by a current source (ADCMT 6243). As the electronic load varies, the boost converter measures efficiency better than 80% for the entire output power range up to 8 W, as plotted in Fig. 14. A peak efficiency of 92% is achieved at $V_{\mathrm{OUT}} = 10$ V when the output power is 2 W. In steady state, the measured switching frequency is ∼1.7 MHz which is close to the specification. For the line regulation measurement, the output voltage is set to be ∼18 V and the input voltage is swept from 3 to 5 V. The measured output voltage varies within 0.25 V, which is less than 1.5%. Three chips were measured and their results are shown in Fig. 15.

In the following measurements, ordinary white-color LEDs in an industry standard footprint (Cree CLA1B-WKW-XD0F0E23) are used. The measured *I*–*V* curves of five randomly picked samples are plotted in Fig. 16, indicating a voltage drop variation of ±2% for the same current of 80 mA. By sweeping the LED modulation frequency and observing the signal

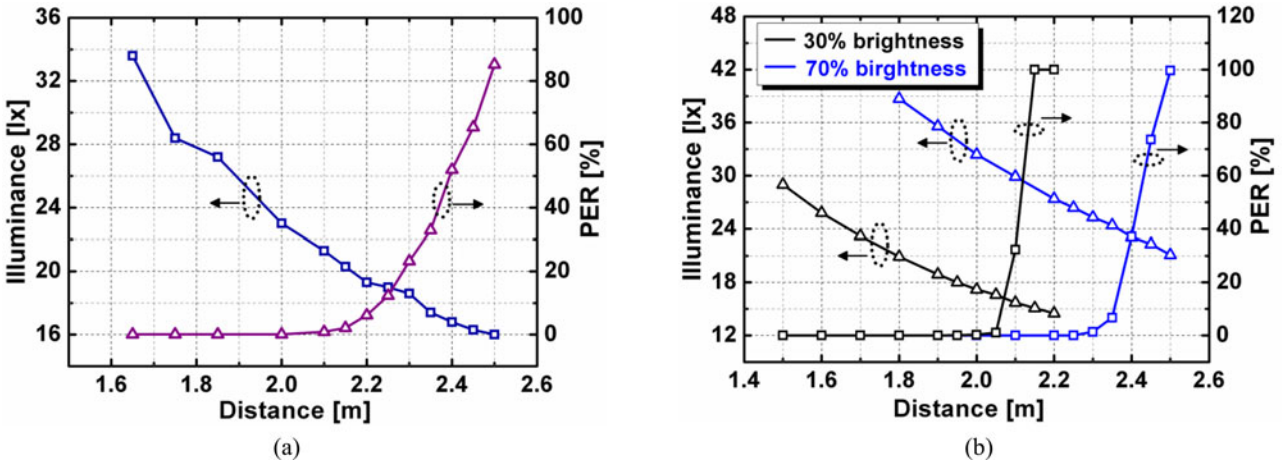

Fig. 22. Measured illuminance and PER: (a) 73.3-kb/s OOK, and (b) 124.4-kb/s VPPM.

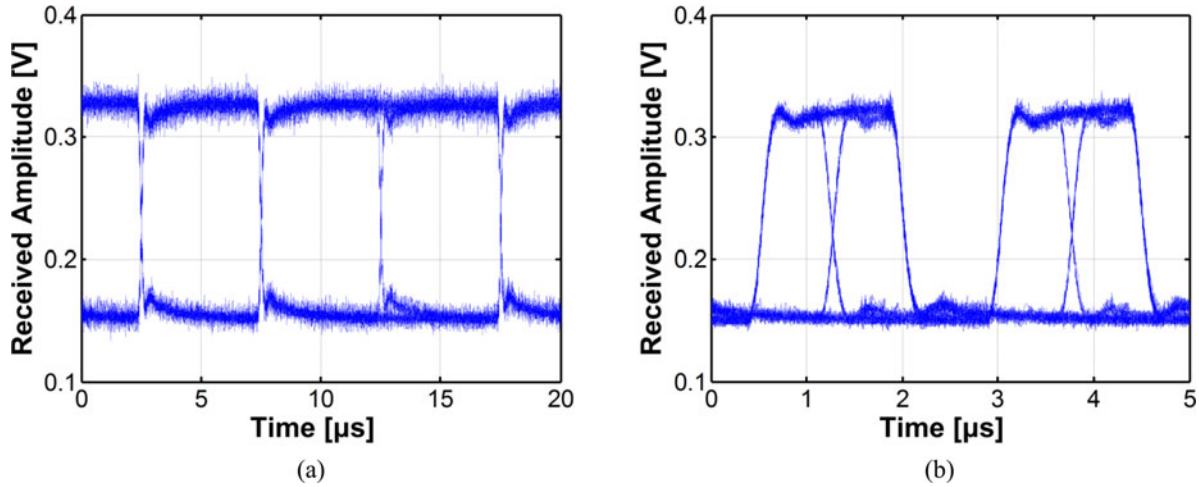

Fig. 23. Measured eye diagrams: (a) 73.3-kb/s OOK at 50% brightness, and (b) 124.4-kb/s VPPM at 30% brightness.

amplitude received by a photodetector (New Focus 1801) with 125-MHz bandwidth, the frequency response can be obtained [16]. The –3dB-bandwidth is around 2.2 MHz, which is wide enough to support 400-kHz VLC modulation.

To evaluate the current balancing of the VLC modulator, a load mismatch is deliberately introduced by using two different branches of LEDs, one with five LEDs in series and the other with four LEDs. As the 400-kHz VLC signal is applied to the VLC modulator, the current flowing through these two branches is measured by an oscilloscope. As shown in Fig. 17, even the voltage drop differs by 3.6 V for the two branches of the LEDs, their current difference is only 0.7 mA corresponding to a $< 1\%$ mismatch. Individual LED branch current versus output voltage is measured and plotted in Fig. 18. As the output voltage is varied from 16 to 19 V, a variation of 1.8 mA is observed in the output current drawn by four LEDs in series.

To drive different numbers of LEDs, the output voltage of the boost converter is adjusted by tuning the resistor divider composed of R_1 and R_2 to set the feedback voltage $V_{\rm FB}$ such that the voltage drop across the VLC modulator is around 1 to 1.5 V. The LED driving power efficiency characterized as the ratio of power obtained by the LEDs over the total input power to the boost converter was measured for various numbers of LEDs, with $V_{\rm FB}$ fixed at $\sim$1 V. As shown in Fig. 19, the efficiency varies within a range from 76% to 85%.

Loaded by two branches of LEDs and five LEDs per branch, the transient response of the VLC transmitter SoC is measured. Fig. 20(a) and (b) shows the measured LED current waveforms under OOK and VPPM at 50% and 30% brightness, respectively. The VPPM waveform showing a 3-ns fall time and an 89-ns rise time demonstrates the VLC modulator speed and the proper design of the power converter bandwidth. The relatively long rise time is due to the larger parasitic capacitance of the HV-NMOS M_{1-4} in comparison to the normal NMOS devices M_{5-8}. The output voltage of the converter measures 19 V, with maximum ripples of 238 and 138 mV under OOK and VPPM, respectively.

With the SoC driving 4 $\times$ 5 white LEDs which consume a maximum power of 6-W, the light intensity versus brightness at different distances measured by a lux meter (Extech Easyview 33) is plotted in Fig. 21, demonstrating 9-level

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON OF THE VLC TX SOC

		This work	PTL′08 [5]	JLT′10 [6]	PTL′08 [17]
Power	VLC	0.81–1.25 mW	N/A	N/A	N/A
	LED	0.6–5.4 W	1.5 W	9.8 W*	4.5 mW
	Balancing	0.08–0.48 W	N/A	N/A	N/A
Power Efficiency	Converter$^{\Delta}$	80%–92%	N/A	N/A	N/A
	LED driving$^{\wedge}$	76%–85%	N/A	N/A	N/A
Data Rate		≤266.6 kb/s	≤50 Mb/s	≤450 Mb/s	≤3 Gb/s
Range	w/o lens	∼2 m	N/A	N/A	N/A
	w/lens	>20 m	2m	0.3 m	0.05 m
Bit Efficiency$^{\#}$		∼5 nJ/bit	N/A	N/A	N/A
Standard Compliant		IEEE 802.15.7	N/A	N/A	N/A
Integration Level		Fully Integrated (VLC TX + LED Driver + Power MOSFET)	Discrete	Discrete	Discrete
3-dB BW of LEDs		2.5 MHz	2.5 MHz	35 MHz	60 MHz

*Estimated from data sheet.
$^{\Delta}$ Total output power /Input power.
$^{\wedge}$Output power consumed by LED/ Input power.
$^{\#}$Power consumed by VLC /Data rate.

TABLE V
PERFORMANCE SUMMARY AND COMPARISON OF THE BOOST CONVERTER

	This Work	TPE′15 [18]	ESSCIR′06 [19]	JSSC′14 [20]
Input Voltage	3–5 V	5 V	3.05–5.5 V	2.7–4.5 V
Output Voltage	6–20 V	5.5–36 V	5.6–25 V	8 V
Max. Output Power	8 W	8.6 W	4.2 W$^{\wedge}$	2.4 W
Switching Frequency	1.7 MHz	1 MHz	0.9/1.2/1.8 MHz	0.9 MHz
Inductor/Capacitor	4.7 μH/5 μF	3.3 μH/20 μF	10 μH/4.7 μF	10 μH/10 μF
Peak Efficiency	92% @ 1.8 W	93% @ 2.4 W	80% @ 3 W	90% @ 0.48 W
Power Device	On-chip	On-chip	Off-chip	Off-chip
Area	2.57 mm^2	4.0 mm$^{2\#}$	0.34 mm^2	1.86 mm^2

$^{\#}$Pads included.
$^{\wedge}$ Estimated at maximum current.

dimming control with an approximately ideal linearity. Afterwards, a lensless VLC receiver consisting of an analog front-end with 100-dBΩ transimpedance gain and 4.6-MHz bandwidth, and a FPGA baseband unit is used for measuring the transmitted VLC signals. Fig. 22 summarizes the measured performance. At PER $< 10\%$ with a 2^{11}–1 PRBS input, the achievable distance is 2.2 m with 19.3-lx illuminance for 73.3-kb/s OOK modulation at 50% brightness. For 124.4-kb/s VPPM, the maximum VLC distances are 2.0 and 2.3 m with illuminance of 16 lx and 25 lx at 30% and 70% brightness settings, respectively. The measured eye diagrams at 50%-brightness OOK and 30%-brightness VPPM are presented in Fig. 23(a) and (b), respectively. Furthermore, by placing an optical lens with focal length of 100 mm and diameter of 10 mm in front of the receiver, the measured error-free communication distance is extended to 20 m.

Table IV summarizes the VLC transmitter SoC performance. For the power consumption, a 0.6−5.4-W is for the LEDs while the VLC baseband DSP unit only consumes less than 1.25 mW. As the LEDs are for illumination like in ordinary applications, the additional power used by VLC is negligibly small, yielding the highest VLC transmission efficiency reported to date at 5 nJ/bit. Meanwhile, the LED driver's performance in terms of power efficiency and input/output voltage ranges is comparable with state-of-the-art prototypes without integrating VLC, as shown in Table V.

VII. CONCLUSION

In this work, a VLC transmitter system architecture consisting of a digital baseband unit, a VLC modulator and a boost LED driver has been proposed and a fully integrated IEEE 802.15.7 PHY-I VLC transmitter SoC has been implemented. Measurement results indicate that simultaneous illumination with nine dimming levels and VLC data transmission with various data rates specified in the standard have been achieved. More importantly, the energy efficiency achieves a record value of ∼5 nJ/bit, demonstrating the importance and advantages of integration for adding low-power, cost-effective VLC capabilities to standard white LED lights.

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