DESIGN AND IMPLEMENTATION OF IEEE 802.15.7 VLC PHY-I TRANSCEIVER

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ABSTRACT

This paper presents the design and implementation of a VLC (visible light communication) transceiver complying with the Type-I physical layer (PHY-I) specified in IEEE 802.15.7 Standard. Both the system architectures and the building blocks are described in detail. The design is implemented by Verilog-HDL and verified on Xilinx Virtex-5 Field-Programmable Gate Arrays (FPGA). Layout implementation using ASIC development tools is also provided for the transmitter design. The system is targeted at information broadcasting with data rates from 11.67 kb/s to 266.6 kb/s. Measurement result proves that the system can achieve a bit error rate (BER) of 10^{-6} when the received illuminance is 18 lx.

INTRODUCTION

Visible light communication is now being regarded as a compelling technology for supplementing conventional RF communications, thanks to its special features including line-of-sight, high security, ultra-wide available spectrum and no RF radiation or interference. High-speed data downlink and high-precision indoor localization are two of the most promising applications. Nowadays, the light sources used for VLC are mostly from LEDs, which are susceptible to digital modulation at frequencies sufficiently high for meaningful data rates without affecting the basic illumination function. As the LEDs are more and more ubiquitously deployed to replace the existing incandescent and fluorescent lights, large-scale commercialization of VLC can be foreseen.

Standardization and IEEE 802.15.7

There are quite a few standards for VLC, including IEEE 802.11 IP PHY, IEEE 802.15.7 and JEITA CP-1221. In particular, IEEE 802.15.7 provides a global standard for short-range VLC utilizing the unlicensed spectrum, from 380 nm to 780 nm. Both the PHY and MAC layers are defined specifically to achieve sufficiently high data rates for audio and video transmission, while the basic functions, for example, illumination and display are not affected [1].

As specified in the standard, there are three different types of PHY with various combinations of digital modulation and coding schemes (MCS). The operating modes, corresponding MCS and achievable data rates of PHY-I are summarized in Table I. For OOK (on-off keying) modulation, the data rates range from 11.67 kb/s to 100 kb/s, while for VPPM (variable pulse position modulation), the data rates are from 35.56 kb/s to 266.6 kb/s.

The transmitted data is first packaged into a physical-layer data unit (PPDU), and then encoded and modulated by one of the above operating modes which are selected by the MAC. As shown in Figure 1, Each PPDU consists of a synchronization header (SHR), a physical-layer header (PHR), and a PHY service data unit (PSDU). The SHR acts as an indication of the beginning of PPDU, and its repeated '01' data pattern facilitates the receiver's clock synchronization. The PHR contains essential information for the receiver to successfully

Table I: PHY-I Operation Modes

Modulation	RLL code	Optical clock rate	RS code	Convolutional code	Data rate
OOK	Manchester	200 kHz	(15,7)	1/4	11.67 kb/s
			(15,11)	1/3	24.44 kb/s
			(15,11)	2/3	48.89 kb/s
			(15,11)	none	73.3 kb/s
			none	none	100 kb/s
VPPM	4B6B	400 kHz	(15,2)	none	35.56 kb/s
			(15,4)	none	71.11 kb/s
			(15,7)	none	124.4 kb/s
			none	none	266.6 kb/s

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demodulate the incoming PSDU, such as the operating mode, the size of the PSDU, etc. The PSDU carries the actual information to be transmitted.

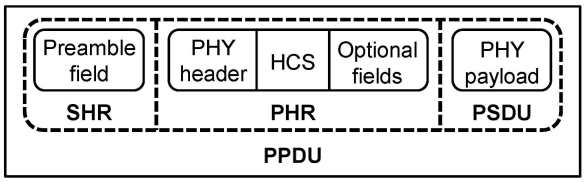

Figure 1: Physical-layer data unit format

Although the 802.15.7 Standard specifies the PHY-I data transmission, the implementation is not described in detail. In addition, there are only basis guidelines on the RX implementation. In this paper, a detailed TX design is implemented based on the specification and an RX architecture that is fully compatible with the TX is proposed and implemented.

TRANSMITTER DESGIN

The block diagram of the PHY-I TX is shown in Figure 2. Both the PHR and the PSDU are encoded, while the SHR is transmitted directly. The PHR is always sent at the lowest data rate for the chosen clock rate with OOK modulation, whereas the PSDU is encoded according to the MCS as defined in the PHR.

Four types of RS encoders, RS(15, 2), RS(15, 4), RS(15, 7), and RS(15, 11), are used in the TX baseband with Galois field (16) [2].

There are two interleavers, one with fixed depth for the PHR, and the other with dynamic depth for the PSDU. The height of the interleavers is defined by the total block size of the RS encoder, which is composed of 15 symbols, i.e. 60 bits. The interleavers shuffle the data sequence to mitigate the burst error effect.

With a rate-1/3, K = 7 convolutional encoder as the base, different code rates, rate-1/4 and rate-2/3, are achieved by puncturing some of the encoded bits.

Manchester and 4B6B encoders are the two types of RLL encoders that are used for 200 kHz and 400 kHz clock rates, respectively. To balance the DC level of the output and provide clock recovery information, the Manchester encoder converts a 1-bit data into a 2-bit transition, and the 4B6B encoder maps each 4-bit data into a 6-bit pattern.

In OOK modulation, a 'high' symbol represents a '1', and a 'low' symbol represents a '0'. In VPPM, a 'high' to 'low' transition represents a '0' and vice versa. The duty cycle of the VPPM is defined by the dimming setting of the TX.

Between the building blocks, data buffers are inserted to make data conversion between serial and parallel. As an example, the RS encoder has a 4-bit serial output but the input for the interleaver is 60-bit parallel. Thus, a serial to parallel data buffer is needed at the interface between the RS encoder and the interleaver.

The top MCS control module recognizes the control command and determines which operation mode is used for data transmission. It coordinates the operation of each sub-module to make sure the data flow is consistent.

An NMOS with five white LEDs in series forms the front-end of the TX, as shown in Figure 2.Commercial white LEDs that consist of blue LEDs with yellow phosphor are used. The NMOS performs as a high speed switch for visible light signal modulation.

RECEIVER DESGIN

Figure 3 shows the block diagram of the complete receiver, which is discussed as follows.

The RX analog front-end is composed of a PD (photodiode) and a TIA (transimpedance amplifier). The PD converts the received light signal into a current signal, which is then converted to a voltage signal and amplified by the TIA. The PD provides a sensitivity of 0.15 A/W for

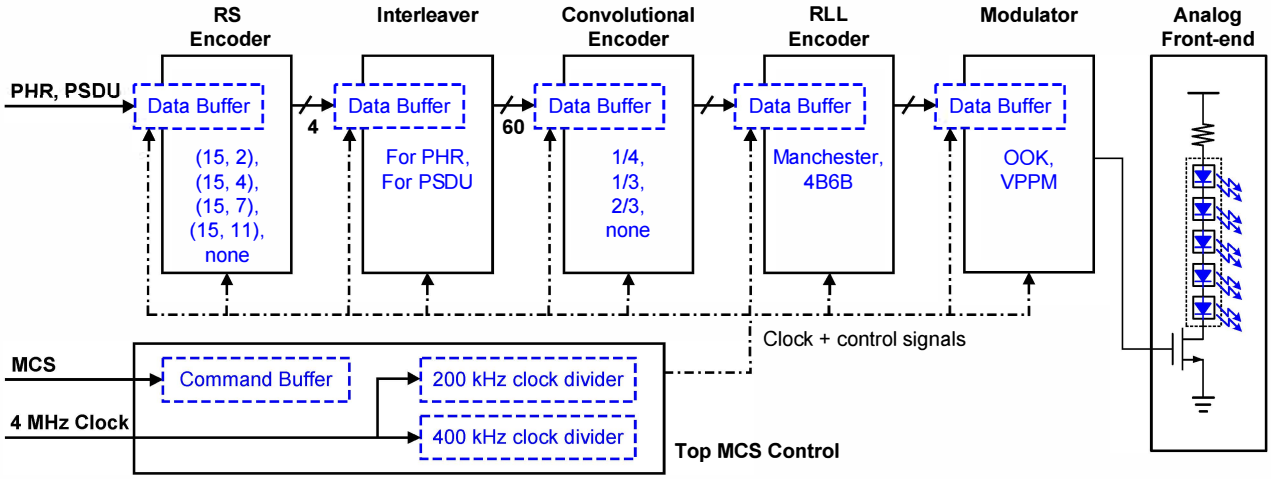

Figure 2: PHY-I TX block diagram

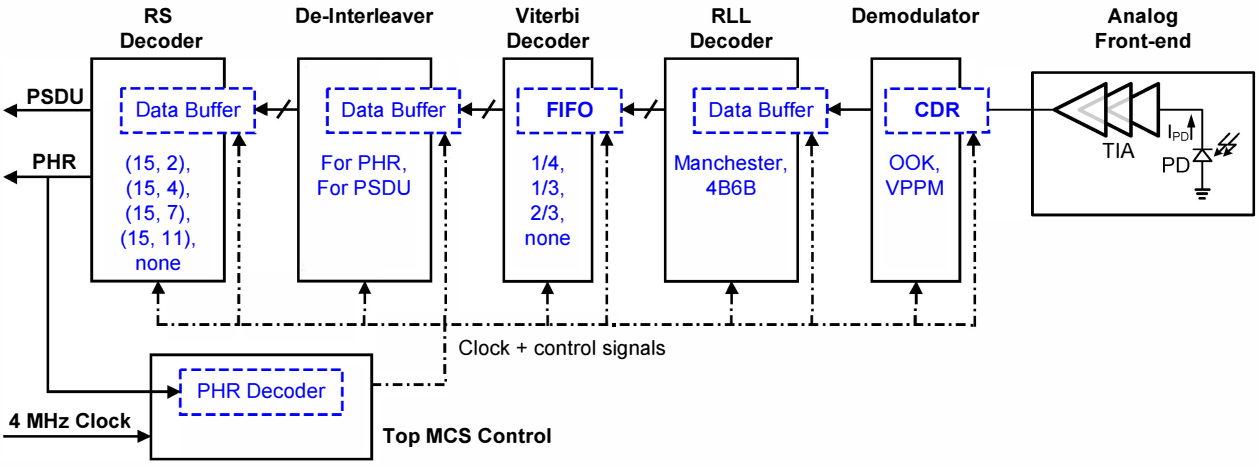

Figure 3: PHY-I RX block diagram

450 nm wavelength light. The TIA is designed to contribute a 114-dBΩ transimpedance gain with a -3 dB bandwidth of 1.4 MHz to cover both the OOK and the VPPM signal.

The demodulator mainly consists of a clock and data recovery circuit. It is achieved by using the phase picking algorithm described in [3]. To find an optimum balance between the dynamic power consumption and CDR accuracy, the oversampling rate is set to be 10 for the 400-kHz data stream. Therefore, the main clock is designed to be 4 MHz, and the bit decision for both OOK and VPPM demodulation is done inside the clock and data recovery module.

Manchester encoded data is decoded by looking at two bits at a time and marking a high to low transition as '1' and low to high transition as '0'. While the 4B6B decoder is implemented using a look-up table. Sixteen 6-bit words are mapped to the corresponding 4-bit symbols, while in case of receiving an erroneous 6-bit word, a soft decision is taken to map it to the nearest symbol based on hamming distance.

Viterbi decoder is implemented using the Xilinx IP core [4]. A standard type parallel architecture with reduced latency is chosen to attain high decoding rate. While the PHR is being decoded, the PSDU is kept in the FIFO as the PHR carries information about the decoding and demodulation scheme to be used for PSDU. Therefore, to reduce the depth of the FIFO and the overall decoding time of a packet, a faster architecture is chosen at the expense of larger area consumption. Also, to increase the error correction capability of the decoder, soft decision capability is enabled in the core.

Following the same pattern as in TX, two separate de-Interleavers are implemented for PHR and PSDU. The de-interleaver must be compatible with the interleaver on the TX side. Therefore the height is fixed to be 60 bits while the depth can be of variable size depending on the length of the PSDU and PHR used in the packet.

Out of the four RS decoder types used in the, RS(15,4) and RS(15,2) have the capability of erasure correction. All of these decoders can be obtained by one master decoder with a few controlled manipulations. The decoder architecture is based on decomposed inversion-less Berlekamp Massey algorithm [5].

EXPERIMENTAL RESULTS

Hardware Implementation and Testing

Figure 4 shows the hardware implementation of the transceiver. The TX and RX designs have been implemented on two separate FPGAs, whose models are Xilinx Virtex-5 xc5vlx110t. Table II summarizes the resource occupied. The layout for the TX design implemented in AMS 0.35 µm process is provided in Figure 5. It occupies an area of 1.56 x 1.56 mm^2.

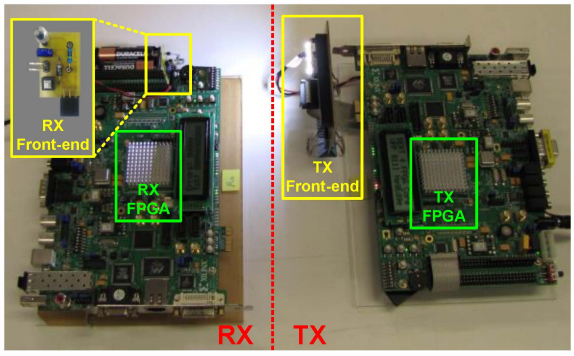

Figure 4: Transceiver hardware implementation

Table II: FPGA Utilization

FPGA Resource	TX		RX	
	Used	%	Used	%
Slice Registers	3567	5	5272	7
Slice LUTs	5038	7	7382	10
bonded IOBs	57	8	19	2
Block RAMs	10	6	5	3

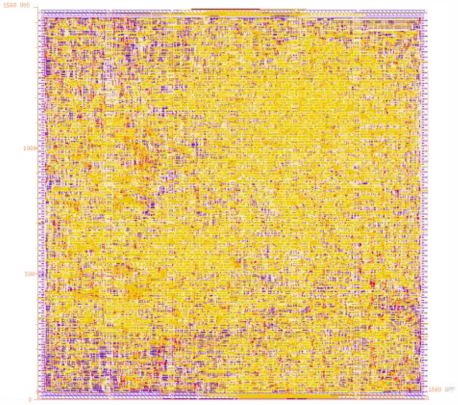

Figure 5: Layout implementation of TX design

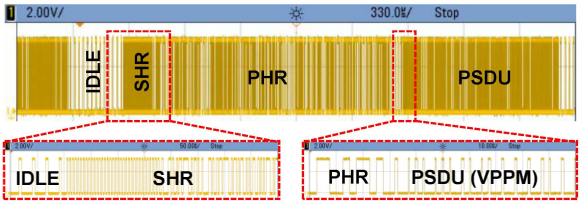

Figure 6: VLC modulated signal

The VLC modulated signal, comprising of relevant PPDU fields, is shown in Figure 6. This signal drives the front-end which is tested with a maximum forward current of 30 mA. Under the DC operating condition, each LED typically generates 9.6 lm luminous flux. The voltage drop across each LED is V_{LED} = 3.1 V, and V_{ds} of the NMOS is 110 mV. The total static power consumption of the analog front-end is 470 mW. With VLC enabled, the LEDs are switched on and off at 50% duty cycle and the power consumption is decreased to be 235 mW. The threshold voltage of the NMOS is 2.8 V and the gate capacitance is less than 60 pF with a max switching delay of only 10 ns, which indicates that the digital baseband signal is able to modulate the LEDs at a frequency higher than 1 MHz.

For the receiver side, the power consumption of the analog front-end is 50 mW.

Bit Error Rate

BER measurement is done using a built in pseudo-random binary sequence (PRBS). The 2^{12}-1 PRBS stream is used as the PSDU and sent along with the PHR. The receiver first synchronizes the locally generated stream with the incoming stream and then calculates the number of errors to measure the BER. Figure 7 shows the BER plot for two data rates of the IEEE 802.15.7 standard. The higher data rate, i.e. 124.4 kb/s, has worse BER, since the higher-speed VPPM is more vulnerable to noise. On the other hand, the 73.3 kb/s scheme has better BER at the expense of lower data rate. With a received illuminance of 18 lx, the BER for 73.3 kb/s and 124.4 kb/s is $< 10^{-6}$ and $> 10^{-2}$, respectively, as shown in Figure 7.

CONCLUSION

In this paper, we present a transceiver design for IEEE 802.15.7 PHY-I, including the block diagrams for both TX and RX, and their detailed description. Implemented on the Xilinx Virtex-5 FPGA, measurement results show that the transceiver system can achieve a BER of 10^{-6} when the data rate is 73.3 kb/s and the received illuminance is 18 lx.

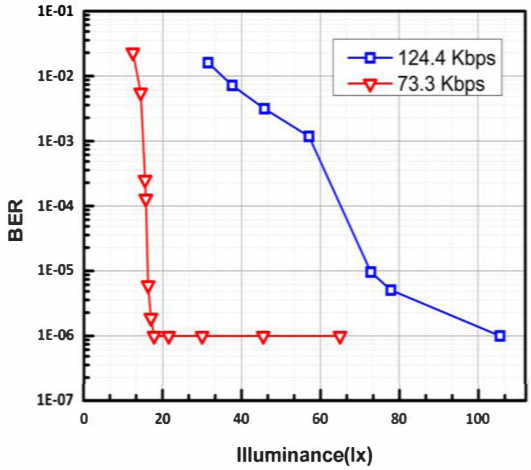

Figure 7: BER at various light intensities

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