Experiment No.: 6

Title: Design and study of PN sequence generator.

Roll No.: _____ Batch: _____
Date of Performance: _____
Date of Assessment: _____

Particulars	Marks
Attendance (05)	
Journal (05)	
Performance (05)	
Understanding (05)	
Total (20)	
Signature of Staff Member	

Experiment No: 6

Title: Design and study of PN (Pseudo-Noise) sequence generator.

Aim: To design and study a 6-bit PN sequence generator and observe the pseudo-random bit sequence it produces.

Objectives:

1. To understand PN (maximal length) sequences and their generation using shift-registers and XOR feedback.
2. To implement a 6-bit PN generator on the trainer kit.
3. To verify the sequence length and observe the output pattern (repeat after 63 cycles).

Theory:

A PN (pseudo-noise) or PN-sequence is a deterministic binary sequence that appears random. A maximal-length PN sequence from an n-stage linear feedback shift register (LFSR) has period 2^n-1.

For a 6-bit PN sequence the period is 2^6-1=63 clock cycles.

The PN generator is built from D flip-flops (to store the shift register), XOR (EX-OR) feedback taps, and a clock generator. In your kit: the clock is produced by an IC555, D flip-flops use IC 74175 (4 D-flip flops) plus additional flip-flops as required, and XOR gates use IC 7486. An inverter (7404) is used where needed.

The shift register shifts on each clock; selected tapped outputs are XORed and fed back to the input bit to create maximal length behavior.

Resetting the register to all zeros prevents sequence generation ensure the register is initialized to a non-zero state to start the PN sequence. i.e. Q0 & Q5 are Ex-Ored & feedback to I/P after inverting. Inverter is used because after resetting all O/Ps are zero & to start PN sequence I/P should be one.

Procedure:

1. Switch ON the power supply of the trainer kit and verify power LED.
2. Connect the **CLK O/P** of the clock generator to the **CLK I/P** of the flip-flop chain (IC 74175 or the kit clock input).

3. Make the feedback connection(s) as shown on the kit diagram **(connect point 'B' to 'A' if required by the kit).** These implement the XOR feedback taps required for 6-bit maximal sequence.
4. Apply reset **(Press reset (RST) S/W on panel)** to initialize the flip-flops; then release reset so the PN sequence can start.
5. Observe PN sequence O/P on C.R.O. together with clock. Continue until sequence repeats; count cycles to verify period = 63 clock cycles.

CLK	Q5	Q4	Q3	Q2	Q1	Q0	O/P
0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	0
2	0	0	0	0	1	0	1
3	0	0	0	1	0	1	0
4	0	0	1	0	1	0	1
5	0	1	0	1	0	1	0
6	1	0	1	0	1	0	0
7	0	1	0	1	0	0	1
8	1	0	1	0	0	1	1
9	0	1	0	0	1	1	0
10	1	0	0	1	1	0	0
11	0	0	1	1	0	0	1
12	0	1	1	0	0	1	0
13	1	1	0	0	1	0	0
14	1	0	0	1	0	0	0
15	0	0	1	0	0	0	1
16	0	1	0	0	0	1	0
17	1	0	0	0	1	0	0
18	0	0	0	1	0	0	1
19	0	0	1	0	0	1	0
20	0	1	0	0	1	0	1
21	1	0	0	1	0	1	1
22	0	0	1	0	1	1	0
23	0	1	0	1	1	0	1
24	1	0	1	1	0	1	1
25	0	1	1	0	1	1	0
26	1	1	0	1	1	0	0
27	1	0	1	1	0	0	0
28	0	1	1	0	0	0	1
29	1	1	0	0	0	1	1
30	1	0	0	0	1	1	1
31	0	0	0	1	1	1	0

CLK	Q5	Q4	Q3	Q2	Q1	Q0	O/P
32	0	0	1	1	1	0	1
33	0	1	1	1	0	1	0
34	1	1	1	0	1	0	0
35	1	1	0	1	0	0	0
36	1	0	1	0	0	0	0
37	0	1	0	0	0	0	1
38	1	0	0	0	0	1	1
39	0	0	0	0	1	1	0
40	0	0	0	1	1	0	1
41	0	0	1	1	0	1	0
42	0	1	1	0	1	0	1
43	1	1	0	1	0	1	1
44	1	0	1	0	1	1	1
45	0	1	0	1	1	1	0
46	1	0	1	1	1	0	0
47	0	1	1	1	0	0	1
48	1	1	1	0	0	1	1
49	1	1	0	0	1	1	1
50	1	0	0	1	1	1	1
51	0	0	1	1	1	1	0
52	0	1	1	1	1	0	1
53	1	1	1	1	0	1	1
54	1	1	1	0	1	1	1
55	1	1	0	1	1	1	1
56	1	0	1	1	1	1	1
57	0	1	1	1	1	1	0
58	1	1	1	1	1	0	0
59	1	1	1	1	0	0	0
60	1	1	1	0	0	0	0
61	1	1	0	0	0	0	0
62	1	0	0	0	0	0	0
63	0	0	0	0	0	0	1
64							

Sequence repeat after

2^{n-1} i.e 63 cycle

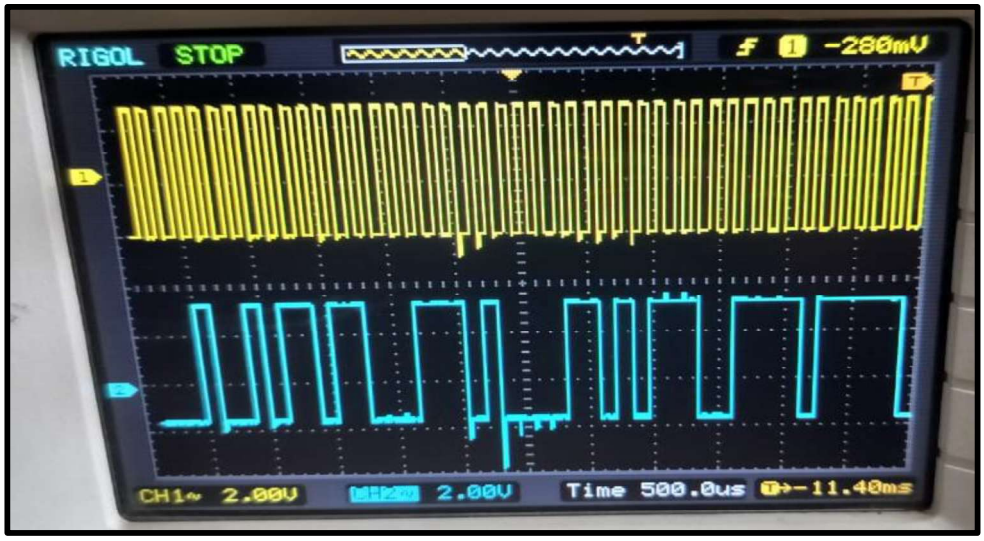
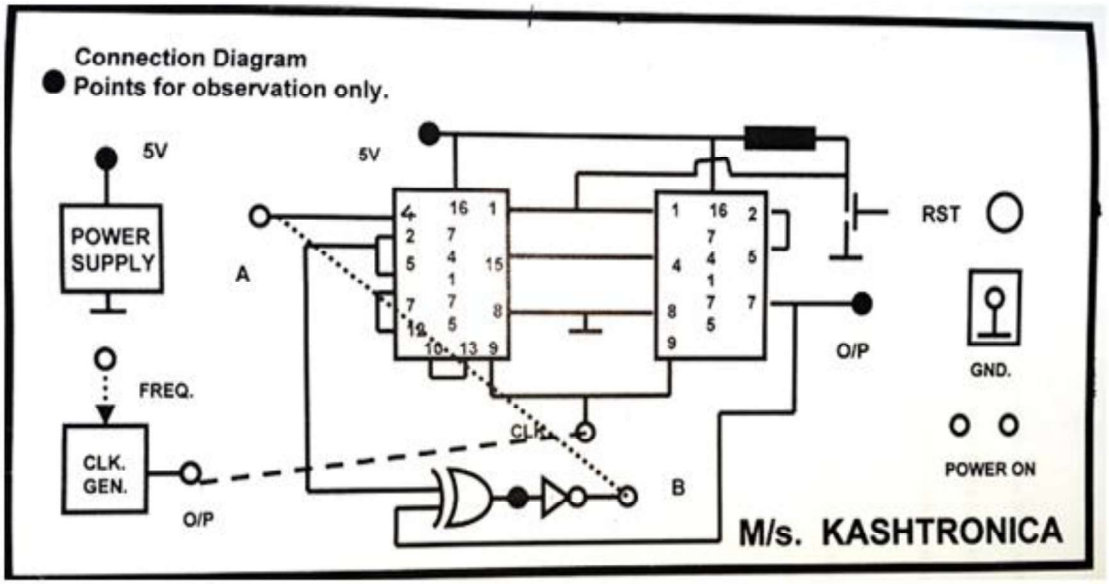
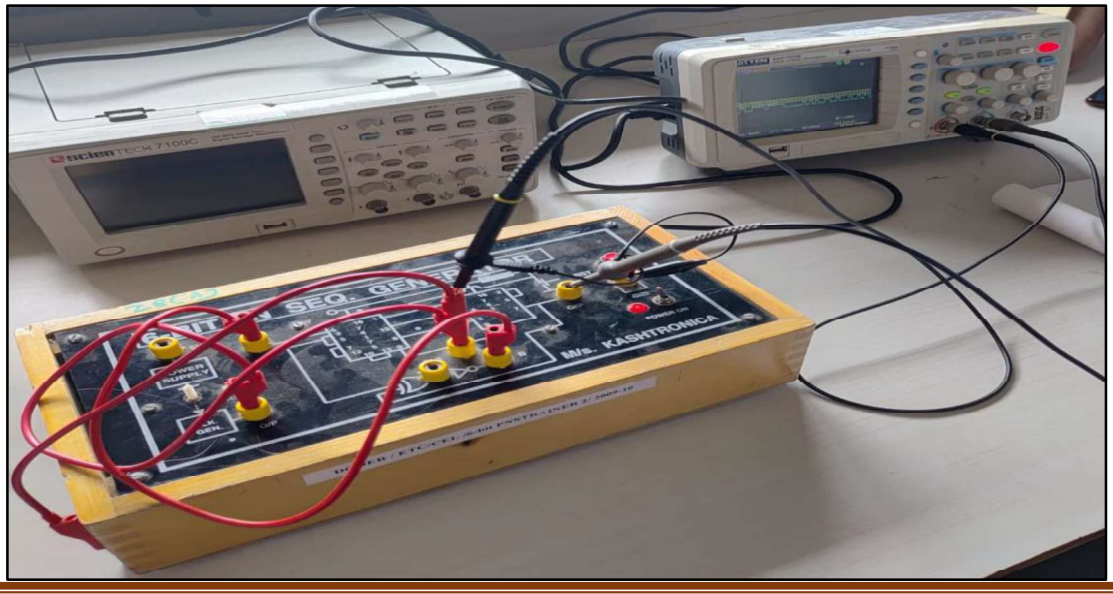

RIGOL STOP
-280mV
CH1~ 2.00V
2.00V
Time 500.0us
-11.40ms

Diagram:


Connection Diagram
Points for observation only.
5V
POWER SUPPLY
FREQ.
CLK. GEN.
O/P
A
5V
B
RST
O/P
GND.
POWER ON
M/s. KASHTRONICA


M/s. KASHTRONICA

Conclusion: