COMPUTER ARCHITECTURE LAB 4

CS 311

Author

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Observations

Test Case	Static Inst.	Dynamic Inst.	No. of Cycles	Stalls	Wrong B.T.*
evenorodd.asm	10	9	13	6	0
fibonacci.asm	22	117	121	12	16
palindrome.asm	17	91	95	18	7
descending.asm	22	542	546	89	88
prime.asm	17	49	53	8	5

Table 1: Number of Instructions executed and stalls for various programs.

Test Case	IPC	Frequency	
evenorodd.asm	0.6923007	1.0 GHz	
fibonacci.asm	0.6694215	1.0 GHz	
palindrome.asm	0.5473648	1.0 GHz	
descending.asm	0.51282054	1.0 GHz	
prime.asm	0.6037736	1.0 GHz	

Table 2: IPC and Frequency

Static Instructions The number of instructions persent inside the program.

Dynamic Instructions The number of instructions executed by the program to produce the desired result.

No. of Cycle The number of clock cycles taken to complete the execution.

Stalls The number of stalls that were made during the program execution.

Wrong Branch Taken The number of times the program fetched wrong program code.

IPC Ratio of Instruction executed per cycle i.e. (Correct Instructions / Cycles).