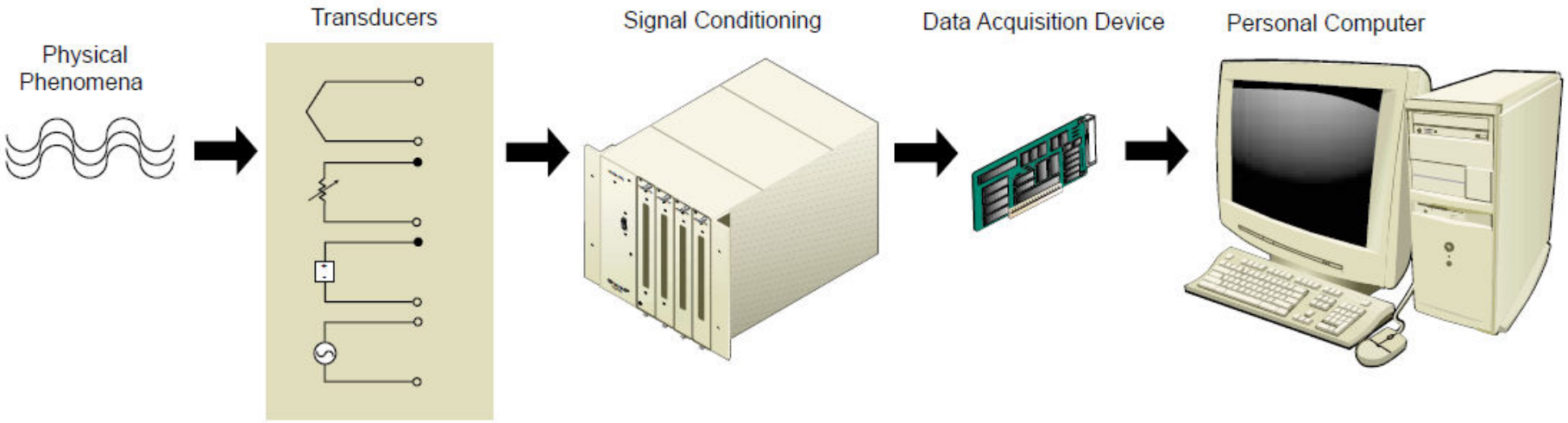
Mechatronics
AEZG511

BITS Pilani
Pilani Campus

Lecture

Signal conditioning

Data Acquisition system



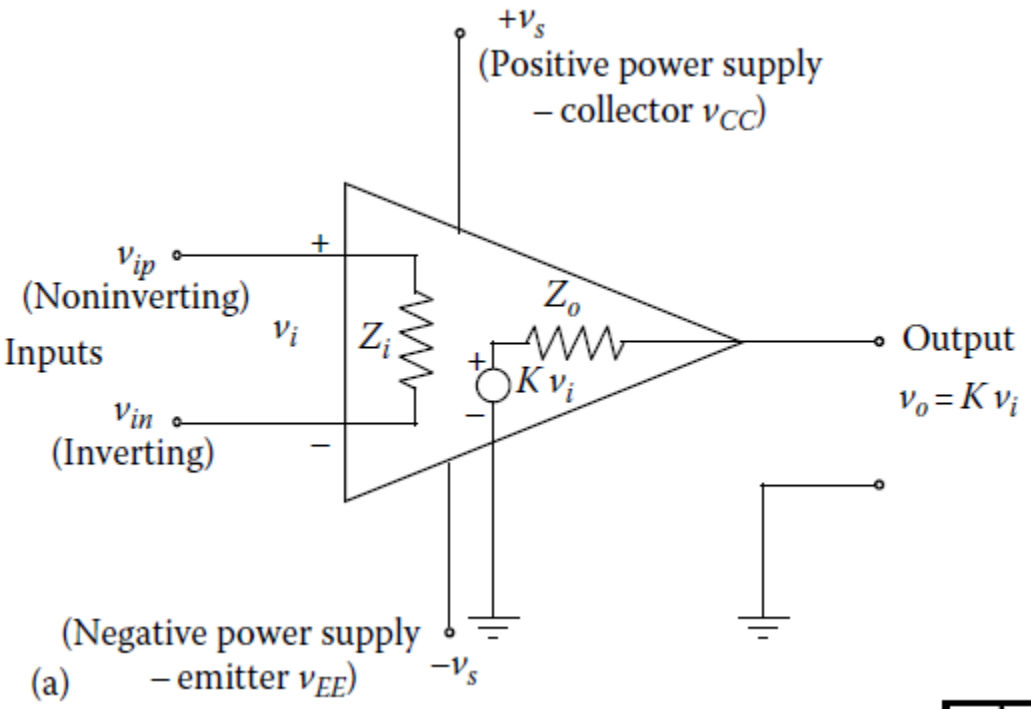
Operational Amplifiers (Op Amps)

Why Study Amplification?

[1]

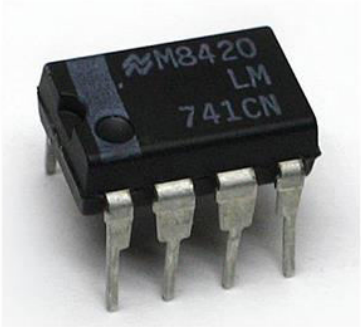
- Sensor signals are in millivolts or milliamps
- The analog front end for a sensor is more complex than the digital control circuitry for the sensor-actuator loop
- The main issues for sensor interfaces are accuracy, noise, offset, drift, and impedance
- All of these issues come back to amplification

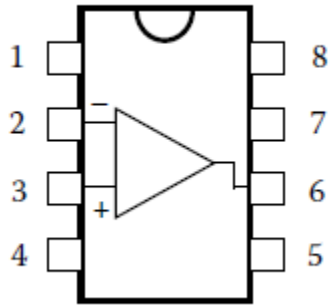
Ideal Op Amp



V_i- The difference in voltage between Non Inv and Inv inputs

K- Output gain (10^5 to 10^7)

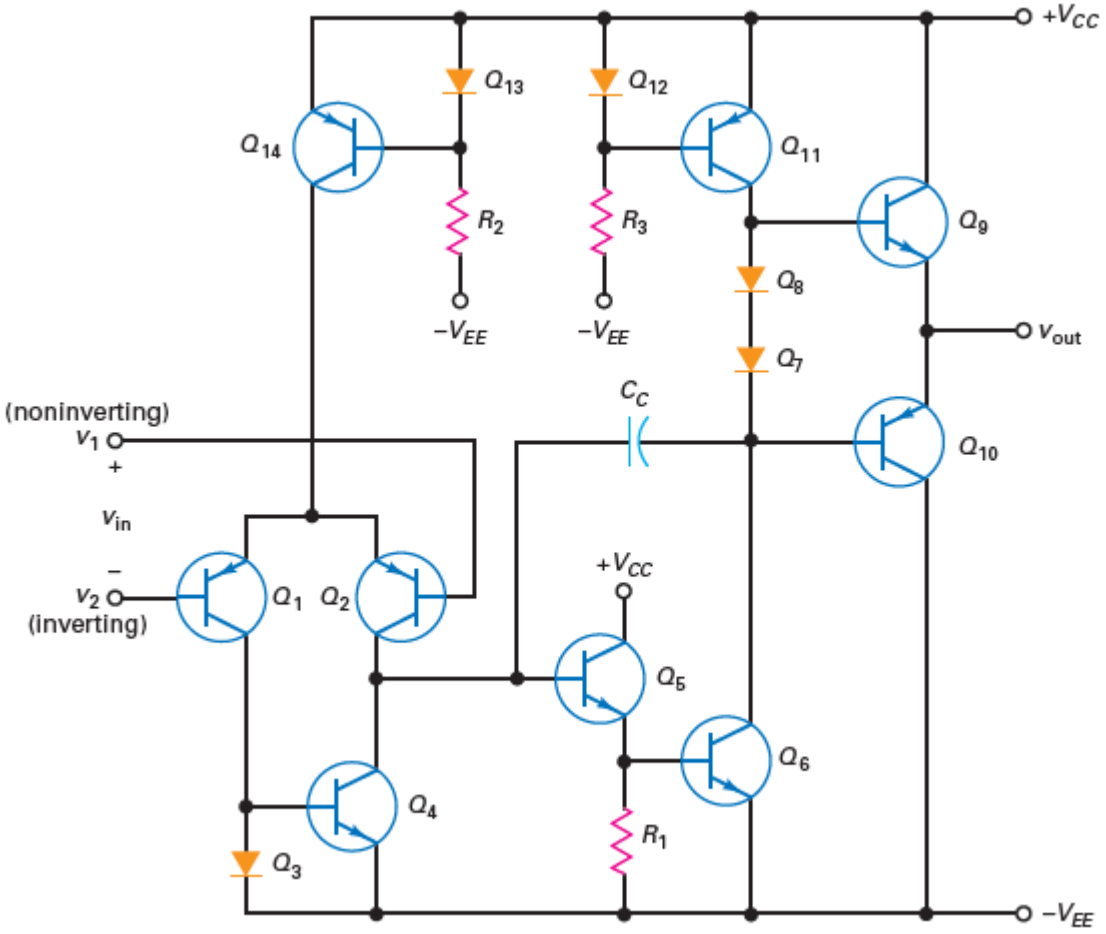




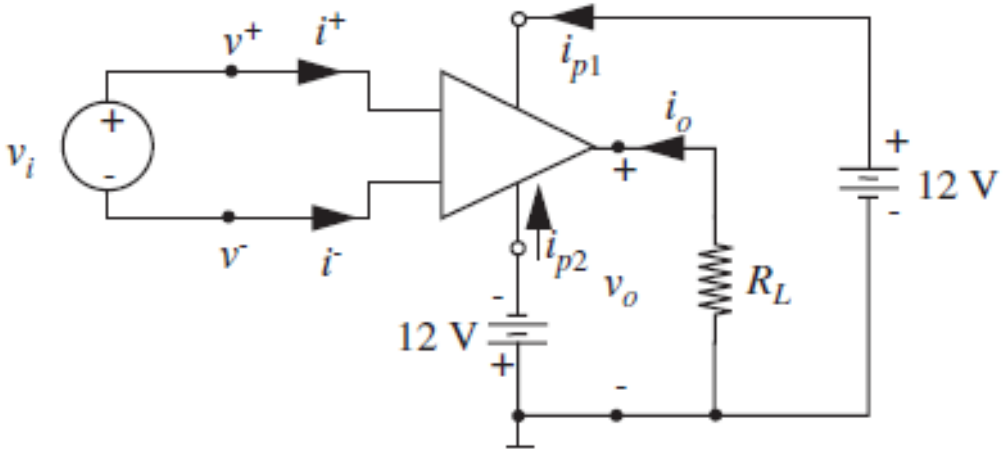
Pin designations:

1 Offset null
2 Inverting input
3 Noninverting input
4 Negative power supply v_{EE}
5 Offset null
6 Output
7 Positive power supply v_{CC}
8 NC (not connected)

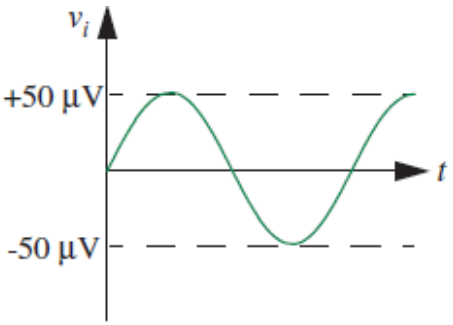
Internal Circuity of Op Amp 741

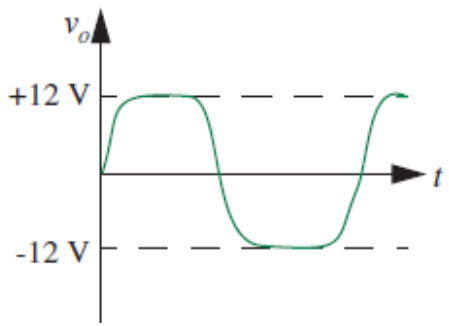


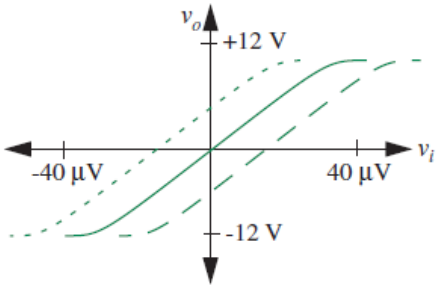
Typical Characteristics of Op amp



(a)

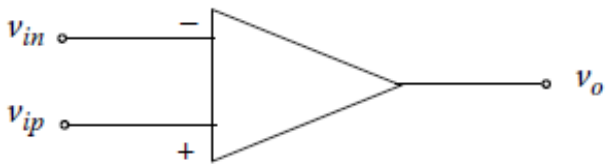






Ideal Op Amp

PARAMETER NAME	PARAMETERS SYMBOL	VALUE
Input current	I_{IN}	0
Input offset voltage	V_{OS}	0
Input impedance	Z_{IN}	∞
Output impedance	Z_{OUT}	0
Gain	K	∞



$$v_o = Kv_i$$

Simplified diagram showing only voltage inputs (without external power supply)

Ideal Op Amp

$$v_o = Kv_i$$

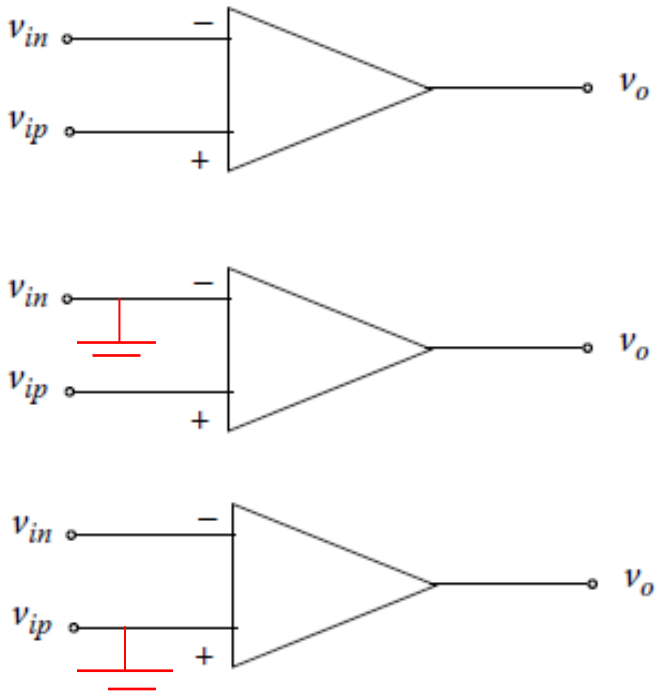
$$v_i = v_{ip} - v_{in}$$

If V_{in} is ground ; $v_o = Kv_{ip}$

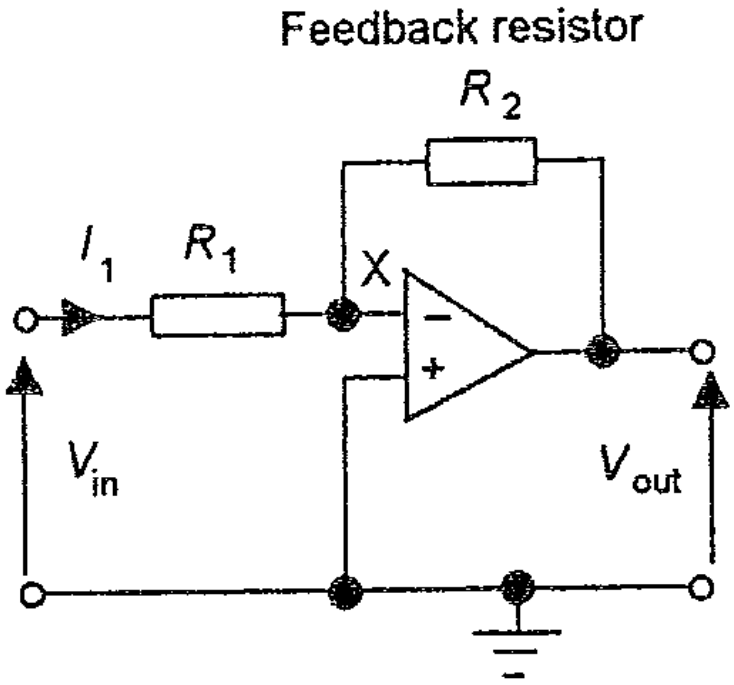
If V_{ip} is ground; $v_o = -Kv_{in}$

This is why V_{in} Is called Non- Inverting and

V_{ip} is called Inverting input



Virtual Ground of Op Amp



This assumption of Virtual Ground saves us from lots of algebraic manipulations!!!

+ terminal is connected to ground

Gain (K) of amplifier is 100,000

Output voltage is say 10 V

Means input voltage is 0.0001.

This can be considered **as Zero!!**

Point X is at "0" Voltage!!

Called Virtual Ground

Ideal Op Amp Assumptions(Summarized)

Input Impedance is Very High (10 Mega Ohms)

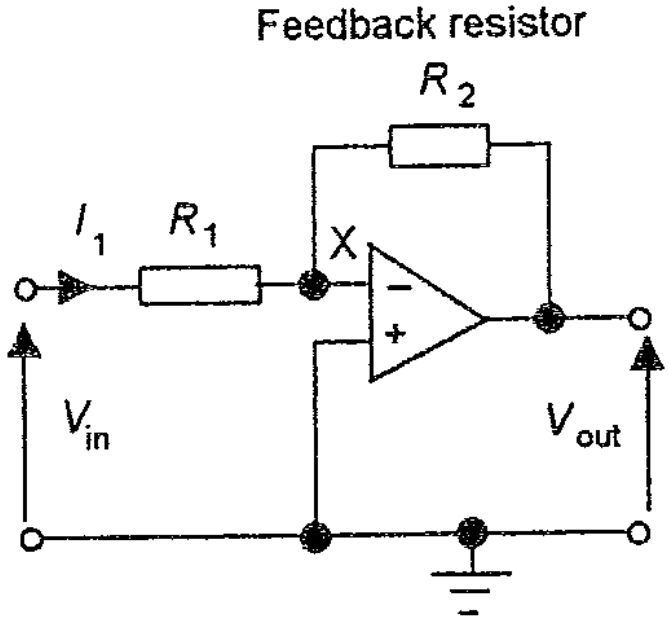
Output Impedance is Very low (10 Ohms)

No current passes through Op amp

Virtual ground assumption can be made safely

Gain is very high (100,000 – 1,000,000)

Inverting amplifier



Potential difference across R1 is

Vin – Vx = I_1 x R_1

Potential difference across R2 is

Vx – Vout = I_2 x R_2

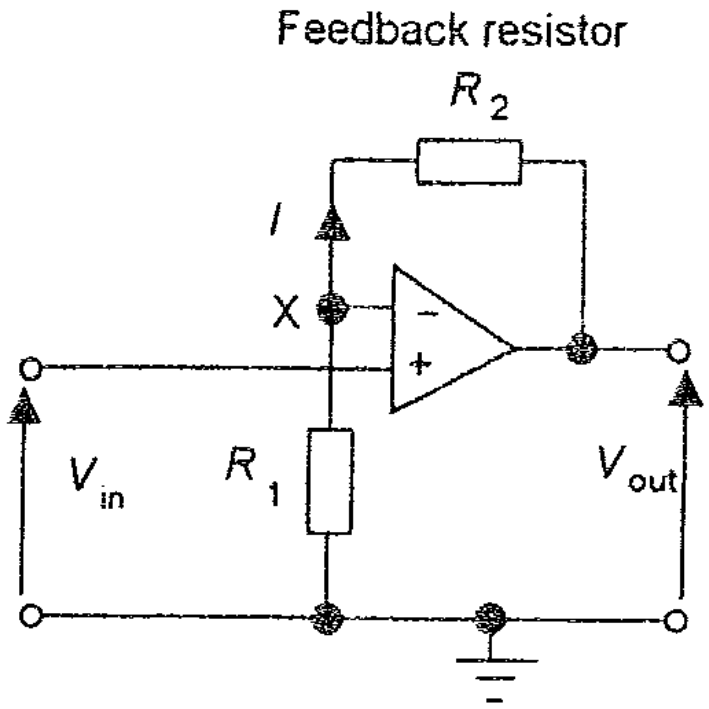
No current can flow through X into Op Amp (Refer our assumptions)

Means $I_1 = I_2$

Again Vx = 0 (based on virtual ground)

$$\text{Voltage gain of circuit} = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$$

Non – Inverting amplifier



This is voltage divider circuit

R2 and R1 are in series with X in between.

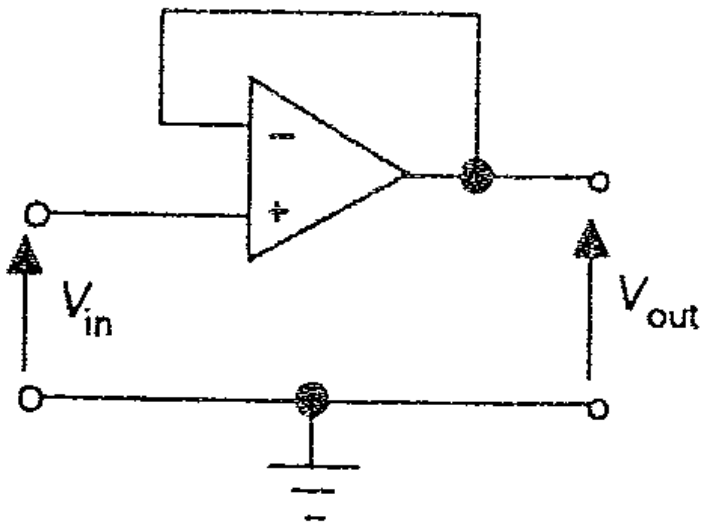
$$V_X = \frac{R_1}{R_1 + R_2} V_{out}$$

Again Vx = Vin (No current flows through Op Amp)

$$\text{Voltage gain of circuit} = \frac{V_{out}}{V_{in}} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1}$$

Voltage Follower

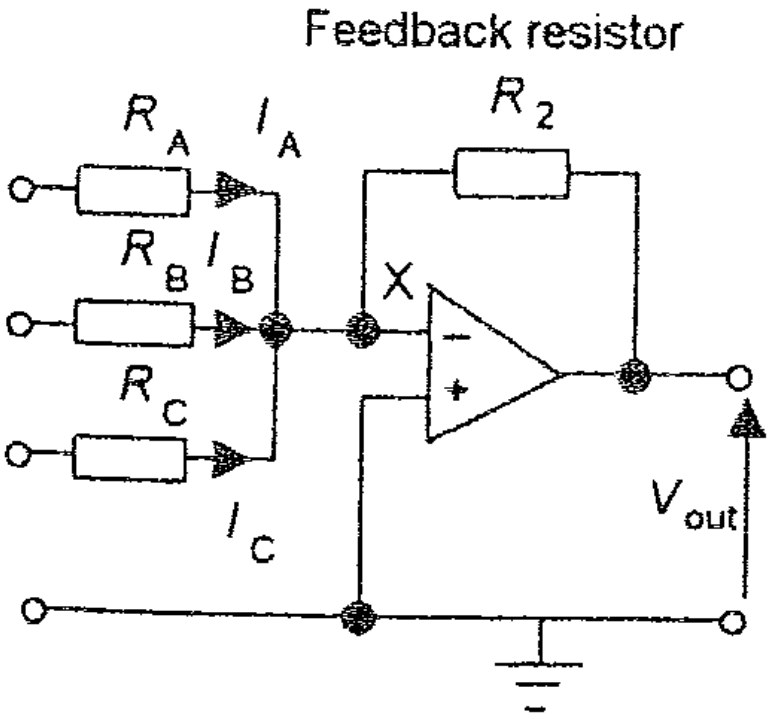
Non Inverting amplifier without resistors is a follower



a) Used in voltage divider circuit

b) As isolators

Summing Amplifier



$$I = I_A + I_B + I_C$$

$$-\frac{V_{out}}{R_2} = \frac{V_A}{R_A} + \frac{V_B}{R_B} + \frac{V_C}{R_C}$$

$$V_{out} = -\left(\frac{R_2}{R_A}V_A + \frac{R_2}{R_B}V_B + \frac{R_2}{R_C}V_C\right)$$

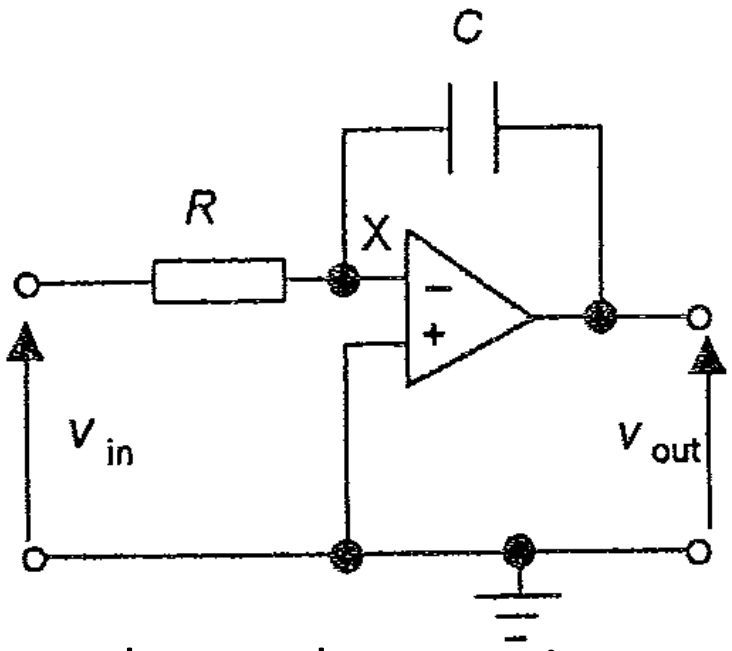
If $R_A = R_B = R_C = R_1$ then

$$V_{out} = -\frac{R_2}{R_1}(V_A + V_B + V_C)$$

How to generate average of these signals?????

Integrating Amplifier

Replace resistor R2 in inverting amplifier with a capacitor



$$q = Cv,$$

$$i = dq/dt = C\, dv/dt.$$

$$\frac{v_{in}}{R} = -C\frac{dv_{out}}{dt}$$

Rearranging this gives

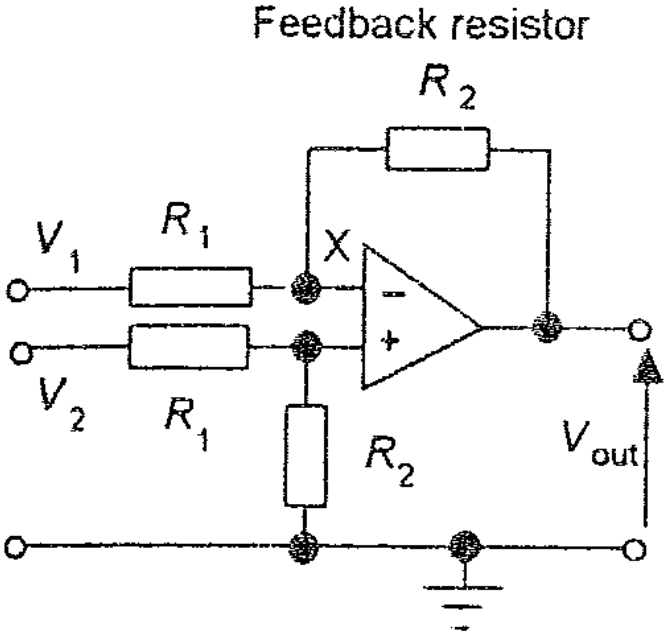
$$dv_{out} = -\left(\frac{1}{RC}\right) v_{in}\, dt$$

Integrating both sides gives

$$v_{out}(t_2) - v_{out}(t_1) = -\frac{1}{RC}\int_{t_1}^{t_2} v_{in}\, dt$$

Interchange the capacitor and Resistor positions you get Differentiating Amplifier – Verify!!!!

Differencing amplifier

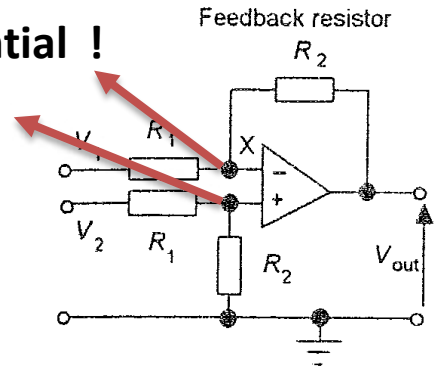


$$\frac{V_X}{V_2} = \frac{R_2}{R_1 + R_2}$$

$$\frac{V_1 - V_X}{R_1} = \frac{V_X - V_{out}}{R_2}$$

$$\frac{V_{out}}{R_2} = V_X\left(\frac{1}{R_2} + \frac{1}{R_1}\right) - \frac{V_1}{R_i}$$

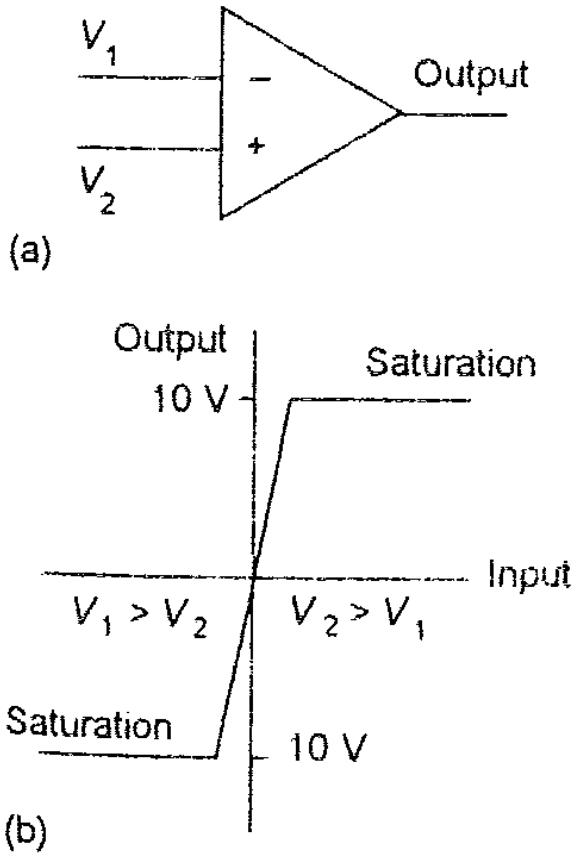
At same Potential !

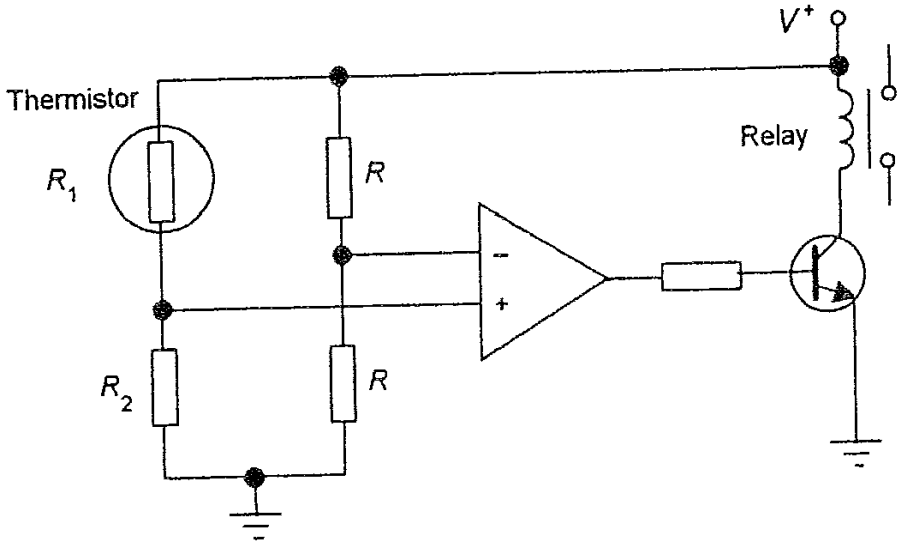


Hence substituting for V_X using the earlier equation,

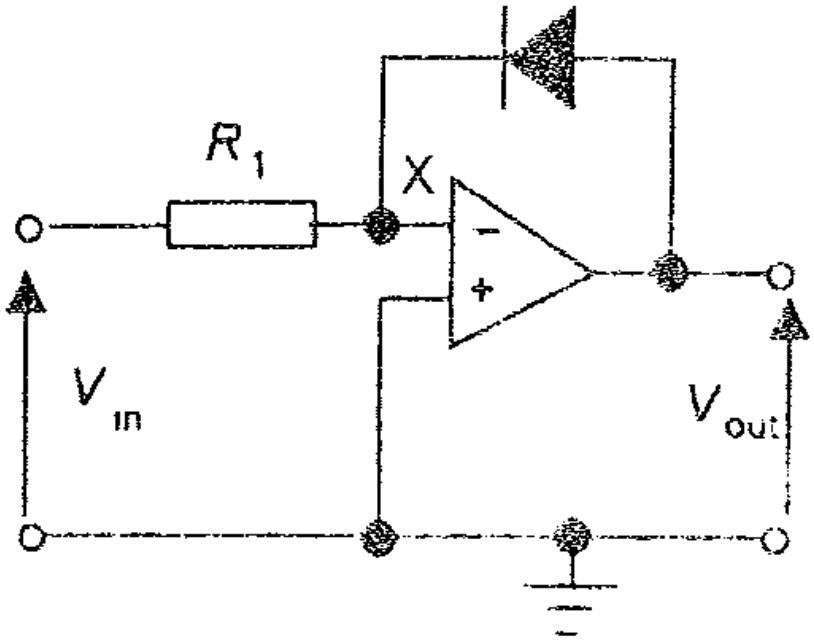
$$V_{out} = \frac{R_2}{R_1}(V_2 - V_1)$$

Voltage Comparator



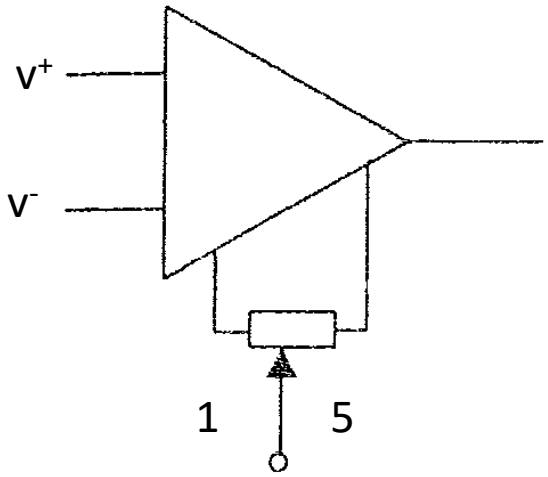


Logarithmic amplifier



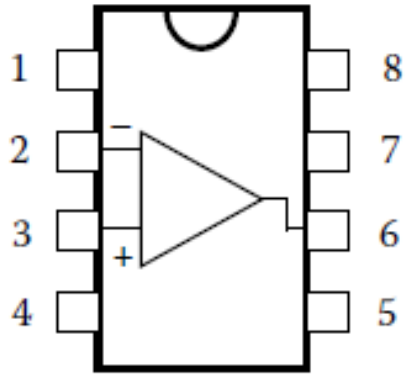
Linearizes exponential signals

Amplifier errors



Offset voltage: Presence of output even if v^+ and v^- are shorted

Sliding contact of the potentiometer to a negative supply, so that Vout is zero, when V+ and V- are equal



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7 Positive power supply v_{CC}
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Slew rate

Example Slew Rate Calculation

Amplifier requirements: 25 kHz & peak voltage 5V

Slew rate = $2 \pi f V$

$= 2 \times 3 \times 25\,000 \times 5$

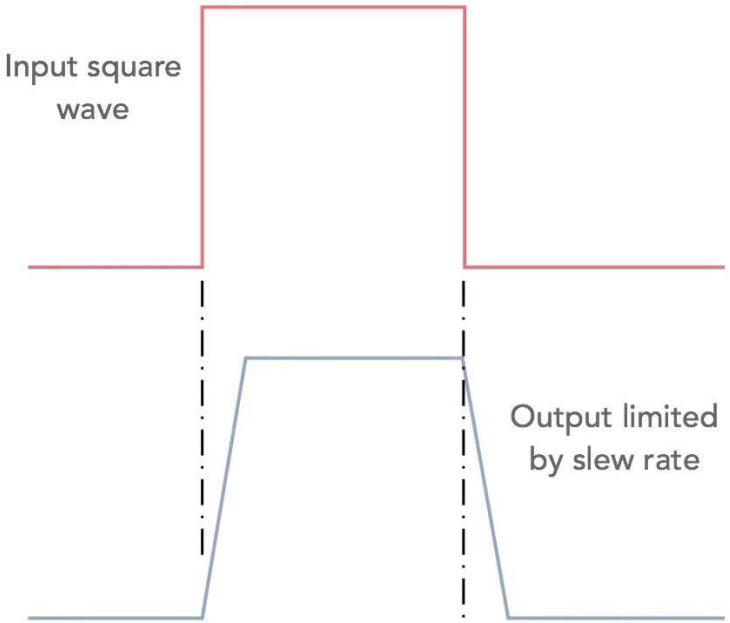
$= 750\,000$ V / s

$= 0.75$ V / µs

	$R_L \geq 2$ kΩ				±10	±13		±10	±13		
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $R_S \leq 10$ kΩ, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50Ω$, $V_{CM} = \pm 12V$	80	95								
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$ to $V_S = \pm 5V$, $R_S \leq 50Ω$	86	96								dB
	$R_S \leq 10$ kΩ				77	96		77	96		
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
Bandwidth (2)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	

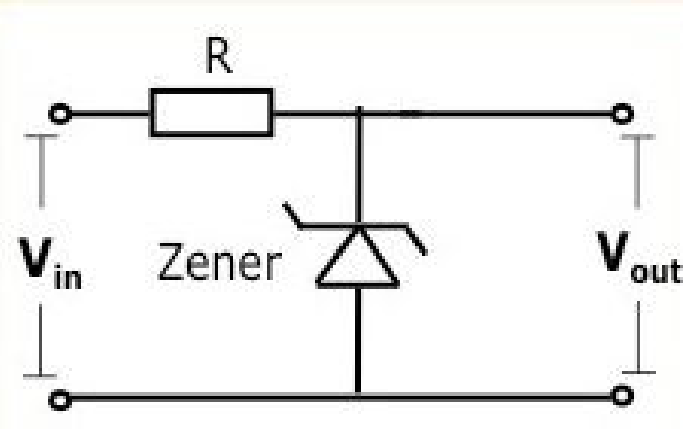
Slew rate often measured in Volts / microsecond

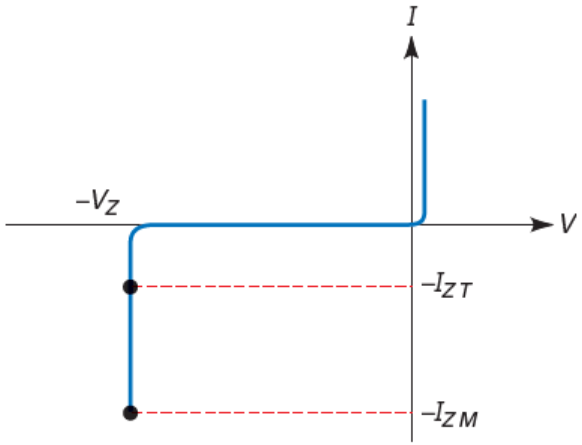
(2) Calculated value from: BW (MHz) = 0.35/Rise Time (µs).

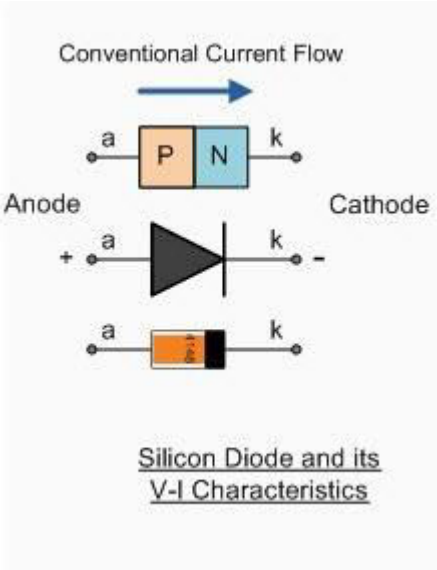


Protectors

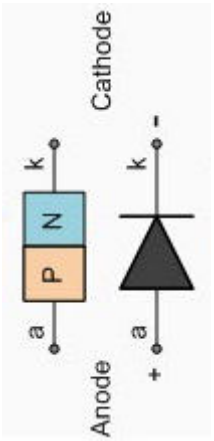
Zener Diode (Voltage Regulator)



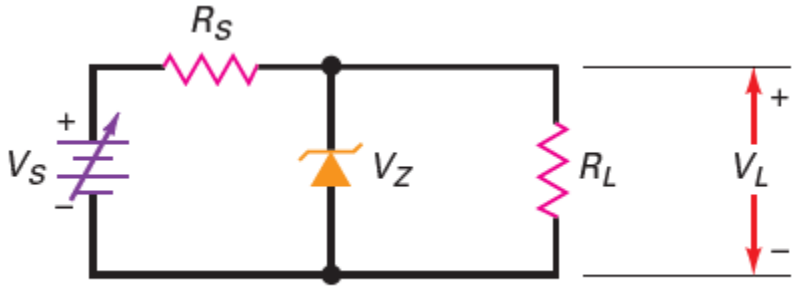


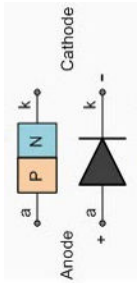


Silicon Diode and its V-I Characteristics



Zener circuit design calculation





Zener voltage V_Z should be 12 Volts

Load current = V_L/R_L= 12/24 = 500 mA

R_S= (V_S – V_Z)/ I_L = (20- 12)/500 mA = 16 Ohms

Load current through resistor

I_S (max) = (24-12) / 16 = 750 mA

I_S (min) = (20-12) / 16 = 500 mA

$I_S = I_Z + I_L$

750 = I_Z + 500 mA

I_z= 250 mA

Power of Zener = 12V *250 mA = 3 Watts

Given,

Vs = 20 Volt to 24Volt

V_L= 12 Volt

R_L = 24 Ohms

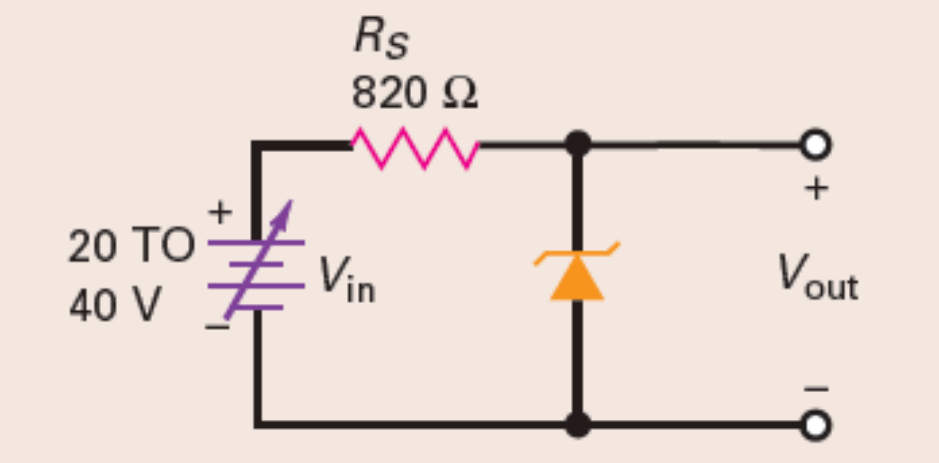
Select **Zener**

V_Z = ? I_Z = ? Power =??

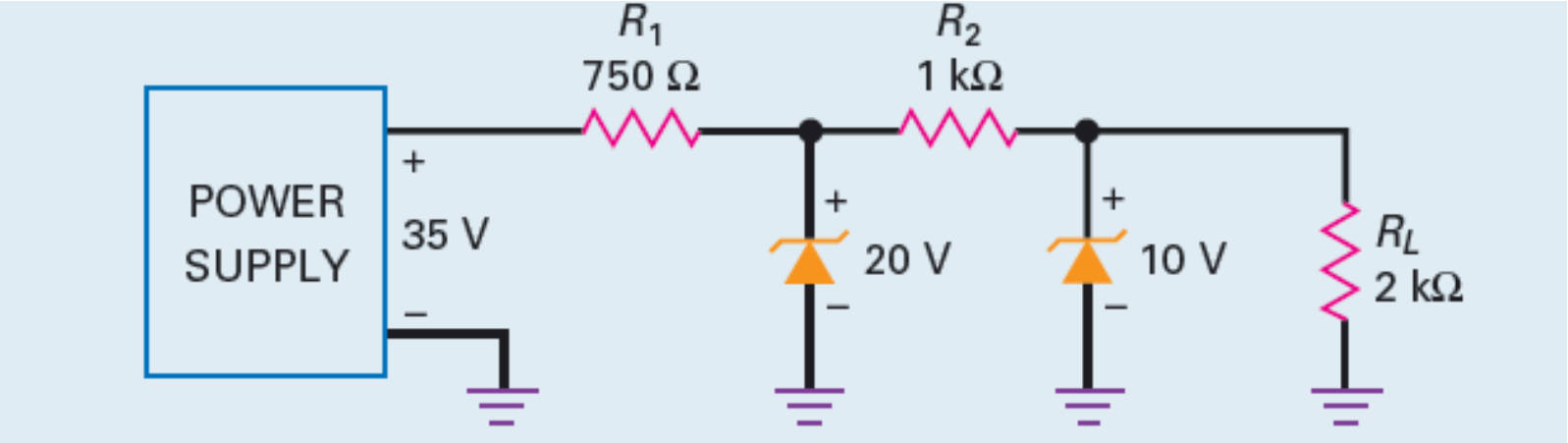
Suppose by chance voltage at source drops to 19 Volts, what will happen?

Zener Calculation (Home work)

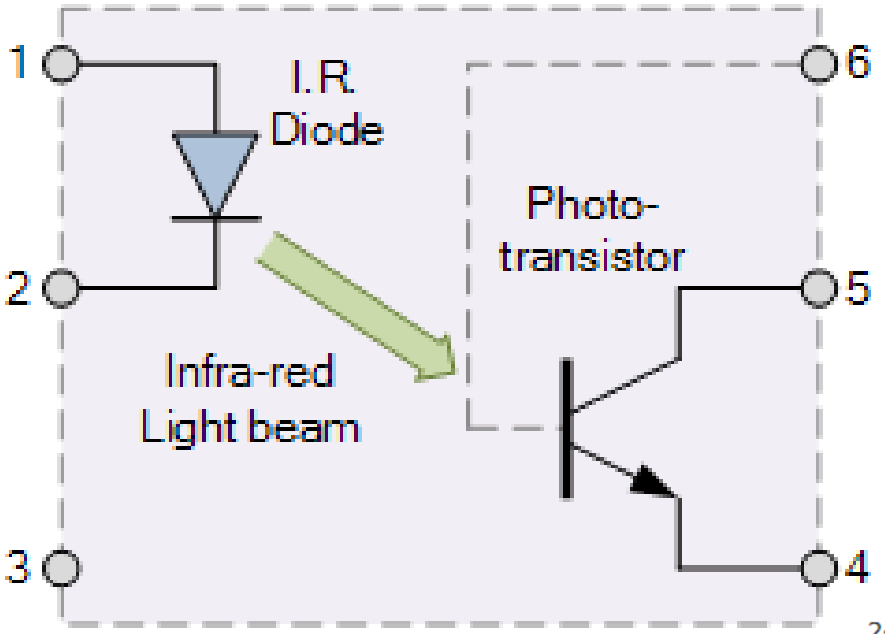
If the Zener diode below is of 10 V breakdown then, what is Vout and Max Zener, min Zener currents



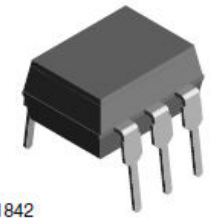
Zener Circuit

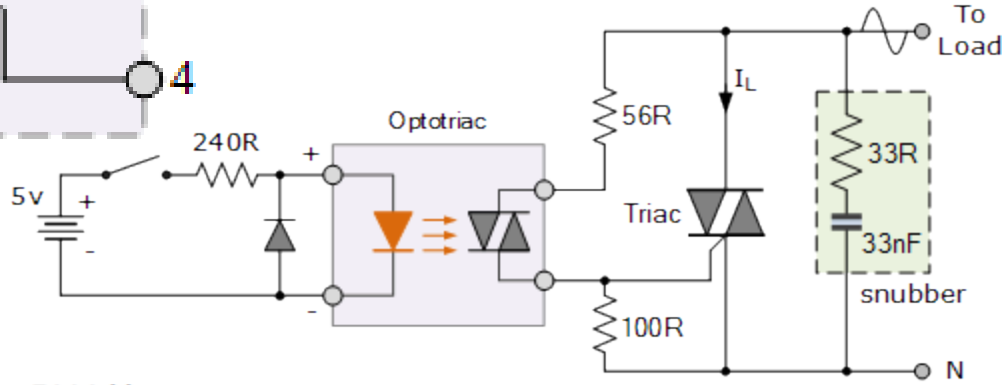


Opto Isolator



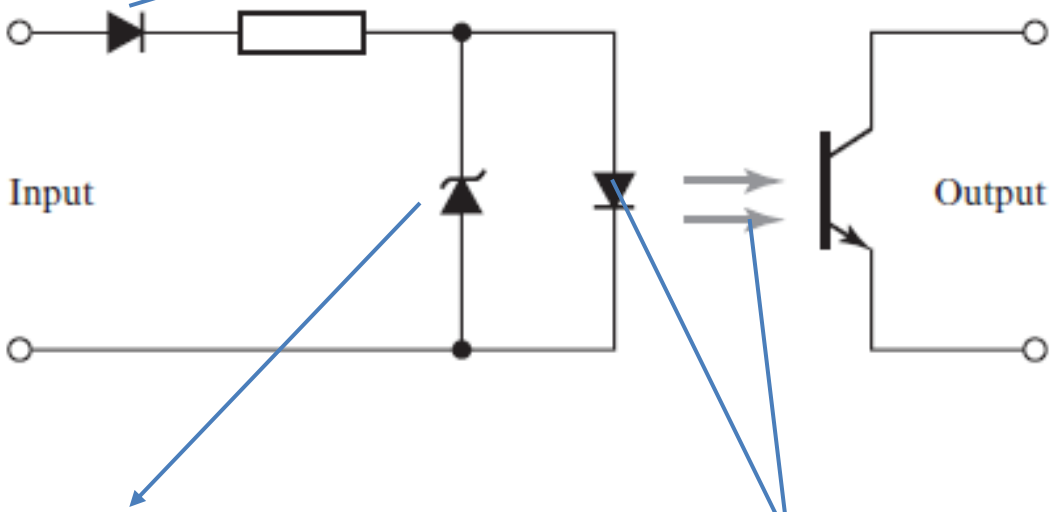
Current from the source signal passes through the input LED which emits an infra-red light whose intensity is proportional to the electrical signal.



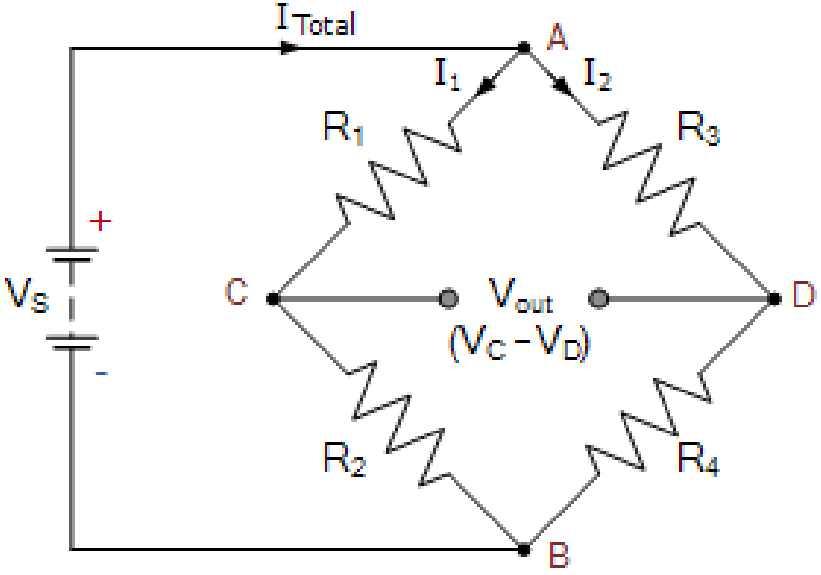


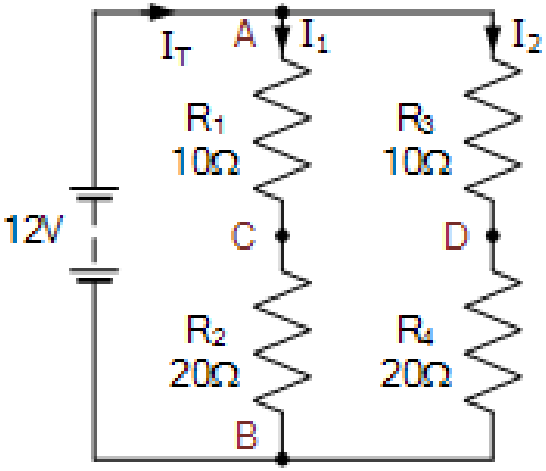
- Isolation test voltage 5000 V_{RMS}

Protection Circuit



Wheatstone bridge

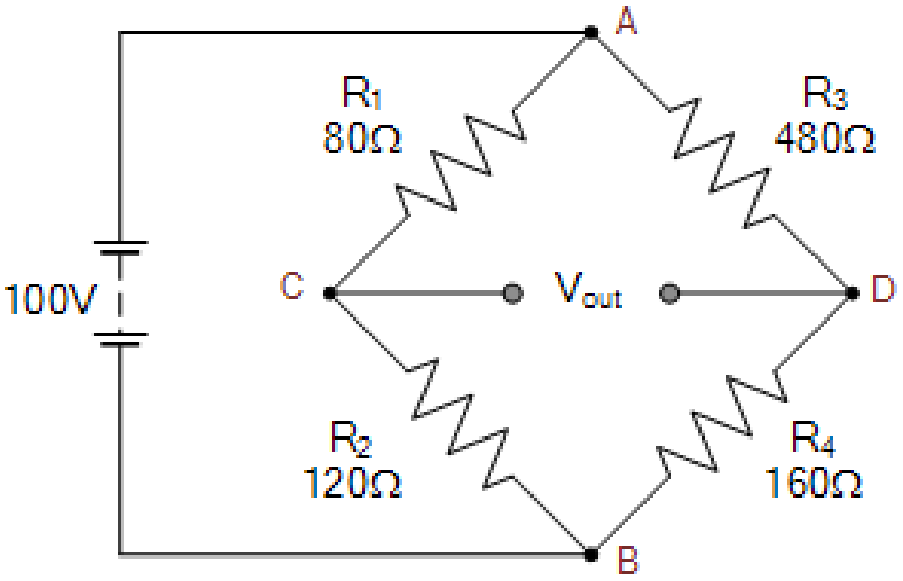




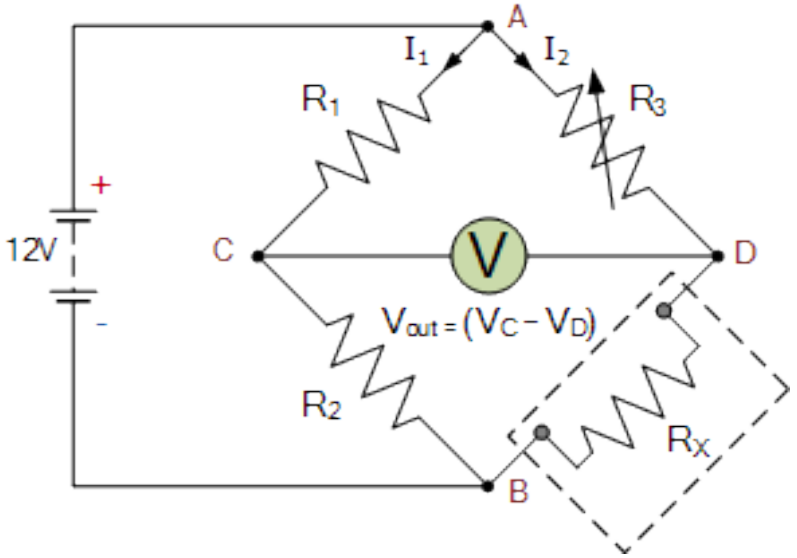
The above circuit is balanced as $V_C = V_D$

As $$\frac{R_1}{R_2} = \frac{R_3}{R_4}$$

Wheatstone bridge

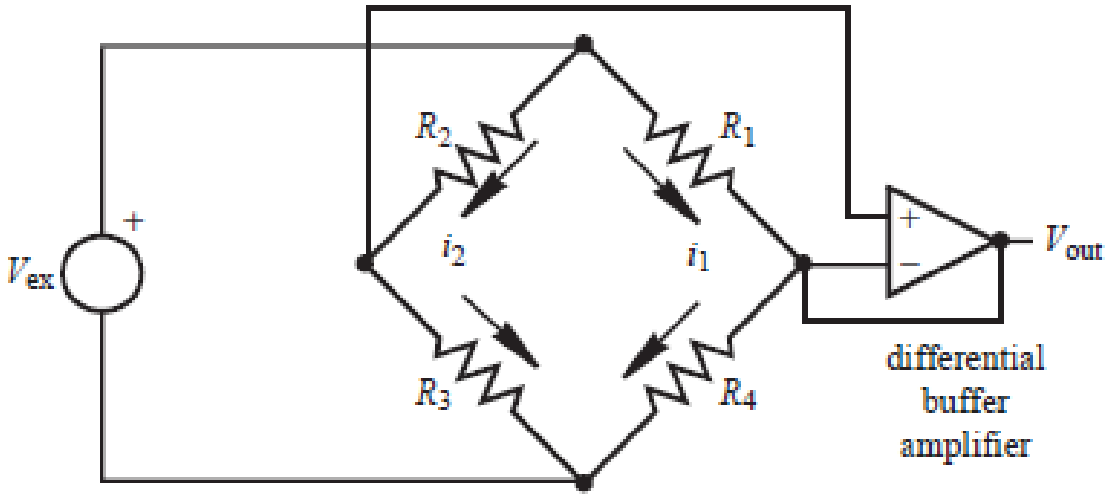


Unbalanced circuit
Vc? Vd ?



Connecting a RTD or strain gauge

Wheatstone bridge



Pass filters configurations

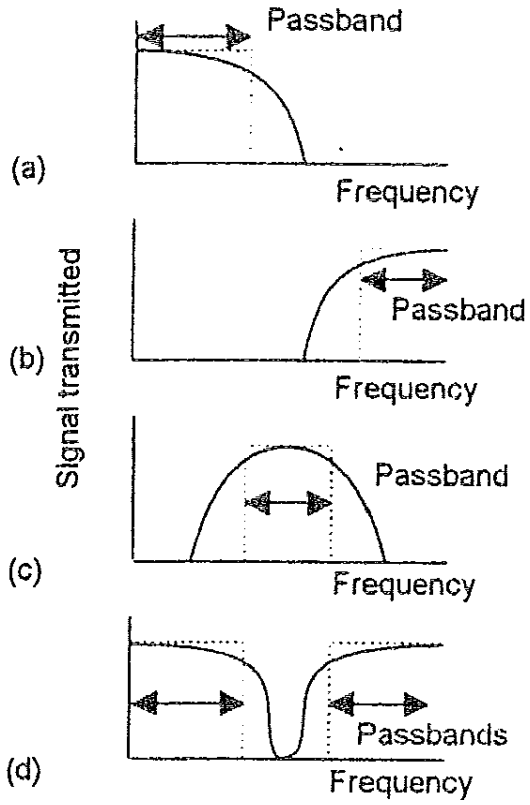
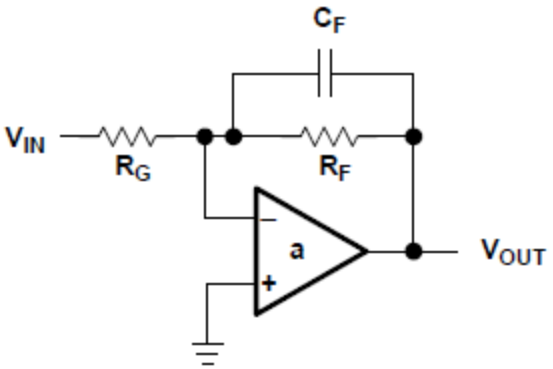


Fig. 3.19 Characteristics of ideal filters: (a) low pass, (b) high pass, (c) band pass, (d) band stop

Low pass filters

$$X_C = 1/2\pi fC.$$

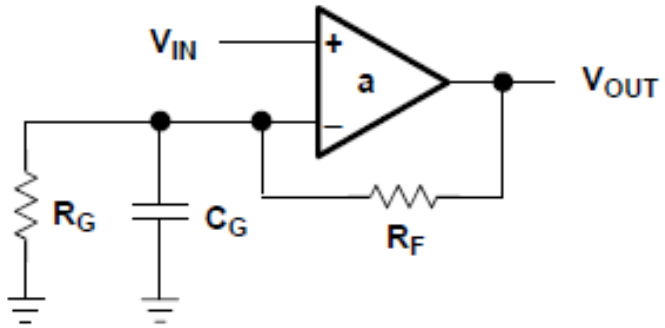


$$\frac{V_{OUT}}{V_{IN}} = -\frac{X_C \parallel R_F}{R_G}$$

At very low frequencies X_C ➡ infinity so R_F dominates the parallel combination in Equation and the capacitor has no effect. The gain at low frequencies is $-R_F/R_G$.

At very high frequencies X_C ➡ 0, so the feedback resistor is shorted out, thus reducing the circuit gain to zero (*The current flows through least resistance path, thereby offering making R_F redundant*)

High Pass filters

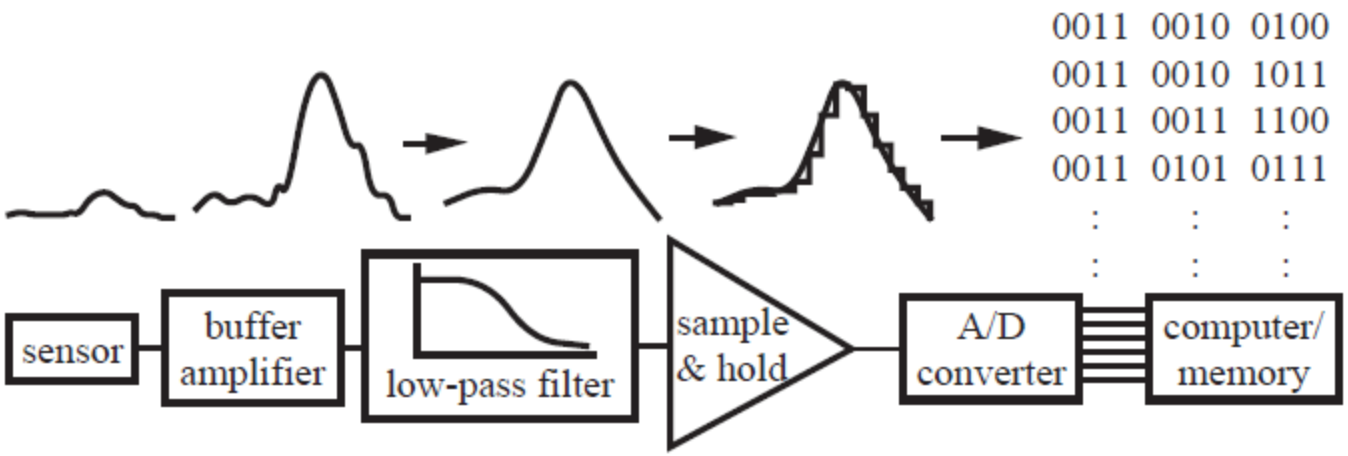


$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{X_C \parallel R_G}$$

At very low frequencies $X_C \Rightarrow \infty$, so R_G dominates the parallel combination and the capacitor has no effect. The gain at low frequencies is $1+R_F/R_G$. At very high frequencies $X_C \Rightarrow 0$, so the gain setting resistor is shorted out thus increasing the circuit gain to maximum.

Analog to Digital Digital to Analog Converters

Analog to Digital Schematic



Nyquist Theorem

When the signal is reconstructed from the samples, it is only when the sampling rate is at least twice that of the highest frequency in the analogue signal that the sample gives the original form of signal.

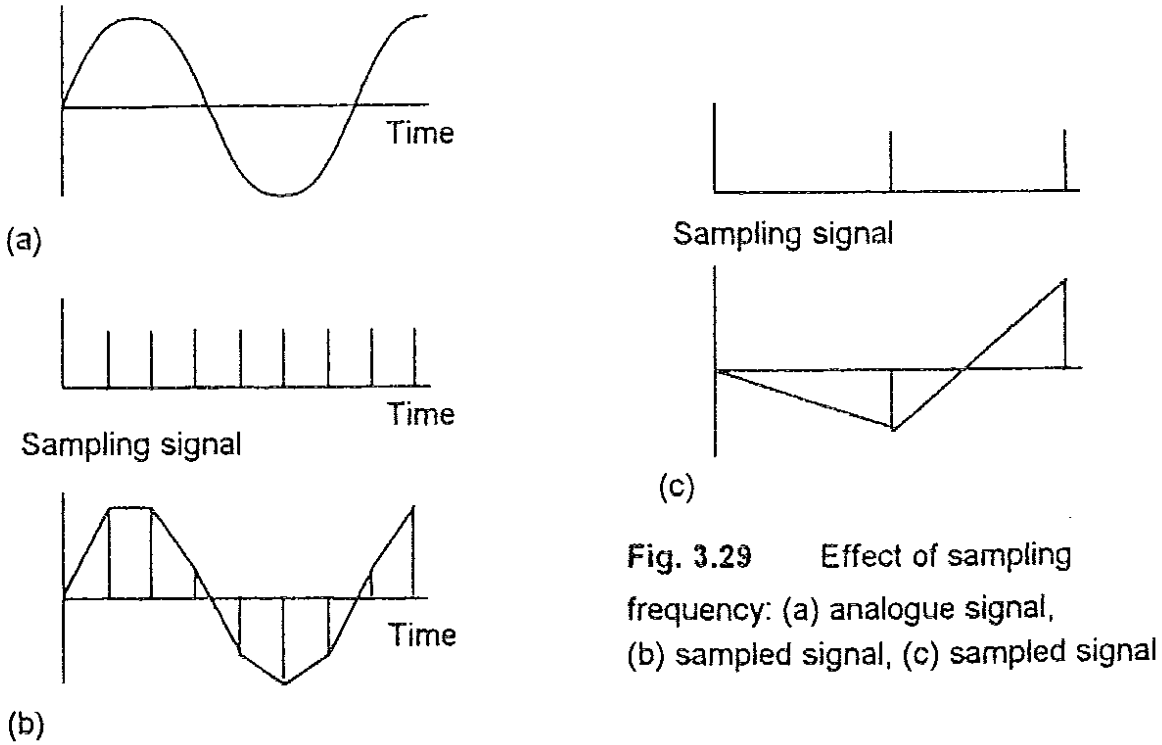
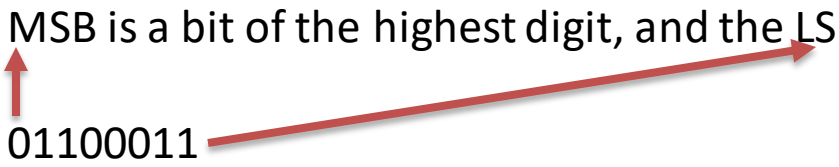


Fig. 3.29 Effect of sampling frequency: (a) analogue signal, (b) sampled signal, (c) sampled signal

A-D characteristics



Conversion Rate: **How many conversions per unit time**

Voltage range: Reference voltage (Analog voltage that controller can handle)

Resolution :

$$\text{Voltage resolution} = \text{range}/2^n$$

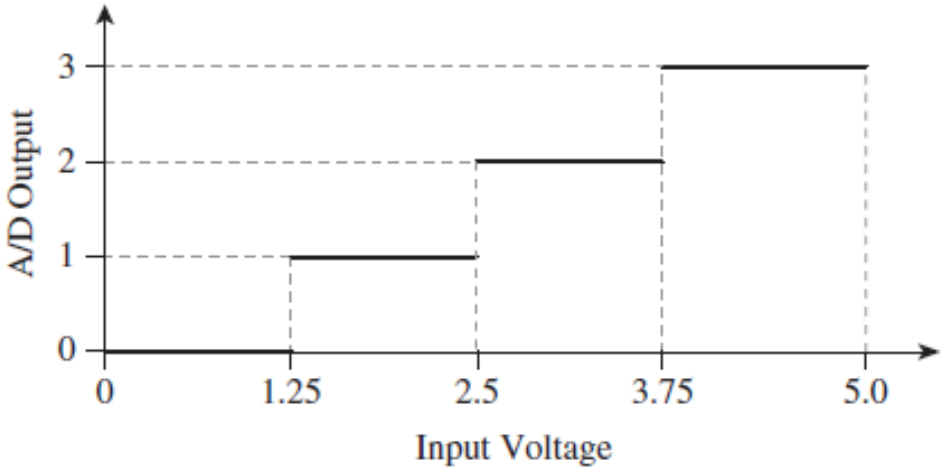
n – number of bits

Quantization Error (Digitization accuracy)

Quantization error = Resolution Error / 2

Say a analog input of 5 V and we use 2 bit converter

Means 0 0 , 0 1, 1 0 and 1 1 are the possible representation



Resolution: ?

Quantization error: ?

Calculation

Consider a thermocouple giving an output of 0.5 mV/°C. What will be the word length required when its output passes through an analogue-to-digital converter if temperatures from 0 to 200°C are to be measured with a resolution of 0.5°C? The full-scale output from the sensor is $200 \times 0.5 = 100$ mV. With a word length n, this voltage will be divided into $100/2^n$ mV steps. For a resolution of 0.5°C we must be able to detect a signal from the sensor of $0.5 \times 0.5 = 0.25$ mV. Thus we require

$$0.25 = \frac{100}{2^n}$$

Hence $n = 8.6$. Thus a 9-bit word length is required.

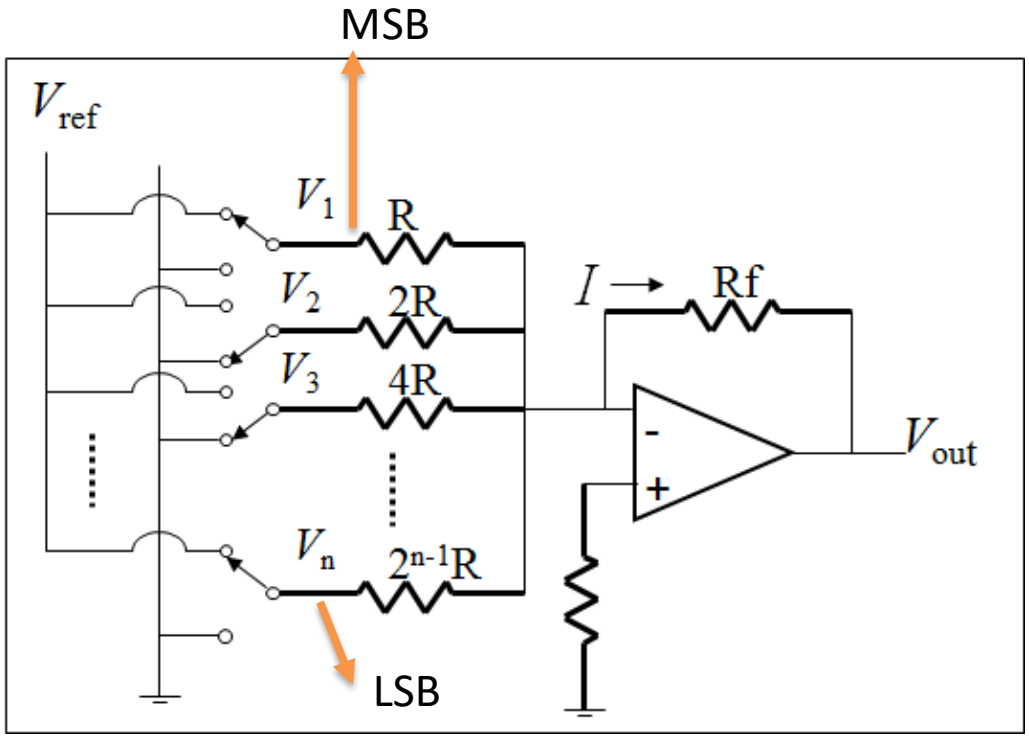
Quantization Error (Digitization accuracy)

Determine the voltage resolution and digitization accuracy of an ideal 12-bit A/D converter with a 0 to 10 V range. Determine the output level if the input voltage is 6.5 V. Also, determine the corresponding analog input voltage at the following digital output values: 0 and 1000.

Solution:

From Equation (5.1), the voltage resolution of this A/D device is $10/2^{12} = 2.441$ mV. Thus, the digitization accuracy of the conversion is $+/-$ 1.220 mV.

Weighted resistor DAC

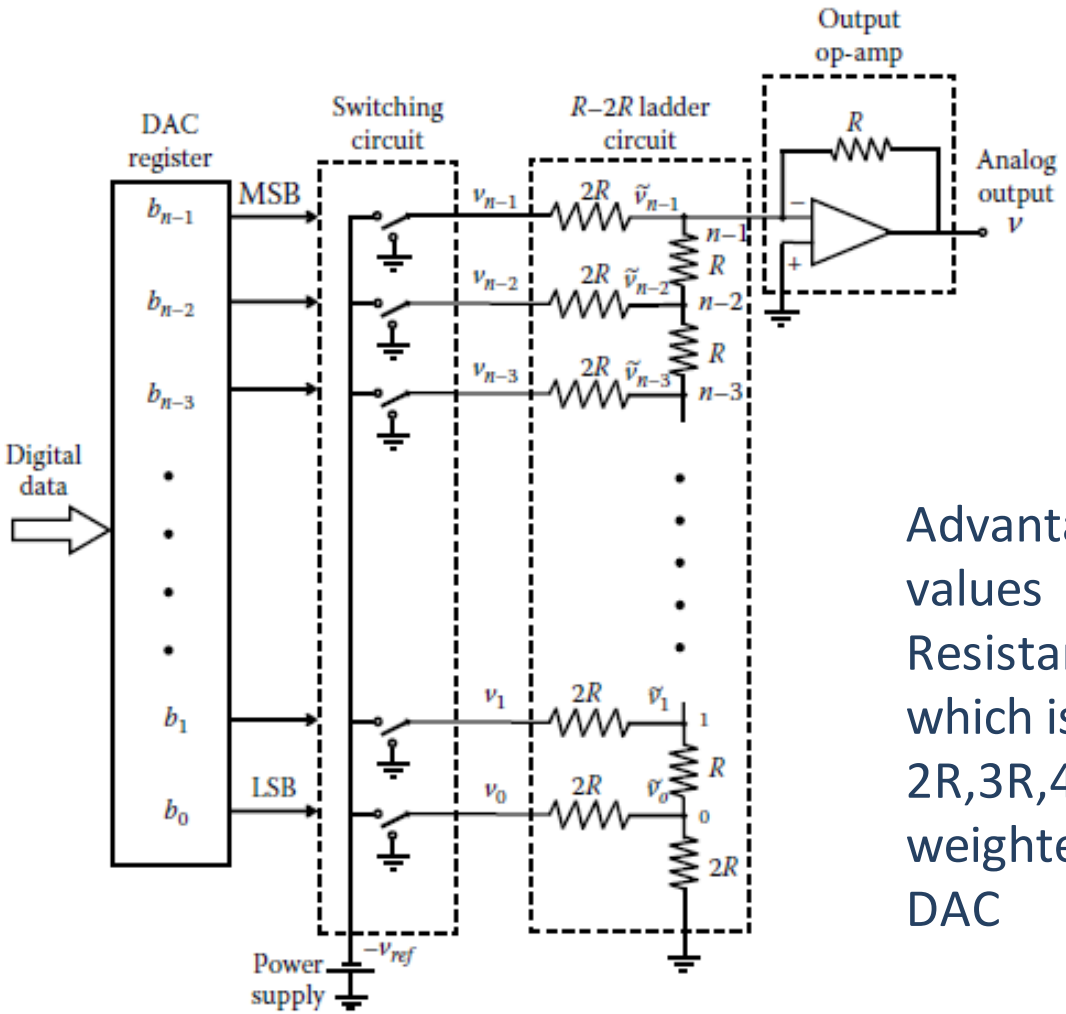


$$V_{out} = -IR_f = -R_f\left(\frac{V_1}{R} + \frac{V_2}{2R} + \frac{V_3}{4R} + \cdots \frac{V_n}{2^{n-1}R}\right)$$

The resistances are increased form MSB to LSB to adjust to the weightage of the binary digits

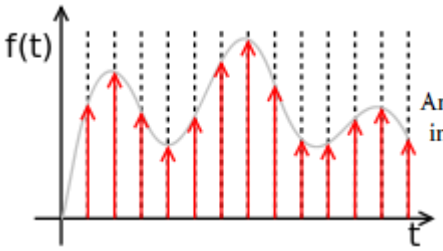
Availability of Accurate resistances is a problem and that too at varying temperatures, Limited to 4 bit conversions

R-2R Ladder DAC

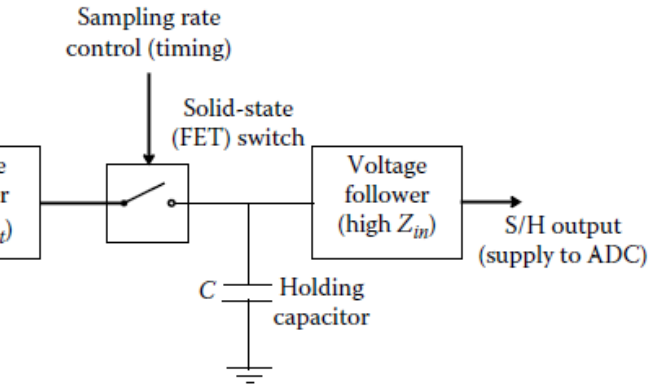


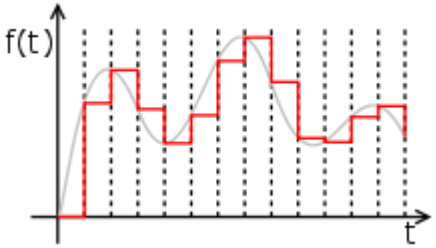
Advantage is only 2 values of Resistances are used which is better than 2R,3R,4R etc used in weighted resistor DAC

Sample and Hold circuit



Sample times



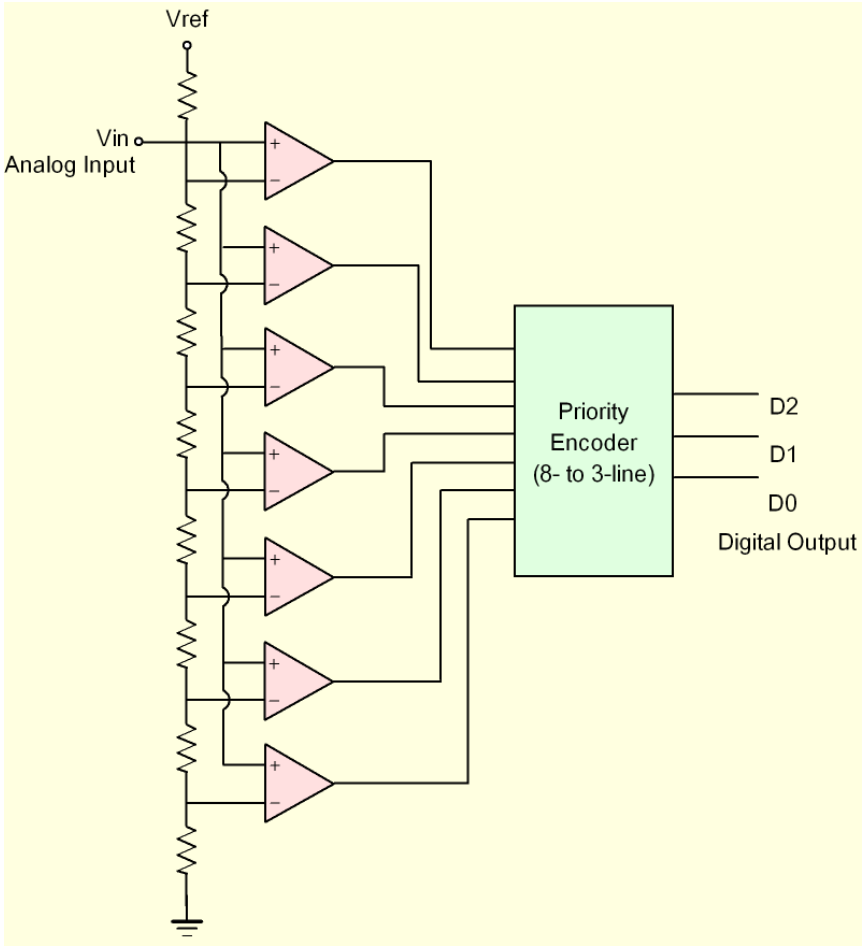


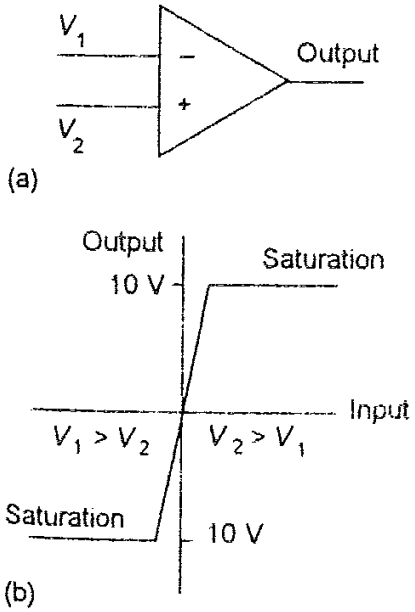
Sample and hold

Zout Voltage follower is used to provide low output impedance during charging of holding capacitor (Closing of FET switch).

Zin voltage follower is used to provide high input impedance once the FET switch is open.

Flash A-D converters

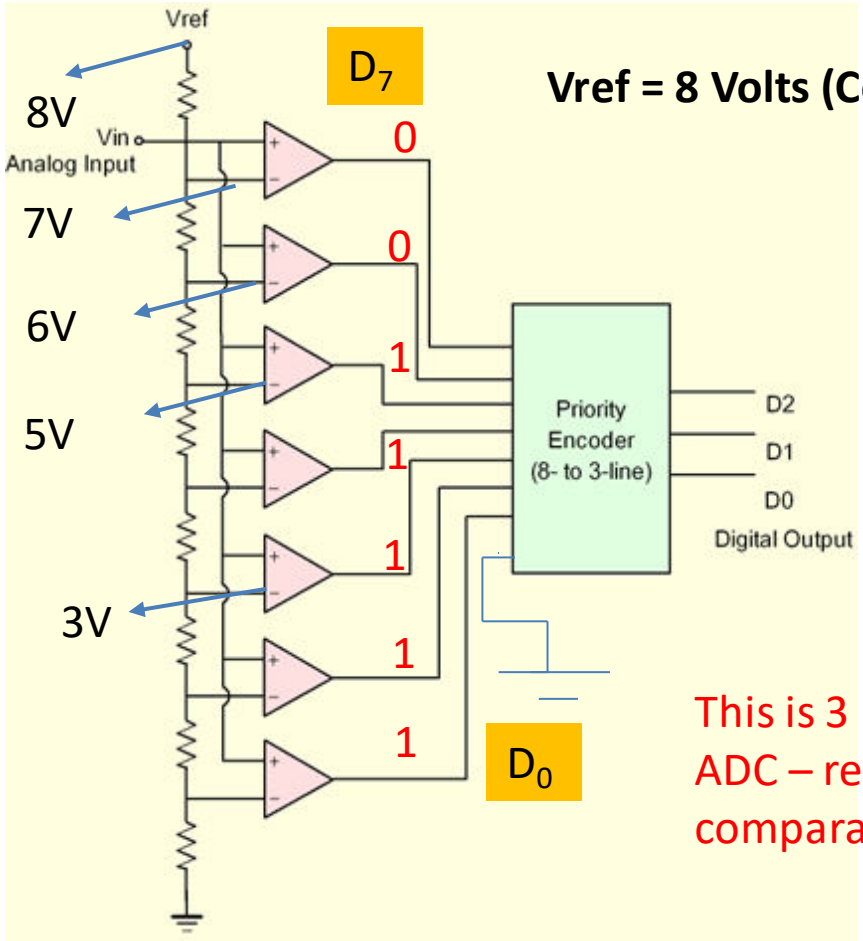




Flash A-D converters

Vin= 5.5 Volts (From Analog input)

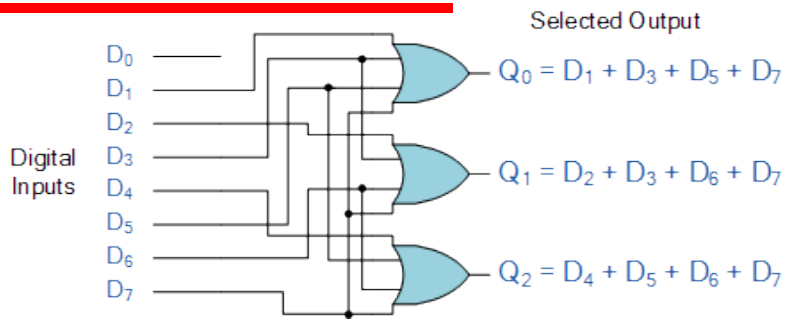
Vref = 8 Volts (Constant)

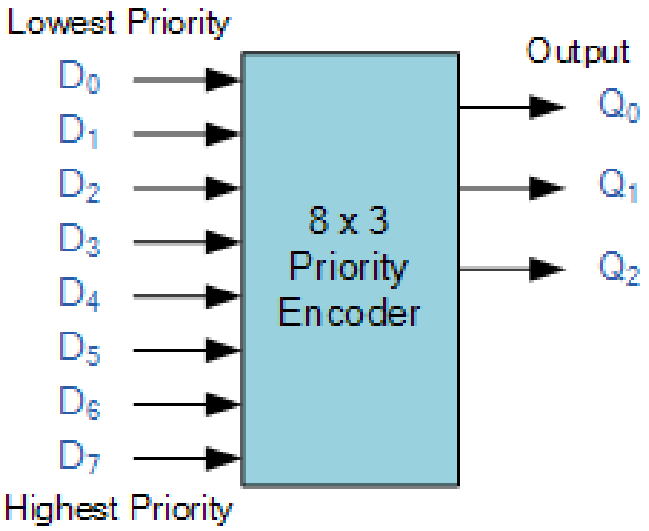


This is 3 bit Flash ADC – requiring 2^3-1 comparators.

Flash A-D converters

Our case is 0 0 1 1 1 1 1 1





Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

X = dont care

Output 1 0 1 corresponds to 5V

Priority Encoders

MOTOROLA

10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

The SN54/74LS147 and the SN54/74LS148 are Priority Encoders. They provide priority decoding of the inputs to ensure that only the highest order data line is encoded. Both devices have data inputs and outputs which are active at the low logic level.

The LS147 encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition does not require an input condition because zero is encoded when all nine data lines are at a high logic level.

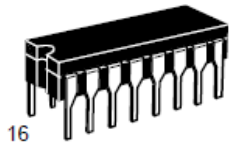
The LS148 encodes eight data lines to three-line (4-2-1) binary (octal). By providing cascading circuitry (Enable Input EI and Enable Output EO) octal expansion is allowed without needing external circuitry.

The SN54/74LS748 is a proprietary Motorola part incorporating a built-in deglitcher network which minimizes glitches on the GS output. The glitch occurs on the negative going transition of the EI input when data inputs 0–7 are at logical ones.

SN54/74LS147
SN54/74LS148
SN54/74LS748

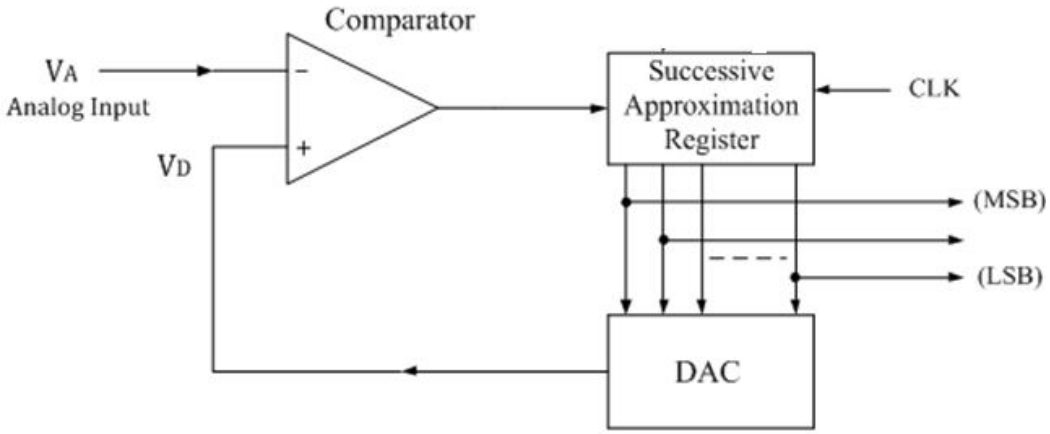
10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09

Successive approximation ADC



n bit word takes **n** steps to make the comparison

If clock has frequency **f,** the time between pules is 1/f

Conversion time is **n/f**

4 bit analysis

-Analog input is 3 Volts(V_A) - Say

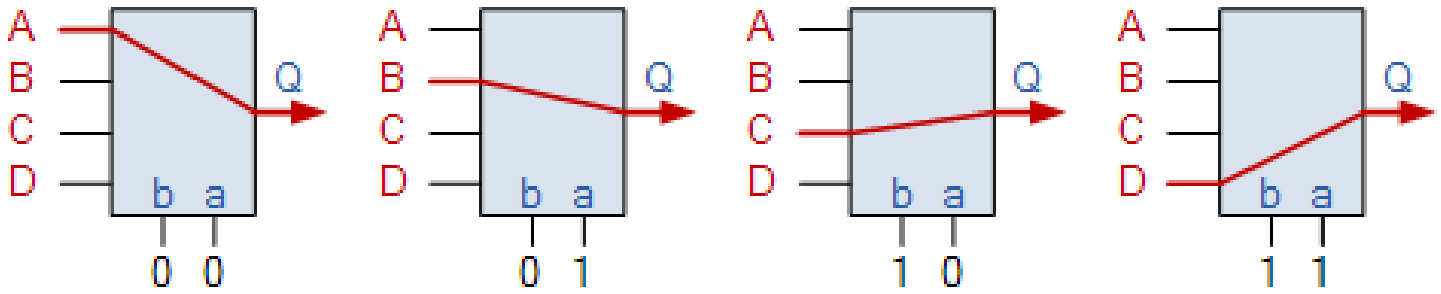
-SAR generates 1 0 0 0

- DAC converts 1 0 0 0 to 8 Volts

Compare it in comparator

- 8>3, true, send next
- 0 1 0 0 (4 volts)
- 4>3 , true, send next
- 0 0 1 0 (2 volts)
- 2> 3, false hence, retain 0 0 1 0
- Send next 1 (LSB)
- 0 0 **1** 1
- Thus the digital O/P **0 0 1 1 of analog 3 Volts**

Multiplexer



- Provides an output from just one of many input data
- Avoids separate ADC and microprocessor for each measurement

Parity bit concept for error detection

At source, The data 10101 is given the even parity bit of 1, resulting in the bit sequence 101011.

Detects loss of data

During transmission of data, Suppose 101011 becomes , say 111011, receiver will detect lack of even parity and nullifies the data.

Thank you