INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

Mid Spring Semester Examination 2023-24

Date of Examination: 19th February, 2024 Session: (AN) Duration: 2 Hrs. Full Marks: 60

Subject No. : EC21201 Subject :Basic Electronics

Department/Center/School: Dept. of Electronics and Electrical Communication Engineering

Specific charts, graph paper, log book etc., required: No

Special Instructions (if any) : Assume room temperature for all calculations. At room temperature $V_T = 26\,mV$, $q = 1.6 \times 10^{-19} C$.

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1. Choose proper answer for the following questions. $[1 \times 5 = 5\,marks]$

A. What happens to the resistance of an intrinsic semiconductor when heated?
(i) The resistance increases
(ii) The current decreases
(iii)The current remains the same
(iv)The resistance decreases

B. For an electron mobility of 1000 $cm^2/V\text{-}s$, with an applied electric field of 0.5 mV/cm, the electron drift velocity is
(i) $2 \times 10^6\ cm/sec$
(ii) $0.5\ cm/sec$
(iii)$0.5 \times 10^{-6}\ cm/sec$
(iv)$1000\ cm/sec$

C. Which of the following is created when group 13 impurities are added to a semiconductor?
(i) Free electrons
(ii) Free Holes
(iii)Bound electrons
(iv)Bound Holes

D. The electrical resistance of the depletion layer is large because
(i) It has only bound electrons
(ii) It has only bound holes
(iii)It has immobilized ions
(iv)It has more free charge carriers

E. For a Bipolar Junction Transistor (BJT) with $\alpha_{DC} = 0.98$ and $I_B = 100\ \mu A$ and $I_C = 4.9\ mA$. The corresponding values of β_{DC} is .....and I_E is..... Respectively.

Q2. With suitable diagrams, explain why AC is allowed to pass through capacitors but DC is blocked? **[5 marks]**

Q3. A cylindrically shaped section of Silicon has a length of $1mm$ and $0.1mm^2$ cross-sectional area. Calculate the its **conductivity** and **resistance** for

(A) When the Silicon is intrinsic.

(B) When it is n-type doped with free electron density of $n = 8 \times 10^{13}\ cm^{-3}$

Assume: Intrinsic electron and hole density in Silicon is $1.5 \times 10^{10}\ cm^{-3}$ at room temperature. Mobility of electrons and holes in Silicon are 1500 $cm^2/V\text{-}sec$ and 500 $cm^2/V\text{-}sec$ respectively at room temperature. **[5 marks]**

Q4. (A) Draw all necessary blocks required to convert 220V (rms), 50 Hz AC line to a DC of 9V. Plot all intermediate output waveform at every stage. Justify your choice of the rectifier circuit. **[2+1+1=4 marks]**

(B) It is desired to achieve DC voltage of 9V with ripple of not more than 10% whereas the output voltage of 9V can deliver 100 mA to the load. Estimate all necessary design parameters (transformer turns ratio, capacitance and PIV of diode). In order to reduce the ripples further to be within 5%, what one should do? **[6 marks]**

(C) Plot the rectified and filtered output as a function of time for 10% and 5% ripples. Show clearly minimum and maximum voltage levels. **[2+1 marks]**

Q5. Plot the output waveforms (v_o) of following circuits (shown in Figure 1) while mentioning clearly the voltage levels, if the input signal v_I is sinusoidal (AC) with a peak-to-peak of 20V for both the circuits (i) and (ii). Assume $V_\gamma = 0.7V$ for diode and Zener diode. **[6+6 marks]**

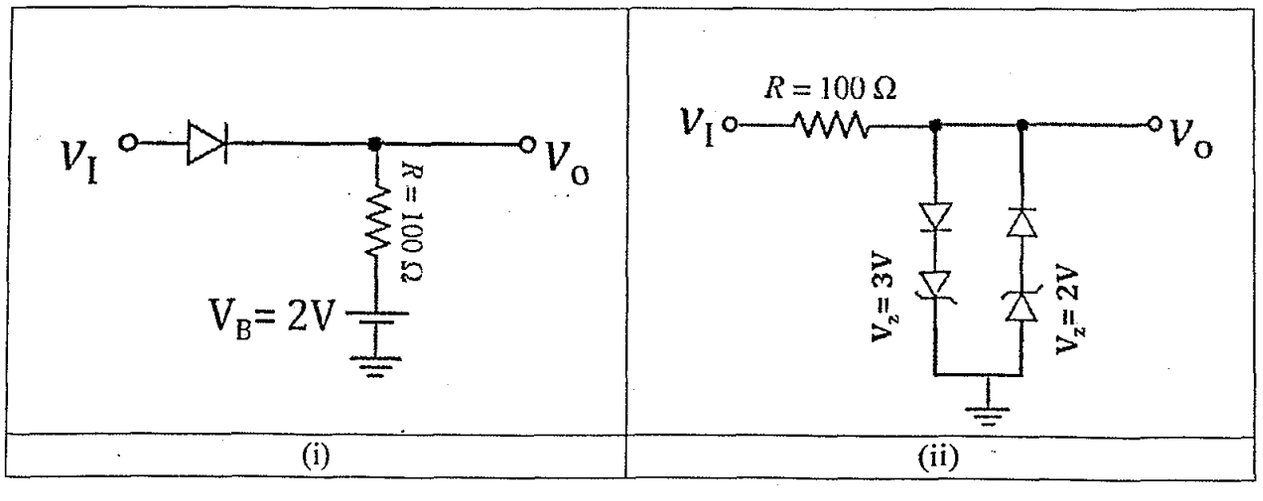

Figure 1: Circuit for Q5

Q6. (A) Consider the circuit in Figure 2. Let $V_\gamma = 0$. The secondary voltage is given by $v_s = V_s \sin(\omega t)$, where $V_s = 24\ V$ and $\frac{\omega}{2\pi} = 50Hz$. The Zener diode has parameters $V_Z = 16\ V$ at $I_Z = 40\ mA$ and $r_z = 2\Omega$. Determine the maximum value of R_i such that the load current can vary over the range $40 \leq I_L \leq 400\ mA$ with $I_Z(min) = 40\ mA$. **[7 Marks]**

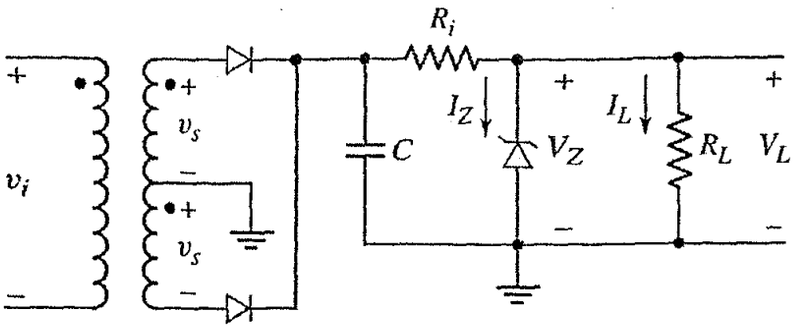

Figure 2: Circuit for Q6 (A)

(B) Design a diode clamper to generate a steady-state output voltage v_O from the input voltage v_I in Figure 3 if $V_\gamma = 1V$ **[5 Marks]**

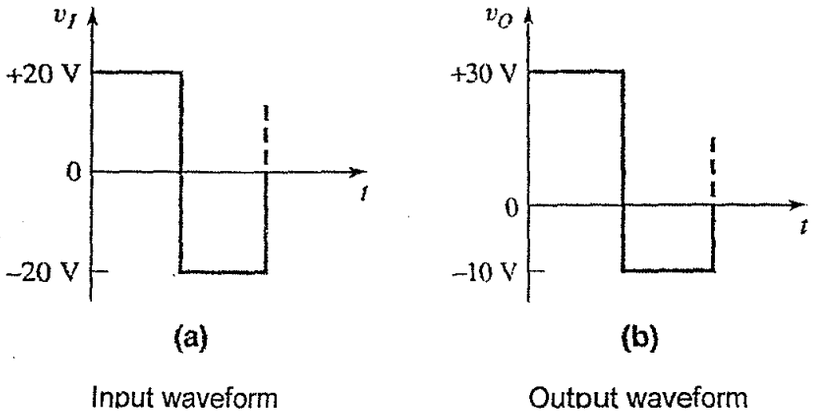

Figure 3: Waveforms for Q6 (B)

Q7. The circuit shown in Figure 4 is designed such that $R_B = R_E = 1k\Omega$ and $R_C = 2k\Omega$. If $\beta = 100$, then

(i) Determine the values of I_C and I_B. Hence, determine V_{CE}. **[4 Marks]**

(ii) If β is changed to 120, determine the percentage variation in I_B, I_C and V_{CE}. **[4 Marks]**

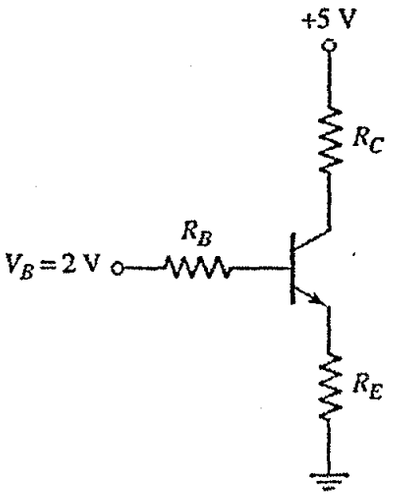

Figure 4: Circuit for Q.7