Enrollment No_____

KADI SARVA VISHWAVIDYALAYA

B.E. SEMESTER – IV(NEW) EXAMINATION NOVEMBER -2022

SUBJECT CODE: - CT 403N **SUBJECT NAME:- Computer Organisation & Architecture**

DATE: 9-Nov.-2022 **TIME: - 10:00 am to 1:00 pm** **MARKS:-70 Marks**

Instructions:

1. Answer each section in separate Answer Sheet.
2. All questions are **compulsory.**
3. Indicate clearly, the options you attempted along with its respective question number.
4. Assume suitable data wherever necessary.
5. Use of scientific calculator is permitted.

SECTION-I

Q-1 (A)	Explain the register transfer process with block diagram and timing diagram.	[05]
(B)	Explain 4 bit adder- subtractor using full adders.	[05]
(C)	List and explain shift micro-operations.	[05]
	OR	
(C)	Explain the registers of the basic computer.	[05]
Q-2 (A)	Explain direct and indirect addressing of basic computer.	[05]
(B)	Explain the basic working principle of the control unit.	[05]
	OR	
Q-2(A)	Explain the design of accumulator logic.	[05]
(B)	Explain the flowchart for interrupt cycle.	[05]
Q-3(A)	Define pseudo instruction and give any 3 examples.	[05]
(B)	Explain assembly language, assembler and state rules of the language.	[05]
	OR	
Q-3(A)	Draw and explain input-output configuration of basic computer.	[05]
(B)	Explain first pass of an assembler with flow chart.	[05]

SECTION-II

Q-4(A) Explain any 5 addressing modes with suitable examples. [05]

(B) Explain the characteristics of RISC. [05]

(C) Explain memory stack organization. [05]

OR

(C) Draw and explain the block diagram showing the status registers. [05]

Q-5(A) What is pipelining? Explain four-segment pipeline. [05]

(B) Explain the instruction pipeline and the difficulties associated with it. [05]

OR

Q-5(A) Explain arithmetic pipelining. [05]

(B) Explain space time diagram for pipelining. [05]

Q-6(A) Write short note on memory hierarchy. [05]

(B) Explain cache memory. [05]

OR

Q-6 (A) Draw block diagram of associative memory and explain. [05]

(B) Explain virtual memory. [05]

Best of Luck

Exam Seat No._____

KADI SARVA VISHWAVIDYALAYA

BE SEMESTER-IV (New) Examination June-2022

Subject Code: CT403-N
Subject Name: Computer Organization & Architecture
Date: 10-06-2022 **Time: 12.30 pm to 01.30 pm** **Total Marks: 70**

Instructions:
1. Answer each section in separate answer sheet.
2. Use of scientific calculator is permitted.
3. All questions are Compulsory.
4. Indicate clearly, the option you attempt along with its respective question number.
5. Use the last page of main supplementary of rough work.

Section-I

Q-1 (A) Define the following. [5]
(1) Register
(2) Microoperations
(3) Instruction code
(4) De-multiplexer
(5) Effective Address

(B) Explain Basic Computer Registers for Computer Organization. [5]

(C) Design a 4-bit combinational circuit decrementer using four full adder circuits. [5]

OR

(C) List out arithmetic microoperations; also design a 4-bit binary adder. [5]

Q-2 (A) Design a circuit which can display register value on a common display using bus system for four register. [5]

(B) What is Instruction Cycle? Draw only its flowchart. [5]

OR

(A) Explain the Design of accumulator logic with block diagram. [5]

(B) Explain BSA and ISZ instruction with necessary sketch. [5]

Q-3 (A) Explain Input-Output configuration with necessary flag. [5]

(B) Draw only flowchart for Second pass assembler. [5]

OR

(A) Define Subroutine and Explain with example. [5]

(B) Draw and Explain flow chart for interrupt cycle. [5]

Section-II

Q-4 (A) (1) Which system is used to encode all expressions, instructions and data in to digital computer? [5]

(a) English Language (c) Binary system
(b) Assembly system (d) Natural language

(2) 2's complement form of the number 001010 is

(a) 111100 (c) 110111
(b) 110110 (d) 111011

(3) Size of Control word in Register Organization

(a) 14 (c) 08
(b) 12 (d) 16

(4) What is correct instruction if you want the control to go to the location 2000h?

(a) MOV 2000h (c) MOV A, 2000h
(b) JMP 2000h (d) RET 2000h

(5) Which register is memory pointer:

(a) Source index (c) Instruction register
(b) Program counter (d) Data register

(B) What is Stack? Explain Register Stack using a block diagram of a 64-word stack. Also explain Push & Pop operations for the same. [5]

(C) List out addressing modes, explain any five with an example of instruction . [5]

OR

(C) Write ALP for subtraction of two numbers and result should store on to memory. [5]

Q-5 (A) What is pipelining? Explain pipeline processing with example [5]

(B) Explain pseudo instruction.. [5]

OR

(A) Discuss instruction format w.r.t. its address size. [5]

(B) Differentiate RISC and CISC. [5]

Q-6 (A) What is auxiliary memory? Explain with its different types. [5]

(B) Discuss stage of RISC pipeline. [5]

OR

(A) Compare RAM and ROM. [5]

(B) Draw and explain four segment CPU pipeline. [5]

-- All the Best --