SUBHAM PRASAD GUPTA

VLSI ENGINEER

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ABOUT ME

I am a B-Tech student at Vellore Institute of Technology, Chennai, specializing in VLSI Design and Technology. Driven by curiosity and a passion for learning, I combine my technical skills with 14 years of fine arts training, musical experience, and disciplined Kung-Fu practice to strive for perfection in everything I do.

SKILLS

- VLSI CAD
- VLSI Physical Design
- Digital Circuit Design
- Verilog/System-Verilog
- TCL/Perl scripting
- 8051 & 8086 Assembly

TOOLS EXPERTISE

- Cadence Tools
  - nclaunch
  - Virtuoso
  - Genus
  - Innovus
- Synopsys TCAD
  - Sentaurus Structure Editor
  - Workbench
- ModelSim / QuestaSim
- Vivado
- Adobe Creative Suite

EDUCATION

B.Tech Electronics Engineering (VLSI Design & Technology)

VIT Chennai (2023–2027)
CGPA: 9.12

Senior Secondary (XI–XII)

Delhi Public School, Ruby Park, Kolkata (2020–2022) — 90.6%

High School (IX–X)

Heritage International Public School, Kushinagar (2018–2020) — 94.6%

EXPERIENCE

SUMMER INTERNSHIP (REMOTE) **May 2025 – July 2025**

Maven Silicon, Bengaluru, India

- Implemented Physical Design of Serial Peripheral Interface (SPI) using QFLOW.
- Participated in bi-weekly mentorship sessions to strengthen knowledge of VLSI design flow.
- Applied learned concepts to practical design projects, enhancing understanding of physical design processes.

SUMMER INTERNSHIP (REMOTE) **May 2025 – June 2025**

1Stop.ai, India

- Developed multiple Verilog projects culminating in a customizable 16-bit RISC-V processor.
- Applied Finite State Machine (FSM) concepts to project design and verification.
- Enhanced skills in RTL coding and system-level verification through hands-on project experience.

PROJECTS

ONGOING PROJECTS

- **FM-Based Netlist Partitioning & Layout Visualization Tool**
  - Netlist partitioning by n-random partitions using FM algorithm, optimized block layout visualization.
- **In-Memory Computing on SRAM (8x8 6T Cell Array)**
  - SRAM design in Cadence Virtuoso with arithmetic & logic operations directly in memory.
- **32-bit RISC-V Architecture with Custom Direct Addressing Mode Instruction Set**
  - RTL design & verification in Verilog/System-Verilog.

COMPLETED PROJECTS

- SPI Physical Design Implementation – Maven Silicon Internship
- Image Recogniser Using Verilog & Python – 2nd Semester DSD Project (2024)
- GUI-based System Verification Environment – 4th Semester (2025)