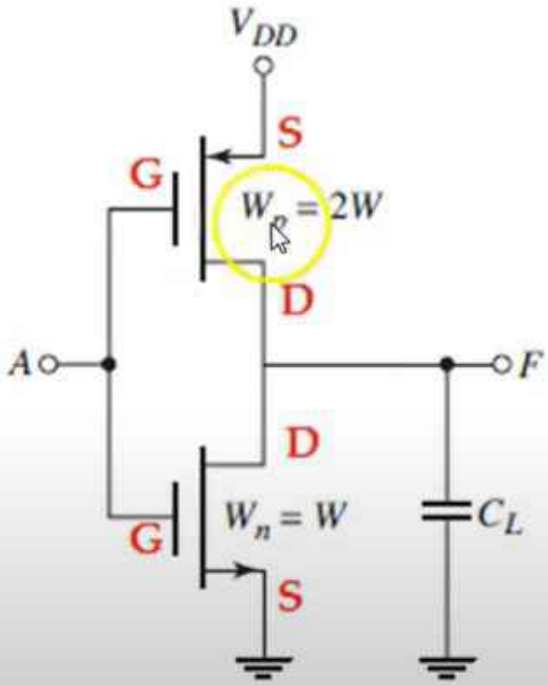
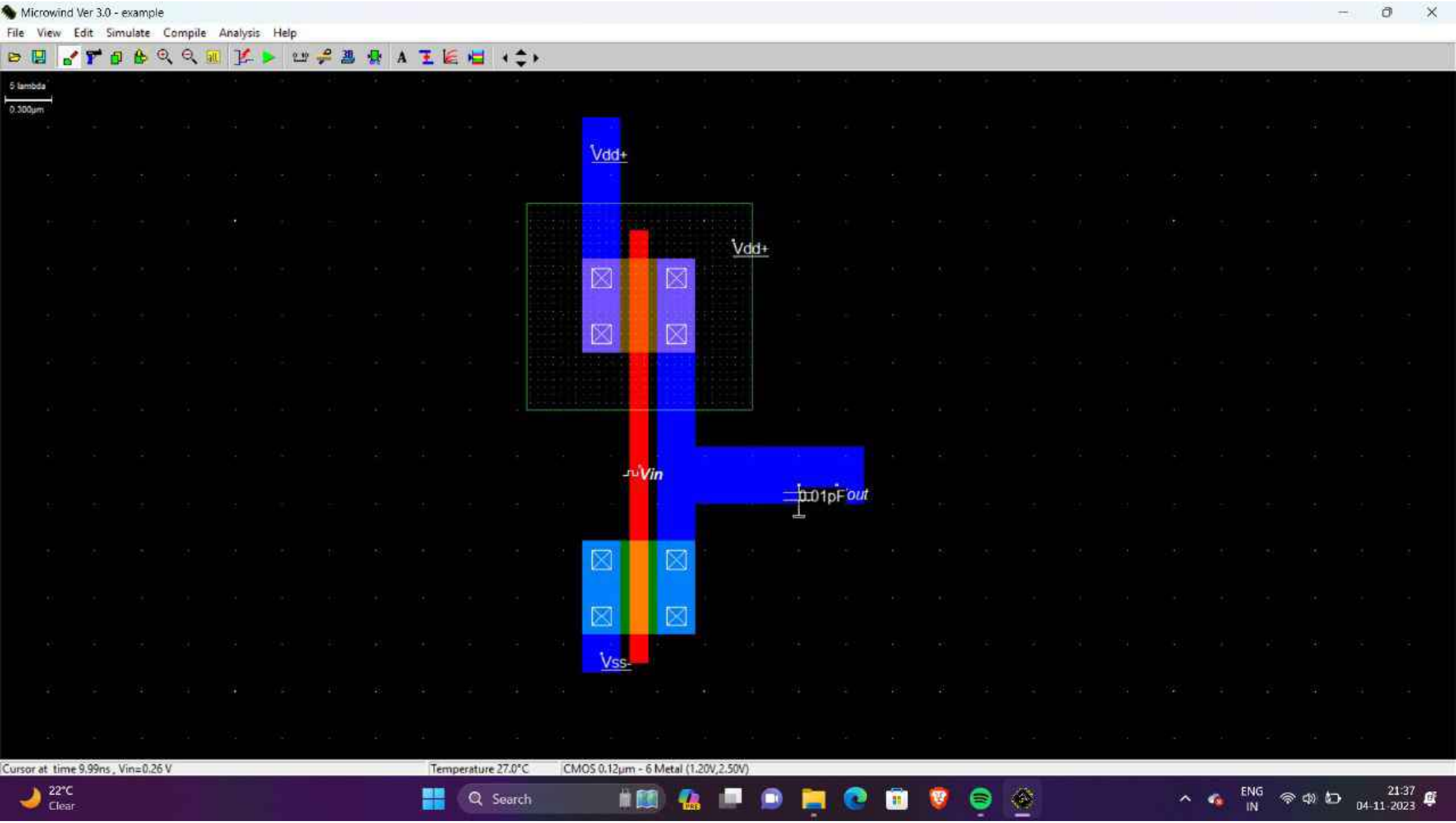
Simulation of CMOS Inveretr using microwind

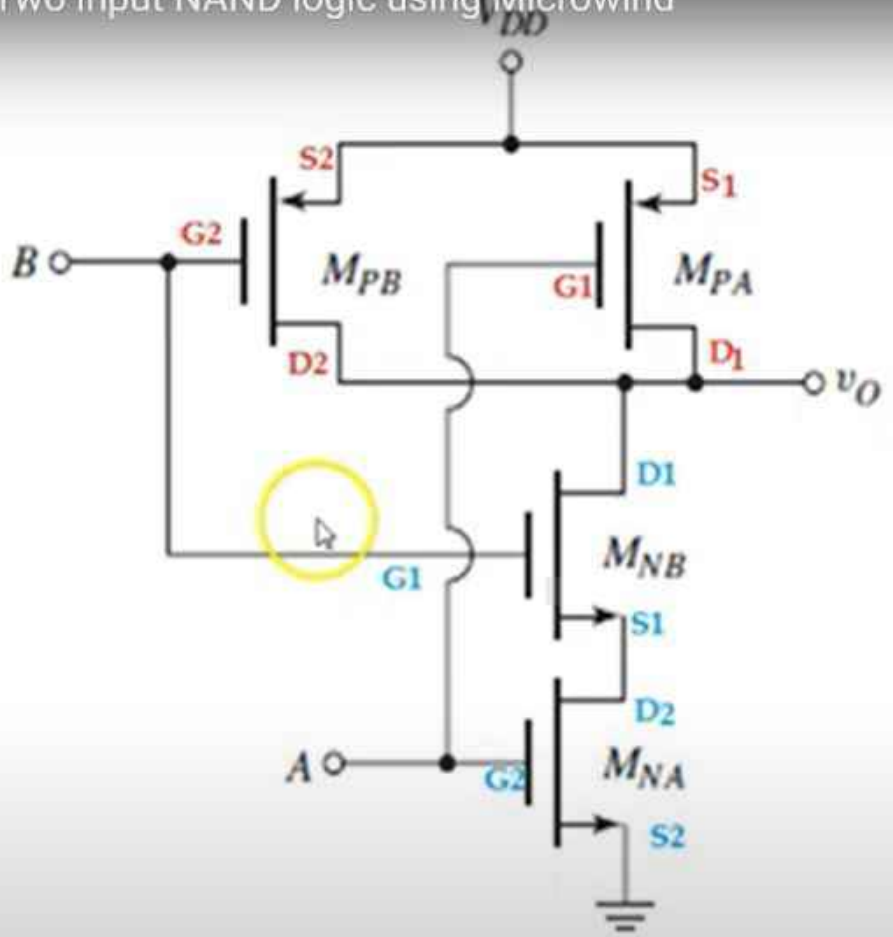
CMOS Inverter

INPUT	OUTPUT
0 (Logic 0)	V_{DD} (Logic 1)
V_{DD} (Logic 1)	**0** (Logic 0)




Microwind Ver 3.0 - example
File View Edit Simulate Compile Analysis Help
5 lambda
0.300µm
Vdd+
Vdd+
Vin
0.01pF
out
Vss-
Cursor at time 9.99ns , Vin=0.26 V
Temperature 27.0°C
CMOS 0.12µm - 6 Metal (1.20V,2.50V)
22°C
Clear
Search
ENG
IN
21:37
04-11-2023

Layout design of Two input NAND logic using Microwind



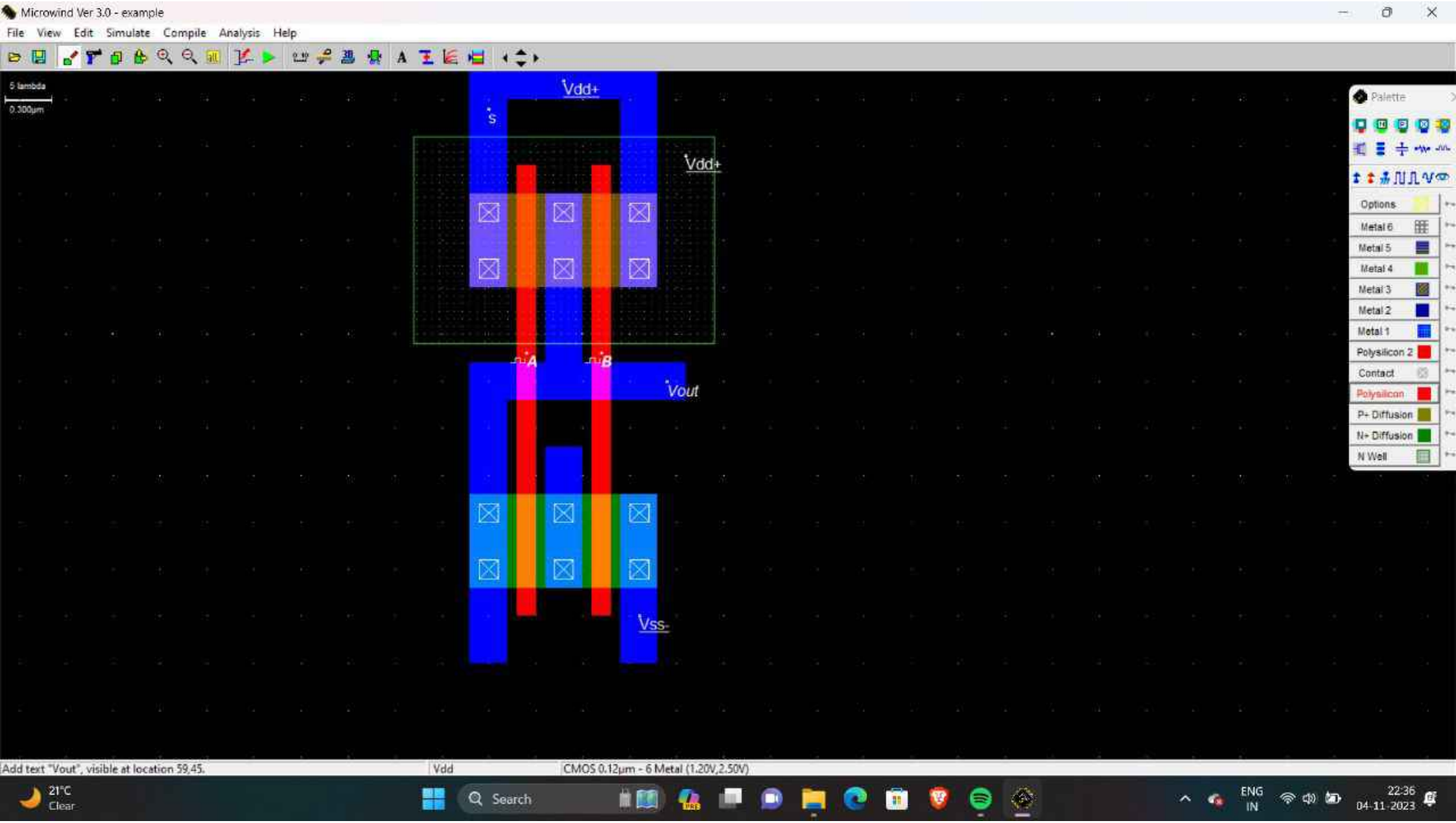
(a)

A	B	v_O
0	0	V_{DD}
V_{DD}	0	V_{DD}
0	V_{DD}	V_{DD}
V_{DD}	V_{DD}	0

(b)

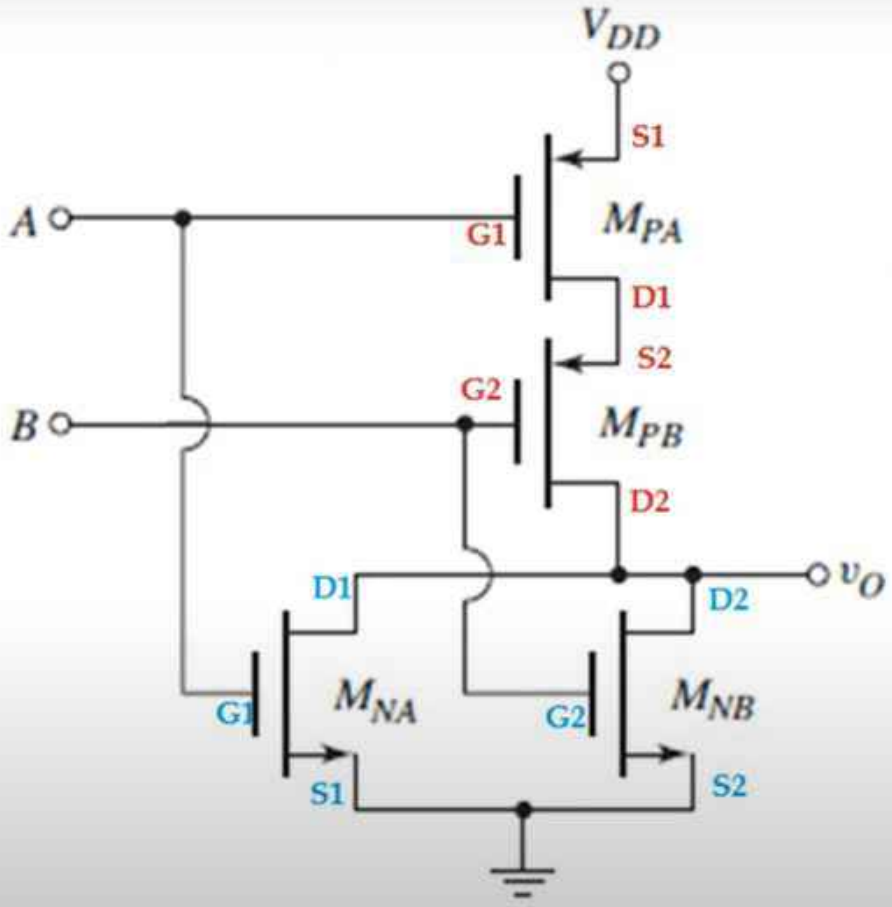
(a) Two-input CMOS NAND logic circuit (b) truth table

0:15 / 14:55


Microwind Ver 3.0 - example
File View Edit Simulate Compile Analysis Help
5 lambda
0.300µm
Vdd+
S
Vdd+
A
B
Vout
Vss-
Palette
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well
Add text "Vout", visible at location 59,45.
Vdd
CMOS 0.12µm - 6 Metal (1.20V,2.50V)
21°C
Clear
Search
ENG
IN
22:36
04-11-2023

Two input NOR gate layout design using Microwind

2-Input CMOS NOR logic circuit

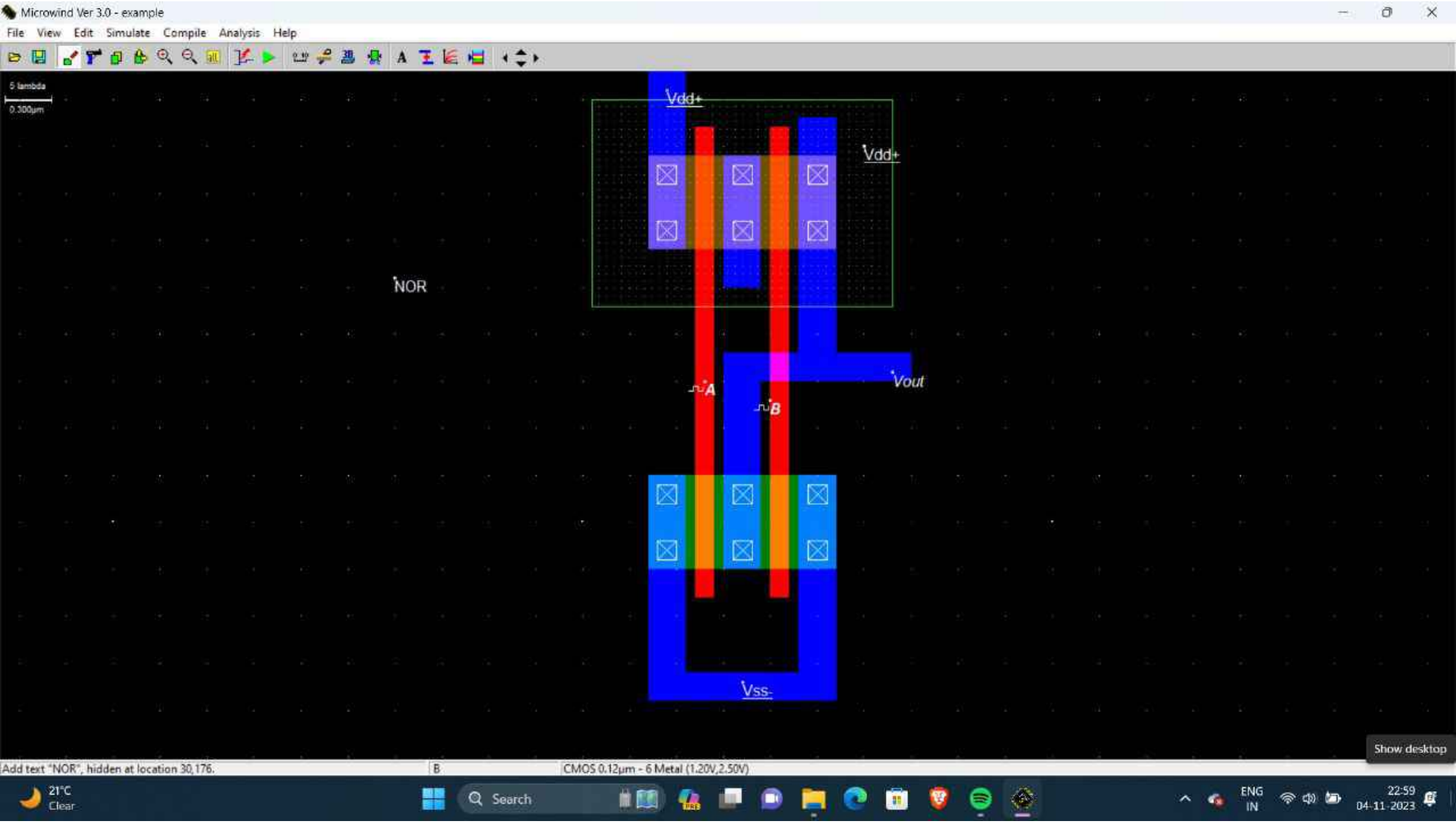


(a)

A	B	v_O
0	0	V_{DD}
V_{DD}	0	0
0	V_{DD}	0
V_{DD}	V_{DD}	0

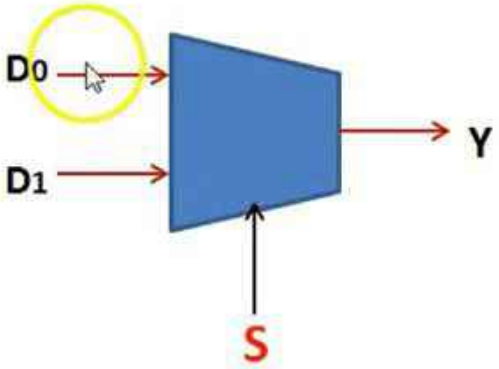
(b)

(a) Two-input CMOS NOR logic circuit (b) truth table


Microwind Ver 3.0 - example
File View Edit Simulate Compile Analysis Help
5 lambda
0.300µm
Vdd+
Vdd+
NOR
A
B
Vout
Vss-
Add text "NOR", hidden at location 30,176.
B
CMOS 0.12µm - 6 Metal (1.20V,2.50V)
Show desktop
21°C
Clear
Search
ENG
IN
22:59
04-11-2023

2:1 Multiplexer

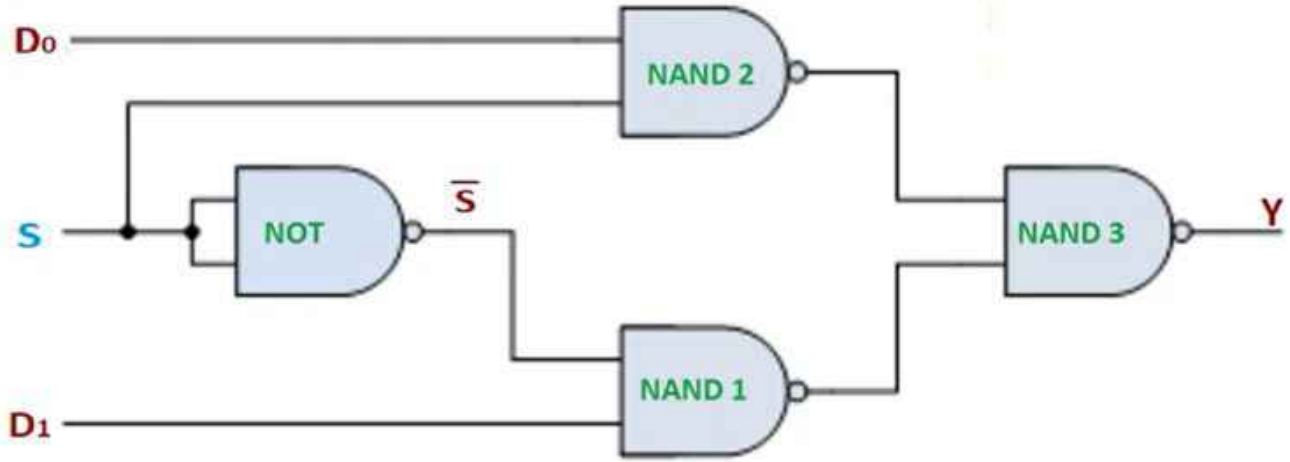
2:1 Mux

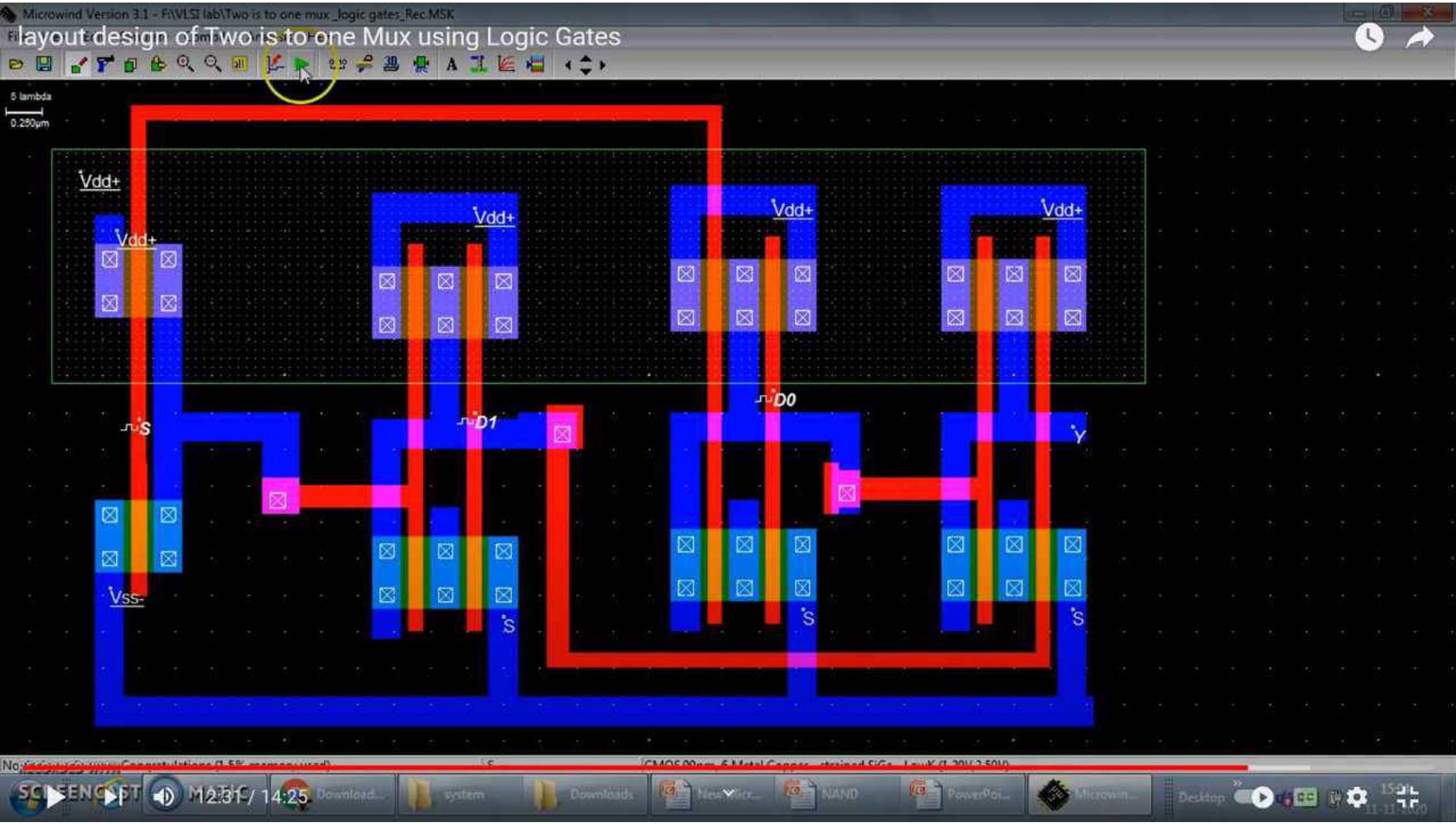


Truth table

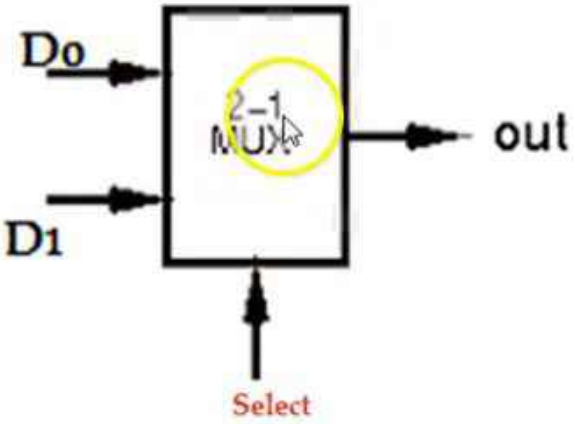
Input 'S'	Output Y
1	D0
0	D1

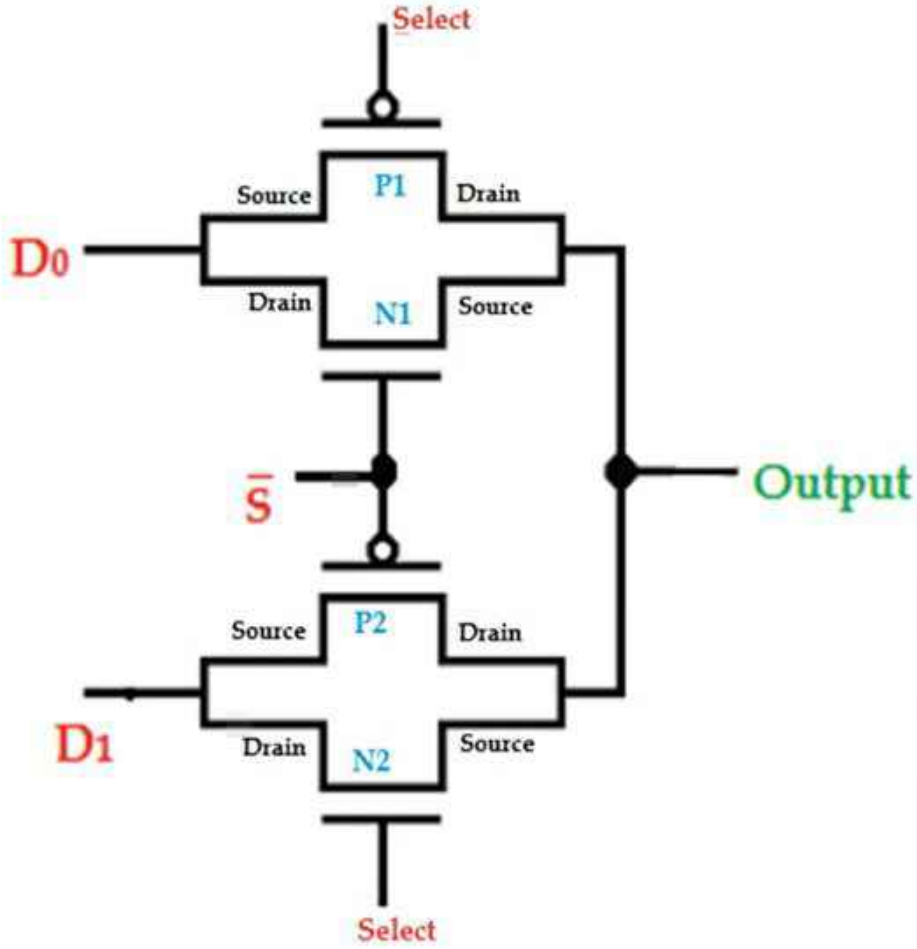
Implementation using logic gates

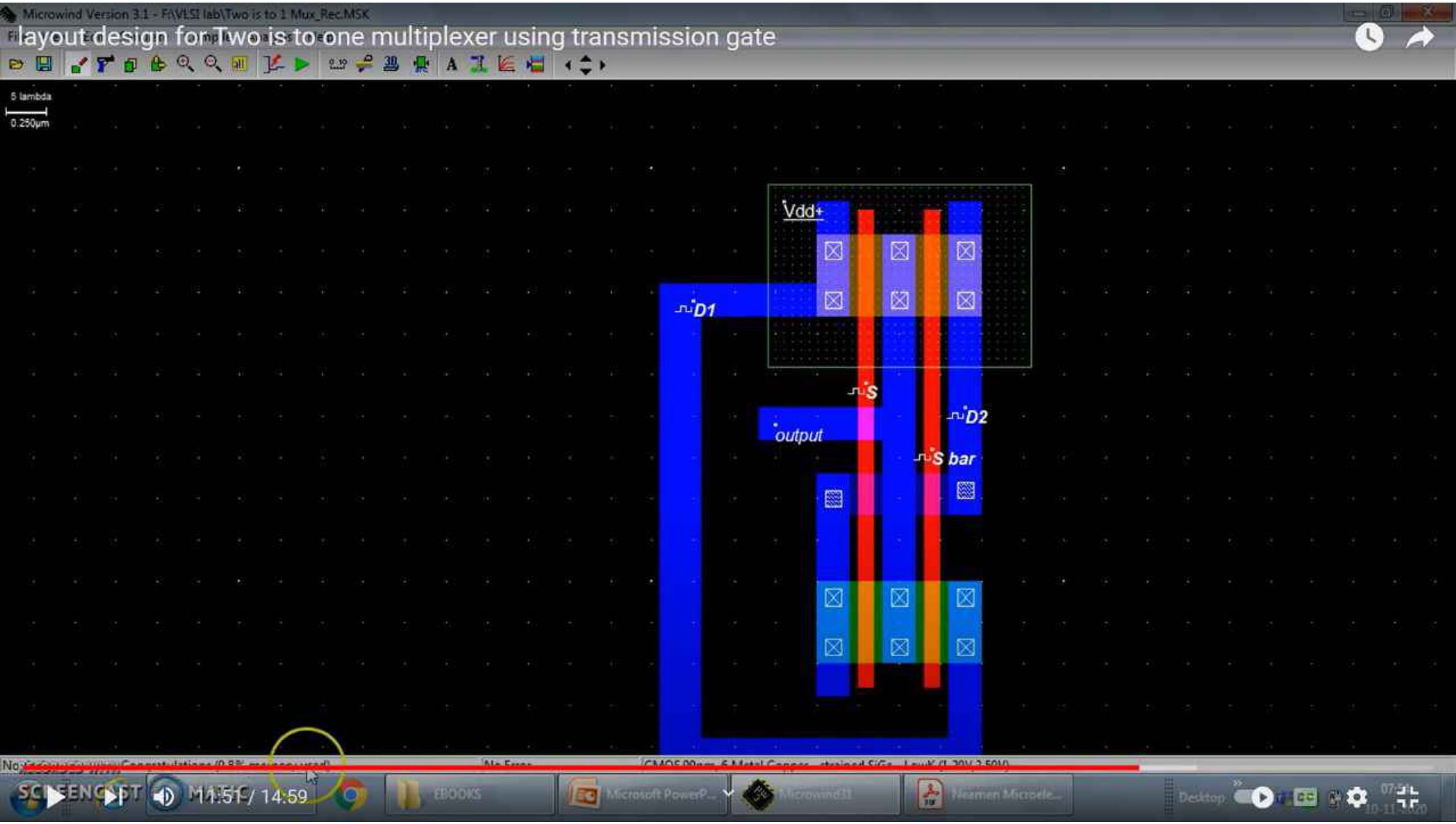



Microwind Version 3.1 - F:\VLSI lab\Two is to one mux _logic gates_Rec.MSK
layout design of Two is to one Mux using Logic Gates
5 lambda
0.280µm
Vdd+
Vdd+
Vdd+
Vdd+
Vdd+
S
D1
D0
Y
Vss-
S
S
S
12:31 / 14:25

2:1 Multiplexer using transmission gate

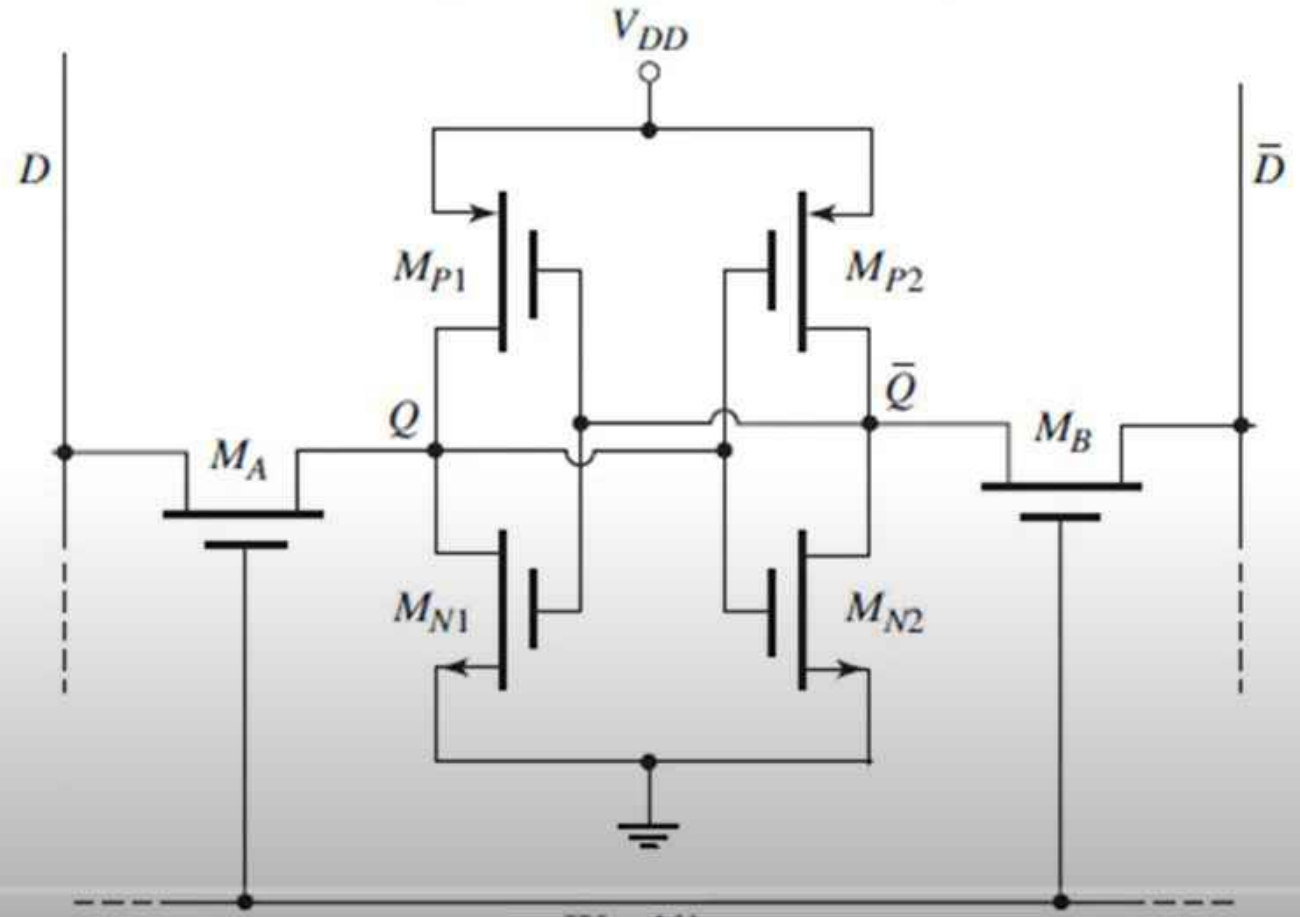


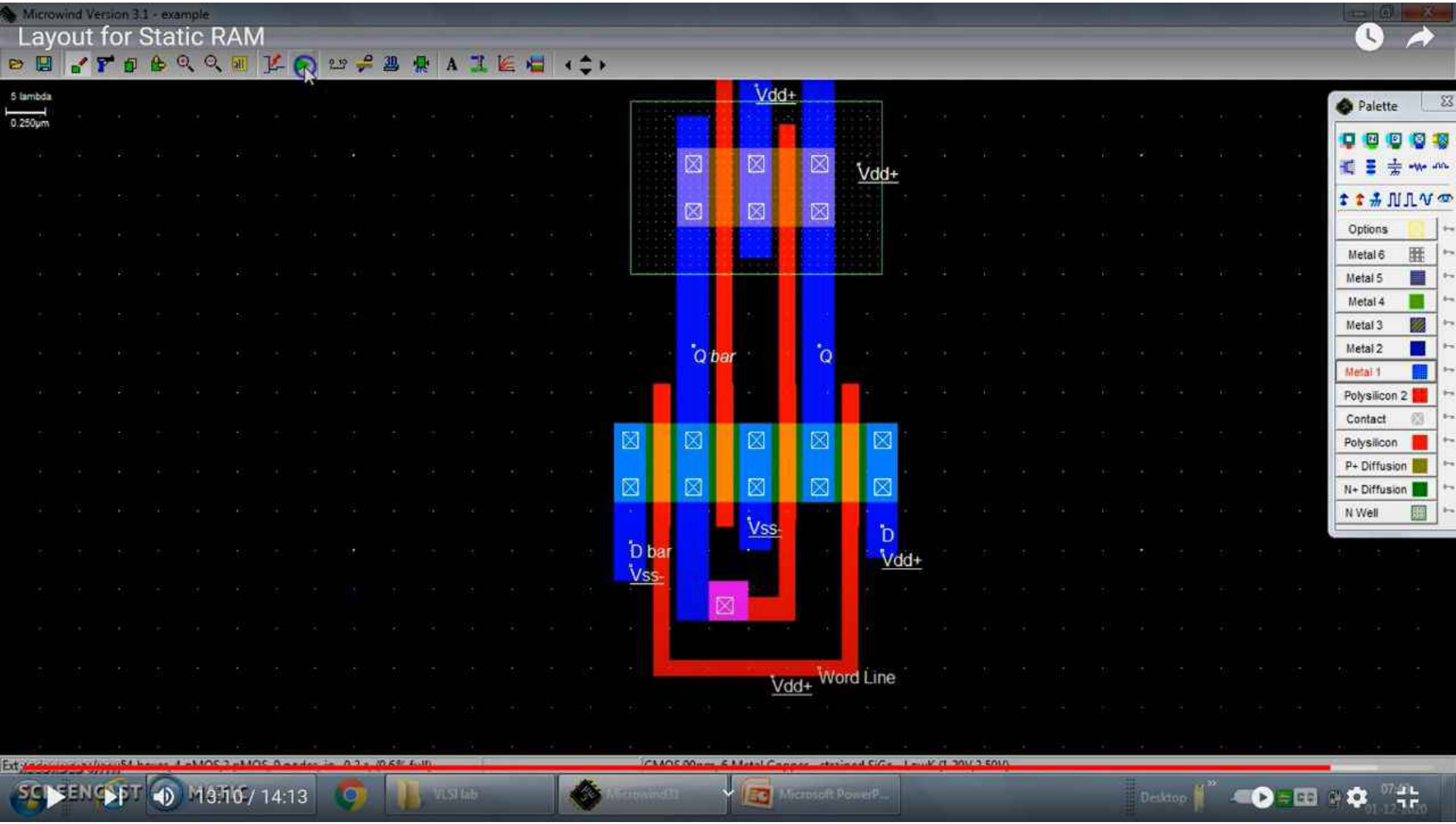



Microwind Version 3.1 - F:\VLSI lab\Two is to 1 Mux_Rec.MSK
layout design for Two is to one multiplexer using transmission gate
5 lambda
0.250µm
Vdd
D1
S
D2
output
S bar
11:51 / 14:59

Layout for Static RAM

A CMOS Static RAM cell




Microwind Version 3.1 - example
Layout for Static RAM
5 lambda
0.250µm
Vdd+
Vdd+
Q bar
Q
Vss-
D bar
Vss-
D
Vdd+
Vdd+
Word Line
Palette
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well
13:10 / 14:13