

**BTECH**  
**(SEM III) THEORY EXAMINATION 2018-19**  
**COMPUTER ORGANIZATION AND ARCHITECTURE**

**Time: 3 Hours****Total Marks: 70**

**Note: 1.** Attempt all Sections. If require any missing data; then choose suitably.

**SECTION A**

**1. Attempt all questions in brief. 2 x 7 = 14**

- a. What do you understand by Locality of Reference?
- b. Which of the following architecture is/are not suitable for realizing SIMD?
- c. What is the difference between RAM and DRAM?
- d. What are the difference between Horizontal and vertical micro codes? .
- e. Describe cycle stealing in DMA.
- f. List three types of control signals.
- g. Define the role of MIMD in computer architecture.

**SECTION B**

**2. Attempt any three of the following: 7 x 3 = 21**

- a. Evaluate the arithmetic statement  $X = (A+B)*(C+D)$  using a general register computer with three address, two address and one address instruction format a program to evaluate the expression .
- b. Perform the division process of 00001111 by 0011 (use a dividend of 8 bits).
- c. A two way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from memory. The main memory size is 128K X 32.
  - i. Formulate all pertinent information required to construct the cache memory.
  - ii. What is the size of cache memory?
- d. What is associative memory? Explain with the help of a block diagram. Also mention the situation in which associative memory can be effective utilized.
- e. A Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.
  - (i) How many bits are there in the operation code, the register code part and the address part?
  - (ii) Draw the instruction word format and indicate the number of bits in each part.
  - (iii) How many bits are there in the data and address inputs of the memory?

## SECTION C

3. Attempt any *one* part of the following: 7 x 1 = 10
- (a) Write short notes on :
    - (i) Instruction pipeline.
    - (ii) DMA based data transfer.
  - (b) Explain the difference between vectored and non-vectored interrupt. Explain stating examples of each.
4. Attempt any *one* part of the following: 7x 1 = 10
- (a) Draw the flow chart of Booth's Algorithm for multiplication and show the multiplication process using Booth's Algorithm for  $(-7) \times (+3)$ .
  - (b) Write short notes on:
    - (i) Amdahl's Law
    - (ii) Pipelining
5. Attempt any *one* part of the following: 7 x 1 = 10
- (a) What is a microprogram sequencer? With block diagram, explain the working of microprogram sequencer.
  - (b) Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation.
6. Attempt any *one* part of the following: 7 x 1 = 10
- (a) Give the block diagram of DMA controller. Why are the read and write control lines in a DMA controller bidirectional?
  - (b) Explain all the phases of instruction cycle.
7. Attempt any *one* part of the following: 7 x 1 = 10
- (a) Explain the basic concept of Hardwired and Software control unit with neat diagrams.

(b)

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

For the following Reservation table:

- i. Calculate the set of the forbidden latencies and collision vector.
- ii. Draw a state diagram, showing all possible initial sequences (cycles) without a collision in the pipeline.
- iii. Simple cycles (SC)
- iv. Greedy cycles among simple the cycles
- v. MAL (minimum average latency)
- vi. What is the minimum allowed constant cycles
- vii. Maxi. Throughput
- viii. Throughput if the minimum constant cycle is used.