SURVEY ON PROCESSORS OF SMART HANDHELD DEVICES

CSN 221: COMPUTER ARCHITECTURE AND MICROPROCESSORS

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1.Introduction

A processor is an integrated electronic circuit(IC) that performs arithmetical, logical, input and output and other basic instructions. These instructions are passed from an operating system. A processor basically includes a ALU and CU. In simple words it is a small chip that processes smart devices such as tablets, mobile, etc. Processors can be categorized into single core and multi core processors. Now a days they are further classified as dual core, triple core, quad core and octa core. Which means these processors can run two CPU's that is Dual core, three CPU's that is Triple core, four CPU's that is Quad core and eight CPU's that is Octa core. Processors today are mostly multi-core that helps in enhanced performance, low power consumption and efficient parallel processing of tasks.

AMD have some exceptional releases and equally highly priced as intel and advanced products. It is very hard to say which is better as both are tough competitors.

Intel Pentium is one of the best and most expensive processor available. It remains one of the most popular in today's market. Intel Celeron is a cheaper version of the Intel Pentium 4 and can be found in most of the budget computers.

2. System on Chip(SoC)

SoC (System on Chip or System on a Chip) technology is part of electronic circuits and it connects all the parts of an electronic system (such as a mobile phone or a digital camera). It basically an integrated circuit(IC) or chip. For example, a SoC in a sound detection device may include a sound receiver, a microprocessor, needed memory, input and output logic, etc. These components are included in a chip.

SoC includes a microcontroller, microprocessor or digital signal processor (DSP) core – multiprocessor SoCs having multiple processor core, memory blocks (RAM, ROM, Flash memory, Electrically Erasable Programmable Read-only memory), timing sources, real-time timers and power on reset generators, USB, SPI, USART, Ethernet ports, interfaces including Analog to Digital Converters and Digital to Analog Converters and maybe some voltage regulators and power management circuits. It is like CPU of smart phones.

Examples of system on chip products(companies)-

- Snapdragon Series (Qualcomm)
- Tegra (NVIDIA)
- Apple A series, T series and W series
- Mediatek M series
- Intel

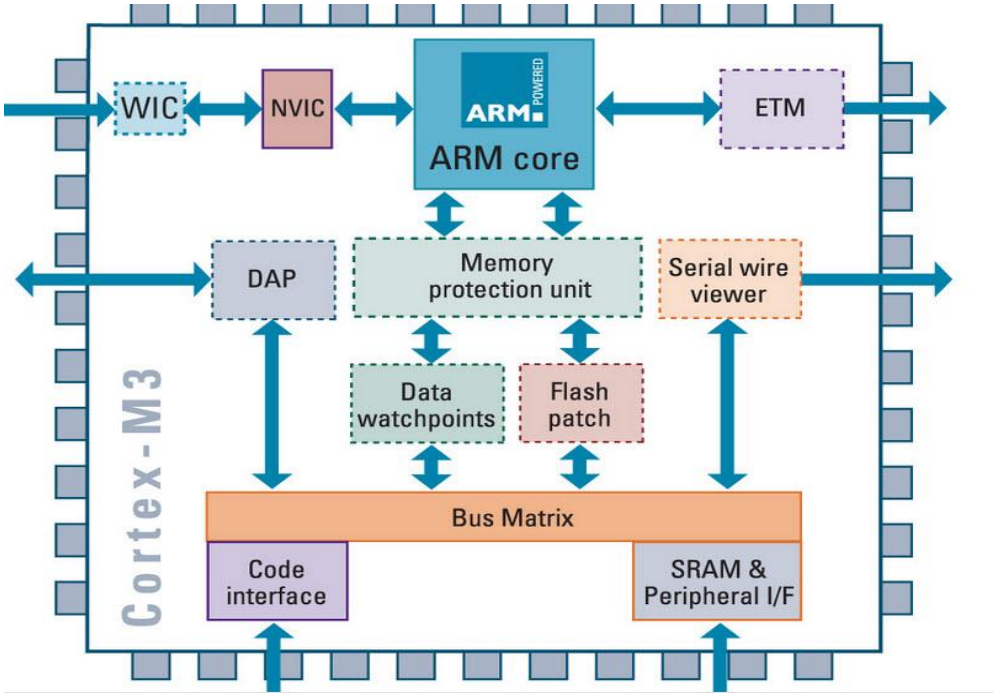
3. System in Package(SiP)

System in Package designs are only implemented when limit of size or performance constraints is reached and our processor demands more because system on chip solutions are very expensive. The higher integration capacity of SiP reduces the number of components in the system and trims the size and routing complexity of the printed circuit board. System in Package design lacks in following areas like similar design infrastructure between semiconductor technologies. Examples of System in Package products is Apple S series.

4. Processor Family

- intel
- AMD
- ARM

We will mainly concentrate on this family of processors because this family of reduced instruction set computing architectures(RISC) has given rise to a totally new type of handheld devices known as smartphones and tablets. It is known for the design of smartphone processors and power-efficient processor designs. In recent years it is used in the products of many prominent electronics companies like Apple A series, Nvidia's Tegra, Samsung's Exynos and Texas Instruments' OMAP products all integrate ARM processors into a system-on-a-chip (SoC).



ARM ARCHITECTURE

4.1 ARM ARCHITECTURE

ARM is famous and is well known for its RISC processors designs. It features in eight different versions of ARM architecture. Full form of ARM is Advanced RISC Machines.

ARM V-SERIES PROCESSORS:

V1

The ARM V1 processor is the first basic processor. ARM founded in November 1990.The ARM V1 processor is developed at Acorn, Cambridge, UK between October 1983 and April 1985.It has fewer than 25,000 transistors. It contains 26-bit addressing and features no coprocessor.

V2

The ARM V2 processor has 32-bit result multiply co-processor (MUL & MLA) and consists of no more than 30,000 transistors. V2(a) is the first ARM processor which contains on chip cache (ARM3).

V3

The ARM V3 processor came with 32-bit addressing, undefined instruction and Abort modes which allows virtual memory. Then a later version V3m featured signed and unsigned long multiply and multiply accumulate instructions.

V4

The ARM V4 is the oldest supported architecture today. It featured load and store instructions for signed and unsigned halfwords and bytes. System mode and privileged mode using user registers. The 26-bit addressing started in V1 was no longer supported in this processor. A subsequent later version V4T featured 16-bit thumb compressed form of instructions.

V5

The ARM V5 comes in three different packages. First the ARM V5T is just a superset of the 4T processor. But it features new instructions like BLX, CLZ and BKPT. Second the V5TE type of processor comes with new signal processing instructions and new multiply instructions for Digital Signal Processor like SMULxy, SMLAxy, SMULWy, SMLAWy, SMLALxy. It also provides math support by Q flag, QADD, QSUB, QDADD, QDSUB. The V5TEJ type processor gives the stimulation of java virtual memory.

V6

The ARM V6 processor provides new multiprocessing instructions for doing byte manipulations and graphics algorithms more efficiently for example LDREX, STREX and features unaligned data handling. It provides 60+ new SIMD instructions namely SMUSD, SMUADX, USAD8.It also comes with security extensions which is a cheaper way to add another dedicated security core. NEON technology introduced in V6 is a 64 and 128-bit hybrid SIMD architecture developed by ARM to stimulate the performance of signal processing applications. The NEON architecture provides 3 times speed to the performance of ARMv5 and 2 times speed to the performance of ARMv6 SIMD.

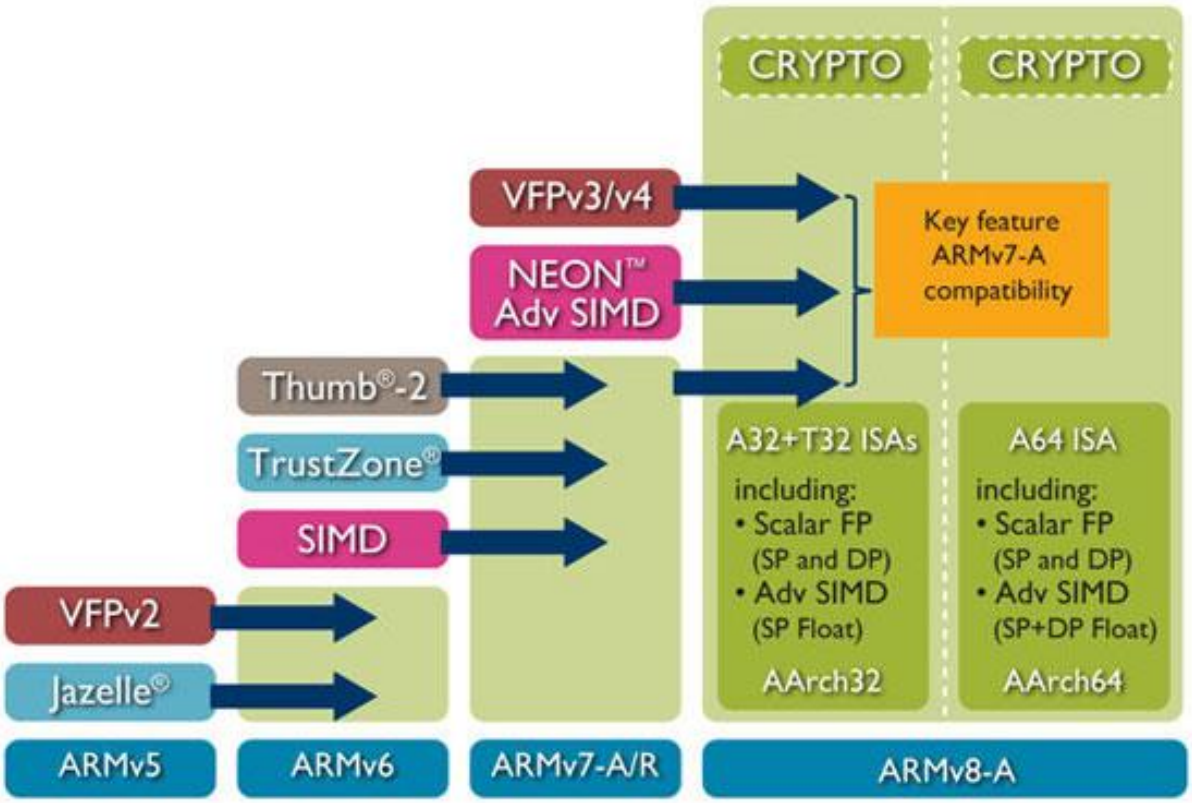
V7

The V7 ARM processor comes in three versions V7A, V7R and V7M. V7A and V7R provides dynamic compiler support and VFP (vector floating point) which helps processor in floating point arithmetic operations and provides execution environment. It features **Jazelle RCT** (Runtime Compiler Target) which provides support for interpreted languages in the processor. Architecture ARMv7 profiles is widely used in Cortex-A5, Cortex-A9, CORTEX R4, CORTEX M3. V7A in CORTEX A5 and A9. V7R in CORTEX R4 and V7M in CORTEX M3.

V8

The latest architecture ARMV8 architecture is the latest architecture launched by the company and it comes in three variants of architecture describing processors and targeting different markets:

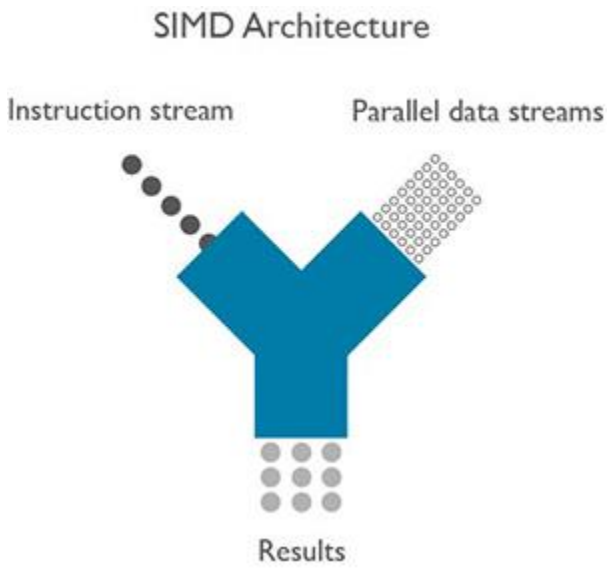
The ARM V8A architecture is the latest generation ARM architecture in the A-profile. It features a 64-bit architecture alongside the well-established 32-bit architecture. The ARM V8R architecture is the latest generation ARM architecture in the R-profile. This architecture features memory structure and a Memory Protection Unit (MPU), and supports the A32 and T32 instruction sets. The ARM V8M architecture is the latest generation ARM architecture in the M-profile. It defines an architecture which aimed at a comparatively cheaper deeply embedded system, where low-latency interrupt processing is vital. It uses a different exception handling model as compared to the other profiles and supports the T32 instruction set.



5. Technologies used in evolving ARM Processors

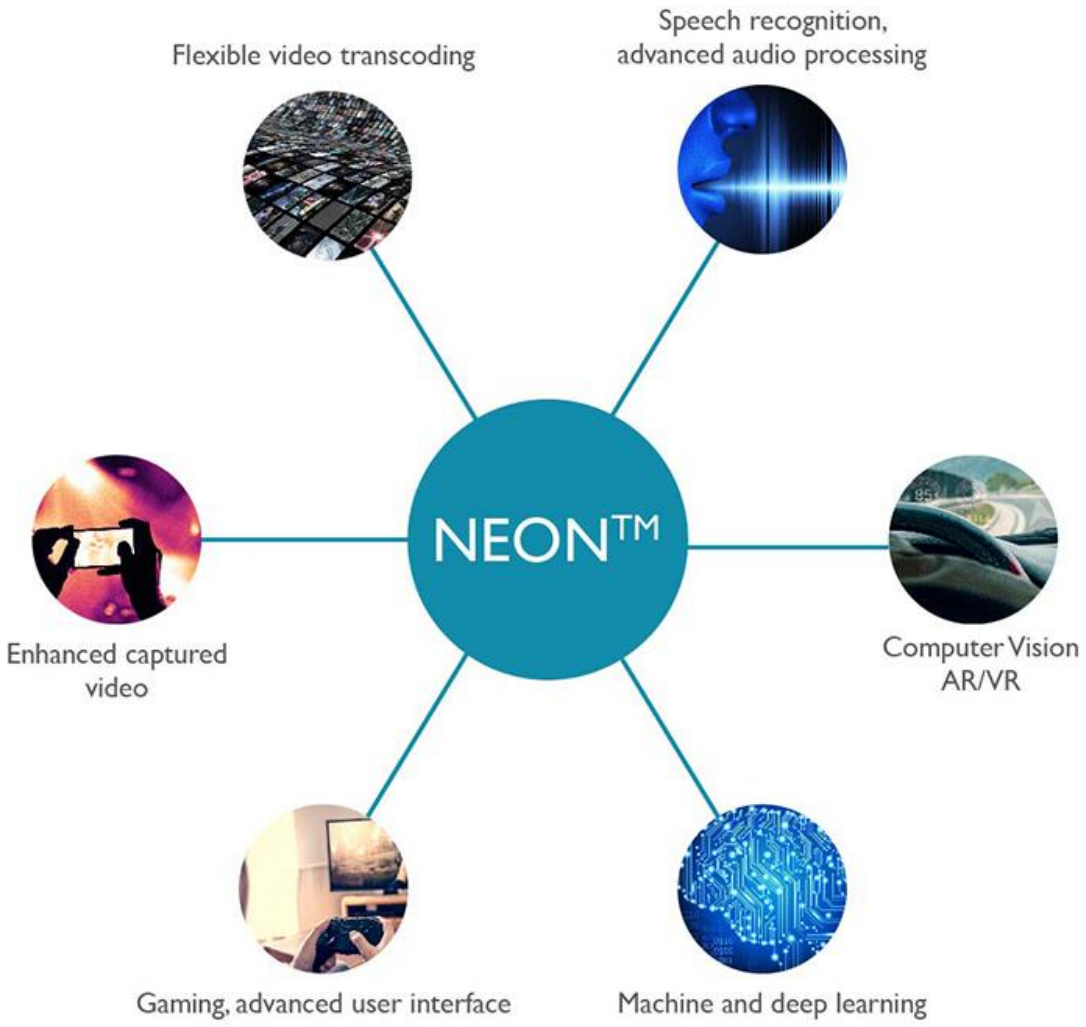
5.1 NEON TECHNOLOGY

This type of technology is used by ARM Cortex-A series and Cortex-R52 processors. It is basically an advanced form of SIMD (single instruction multiple data) architecture. SIMD architecture makes use of data level parallelism. There are parallel computations, but there is only one process (instruction) at a time.



In SIMP architecture when the data is loaded the instruction acts on all the data in one operation. If we have an application where same value is subtracted or added from a large number of points in data like if we want to change the brightness then we need to change the value of each pixel of image and each pixel contains red, blue and green portion of colour in this case SIMP architecture is extremely useful as all the change will be done in a single operation.

Neon technology helps in improving the performance in fields of:



Neon technology supports multiple data types 8-bit/16-bit/32-bit integer data type in V7 A/R and an extra 64 bit in V8 while only 32 bit floating point data type in V7 A/R and an extra 16 bit in V8 A/R. Neon technology is basically a packed form of SIMD architecture. NEON instructions allow up to:

16x8-bit, 8x16-bit, 4x32-bit, 2x64	bit integer operations
8x16-bit, 4x32-bit, 2x64-bit	floating-point operations

5.2 FLOATING POINT TECHNOLOGY

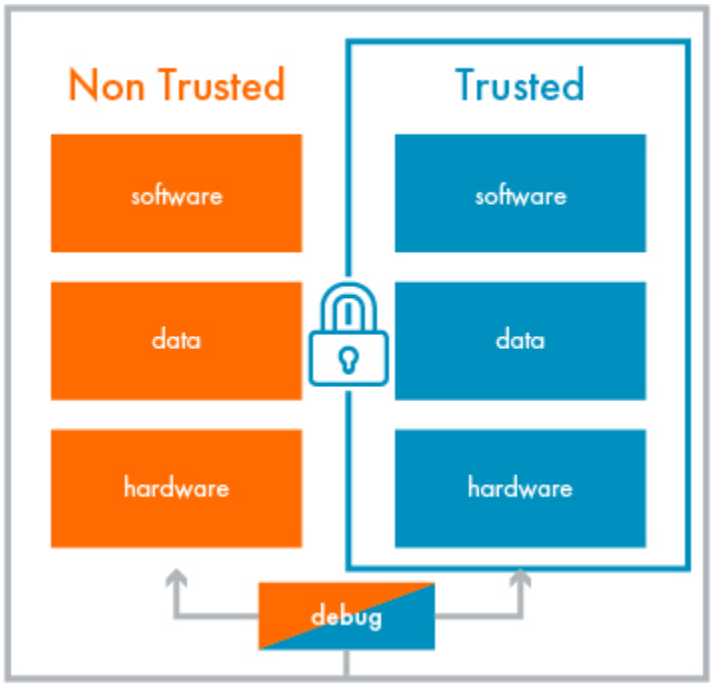
Floating point data type is a type of data type that deals with the fractions and decimals. Floating point unit in processor deals with the addition, subtraction, multiplication, division and other operations done on floating point numbers. Trigonometric and logarithmic operations can be done with help of this unit. This type of unit is required in processor because it is important for a wide range of digital signal processing (DSP) applications. Usage of this only suitable when high accuracy is required. Many applications benefit from the dynamic range and precision of floating-point to deal with large data sets or data sets with unpredictable range.

Applications are :-

- Automotive control applications
    - Powertrain
    - ABS, Traction control & active suspension
- 3D Graphics
    - Digital consumer products
    - Set-top boxes and games consoles
- Imaging
    - Laser printers, still digital cameras, and digital video cameras
- Industrial control systems
    - Motion controls

5.3 TRUSTZONE TECHNOLOGY

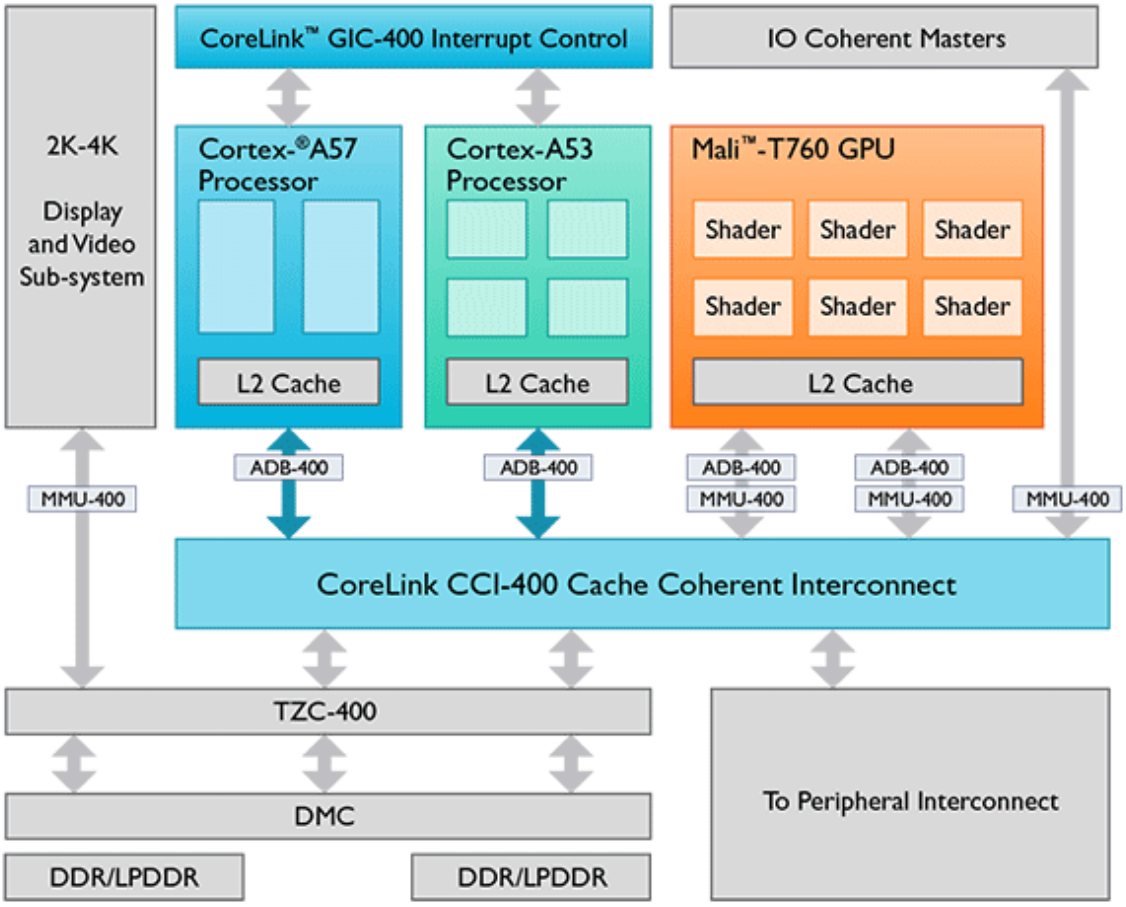
ARM Trust Zone technology is a System on Chip (SoC). It also ensures the security of CPU system wide. This technology can be implemented into ARM Cortex-A and Cortex-M23 and Cortex-M33 based systems. It is used Cortex-A to create a Trusted Execution Environment(TEE) by running a trusted boot and trusted operating system.



Consider on above diagram that there are two different processor families one is protected by Trust Zone technology thus it provides system-wide hardware isolation for trusted software. Thus, one processor family is part of secure world and all applications that run in this secure world are called trusted apps. Only trusted apps can run in secure world with non-secure software blocked from accessing secure resources directly. Inside processors software either resides in the secure world or in the insecure world and a switch between these two worlds is done by a software known as the secure monitor.

5.4 big.LITTLE TECHNOLOGY

This technology is an example of heterogeneous processing architecture as it uses two different processors. The two type of are processors have different function to perform “big” processor takes care of the heavy tasks or in other words they provide maximum compute performance while the other one “LITTLE” processor is designed for maximum power efficiency. Both the parts are logical and consistent and they share the same instruction set architecture (ISA).



Cortex- A57 – “big” Cortex- A53 – “LITTLE”

In smartphones for hardcore gaming a “big” processor is dedicated to give high performance while in case long hours of texting reading we do not require “big” processor as battery life is one of the important issues in today’s world. Hence, “LITTLE” processor is dedicated to save the battery life in periods of low-processing intensity.

5.5 COMPUTE LIBRARY

This technology is just a hub of low level software functions which are optimized for ARM CPU and GPU architectures. It's one of the major feature is its portability which helps developers to recompile CPU functions and hence a code can be transferred between V7 and V8 processor and can compile in both 32/64-bit versions.

When compared to its competitors Compute Library technology has far ahead and far more efficient. As it is a very useful tool that helps in reducing the cost and effort of the developers targeting image processing, computer vision and ML applications. Hence help their product to reach market in time. The compute Library technology has been used widely and utilized by several consumer and mobile silicon vendor to improve their product.

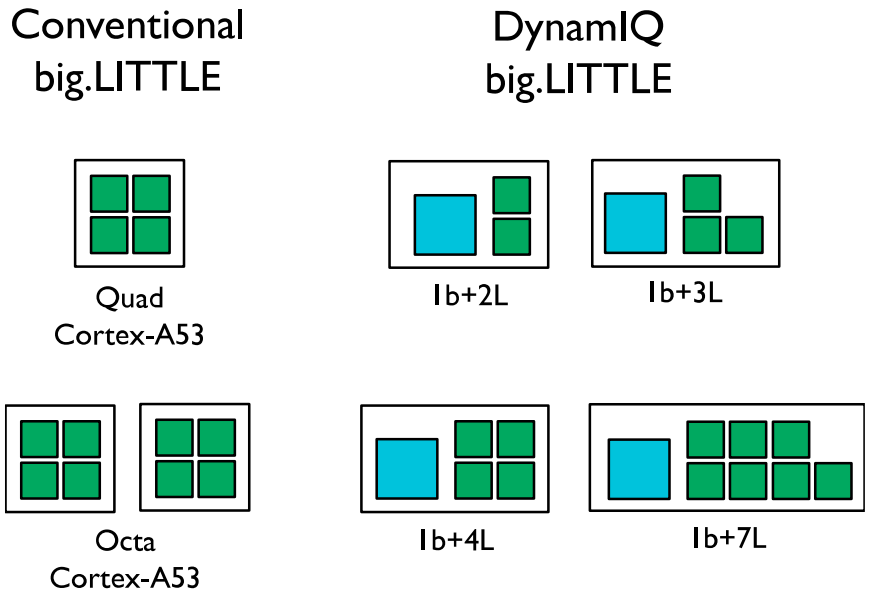
The compute library contains software functions like:

1	Basic arithmetic, mathematical, and binary operator functions
2	Color manipulation (conversion, channel extraction, and more)
3	Convolution filters (Sobel, Gaussian, and more)
4	Canny Edge, Harris corners, optical flow, Pyramids (such as Laplacians)
5	HOG (Histogram of Oriented Gradients)
6	SVM (Support Vector Machines)
7	Convolutional Neural Networks building blocks (Activation, Convolution, fully connected, Locally connected, Normalization, Pooling, Soft-max)
8	H/SGEMM (Half and Single Precision General Matrix Multiply)

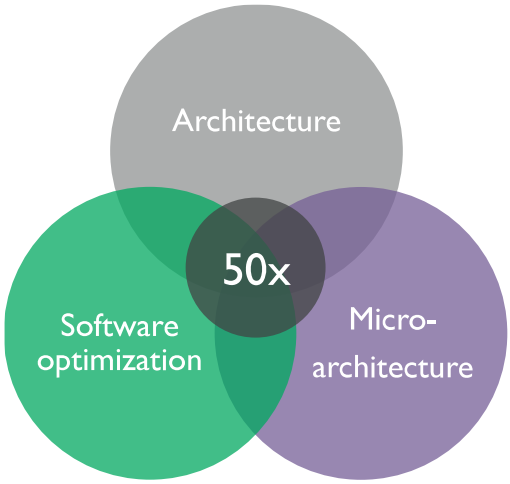
5.6 DynamIQ

In a typical modern big.LITTLE system HMP matches the right tasks to the right processes to maximize efficiency and performance when you need it today big little operates across two cluster of processors connected by a coherent interconnect up to four big or up to four little in each cluster all cores in the cluster are same and each cluster runs under its own shared cache. With all cores running at the same frequency with the same implementation and the same cache sizing. This is an advance form of big.LITTLE designed for the future generation of CPUs and intelligent solutions with architecture, microarchitecture and software optimizations rearchitecting the compute experience.

The next generation of big.LITTLE technology arm Dynamic brings the biggest change in arm multiprocessor cluster design since the introduction of the four core cluster with cortex a75 and cortex a55 arm now supports upto 8 cores in a single cluster but now more importantly the cores can now all be different to each other different microarchitecture different implementations cache configurations and frequencies each core has its own private cache and the cluster has a shared l3 which delivers even more performance and possibilities to optimize designs. The ability to have different CPU's opens a much wider range of possible configurations example two big and four little for mid-range systems or zero big eight little for zero end systems or two big six little for higher end systems all the way up to four big four small for premium offering a very flexible or scalable solution for area efficiency and performance. This enables new more enhanced user experiences with greater privacy and security for intelligent devices from the edge to the cloud. The microarchitecture provides fast dedicated flexibly sized l2 cache close to each core while the shared l3 cache enables simplified and more rapid thread migration between the CPU this low latency interaction results in more performance for the system and option of frequency control of each core combined with scheduler you can more preciously manage power and performance required for each software task. Dynamic technology will enable next level intelligent solutions for smartphones delivering a step change in efficiency performance and safety.



Dynamic technology helps in saving memory by providing a an autonomous CPU memory power solution in which the CPU automatically adapts the memory(local) which depends on the type of application running on the system.In the coming years Dynamic technology will provide 50x boost in AI performance and delivering up to 10x faster response times between CPU and specialized accelerator hardware as compared to the non-dynamic processors.



5.7 Graphics Technologies

Arm Mali is the best selling GPU presently in the world and graphics technologies help in providing increasingly complex graphics within the power capacity and the thermal limits of the mobile devices. Arm Mali technologies include:

5.7.1 Adaptive Scalable Texture Compression (ASTC)

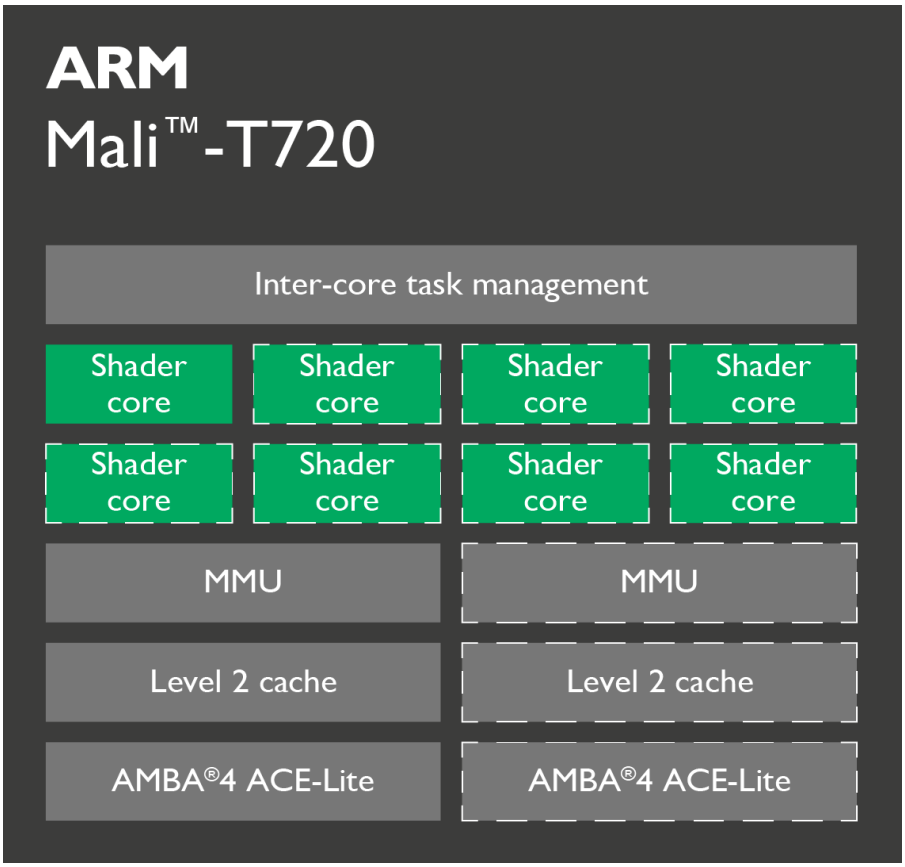
This technology has been developed by ARM and AMD and is considered as the official extension to both the OpenGL and OpenGL ES graphics APIs. Textures are fundamental to way we do graphics today we use geometry to describe what's in the world and where it is the world but we use shaders in combination to textures to make that geometry visible without textures nothing really interesting happens there is a problem though, textures are quite big the reason they provide so much richness they provide to the world we create is that they are full of info lots of bits are needed to store that info both that takes up device memory footprint not big deal on pc but it is a big problem on a mobile but worse they consume bandwidth on your when you are rendering you have to read those bits here memory bandwidths directs directly to power so the amount of power it can consume is substantial portion of the whole device budget so we need to compress them. We require a texture compression system. We use the texture for all sorts of things. We can do many things with textures and individually these things have different texture requirements for texture compression system. For example, if you are using a cube app to store external lighting there is no limit how bright the external light can be so that requires a completely different compression system. Dimensionality there is no use of 3D because there are no formats but 3d textures are interesting if we could find a way to store it in devices. Textures are used for many different things each use has its own compression requirements:

1. Number of Color Components
2. Dynamic Range(LDR vs HDR)
3. Dimensionality (2D vs 3D)

4. Quality which is bit rate

Texture Compression is important because textures are very big as mentioned that is why we use jpg and png coding techniques but what about a compression that hardware can understand so we save memory and time to compress and decompress it every time we pass it to the GPU so it's using all its bandwidth still. Hardware needs complete pure random access to the texture because we have no idea what direction we will be scanning. In case of png, we have to unpack it every time. Texture compress works in the way is that we have blocked so it scans across blocks no matter which direction we are going for scanning. So we unpack just the block we need. We can use the texture coordinate to study which block we are using and then decompress the block into the local cache to get the actual pixel data. Now we need to know the details of the block we need to know dimensions of the block to know which block we are loading. We need to know the block size in memory to skip forward to it. We also need to know how the block is encoded we need to have exact details to how to decode the block. Different codec supports different bit rates and footprints. Different codecs support different color codings.

Last Image is ASTC compressed to 3.56bpp

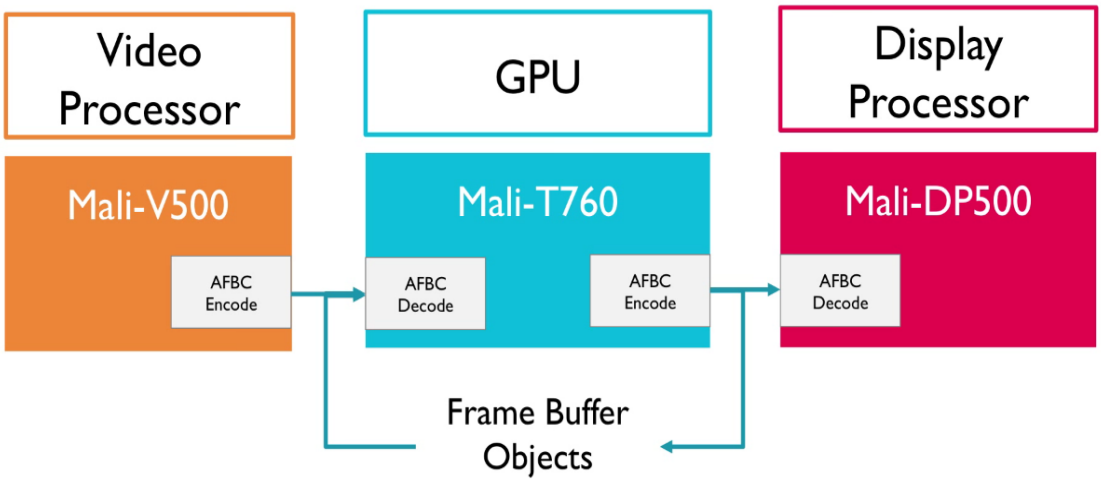


ASTC scales bit rate from 8bpp to 1bpp in fine steps. It has orthogonal choice of base formats like L, LA, RGB, RGBA. It also supports both LDR low dynamic range and HDR high dynamic range pixel formats. It works on both 2D and 3D textures and maintains fine quality. It also supports 1 to 4 color channels, together with modes for uncorrelated channels for use in mask textures and normal maps. ASTC is widely supported by all major hardware vendors and it is free to use. ASTC is developed jointly by ARM and with the help of AMD engineers. ASTC can run in wide number of GPUs for example:

ASTC supports on

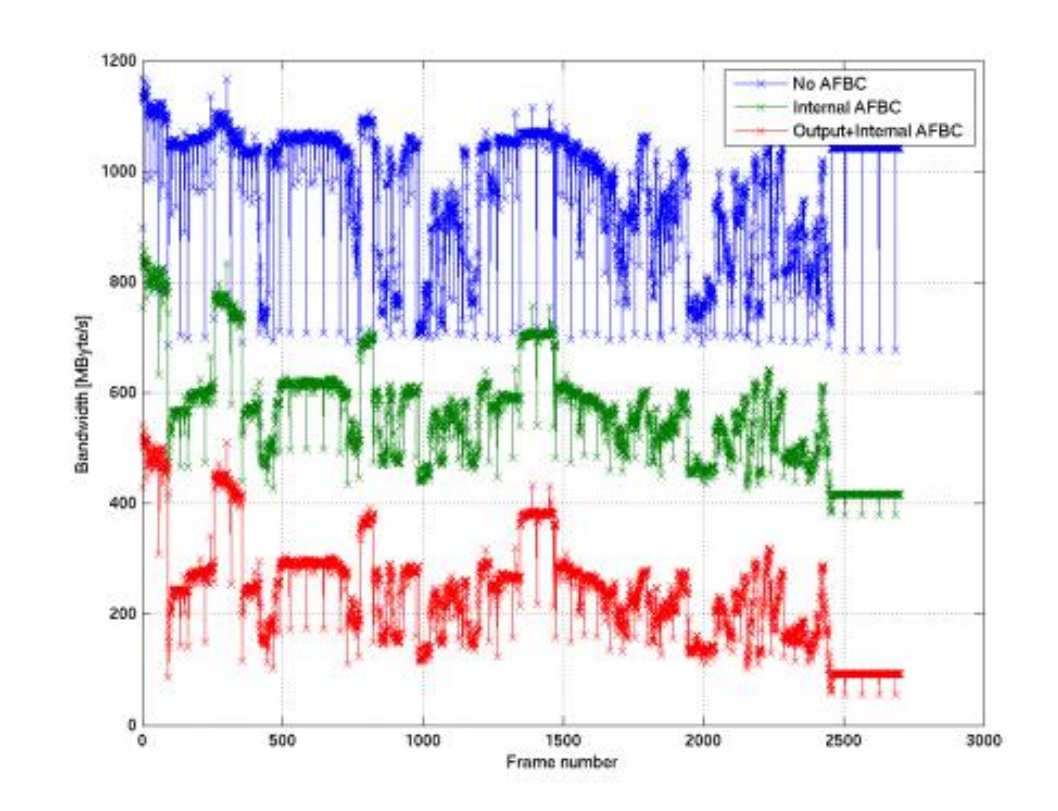
1. 2nd generation Mali-T600 series
2. 2nd generation Mali-T700
3. 2nd generation Mali-T800 series
4. The smaller LDR Profile supports 2D low dynamic range images only.

5.7.2 Arm Frame Buffer Compression (AFBC)



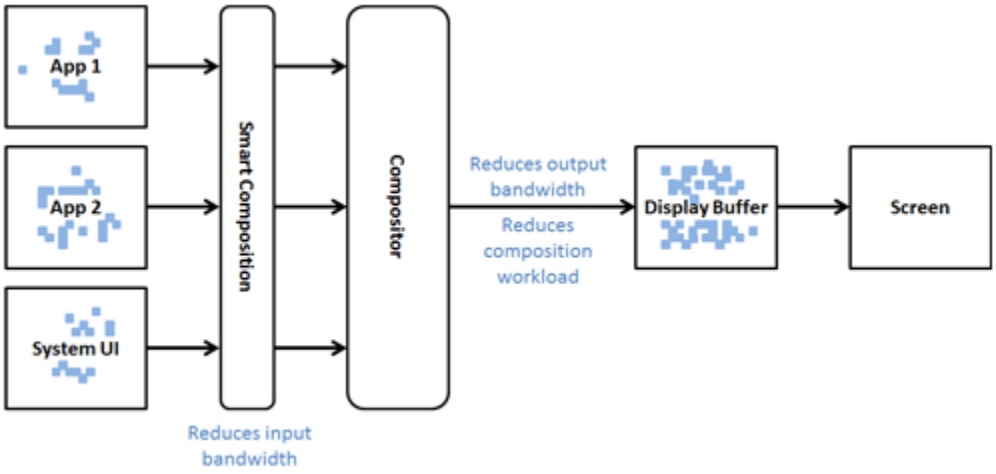
ARM Frame buffer compression helps in reducing system level bandwidth and power cost of transferring spatially coordinated image data by 50% and does not even loses quality compared to other non-compressed forms. It solves the difficulty of using increasingly complex designs within the thermal capacity of the smart handheld devices. One the major problem is post video processing which is most bandwidth intensive. GPU must read the video and apply the effects when one is using video steams as textures in 2D or 3D scenes. By its significant reduction in the bandwidth it helps in power saving by reducing SoC energy consumption.

As shown in the above diagram the video streams from the Video Processor are AFBC encoded and is unpacked at GPU which then encodes and passes on to the Display Processor thus it is transported as AFBC encoded thus helps in reducing the bandwidth and power consumption. The Display reads it without decoding and only decodes when moving to display memory. One of its features is AFBC do uses any area and is added at zero area cost. AFBC thus minimizes the amount of data to be transferred between the IP blocks within a SoC. AFBC protocol supports both YUV and RGB formats where in YUV the compression ratio is about 50%.



The above image is an example of a Arm Frame Buffer Compression protocol applied on a 4K H.264 video stream. As shown in the image the blue parts or the top most part corresponds to the bandwidth from 800MBytes to about 1200MBytes the higher rates if bandwidth is needed as it is not AFBC coded. While the middle part or the green part falls in the bandwidth region from around 400Mbytes to 800Mbytes. This sample is only internally AFBC coded. Its actually shows the bandwidth of Mali V500 which only uses AFBC for internal reference frame compression. While the red part or the lowermost part bandwidth ranges from 50Mbytes to 500Mbytes which is quite less than the above two cases. The red part sample shows the bandwidth which is both internally and externally AFBC coded with a AFBC enabled display processor. The power saving however also depends on the memory system and on the SoC but power consumption is most commonly of the order 150mW per GByte/s in mobile systems. Considering the battery life of the handheld devices this worthwhile. As demand of high battery life among these in increasing in market ASBC provides a better option as compared to other non-ASBC devices.

5.7.3 Smart Composition



This feature also help in reducing bandwidth while reading in textures during frame composition. Smart Composition can reduce the standard Android User texture read bandwidth by greater than 50%. As shown in the diagram before giving frames for final frame composition to the compositor the Smart Composition determines whether there is need to keep the portion of the frame and the kept or composited portion can be reused.

5.7.4 Transaction Elimination

Transaction Elimination is also a type of bandwidth saving feature but is a key feature among all to save bandwidth thus power. It is a key bandwidth saving feature of ARM Mali and thus allows significant power saving on System on Chip level. The best part of transaction Elimination is that there is no change or compromise to image quality. Transaction Elimination works in a way in which it compares present frame with previous frames and thus performs only partial update only to particular parts of the frame and hence saving the amount of data to be transferred per frame. It has 16*16 pixels tile size and per tile comparison between frame buffers. Transaction Elimination is very useful for mobile games 1st person shooting games for saving bandwidth. Transaction elimination can be used in almost every irrespective of the GPU.

6.Processors and Benchmarks

6.1 Linpack Benchmark

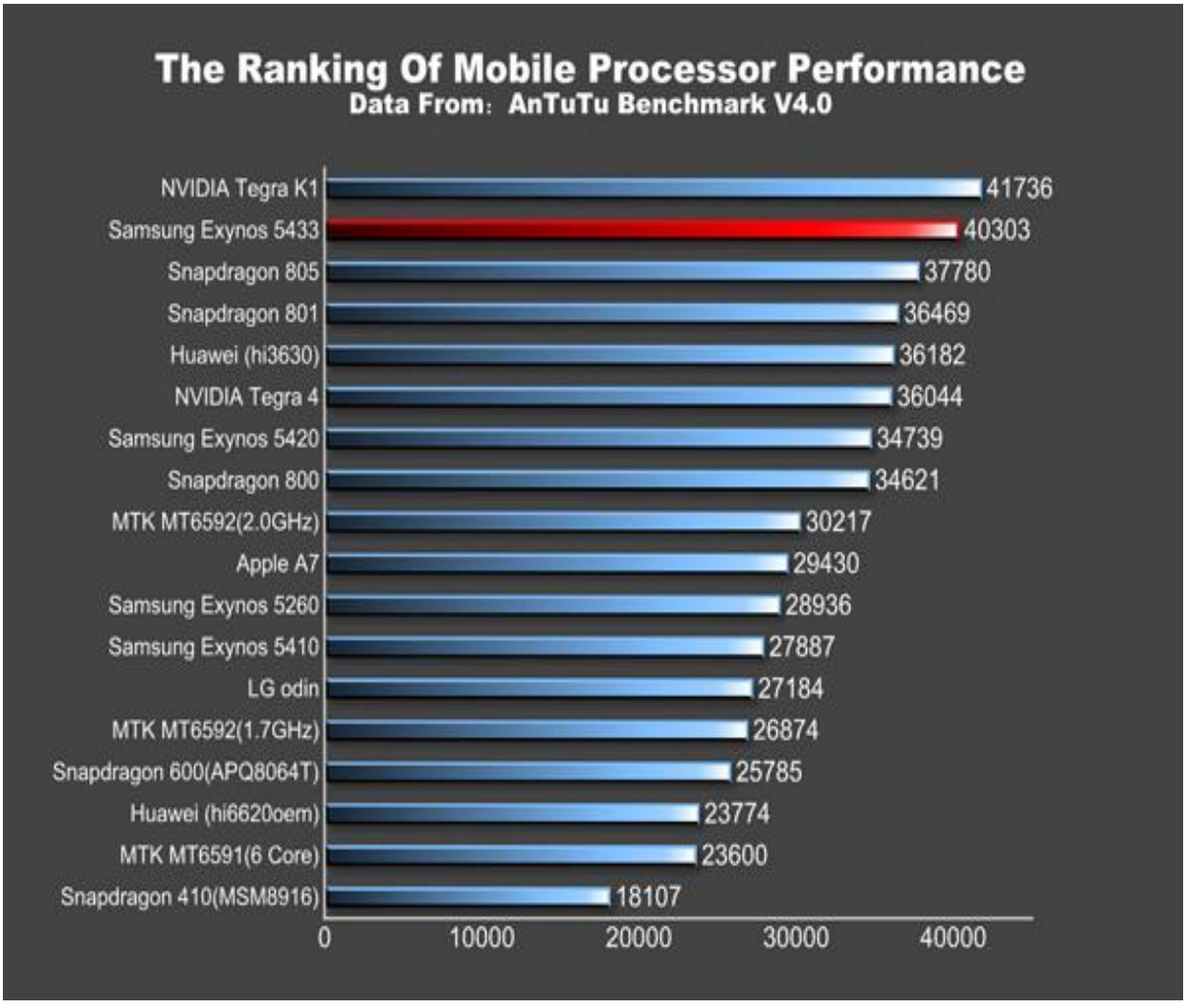
Linkpac Benchmark works on how fast your Andriod device or your processor can solve a dense n by n system of linear equation. It is basically measure of systems floating point computing power introduced by Jack Dongarra. Basically this determines by solving a system of linear equation gives idea about how fast the processor will perform will solving the real life problems. As we know peak performance is the maximum theoretical performance that a computer can acheieve but the actual or real performance will always be less than the peak performance. The performance is calculated in machine's frequency, cycles per second.

Double Precision and Single Precision (SP) 100x100

CPU	MHz	Android	v7/v5 DP MFLOPS	v5 DP MFLOPS
ARM 926EJ	800	2.2	5.7	5.6
ARM v7-A8	800	2.3.5	80.2	
ARM v7-A9	800	2.3.4	101.4	10.6
ARM v7-A5	1500 C1	4.4.2	121.5	
ARM v7-A9	1300a	4.1.2	151.1	17.1
ARM v7-A9	1500	4.0.3	171.4	
ARM v7-A9	1500a	4.0.3	155.5	16.9
Atom Z3745C	1866	4.4.2	168.2	59.4
ARM v7-A9	1400	4.0.4	184.4	19.9
ARM v7-A9	1600	4.0.3	196.5	
QUAL-S4	1500	4.0.3	254.9	
Atom Z3745D	1866	4.4.2	282.3	
Atom Z3745I	1866	4.4.2	362.6	
QUAL-800	2150	4.4.3	389.5	35.4
ARM v7-A15	2000b	4.2.2	459.2	28.8
QUAL-800I	2150	4.4.3	629.9	
ARM v7-A15I	2000b	4.2.2	826.4	
ARM v8-A53	1300	5.0.2		21.4

6.2 AnTuTu Benchmark

AnTuTu Benchmark covers almost all the aspects and is all in one benchmark it runs test on CPU, GPU, memory and storage. Unlike the Linpack benchmark it run tests and evaluates both the integer and also the floating point performance of the computer. Multiplications, Divisions, and other calculative tests run to determine the CPU performance. For determining the performance of GPU it runs test on 2D and 3D performance of computer. Its memory test runs test on the memory bandwidth and latency. While the storage test run test on the speed to read write on the device's flash memory.



AnTuTu Benchmark Scores till sept 17

Device	CPU	UX	3D	Total Score
1 iPhone 8 Plus	51240	74817	76133	217210
2 iPhone 8	62740	71027	60149	209113
3 OnePlus 5	39207	57362	73614	181088
4 HTC U11	38651	57309	73282	179961
5 nubia Z17	37406	55440	73016	176441
6 Samsung Galaxy Note 8（N950F）	37976	53339	72874	174559
7 Samsung Galaxy Note 8（N950U）	37464	53988	71731	173716
8 Mi 6	36527	54232	71502	172740
9 Samsung Galaxy S8（G950N）	38166	51335	72105	171946
10 Samsung Galaxy S8+（G9550）	37191	52964	70001	170793
11 Sony Xperia XZ Premium	36358	53215	69326	169329
12 iPhone 7 Plus	47869	54523	53551	168481

iPhone 8 tops the list in case of smartphone processor performance

6.3 CF-BENCH

This is also one of the all in one benchmarks created by Android developer Chainfire. They created this first for their personal use and then it was released in the public. It basically runs test on CPU memory and storage. While unlike the others it provides repeatable, consistent scores while test both native and java code performance.

Overclocked Benchmarks

Device	Native	Java	Overall
Samsung Galaxy S2 (I9100) **@ 2x1600mhz, Android 2.3.4**	**100626**	**90404**	**94492**
Motorola Atrix 4G (Olympus) @ 2x1450mhz, Android 2.3.4	**94020**	**83738**	**87850**
Samsung Galaxy Tab (P1000) @ 1x1400mhz, Android 2.3.7	**81764**	**78282**	**79674**
HTC Sensation (Pyramid) @ 2x1782mhz, Android 2.3.4	**55829**	**44996**	**49329**
HTC Evo 3D CDMA (Shooter) @ 2x2050mhz, Android 2.3.3	**49345**	**41717**	**44768**
HTC Evo 3D GSM (ShooterU) @ 2x1188mhz, Android 2.3.4	**26861**	**23806**	**25028**
LG Optimus 2X (Star, G2X) @ 2x1000mhz, Android 2.3.7	**41472**	**2252**	**17940**
Samsung Galaxy S3 (I9300) @ 4x1800mhz, Android 4.0.4	**31557**	**8146**	**17510**
HTC One X (EndeavorU) @ 4x1700mhz, Android 4.0.3	**27303**	**6787**	**14993**
HTC Incredible @ 4x1500mhz, Android 4.0.4	**26004**	**7293**	**14777**
Samsung Galaxy Note (N7000) @ 2x1400mhz, Android 2.3.6	**29092**	**4502**	**14338**
Motorola Xoom @ 2x1704mhz, Android 3.2	**16323**	**4876**	**9454**

Here overclocking means basically increasing the clock speed by changing the voltage and multiplier in order to get every bit of performance you possibly can out of your CPU. Stock speed is the normal processing speed optimized your provided by your computer without any outside hinderance.

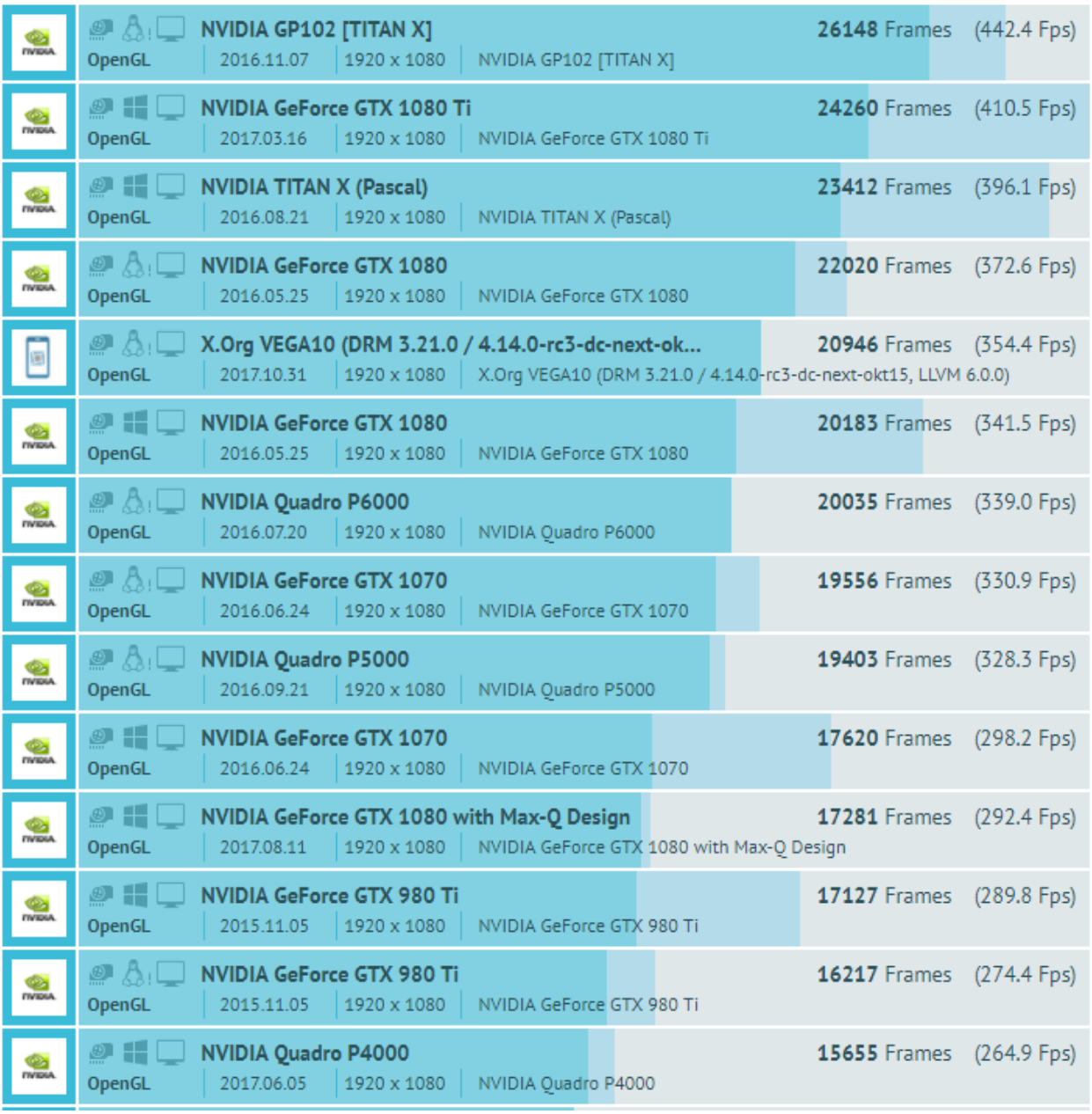
Clocked benchmarks

Device	Native	Java	Overall
Samsung Galaxy S2 (I9100) 2x1200mhz, Android 2.3.3	**194482**	**10073**	**83836**
Motorola Atrix 4G @ 2x1000mhz, Android 2.3.7	**63890**	**57587**	**60108**
Samsung Galaxy Tab (P1000) @ 1x1000mhz, Android 2.3.3	**42170**	**39837**	**40770**
HTC Evo 3D CDMA (Shooter) @ 2x1188mhz, Android 2.3.4	**38333**	**32905**	**35076**
HTC Sensation (Pyramid) @ 2x1188mhz, Android 2.3.4	**36879**	**30630**	**33129**
HTC Evo 3D GSM @ 2x1188mhz, Android 2.3.4	**26861**	**23806**	**25028**
LG Optimus 2X (Star, G2X) @ 2x1000mhz, Android 2.3.7	**41472**	**2252**	**17940**
HTC One X @ 4x1500mhz, Android 4.0.4	**25423**	**6970**	**14351**
Samsung Galaxy S3 (I9300) @ 4x1704mhz, Android 4.0.4	**25483**	**6715**	**14222**
Motorola Xoom @ 2x1000mhz, Android 3.1	**25154**	**3707**	**8285**
Asus EeePad Transformer @ 2x1000mhz, Android 3.1	**15108**	**3523**	**8157**
Samsung Galaxy Note (N7000) @ 2x1400mhz, Android 4.0.3	**13269**	**4410**	**7953**

6.4 GLBenchmark

GL Benchmark basically focus only on the GPU part and its performance which contains 33 diiferent test which run on device to test its abilty to handle ability to handle texture-based and direct lighting, bump, environment and radiance mapping, soft shadows, and vertex shader-based skinning. The best feature is that GLBenchmark let you run off screen test that helps you to avoid any Vsync limitation of your screen.

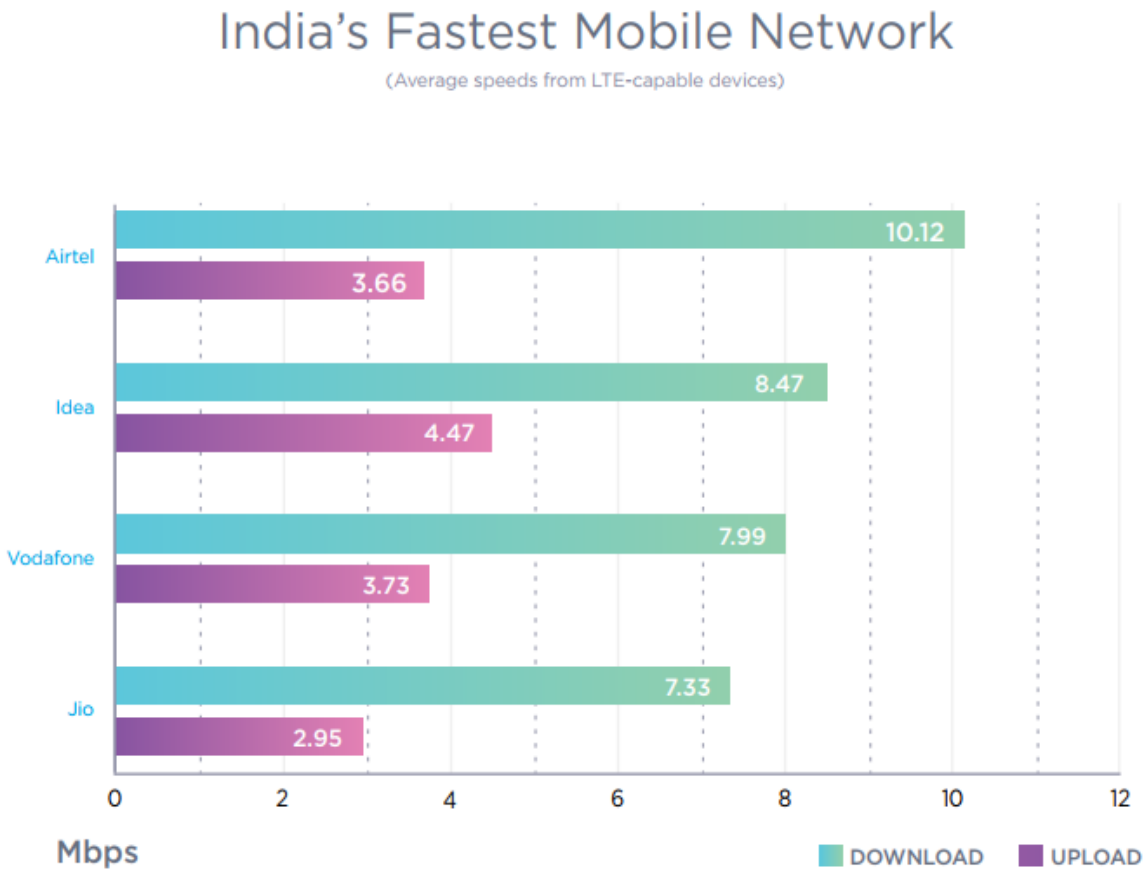
GLBenchmark Scores



6.5 Ookla speedtest.net

This basically measures the internet speed provided by your mobile device internet connection. Its results have revealed high differences in the speed while comparing 3G network to a 4G network.

Benchmarks for 2017 India's Fastest Mobile Network



Airtel tops the list with highest downloading speed of 10.12 Mbps. The speeds recorded in above benchmark score is the average internet speed of all the users so it may vary from place to place region to region on the availability of 3G/4G network.

7. All About Best Processors

7.1 Qualcomm Snapdragon 835

Main features:

1. **Battery life:** Battery life being one of the major issues and feature demanded by the users in current time. As claimed by Qualcomm the new snapdragon 835 uses 25% less battery as compared to its previous and competitive versions. Effect can be seen in new model of iphone X coming with two battery attached inside smartphones.

2. **Quickcharge 4.0 :** Quickcharge one of the step to help sustain battery of smartphones is a key feature consumer look in smartphones in todays world. Quickcharge 4.0 as compared to previous version Quickcharge 3.0 is 25% faster and it also sustains 25% more battery life.

3. **Performance:** Qualcomm is using updated and more efficient version of its Kyro CPU 280. It is a octa core processor eight CPU cores working together to give out the best performance. It is based on Arm's big.LITTLE design where work is divided according to the complexity of application being run by the user. Games and heavy applications run on big while less complex applications run on little CPU.

4. **Faster networks:** One of the best feature of the Qualcomm Snapdragon 835 is X16 LTE speed. This enables us to use 4 gigabyte 4G connection this feature currently might not be available on other processors anywhere in the world. This helps users to get high speed 4G network enabled on there phones.

5. **Audio and Video:** Camera is improved with auto video stablisation feature while audio now supports 32-bit, 384KHz audio DACs. Its secured with the new iris recognition technology.

7.2 Tegra X1 chip:

Main features:

1. Performance (CPUs)

The tegra X1 uses ARM V8(64 bit) processing cores. Made by one of the leading GPU manufacturing company the tegra X1 uses V8 instead of its previous models using the Denver CPU cores because V8 enables to use wide number of transistor as compared to Denver CPU cores and also helps maintaining the temperature of the device. Thus more processing under the thermal limit of the hardware. Also Nvidia wanted to move to 20nm smaller models but Denver CPUs were technically not ready for it. The CPU is octacore with 4 by 4 big.LITTLE system. 4 CPUs for big while 4 CPUs dedicated to LITTLE. Its uses Cortex A57 for the big ones while the Cortex A53 for the LITTLE ones.

2. GPU

Nvidia has brought its Tegra X1 to a whole different level in world of gaming, video processing. It has not implemented its desktop GPU version but is far better as compared to its previous models. Its uses 256 CUDA cores, two geometry units, 16 texture units, 16 ROPs and has massive development in memory bandwidth with 25.6GBps speed.

REFERENCES

- https://developer.arm.com/products/processors/classic-processors
- https://en.wikipedia.org
- https://kb.wisc.edu/showroom/page.php?id=4927
- http://www.diit.unict.it/users/gascia/COURSES/sist_emb_14_15/download/SE15_ARM_Processors_and_Architectures
- https://developer.arm.com/products/architecture
- https://www.qualcomm.com/products/platforms/snapdragon-800-series-comparison
- https://www.androidpit.com/fastest-smartphone-processors
- https://en.wikipedia.org/wiki/List_of_Qualcomm_Snapdragon_systems-on-chip
- https://www.notebookcheck.net/Smartphone-Processors-Benchmark-List.149513.0.html
- http://www.trustedreviews.com/news/snapdragon-835-phones-processor-specs-speed-benchmark-chipset-cores-2944086
- https://www.pcworld.com/article/255977/how_to_benchmark_your_android_device.html
- https://shield.nvidia.com/blog/tegra-x1-processor-and-shield
- www.nvidia.com › NVIDIA Home › Products › Tegra Mobile Processors