ENPM607 – Digital Computer Architecture | Project – 2

Due: December 18th, 2018 11:59 PM (EST)

Shubham Deshkar | UID: 115484689

INTRODUCTION:

The project is about simulating the behavior of MMU for ARM Cortex A-53 CPU. Many of the behaviors and functionality was implemented in this project.

BEHAVIOUR:

* Two L1 caches are implemented. One for data and one for instruction. The capacity of these caches is 8K Bytes.
* One large size L2 cache is implemented of size 128K Bytes.
* For address translation two micro-TLBs are involved, one for data one for instructions. Then a next level TLB is used as a Unified TLB in case the micro TLBs miss to convert the virtual address from the process to a physical address.
* The Unified TLB is implemented and initialized in a way that tags missed by micro-TLB are always found in Unified TLB. Hence the possibility of page fault is eliminated.
* Also, all the physical addresses not found in any of the hierarchical structure will always be found in the disk.
* An update function is used to simulate write through policy when a miss occurs.
* All the clocks cycles are meticulously counted and the information of number of clock cycles traversed, number of misses and number of hits are displayed at the end of the program.
* Note that a virtual program is written in the form of address only to easily simulate the system.
* The code is written in Java and hence a proper Java SDK configure IDE is required to test the system otherwise the code will be found in the src folder.
* The system exclusively reads from the text files as its inputs and initializes the memory objects using it as a page table.
* Also, at the end an updated page table for each memory object is also displayed so as to check if the write through policy has worked perfectly or not.
* The code is also ridden with a lot of comments to clarify the objective of the system
* The system/simulator excessively dumps the control of the system on the console, so it is known how each of the virtual address is converted into physical address and where was it found and where the miss occurred or hit occurred. Plenty of such information is dumped on the console output to experience the simulation of the MMU in the CPU.
* One such example is given below.

initialized disk memory with 1048576000 Bytes of memory

Main Memory initialized with 1048576 Bytes of memory

initialized L2 cache with 131072 Bytes of memory

TLB initialized with 512 entries

initialized L1 cache with 8192 Bytes of memory

initialized L1 cache with 8192 Bytes of memory

TLB initialized with 10 entries

TLB initialized with 10 entries

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PC: 15

TLB received: 10101010

TLB tag: 1010 1010 found!

pageAdd: 1259 offset: 1010

TLB HIT

physical address generated from micro-TLB: 12591010

PC: 25

TLB received: 23451001

TLB tag: 2345 2345 found!

pageAdd: aa01 offset: 1001

physical address generated from micro-TLB: aa011001

TLB HIT

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\*\*DATA\*\*

L1 phys: 12591010

L1 CACHE HIT!

Data found: 1010

\*\*INST\*\*

L1 phys: aa011001

L1 CACHE HIT!

Instruction found: 1001

PC: 35

TLB received: 15902307

TLB tag: 1590 1590 not found in TLB

TLBdata MISS!

TLB received: 15902307

TLB tag: 1590 1590 found!

pageAdd: 1100 offset: 2307

physical address from level2 TLB: 11002307

PC: 45

TLB received: 1f0152c3

TLB tag: 1f01 1f01 found!

pageAdd: c6f9 offset: 52c3

physical address generated from micro-TLB: c6f952c3

TLB HIT

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\*\*DATA\*\*

L1 phys: 11002307

L1 CACHE MISS!

L2 phys: 11002307

L2 CACHE MISS!

mainMem. phys: 11002307

mainMem. MISS!

disk phys: 11002307

DISK HIT!

Data found: 2307

\*\*INST\*\*

L1 phys: c6f952c3

L1 CACHE MISS!

L2 phys: c6f952c3

L2 CACHE MISS!

mainMem. phys: c6f952c3

mainMem. MISS!

disk phys: c6f952c3

DISK HIT!

Instruction found: 52c3

PC: 55

TLB received: 1f325911

TLB tag: 1f32 1f32 found!

pageAdd: defa offset: 5911

TLB HIT

physical address generated from micro-TLB: defa5911

PC: 65

TLB received: 10111101

TLB tag: 1011 1011 not found in TLB

TLBdata MISS!

TLB received: 10111101

TLB tag: 1011 1011 found!

pageAdd: 1a0b offset: 1101

physical address from level2 TLB: 436932865

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\*\*DATA\*\*

L1 phys: defa5911

L1 CACHE HIT!

Data found: 5911

\*\*INST\*\*

L1 phys: 1a0b1101

L1 CACHE MISS!

L2 phys: 1a0b1101

L2 CACHE HIT!

Instruction found: 1101

PC: 75

TLB received: 12345679

TLB tag: 1234 1234 found!

pageAdd: 270c offset: 5679

TLB HIT

physical address generated from micro-TLB: 270c5679

PC: 85

TLB received: 1765a201

TLB tag: 1765 1765 found!

pageAdd: c990 offset: a201

physical address generated from micro-TLB: c990a201

TLB HIT

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\*\*DATA\*\*

L1 phys: 270c5679

L1 CACHE MISS!

L2 phys: 270c5679

L2 CACHE MISS!

mainMem. phys: 270c5679

mainMem. HIT!

Data found: 5679

\*\*INST\*\*

L1 phys: c990a201

L1 CACHE HIT!

Instruction found: a201

PC: 95

TLB received: 27071995

TLB tag: 2707 2707 not found in TLB

TLBdata MISS!

TLB received: 27071995

TLB tag: 2707 2707 found!

pageAdd: 10cb offset: 1995

physical address from level2 TLB: 10cb1995

PC: a5

TLB received: 23071995

TLB tag: 2307 2307 found!

pageAdd: 9991 offset: 1995

physical address generated from micro-TLB: 99911995

TLB HIT

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\*\*DATA\*\*

L1 phys: 10cb1995

L1 CACHE MISS!

L2 phys: 10cb1995

L2 CACHE HIT!

Data found: 1995

\*\*INST\*\*

L1 phys: 99911995

L1 CACHE MISS!

L2 phys: 99911995

L2 CACHE MISS!

mainMem. phys: 99911995

mainMem. HIT!

Instruction found: 1995

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CLKs: 200488

HITs: 17

MISS: 15

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Printing Updated page tables/memories of:

microTLB data

1234 270c

1010 1259

1f32 defa

1100 2307

10cb 1995

microTLB inst

2307 9991

2345 aa01

1f01 c6f9

1765 c990

1a0b 1101

L1 cache data

1259 1010

defa 5911

1100 2307

defa 5911

270c 5679

10cb 1995

L1 cache inst

aa01 1001

c990 a201

c6f9 52c3

9991 1995

L2 cache

1a0b 1101

10cb 1995

1100 2307

c6f9 52c3

270c 5679

9991 1995

main memory

270c 5679

9991 1995

1100 2307

c6f9 52c3

Process finished with exit code 0

* There are several text files in the submission which are used as input file for initializing the page tables of the structures.