

## COA Lab

**Name – Mohit Jaiswal**

**Class – A**

**Batch – A3**

**Roll No. – 57**

**PRN No. - 202101040048**

**Practical 08** - Design Program using Control Transfer instruction using CPU simulator.

### **Multiplication using Successive Addition Method**

$$6 * 5 = 30$$

Final Result = 78

# CPU Simulator Screenshot:-

The screenshot displays the CPU Simulator interface, which includes several panels for managing and monitoring the simulation.

**CPU INSTRUCTIONS IN MEMORY (RAM)**

PAdd	LAdd	Instruction	Base
0500	0000	IN 0, R00	0500
0506	0006	IN 0, R01	0500
0512	0012	SUB #48, R00	0500
0518	0018	SUB #48, R01	0500
0524	0024	MOV #0, R03	0500
0530	0030	ADD R00, R03	0500
0535	0035	DEC R01	0500
0538	0038	CMP #0, R01	0500
0544	0044	JNZ 30	0500
0548	0048	OUT R03, 1	0500
0554	0054	HLT	0500

**SPECIAL CPU REGISTERS**

Register	Value
PC	55
SR	1
SP	8164
BR	500
SR Status Flag	
OV	<input type="checkbox"/>
Z	<input checked="" type="checkbox"/>
N	<input type="checkbox"/>
CPU Mode	User
IR	HLT
MAR	554
MDR	HLT

**GENERAL PURPOSE CPU REGISTERS**

Reg	Val (D)	C	Val (D)
R00	6		
R01	0		
R02	0		
R03	30		
R04	0		
R05	0		
R06	0		
R07	0		
R08	0		
R09	0		
R10	0		
R11	0		
R12	0		
R13	0		
R14	0		
R15	0		
R16	0		
R17	0		
R18	0		
R19	0		
R20	0		
R21	0		
R22	0		
R23	0		
R24	0		
R25	0		
R26	0		

**PROGRAM STACK (RAM)**

Pos	Val (D)	Addr
33	6	0000
32	32	0000
31	0	0000
30	0	0000
29	0	0000
28	0	0000
27	0	0000
26	0	0000
25	0	0000
24	0	0000
23	0	0000
22	0	0000

**Program Control**

STEP: ☒ by instruction, ☐ by single tick

RUN: Fast | Slow

STOP: Fast | Slow

RESET PROGRAM

SHOW PCB...

**Advanced**

COMPILER... OS 0...

INPUT OUTPUT... VIRTUAL OS...

INTERRUPTS...

**Registers**

Reg Value: 0 CHANGE RESET ALL

Show Reg Access Status: ☐

Select Register Set Size: 32