INVITED PAPER

Multilevel Converters: An Enabling Technology for High-Power Applications

Multilevel converters generate voltage and current waveforms of improved quality, that can be used to power drives for trains and other vehicles, and many other applications.

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ABSTRACT | Multilevel converters are considered today as the state-of-the-art power-conversion systems for high-power and power-quality demanding applications. This paper presents a tutorial on this technology, covering the operating principle and the different power circuit topologies, modulation methods, technical issues and industry applications. Special attention is given to established technology already found in industry with more in-depth and self-contained information, while recent advances and state-of-the-art contributions are addressed with useful references. This paper serves as an introduction to the subject for the not-familiarized reader, as well as an update or reference for academics and practicing engineers working in the field of industrial and power electronics.

KEYWORDS | High-power applications; multilevel converters; power electronics; power quality

Manuscript received March 12, 2009; revised May 1, 2009. First published October 21, 2009; current version published October 28, 2009. This work was supported by the Chilean National Fund of Scientific and Technological Development under Grant 1080582, by the Spanish Science and Technology Ministry and the Spanish Science and Education Ministry under projects DPI2001-3089 and TEC2006-03863, and by the Universidad Técnica Federico Santa María.

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Digital Object Identifier: 10.1109/JPROC.2009.2030235

I. INTRODUCTION

Power converters are an enabling technology for industrial processes powered by electric drive systems. They are potentially useful for a wide range of applications: transport (train traction, ship propulsion, and automotive applications), energy conversion, manufacturing, mining, and petrochemical, to name a few. Many of these processes have been continuously increasing their demand of power to reach higher production rates, cost reduction (large-scale economy), and efficiency. The power electronics research community and industry have reacted to this demand in two different ways: developing semiconductor technology to reach higher nominal voltages and currents (currently 8 kV and 6 kA) [1]–[3] while maintaining traditional converter topologies (mainly two-level voltage and current source converters); and by developing new converter topologies, with traditional semiconductor technology, known as multilevel converters [4]–[9]. The first approach inherited the benefit of wel-known circuit structures and control methods. However, the newer semiconductors are more expensive, and by going higher in power, other power-quality requirements have to be fulfilled, introducing the need of power filters. The second approach uses the well-known and cheaper semiconductors, but the more complex circuit structures came along with several challenges for implementation and control. Nevertheless, these challenges turned rapidly into new opportunities, since the more complex circuit structures enabled more control degrees of freedom that could be used to improve power conversion in several aspects, especially

in relation to power quality and efficiency. This fact has boosted multilevel converter development during the last two decades, with a continuous evolution.

Multilevel converters are currently considered as one of the industrial solutions for high dynamic performance and power-quality demanding applications, covering a power range from 1 to 30 MW [4]–[9]. Among the reasons for their success are the higher voltage operating capability, lower common-mode voltages, reduced voltage derivatives (dv/dt), voltages with reduced harmonic contents, near sinusoidal currents, smaller input and output filters (if necessary), increased efficiency, and, in some cases, possible fault-tolerant operation [4]–[9]. Recent contributions, especially dedicated to multilevel converters, like special sections in journals [10]–[12], conference tutorials [13]–[17], and books or book chapters [18]–[21], show the importance reached by this technology nowadays. In addition, leading manufacturers in the field of power electronics and drives commercialize multilevel converters, covering a wide variety of topologies, control methods, and applications.[1]

Due to the power levels reached by this technology, it has become an important alternative for high-power medium-voltage fans, compressors, pumps, conveyors, ship propulsion drives, locomotive traction drives (including linear motor drives for maglev trains), and steel rolling mills, to name a few [22]–[27]. Recently, they have been proposed to enable new possibilities for several important applications like electric and hybrid vehicles, wind energy conversion, photovoltaic energy conversion, uninterruptible power supplies, reactive power compensation, and regenerative applications [6], [28]–[43], among others.

This paper presents a tutorial on multilevel converter technology. The compromise between the depth and span of the topic coverage has been settled in a way that provides a comprehensive introduction for the nonexpert electric and electronics engineers. Nevertheless, the state of the art, recent advances, and trends are also addressed, which will interest the more familiarized power-electronics engineer, from industry and academia.

The paper is organized as follows. The next section will introduce the multilevel converter conceptual background. The operating principle and main characteristics of different multilevel topologies and multilevel modulation methods are presented in Sections III and IV, respectively. Section V is dedicated to review rectifier configurations for multilevel inverters for regenerative and nonregenerative applications. Several operational and technological issues related to multilevel converters are addressed in Section VI, which include multilevel inverter modeling, dc-link voltage unbalance, and operation under faulty conditions. Some multilevel inverter applications are reviewed in Section VII. Lastly, a summary of relevant remarks is included in the conclusion in Section VIII.

[1]See http://www.abb.com/; http://www.siemens.com/; http://www.alstom.com/; and http://www.mitsubishielectric.com/.

II. THE MULTILEVEL CONVERTER CONCEPT

Multilevel converters are power-conversion systems composed by an array of power semiconductors and capacitive voltage sources that, when properly connected and controlled, can generate a multiple-step voltage waveform with variable and controllable frequency, phase, and amplitude. The stepped waveform is synthesized by selecting different voltage levels generated by the proper connection of the load to the different capacitive voltage sources. This connection is performed by the proper switching of the power semiconductors.

The number of levels of a converter can be defined as the number of steps or constant voltage values that can be generated by the converter between the output terminal and any arbitrary internal reference node within the converter. Typically, it is a dc-link node, and it is usually denoted by N and called neutral. To be called a multilevel converter, each phase of the converter has to generate at least three different voltage levels. This differentiates the classic two-level voltage source converter (2L-VSC) from the multilevel family. Some single-phase examples of this concept and their respective waveforms are given in Fig. 1 for different number of levels. It is worth mention that, generally, the different voltage levels are equidistant from each other in multiples of V_{dc}.

Two-level converters can generate a variable frequency and amplitude voltage waveform by adjusting a time average of their two voltage levels. This is usually performed with pulse-width modulation (PWM) techniques [44]. On the other side, multilevel converters add a new degree of freedom, allowing the use of the voltage levels as an additional control element and giving more alternatives to generate the output waveform. For this reason, multilevel inverters have intrinsically improved power quality, characterized by: lower voltage distortion (more sinusoidal waveforms), reduced dv/dt, and lower common-mode voltages, which reduce or even eliminate the need of output filters.

When considering a three-phase system, the levels of one phase are combined with those of the other phases, generating more different levels in the line-to-line voltage. For a converter with n_p phase to neutral voltage levels, $n_{ll} = 2n_p - 1$ levels can be found in the line-to-line voltage (a zero level is redundant). Something similar happens in the three-phase load voltage, where combinations of the line voltages are produced, obtaining $n_{\text{load}} = 2n_{ll} - 1$ voltage levels. However, only n_p is used to refer to the number of levels of the converter, since these are the levels generated by the converter independently of the number of phases or the load connection type.

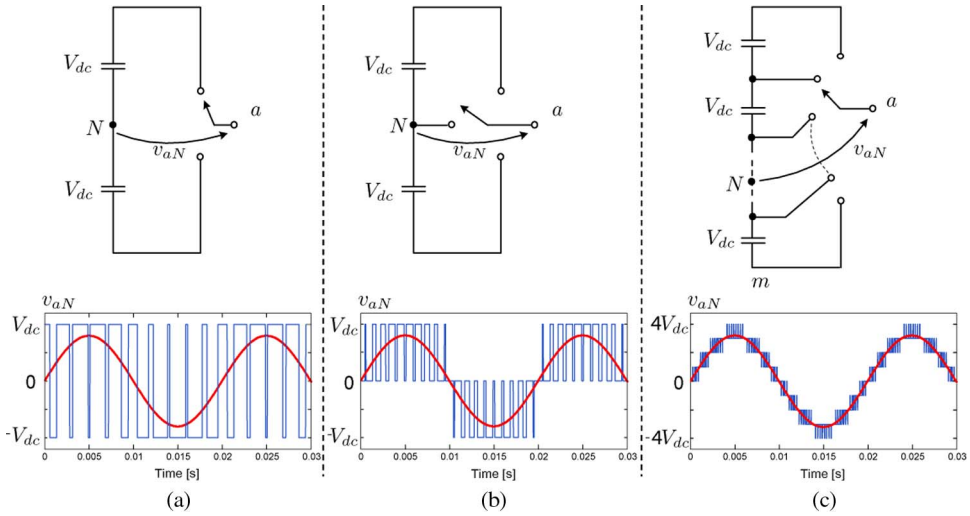

Fig. 1. *Converter output voltage waveform: a) two level, b) three level, c) nine level.*

There are many ways to combine power semiconductors and capacitive dc sources to generate multilevel output voltages. However, only some of them have become important from a practical point of view, and these are analyzed in the following section.

III. CONVERTER TOPOLOGIES

Over the years, many different multilevel converter topologies have been reported [4]–[9]. They can be classified in two main groups, as shown in Fig. 2, depending on the number of independent dc sources used in their structure. The most known and established topologies are the neutral point clamped (NPC) or diode clamped, the flying capacitor (FC) or capacitor clamped, and the cascaded H-bridge (CHB), each introduced for the first time in [45]–[47], respectively. The FC and CHB are also referred as multicell converters (MCs) due to their modular structure composed of several smaller power converters called power cells.

More recently, numerous variations and even combinations of these topologies have been presented to satisfy particular applications requirements or to improve an operational feature. Some of these variations include the active NPC (ANPC) [48], which produces a more equal semiconductor junction temperature distribution, enabling a substantial increase of the converter output current and power at nominal operation compared to the regular NPC. Another variation is the stacked MC [49]–[51], which basically can be described as a combination of serial and

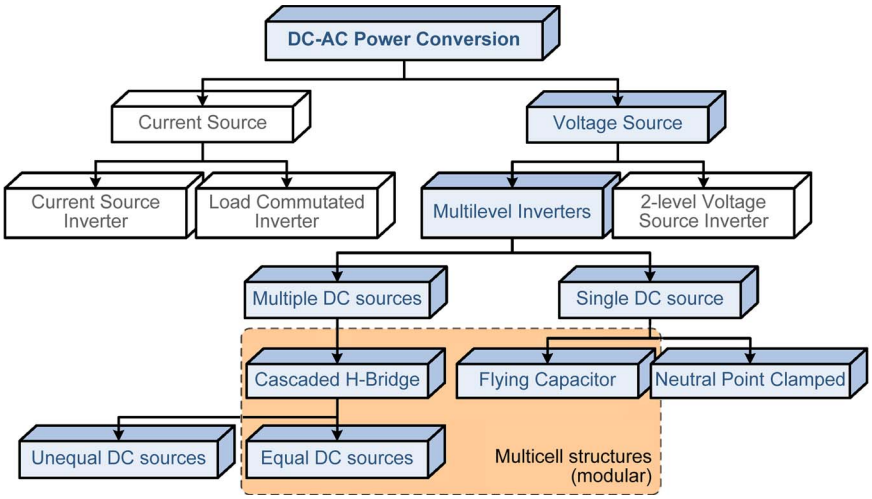

Fig. 2. *Multilevel converter classification.*

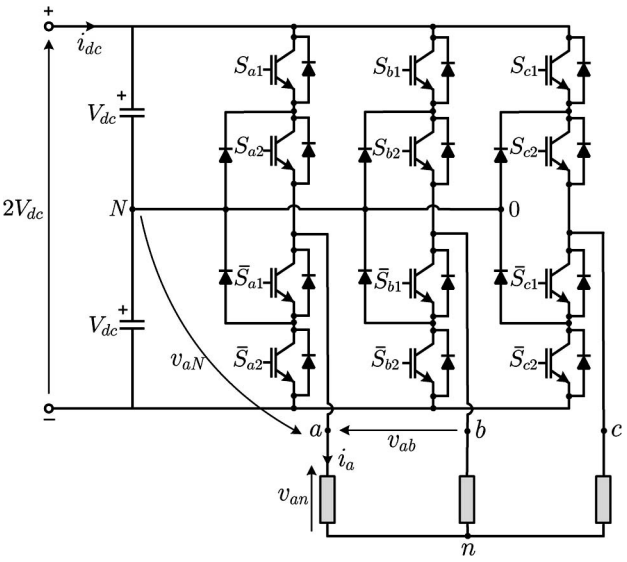

Fig. 3. ***Three-level neutral point clamped power circuit.***

parallel connected flying-capacitor power cells. This converter allows a higher voltage operation, reduction in capacitor volume, and better quality output voltages than the traditional FC. The CHB, traditionally fed by equal dc voltage sources, has also been modified by introducing an asymmetry in the dc voltage sources. This modified version is known as the asymmetric or hybrid CHB [52]–[57]. It generates considerably more output voltage levels than any other topology using less semiconductors and capacitors. Asymmetric or hybrid topologies have also been proposed based on the NPC structure [58].

A. Neutral Point Clamped Converters

An NPC converter is basically composed of two traditional two-level VSCs stacked one over the other with some minor modifications. As can be seen in Fig. 3, the negative bar of the upper converter and the positive bar of the lower one are joined together to form the new phase output, while the original phase outputs are connected via two clamping diodes to form the neutral point N, dividing the dc-link voltage in two. Now each power device has to block only half of the total converter voltage; hence with the same semiconductor technology, the power rating of the converter can be doubled. In addition, the neutral point enables the generation of a zero voltage level, obtaining a total of three different voltage levels.

The switching state of a converter is a set of signals used to control each switching device of the power circuit. They can modify its conduction state and the way the load is connected to the different nodes of the dc side circuit. Hence a particular switching state generates a corresponding output voltage level. For the NPC shown in Fig. 3, the switching signals are S_{ij}, with the subscript i and j representing the corresponding phase (a, b, or c) and switch number (1 or 2), respectively. Note that there are only two control signals per phase; the other two switches receive inverted gating signals to avoid the dc-link short-circuit. The gate signal is of binary nature, representing by 0 the OFF state of the switch and by 1 the ON state. Fig. 4 shows the three different switching states for one phase of

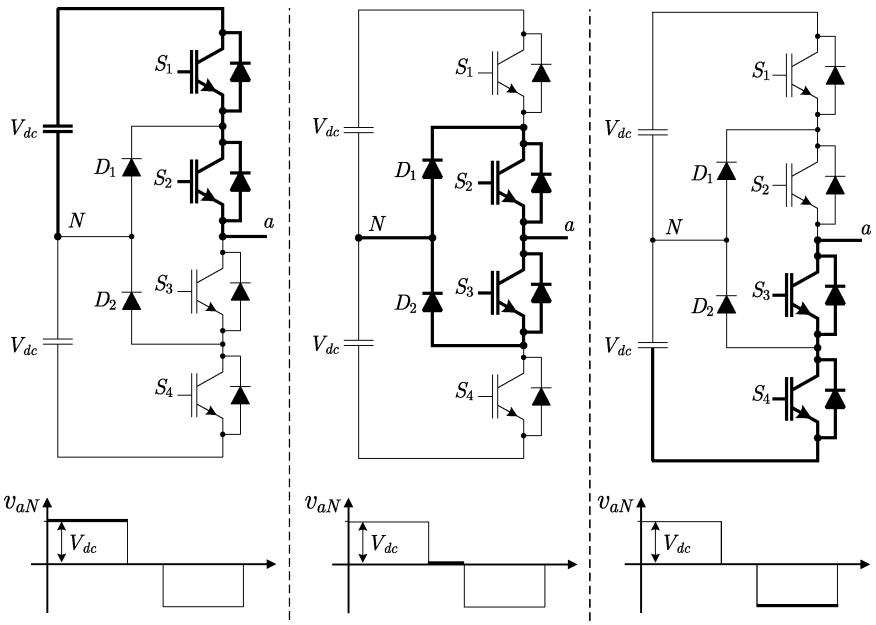

Fig. 4. ***Three-level NPC switching states and corresponding output voltage levels.***

the NPC and their corresponding output voltage levels. The obtained equivalent circuit is highlighted to show how the output node a is linked to the positive, neutral, and negative nodes of the dc side circuit. Note that one of the four binary combinations $(S_{a1}, S_{a2}) = (1, 0)$ is not used since it does not provide a current flow path for the load. The same switching states can be applied for phases b and c.

The NPC topology can be extended to higher power rates and more output voltage levels by adding additional power switches and clamping diodes to be able to block higher voltages. Fig. 5 shows a phase of a five-level NPC converter. Here the name diode clamped (DC) makes more sense, since there are more voltage-level clamping nodes than only the neutral N. Note that the number of clamping diodes needed to share the voltage increases dramatically. This fact, together with the increasing difficulty to control the dc-link capacitor unbalance, has kept the industrial acceptance of the NPC topology up to three levels only.

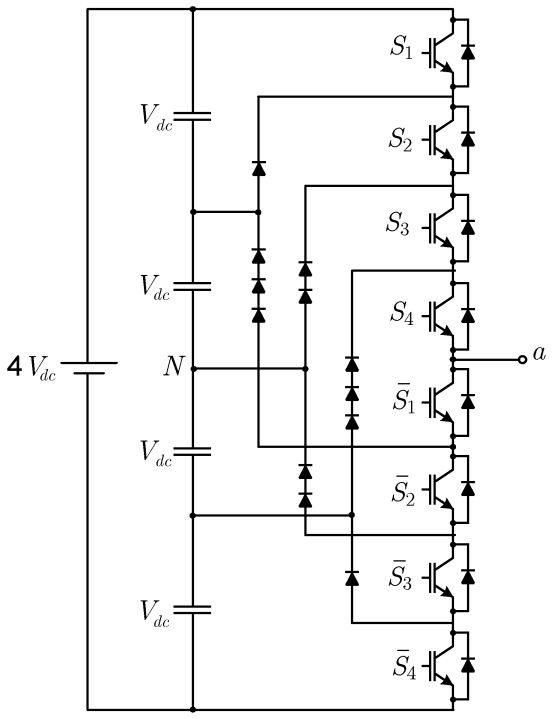

Fig. 5. *A phase of a five-level NPC.*

B. Flying Capacitor Converters

The FC topology is in some way similar to the NPC, with the main difference being that the clamping diodes are replaced by flying capacitors, as can be seen in Fig. 6. Here the load cannot be directly connected to the neutral of the converter to generate the zero voltage level. Instead, the zero level is obtained by connecting the load to the positive or negative bar through the flying capacitor with opposite polarity respect the dc-link. Like with the NPC, only two gating signals are necessary per phase to avoid dc-link and flying capacitor short-circuit. However, in the FC, the inverted gating signals are related to different switching devices, as shown in Fig. 6. The switching states and their equivalent power circuits with the corresponding output voltage levels are illustrated in Fig. 7.

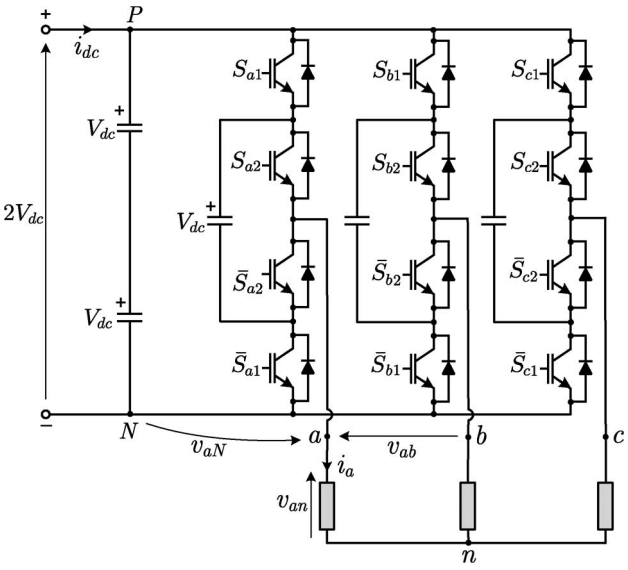

Fig. 6. *Three-level flying capacitor power circuit.*

Another difference with the NPC is that the four combinations of (S_{a1}, S_{a2}) are allowed. Only three are shown in Fig. 7. The middle circuit in Fig. 7 shows $(S_{a1}, S_{a2}) = (1, 0)$, which generates the zero level. The same level is obtained with $(S_{a1}, S_{a2}) = (0, 1)$. This property is known as voltage-level redundancy and can be used for control or optimization purposes.

Perhaps the main and most important difference with the NPC topology is that the FC has a modular structure and can be more easily extended to achieve more voltage levels and higher power rates. This can be easily observed by redrawing the FC as illustrated in Fig. 8, where an additional pair of switching devices and a capacitor are connected to form a four-level FC converter. Note that each pair of switches together with one capacitor forms a power cell or module. They can be connected one after the other, and each one provides one additional voltage level to the output. The addition of power cells increases the number of voltage-level redundancies, which can be used as extra degrees of freedom for control or optimization purposes.

C. Cascaded H-Bridge Converters

CHBs are multilevel converters formed by the series connection of two or more single-phase H-bridge inverters, hence the name. Each H-bridge corresponds to two voltage source phase legs, where the line–line voltage is the converter output. Therefore, a single H-bridge converter is able to generate three different voltage levels. Each leg has only

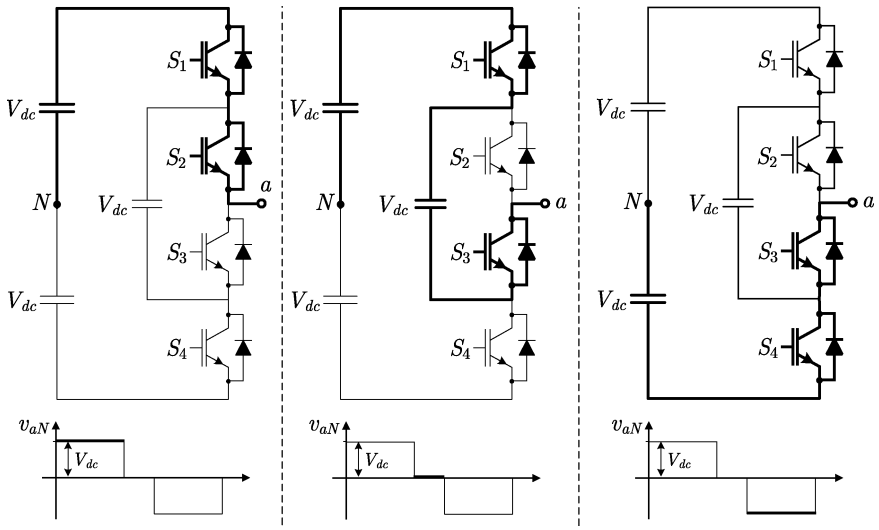

Fig. 7. *Three-level FC switching states and corresponding output voltage levels.*

two possible switching states, to avoid dc-link capacitor short-circuit. Since there are two legs, four different switching states are possible, although two of them have redundant output voltage. Fig. 9 shows the three different output voltage levels and their corresponding equivalent circuits. The zero level can be generated connecting the phase outputs to the positive or the negative bars of the inverter (only the first one is illustrated in Fig. 9).

When two or more H-bridges are connected in series, their output voltages can be combined to form different output levels, increasing the total inverter output voltage and also its rated power. Fig. 10 shows four H-bridges connected in series and a qualitative example of their possible individual three-level output voltages. The total converter output voltage is also illustrated presenting nine different voltage levels. In general terms, when connecting k H-bridges in series, $2k+1$ different voltage levels are obtained (two per H-bridge and the zero, common to all), and a maximum output voltage of kV_{dc} is possible.

CHB presents more redundancies than the previous topologies, since each H-bridge or power cell has one redundant switching state, and the series connection inherently introduces more redundancies.

This can be clearly appreciated in Table 1, where all the switching states of a two-cell or five-level CHB inverter are listed. The number of redundancies grows overproportionally when increasing the number of cells. These redundancies and the natural modularity of this topology are advantages that enable fault-tolerant operation, as will be discussed later. Another advantage is the effective increase in the output voltage and power, since all semiconductors have only to block V_{dc}. The main drawback is the fact that each H-bridge inverter needs an isolated dc-source, usually provided by a three-phase rectifier fed by a transformer. Hence, for a three-phase five-level inverter, a three-phase transformer with six secondary three-phase windings and the corresponding diode bridges are necessary, increasing the volume and cost of the converter.

The H-bridge converters that are connected in series do not necessarily need to have the same dc input voltages. In fact, a proper choice of voltage asymmetry between cells can produce a different combination of voltage levels and eliminate redundancies. As shown in Fig. 11, an asymmetry or voltage ratio of 1 : 3 for a two-cell CHB leads to the same nine levels achieved with a four-cell CHB of Fig. 10. The asymmetric fed topology achieves same output voltage quality with less hardware. However, in case of using the same power semiconductor technology, the total output voltage is reduced, since the maximum blocking voltage of the device will limit the value of the permitted dc source.

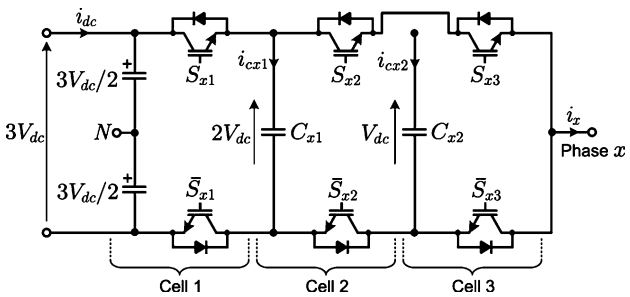

Fig. 8. *Four-level FC (only one phase shown).*

IV. MULTILEVEL CONVERTER MODULATION METHODS

Together with the development of multilevel inverter topologies appeared the challenge to extend traditional

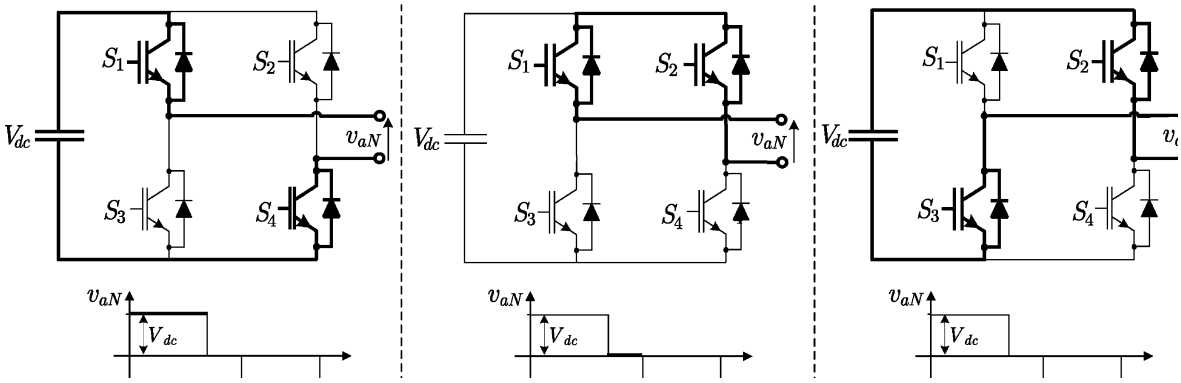

Fig. 9. *Three-level H-bridge switching states (single phase).*

modulation methods to the multilevel case. On one hand, there is the inherent additional complexity of having more power-electronics devices to control, and on the other the possibility to take advantage of the extra degrees of freedom provided by the additional switching states generated by these topologies. As a consequence, a large number of different modulation algorithms have been adapted or developed depending on the application and the converter topology, each one having unique advantages and drawbacks. A classification of the most common modulation methods for multilevel inverters is presented in Fig. 12. The modulation algorithms are here classified depending on the average switching frequency with which they operate, i.e., high or low. For high-power applications, high switching frequencies are considered those above 1 kHz.

A. PWM Algorithms for Multilevel Converters

1) Phase Shifted (PS-PWM): Phase-shifted PWM (PS-PWM) is a natural extension of traditional PWM techniques,

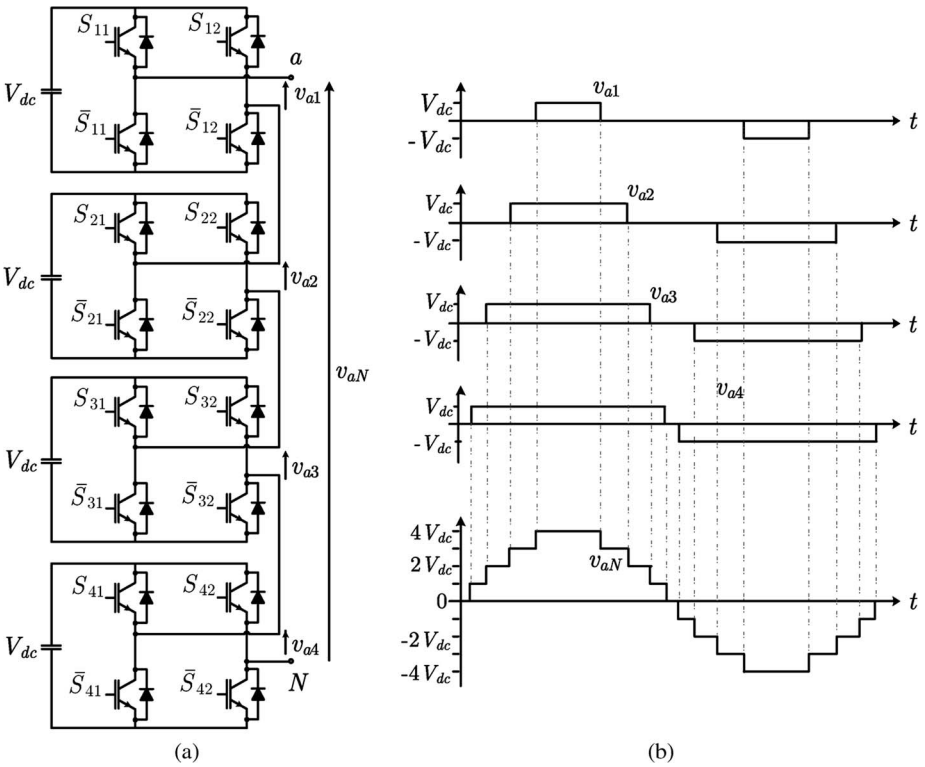

Fig. 10. *Nine-level cascaded H-bridge: (a) power circuit and (b) output voltage waveform synthesis (single phase).*

Table 1 Five-Level CHB Switching States

Total inverter output voltage	Switching state				Individual cell output voltage	
v_{aN}	S_{11}	S_{12}	S_{21}	S_{22}	v_{a1}	v_{a2}
$2V_{dc}$	1	0	1	0	V_{dc}	V_{dc}
V_{dc}	1	0	1	1	V_{dc}	0
			0	0		
	1	1	1	0	0	V_{dc}
	0	0				
0	0	0	0	0	0	0
	0	0	1	1		
	1	1	0	0		
	1	1	1	1		
	1	0	0	1	V_{dc}	$-V_{dc}$
	0	1	1	0	$-V_{dc}$	V_{dc}
$-V_{dc}$	0	1	0	0	$-V_{dc}$	0
			1	1		
	0	0	0	1	0	$-V_{dc}$
	1	1				
$-2V_{dc}$	0	1	0	1	$-V_{dc}$	$-V_{dc}$

specially conceived for FC [59] and CHB [60] converters. Since each FC cell is a two-level converter, and each CHB cell is a three-level inverter, the traditional bipolar and unipolar PWM techniques can be used, respectively. Due to the modularity of these topologies, each cell can be modulated independently using the same reference signal. A phase shift is introduced between the carrier signals of contiguous cells, producing a phase-shifted switching pattern between them. In this way, when connected together, a stepped multilevel waveform is originated. It has been demonstrated that the lowest distortion can be achieved when the phase shifts between carriers are 180 or $360°/k$ for a CHB or FC converter, respectively (where k is the number of power cells). This difference is related to the fact that the FC and CHB cells generate two and three levels, respectively. A seven-level CHB example of the operating principle is illustrated in Fig. 13.

Since all the cells are controlled with the same reference and same carrier frequency, the switch device usage

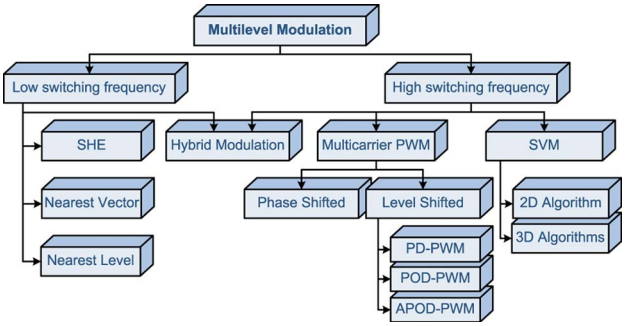

Fig. 12. ***Multilevel converter modulation methods.***

and the average power handled by each cell is evenly distributed. For the case of the CHB, this means that multipulse diode rectifiers can be used to reduce input current harmonics. For the FC, the advantage of the even power distribution is that once the flying capacitors are properly charged (initialized to their corresponding values), no unbalance will be produced due to the self-balancing property of this topology [61], [149]; hence there is no need to control the dc-link voltages. Another interesting feature is the fact that the total output voltage has a switching pattern with k times the frequency of the switching pattern of each cell. This multiplicative effect is produced by the phase-shifts of the carriers. Hence, better total harmonic distortion (THD) is obtained at the output, using k times lower frequency carriers. The corresponding implementation diagram is illustrated in Fig. 14. Note that the same nomenclature is used for the gating signals S_{xy} as for those defined in Fig. 10(a), only here it is used for three cells instead of four.

2) Level Shifted (LS-PWM): Level-shifted PWM (LS-PWM) is the natural extension of bipolar PWM for multilevel inverters. Bipolar PWM uses one carrier signal that is

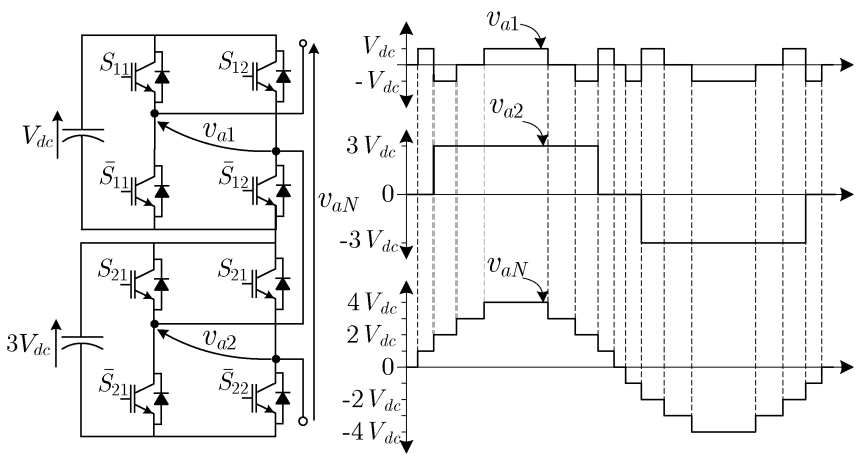

Fig. 11. ***Nine-level H-bridge switching states (single phase).***

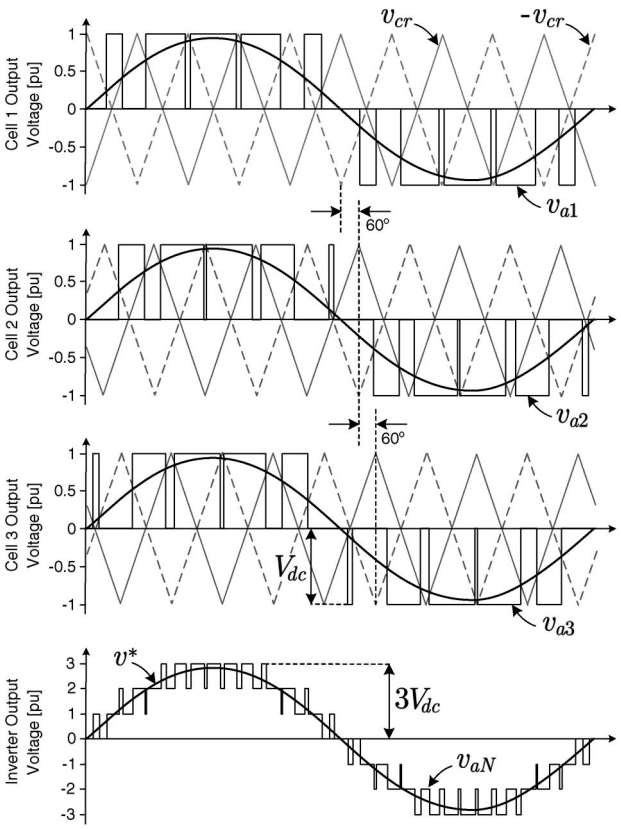

Fig. 13. ***Three-cell (seven-level) PS-PWM waveform generation for CHB.***

compared to the reference to decide between two different voltage levels, typically the positive and negative busbars of a VSI. By generalizing this idea, for a multilevel inverter, $m - 1$ carriers are needed. They are arranged in vertical shifts instead of the phase-shift used in PS-PWM.

Each carrier is set between two voltage levels; hence the name "level shifted." Since each carrier is associated to two levels, the same principle of bipolar PWM can be applied, taking into account that the control signal has to be directed to the appropriate semiconductors in order to generate the corresponding levels. The carriers span the whole amplitude range that can be generated by the converter. They can be arranged in vertical shifts, with all the signals in phase with each other, called phase disposition (PD-PWM); with all the positive carriers in phase with each other and in opposite phase of the negative carriers, known as phase opposition disposition (POD-PWM); and alternate phase opposition disposition (APOD-PWM), which is obtained by alternating the phase between adjacent carriers [62]. An example of these arrangements for a five-level inverter (thus four carriers) is given in Fig. 15(a)–(c), respectively.

This modulation method is especially useful for NPC converters, since each carrier can be easily associated to two power switches of the converter. In Fig. 16, a qualitative example for a three-level NPC is illustrated. From Fig. 16(a), it can be observed that the times during which the value of the reference is greater than the value of both carriers, the upper switches are turned on connecting the load to the positive busbar. During the times the reference value is between both carriers ($v_{cr2} \leq v^* \leq v_{cr1}$), the output is connected to the neutral point N. Finally, the times in which the reference value is lower than both carriers, the lower switches are turned on, connecting the load to the negative busbar. The control diagram that performs this algorithm is shown in Fig. 16(b). Note that the gating signals of Fig. 16(b) are defined for the three-level NPC, as shown in Fig. 4.

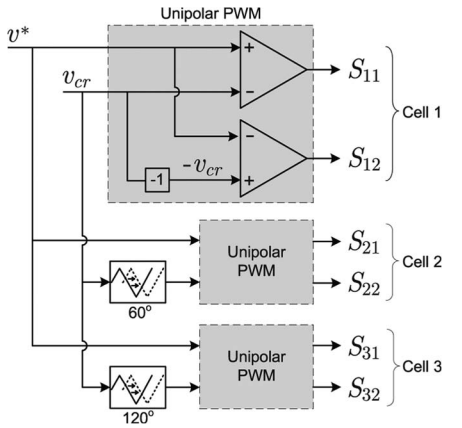

Fig. 14. ***Three-cell (seven-level) PS-PWM control diagram for CHB.***

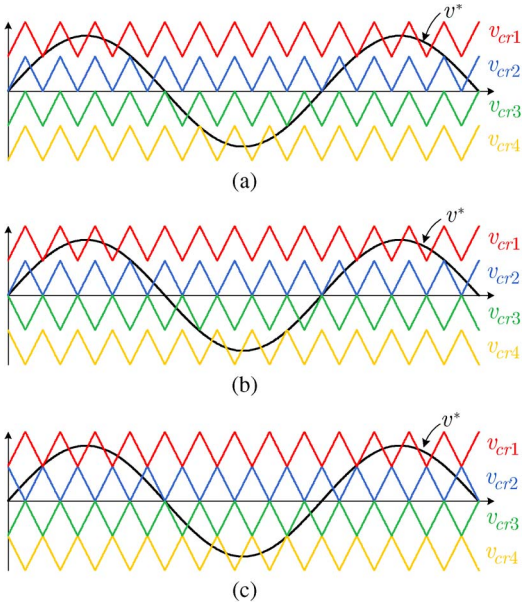

Fig. 15. ***LS-PWM carrier arrangements: (a) PD, (b) POD, and (c) APOD.***

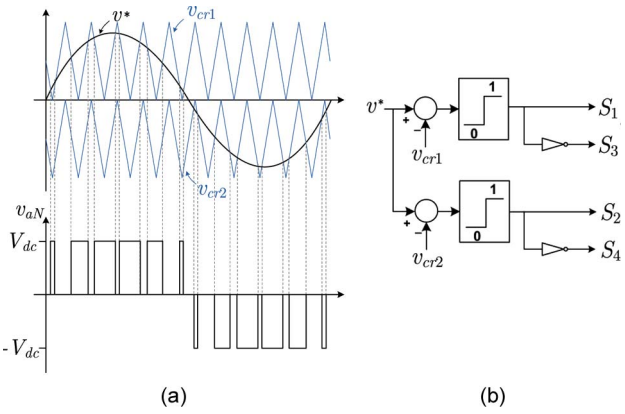

Fig. 16. ***LSPWM for NPC: (a) waveform generation and (b) control diagram.***

LS-PWM leads to less distorted line voltages since all the carriers are in phase compared to PS-PWM [18]. In addition, since it is based on the output voltage levels of an inverter, this principle can be adapted to any multilevel converter topology. However, this method is not preferred for CHB and FC, since it causes an uneven power distribution among the different cells. This generates input current distortion in the CHB and capacitor unbalance in the FC compared to PS-PWM.

3) Hybrid PWM Modulation: Hybrid PWM (H-PWM) is an extension of PWM for CHB with unequal dc sources [8]. The main challenge is to reduce the switching losses of the converter by reducing the switching frequency of the higher power cells. Therefore, instead of using high-frequency carrier-based PWM methods in all the cells, the high-power cells are operated with square waveform patterns, switched at low frequency, while only the small power cell is controlled with unipolar PWM.

Consider, for example, a three-cell (in each phase) CHB inverter with $V_1 < V_2 < V_3$ as the three unequal dc source voltage values. Then, the square wave operation for

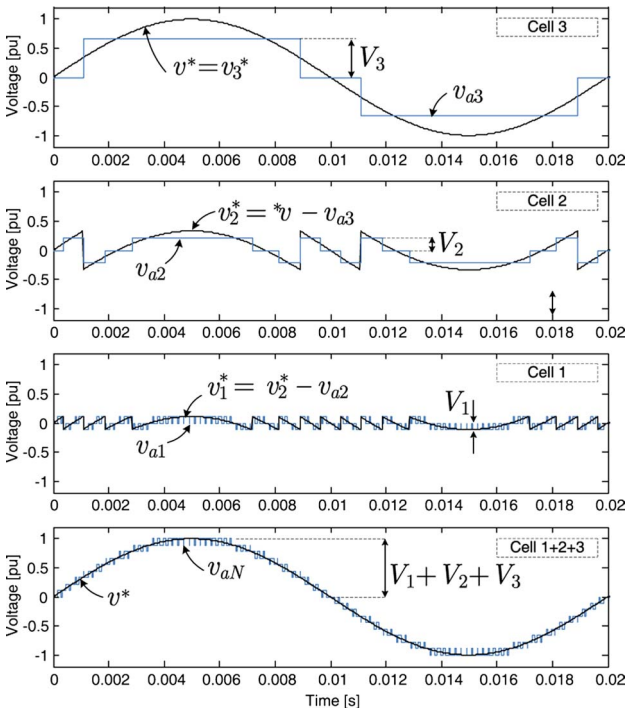

Fig. 18. ***Output voltages for CHB with unequal dc sources for hybrid modulation.***

cell 3 can be obtained by simply comparing the reference to $\pm h_3 = \pm(V_1 + V_2)$, as shown in the control diagram in Fig. 17. The output of this comparator indicates if this cell is generating $-V_3$, zero, or V_3 at the output. Considering a sinusoidal reference, the generated output voltage for cell 3 using this comparator is shown in Fig. 18(a), switching at fundamental frequency (each switch has a turn-on and turn-off during one cycle). The difference between the reference v^* and this output v_{a3} is the error or the unmodulated part of the reference, which is left for modulation to the other two cells. Hence, this difference can then be used as reference for cell 2. Again, a comparator $\pm h_2 = \pm V_1$ is used to generate the output of cell 2

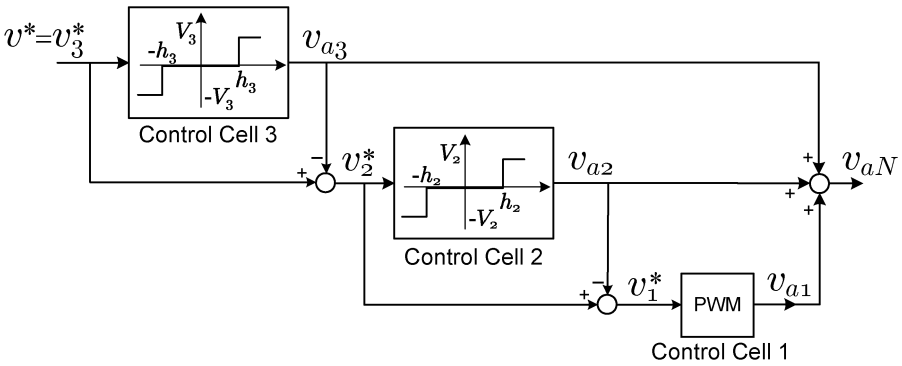

Fig. 17. ***Hybrid modulation operating principle for CHB with unequal dc sources.***

(note that, in general, the comparator level for cell k is $h_k = V_{k-1} + V_{k-2} + \cdots + V_1$, i.e., the sum of the smaller dc sources (to avoid overmodulating references for the smaller cells). For example, the output waveform in Fig. 18(b) is obtained, with few commutations per cycle. In the same way as with cell 3, the square wave operation of cell 2 is a gross approximation of its reference; therefore this new error (difference between v_2^* and v_{a2}) becomes the reference for the last cell. Since there are no more cells left, and this is the one with the lowest power, the square waveform operation is replaced by traditional unipolar PWM, as shown in the control diagram of Fig. 17. The reference and output of cell 1 is given in Fig. 18(c). The series connection of the cells delivers a total output voltage $v_{aN} = v_{a1} + v_{a2} + v_{a3}$, as the one illustrated in Fig. 18(d), which looks like a traditional high-frequency PWM multilevel waveform pattern, while in fact only the low-power cell is operating at higher switching frequencies, improving the converter efficiency. This method is only feasible if the dc-link voltages of the higher power cells are integer multiples of the small one, and $V_3 \leq 2(V_1 + V_2)$ and $V_2 \leq 2V_1$; otherwise overmodulation in the small power cell will occur. The optimal asymmetry that fulfills these conditions for a three-cell inverter is $V_1 : V_2 : V_3 = 1 : 2 : 6$ and is the example shown in Fig. 18, leading to 19 different voltage levels).

B. Space Vector Modulation Algorithms for Multilevel Converters

The space vector modulation (SVM) algorithm is basically also a PWM strategy with the difference that the switching times are computed based on the three-phase space vector representation of the reference and the inverter switching states rather than the per-phase in time representation of the reference and the output levels as in previous analyzed methods.

1) State-Space Vector Representation of the Inverter: The voltage state-space vector v_s combines simultaneously the values of the three-phase variables and maps them into a unique vector in the α–β complex plane by

$$v_s = \frac{2}{3}[v_a + a v_b + a^2 v_c] \tag{1}$$

where $\alpha = -(1/2) + (j\sqrt{3}/2)$. By replacing in (1) the phase output voltages of the inverter (v_a, v_b, v_c) for each possible switching state, the inverter state-space vectors can be obtained. An example for a three-phase three-level NPC inverter is given in Fig. 19. Note that the NPC has three phases and three output levels or switching states, resulting in 3^3 possible combinations; hence 27 state-space vectors (in general, the number of state vectors of a three-phase N-level converter is N^3). However, only 19 are different, and eight are redundant. There is triple redundancy

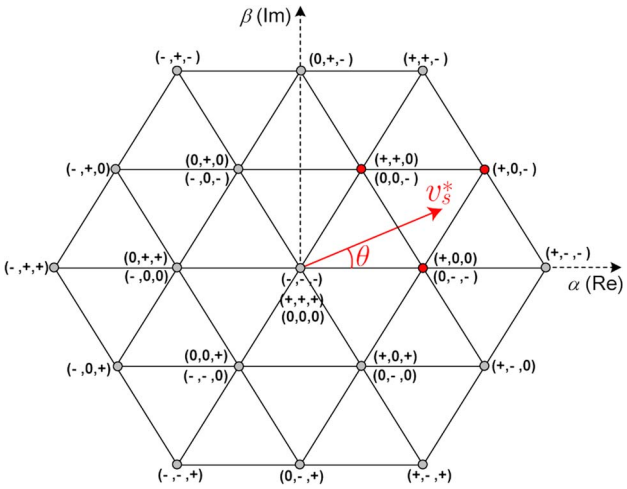

Fig. 19. ***Three-phase three-level converter state-space vectors.***

in the zero state vector and double redundancy in the six short state vectors. For example, the zero vector can be obtained in three ways: 1) connecting the three-phase outputs to the positive busbar $(v_a = v_b = v_c = +V_{dc})$, corresponding to the switching state $(+,+,+)$; or to the neutral point $(v_a = v_b = v_c = 0)$, corresponding to the state (0,0,0); or to the negative busbar $(v_a = v_b = v_c = -V_{dc})$, corresponding to the state $(-,-,-)$. From the load point of view, redundant vectors have the exact same influence, and it makes no difference which one is used. From the inverter point of view, they are different switching states, and this can be used as an additional degree of freedom for other control purposes, as will be discussed later in Section VI-A. It is worth mentioning that, since the possible output levels of the inverters are fixed ($-V_{dc}$, zero, and V_{dc}), the state-space vectors are also fixed. Note that for a traditional two-level VSI, only seven different space vectors are obtained [44], while by just adding a third level like in NPC, 19 different can be generated. This increases overproportionally in relation to the numbers of levels and is in direct accordance with the output power quality, as a more dense state-space vector representation in the α–β plane is obtained, in the same way more levels are a more dense coverage of the amplitude range in the per-phase time representation.

The three-phase reference can also be mapped to the α–β plane using the same transformation (1) but replacing the phase reference voltages instead of the phase output voltages. Since the references are not switched variables with fixed voltage values as the output phase voltages of the inverter, the reference space vector v_s^* can be mapped anywhere in the α–β plane and not necessarily coincide with any of the inverter space vectors, analogous to the per-phase time representation, where the reference signal does not necessary match an inverter output level. For balanced three-phase sinusoidal references, as is usual in

power-converter systems, the resulting reference vector v_s^* is a rotating space vector, with the same amplitude and angular speed (ω) of the sinusoidal references, with an instantaneous position with respect to the real axis α given by $\theta = \omega t$ as the one illustrated in Fig. 19.

SVM techniques can be classified into algorithms for balanced or unbalanced systems, depending on the application. It is important to know if the reference vector also contains harmonics or if the control technique must compensate harmonics or zero sequence components in three-phase four-wire systems with neutral. In case of generating purely sinusoidal reference voltages, the use of balanced algorithms is enough; however, for the other cases, three-dimensional techniques should be considered.

2) SVM Algorithms for Multilevel Balanced Systems: The basic idea of SVM is to use the state-space vector representation introduced earlier to combine or modulate three state-space vectors of the inverter, so that their time average equals the reference space vector, in the same way PWM combines the levels to obtain a time average of the reference in the per-phase representation. The modulation principle of SVM can be summarized by

$$v_s^* = \frac{1}{\tau_s}(t_1 v_1 + t_2 v_2 + t_3 v_3) \tag{2}$$

where $T_s = t_1 + t_2 + t_3$ is a fixed modulation period (analogous to the carrier period in PWM), v_1, v_2, and v_3, and the three closest vectors to the reference (highlighted in red in the qualitative example shown in Fig. 19). The problem is then reduced to finding an algorithm capable of finding the closest vectors to the reference and computing the ON times of each vector t_1, t_2, and t_3. Once these are computed, each vector is generated during the corresponding time, achieving the desired time average over T_s that equals the reference.

There are additional challenges, like the use of the vector redundancies for other purposes like switching frequency reduction by using a particular sequence in which the vectors are generated or to use the redundancies for dc-link voltage unbalance control [21].

Many SVM algorithms based on the previous concept have been reported. They differ in how the three nearest vectors are chosen, how the times are computed, the sequence used to generate the vectors, and the computational effort necessary for implementation. In [63], a coordinate transformation is introduced to the α–β plane, shifting the complex axis β from 90° to 60° with respect to the α-axis, also called hexagonal coordinates or h–g plane. The advantage is that, when normalized, each vector can be expressed by two integer values in the h- and g-axis, instead of fractional complex components of the β-axis. This greatly simplifies the determination of the three closest vectors to the reference, since they can be located using round functions (floor and ceil). In addition, the ON times can be easily obtained as the fractional parts of the reference in the h- and g-axis.

Another very low computational cost method is presented in [63]. This method is based on the decision-based pulse-width modulation developed for conventional two-level converters [44]. This iterative algorithm is based on the determination of the switching sequence and the duty cycles only considering a sextant of the inverter state-space region shown in Fig. 19. This is achieved by rotating the space vector reference to its equivalent in the first sextant in order to facilitate the calculations. This algorithm presents the advantage compared with other methods of eliminating complex mathematical calculations in the switching sequence determination. In addition, the numeric computation of the ON times is reduced to a simple addition.

An alternative SVM method based on this iterative algorithm is presented in [63]; the main difference is that the space vectors and their ON times are calculated using very simple geometrical considerations. In this geometrical algorithm, the rotation needed in the iterative algorithm is avoided, reducing the computational cost even more. Moreover, the low computational cost of this method is always the same, and it is independent of the number of levels of the converter.

The geometrical modulation algorithm uses as input the normalized reference voltage vector in order to be independent of the dc-link voltage and the numbers of levels of voltages of the converter. In this way, the state-space vectors of the converter are placed in the control region in geometrical positions denoted by entire values between zero and $n_p - 1$, where n_p is the number of levels of the multilevel converter. Also, this reference voltage is normalized again, scaling the imaginary part and dividing it by $\sqrt{3}$ [65]. By doing this, the control region is defined by 45° slope triangular regions and allows using very simple online computations to determine the switching sequence and the ON times.

3) SVM Algorithms for Multilevel Unbalanced Systems: In power converters with neutral connection (usually also named unbalanced systems), the two-dimensional α–β plane is not enough to fully represent the converter system, since the common-mode voltages and currents through the neutral are not considered. An additional γ component (third dimension) is introduced

$$\gamma = (v_a + v_b + v_c). \tag{3}$$

The reference vector and the converter switching states are now mapped into this three-dimensional (3-D) region, originating 3D-SVM methods.

a) 3-D SVM algorithm for multilevel converters: The α–β–γ representation offers interesting information about the zero sequence component of currents and voltages, but the additional dimension adds complexity to the modulation algorithm [67]. Therefore, the natural Cartesian coordinates are used for 3-D multilevel converter modulations to facilitate these calculations. An extension of the geometrical α–β algorithm introduced in the previous section has been reported for the three-dimensional Cartesian a–b–c plane in [67]. In the 3D-SVM method, the nearest four space vectors to the reference vector are considered (four because now the reference voltage vector is mapped into the 3-D space). After a normalization of the reference voltage vector, the control region is defined by a cube with vertexes in positions from zero to $n_p - 1$ in each axis a, b, and c. This cube is formed by a certain number of subcubes depending on the number of the levels of the converter. As an example, the state-space vectors of a three-phase three-level converter are shown in Fig. 20. In this space vector representation, the switching states are defined as 0, 1, and 2 corresponding to previously defined states $-$, 0, and $+$, respectively. This 3D-SVM algorithm considers the subcube where the reference vector is located. Thanks to the normalization of the desired reference voltage vector, the closest vector of this subcube to the origin is easily calculated as the integer part of each component of the reference voltage vector.

In each subcube, the four nearest state-space vectors to the reference vector must be identified [67]. The subcubes are divided in six regular tetrahedrons, so the 3D-SVM has to find out the tetrahedron where the reference vector is located, because the vertexes of this tetrahedron are the state-space vectors, which will be used for modulation and form the switching sequence. The determination of the tetrahedron is a very fast algorithm with low computational cost because it implies simple comparisons. Finally, in [67], a table summarizing the switching sequence and the duty cycles corresponding to each tetrahedron is presented. The numeric calculations of the ON times are reduced to simple additions. This reduces significantly the computational requirements and enables this technique to be used as a modulation algorithm in those applications where a 3-D vector region is required (systems with or without neutral, with unbalanced load, with triplen harmonics), and it is independent of the number of levels of the converter. Finally, it is important to notice that the 3D-SVM can also be applied to multilevel balanced systems achieving zero common-mode voltage.

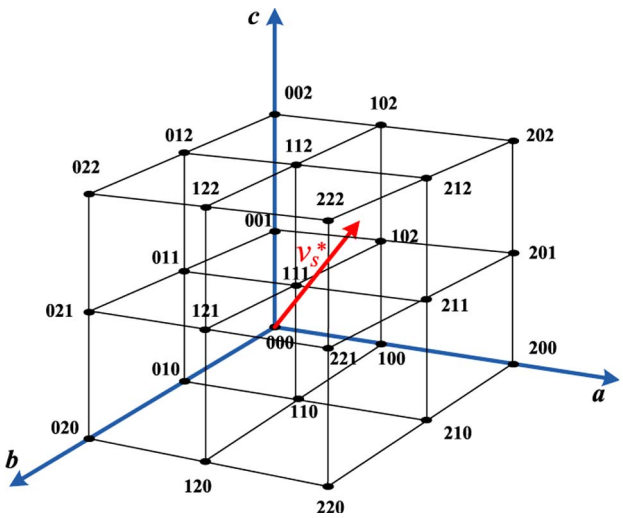

Fig. 20. *State-space vectors of a three-phase three-level converter using the 3-D Cartesian coordinates. This control region is plotted using the normalized phase-to-neutral voltages.*

b) SVM algorithms for multilevel four-leg four-wire inverters: A wide range of industrial applications use four-leg and four-wire converters (4L-4W) since they provide more zero-sequence control capability. This can be applied to active power filters or neutral current compensator applications for compensating harmonics and zero sequence. Four-leg converters have voltage vectors with γ component different from zero leading to the use of 3-D representations.

A generalized 3D-SVM algorithm with low computational cost for four-leg multilevel converters was proposed in [68]. This 3-D algorithm is a generalization of that proposed in [67]. Compared with [67], as the topology changes, the state-space vectors of the converter also change. However, once the subcube is known, almost all the necessary calculations to determine the switching sequence and the duty cycles are exactly the same. This 3D-SVM technique optimizes the switching sequence, minimizing the number of commutations for 4L-4W converters. As for the 3L-3W case, the low computational cost of this method is always the same, and it is independent of the number of levels of the converter.

In general, one of the advantages of SVM techniques for multilevel converters is the reduction of computation and implementation complexity compared to carrier-based PWM algorithms because the number of carriers does not increase as the number of converter levels increases. This advantage makes the digital implementation of the algorithms easier. In addition, the vector redundancies and the switching sequences can be used for other control purposes and can be designed according to a specific criterion depending on the application. It has to be noticed that in order to achieve a proper time average, the modulation period T_s is small, leading to high switching frequencies, comparable to carrier-based PWM (above 1 kHz), and therefore not useful for very high-power applications.

C. Other Modulation and Control Algorithms for Multilevel Converters

1) Selective Harmonic Elimination (SHE): Converters for very high-power applications are usually controlled with

low switching frequency algorithms, below 1 kHz. If traditional carrier-based PWM methods were used reducing the carrier frequency to these levels, low-order harmonics would appear in the output voltage, increasing distortion, which consequently will translate into performance problems. Selective harmonic elimination (SHE) is a low switching frequency PWM method developed for traditional converters in which a few (generally from three to seven) switching angles per quarter fundamental cycle are predefined and precalculated via Fourier analysis to ensure the elimination of undesired low-order harmonics [44]. Basically, in SHE, the Fourier coefficients or harmonic components of the predefined switched waveform with the unknown switching angles are made equal to zero for those undesired harmonics, while the fundamental component is made equal to the desired reference amplitude. This set of equations is solved offline using numerical methods, obtaining a solution for the angles.

This concept has also been extended for multilevel waveforms [69]–[71]. The basic idea is kept, i.e., a previously defined voltage waveform with a fixed number of switching angles, like the one in Fig. 21, is generated by the converter. By precalculating appropriately these switching angles, a number of undesired low-order harmonics can be eliminated in the output voltage. With m switching angles in a quarter-cycle, m control degrees of freedom are obtained, from which $m - 1$ can be used to eliminate undesired harmonics and the last one to control the amplitude of the fundamental component for reference tracking. As with traditional SHE, this can be achieved by computing the corresponding Fourier coefficients of the predefined waveform with the switching angles as unknown variables

$$h_n = \frac{4V_{dc}}{n\pi}\sum_{k=1}^{m}\cos(n\alpha_k) \tag{4}$$

where h_n is the amplitude of harmonic n. Note that $\alpha_1 < \alpha_2 < \ldots < \alpha_m < \pi/2$. The harmonics that should be eliminated are set to zero. The set of equations is then solved using numerical methods several times to cover a wide range of modulation indexes (amplitudes for the fundamental component). The solutions (angles) are stored in a lookup table, which is then used to modulate the converter.

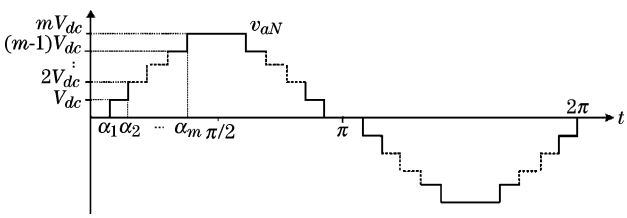

Fig. 21. ***Multilevel selective harmonic elimination.***

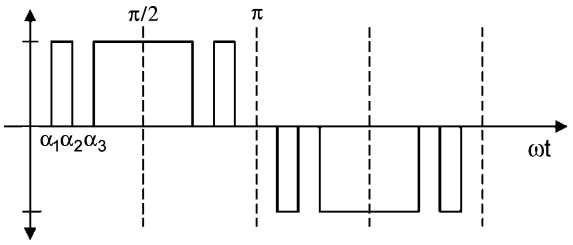

Fig. 22. ***Three-level selective harmonic elimination.***

As an example for a three-level converter, like the NPC, a typical waveform considering three switching angles $(\alpha_1, \alpha_2, \alpha_3)$ is given in Fig. 22. The corresponding Fourier series is given by

$$v_{aN} = \frac{4V_{dc}}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\{\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)\} \times \sin(n\omega t)|. \tag{5}$$

From this equation, three coefficients of the Fourier series can be forced to a desired value. Naturally, the first coefficient corresponds to the fundamental component and is set to the desired modulation index, while usually the fifth and seventh coefficients are set to zero (for fifth and seventh harmonic elimination)

$$\begin{aligned} M\cdot\frac{\pi}{4} &= \cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) \\ 0 &= \cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) \\ 0 &= \cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) \end{aligned} \tag{6}$$

where M is the modulation index. The third harmonic and its multiples are usually not eliminated using SHE, since they are naturally eliminated by the three-phase load connection. Fig. 23 shows the angles obtained for this example, the implementation diagram, and the output voltage with its corresponding spectrum, from which can be appreciated that the fifth and seventh harmonic are effectively eliminated.

Note that there is no control over the noneliminated harmonics, which usually tend to increase, since the eliminated harmonic energy present in the switched waveform is redistributed over the other ones. If these harmonic levels are not suitable for a particular application, additional angles can be introduced, eliminating more harmonics. For high power grid connected converters, there are very demanding grid codes making necessary several

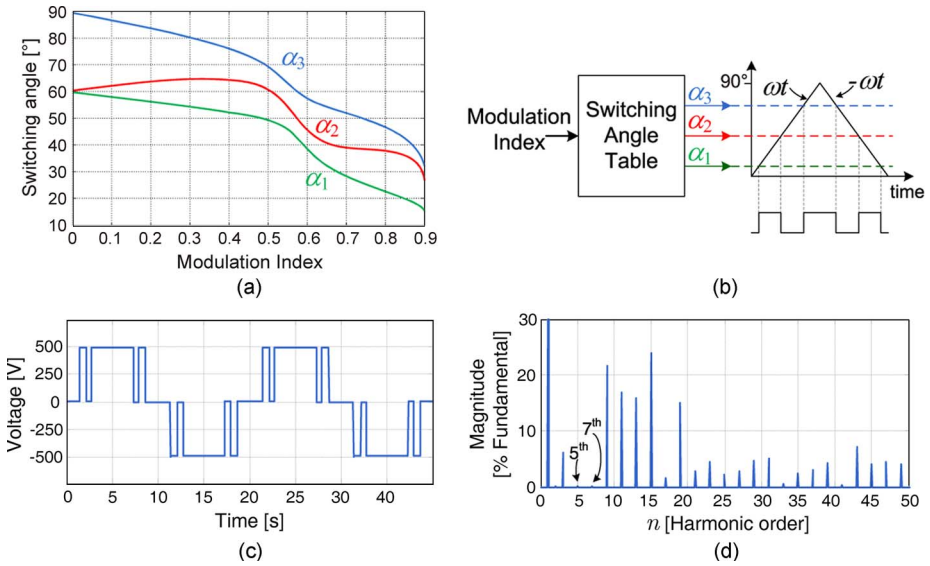

Fig. 23. ***Three-level selective harmonic elimination: (a) angles solution, (b) implementation diagram, (c) output voltage, and (d) output voltage spectrum.***

angles, which increases the switching frequency and losses or introduces the use of additional filters. In this case, a variation on SHE called selective harmonic mitigation technique (SHM) is more suitable. The main difference with SHE is that it does not force the angles to completely eliminate the harmonics by setting them to zero. Instead, inequalities are used to limit the harmonic content to acceptable values [72]. In this way, the harmonic spectrum of the obtained waveforms can fulfill current grid code regulations for the integration of energy systems into the distribution grid. The great advantage of SHM compared with SHE is the reduction (or even elimination) of the necessary grid connection filters, without sacrificing the power quality of the system. This leads to a reduction of the economical cost, volume, and weight of the overall power system.

For converters with a higher number of levels, like CHB, SHE is also known as staircase modulation because of the stair-like shape of the voltage waveform. The basic idea is identical to SHE; the difference is that each angle is associated to a particular cell. The operating principle of this technique is to connect each cell of the inverter at specific angles to generate the multilevel output waveform, producing only a minimum of necessary commutations [21]. The operating principle is illustrated in Fig. 24; note that only one angle needs to be determined per power cell. These angles can be computed using the same principles of SHE exposed before.

The main advantage, like in SHE, is that the converter switches very few times per cycle, reducing the switching losses to a minimum. In addition, low-order harmonics are eliminated, facilitating the reduction of output filter volume, weight, and cost.

All these methods require numerical algorithms to solve this set of equations, which are performed for several modulation indexes, leading to important calculations that are impossible to run in real time with current microprocessors and thus are executed offline. Therefore, the solutions are stored in lookup tables, and interpolation is used for those unsolved modulation indexes. This makes SHE-based modulation algorithms not suitable for applications demanding high dynamic performance.

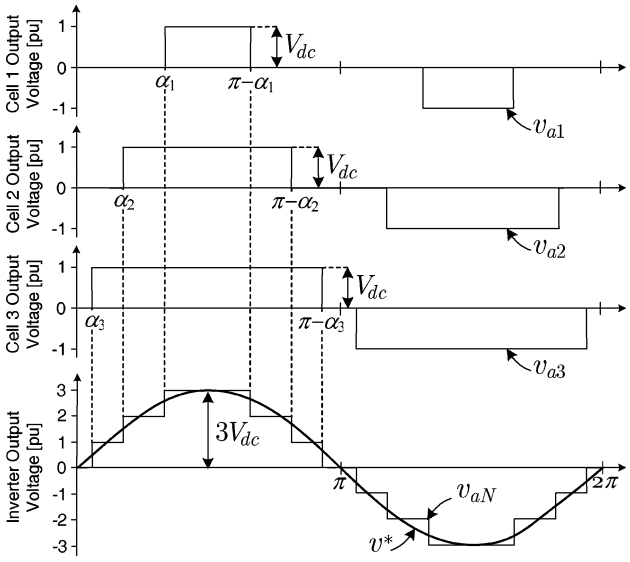

Fig. 24. ***Seven-level staircase modulation for CHB.***

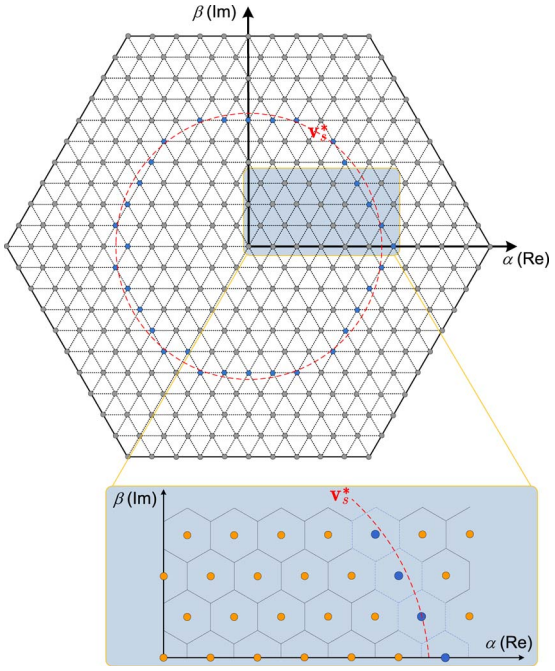

Fig. 25. ***Multilevel nearest vector control operating principle.***

2) Nearest Vector Control: Another method with low switching frequency is nearest vector control (NVC), which is also known as space vector control (not to be confused with the motor drive control technique with the same name). It was introduced in [73] as an alternative to SHE or staircase modulation to provide a low switching frequency modulation method, without the offline requirements and poor dynamic performance of SHE. The basic idea is to take advantage of the high number of voltage vectors generated by a multilevel converter by simply approximating the reference to the closest voltage vector that can be generated in the α–β plane, without even need of modulation. Therefore, this method is referred to as nearest vector control instead of modulation, since no time average approximation of the reference is performed.

This operating principle is shown in Fig. 25, where the state-space vectors for an 11-level multilevel inverter are illustrated, with a zoom to the NVC operating principle. Each dot is one of the possible voltage vectors generated by the inverter; they are surrounded by hexagons that represent the boundary of the area in which they are the closest available vector. The red dashed line is the voltage space vector reference ($\mathbf{v}_s^*$) trajectory through the complex plane. Hence, when the reference falls into a certain hexagon, the corresponding vector will be generated by the inverter. The selected vectors according to the illustrative example in Fig. 25 are highlighted in blue.

The natural selection of the closest vector produces a strong reduction in the number of commutations, since no commutations are forced by a modulator, reducing in this way the switching losses. This method, however, does not eliminate low-order harmonics (like SHE) and, due to its inherent low and variable switching frequency nature, can introduce low-order harmonics in the load voltage. This can be compensated by using multilevel converters with a high number of levels (usually above seven), which have a more dense state-space vector availability, resulting in a better vector approximation and smaller error. They also have an intrinsic low THD due to the small dv/dt, reducing the effect of the low-order harmonics. An alternative method that also reduces the common-mode voltages is presented in [74].

These methods have very simple operating principles; however, the implementation is not as straightforward, since an algorithm capable of finding numerically the closest vector needs to be programmed. This technical issue can be found in detail in [73] and [74].

3) Nearest Level Control or Round Method: The nearest level control (NLC), also known as the round method, is somehow the per-phase time-domain counterpart of NVC [75], [76]. Basically, the same principle is applied but to voltage levels instead of space vectors, thus selecting the nearest voltage level that can be generated by the inverter to the desired output voltage reference. Unlike with SVC, where the three phases were controlled directly with the vector selection, here the three phases are controlled independently with their respective 120° phase-shifted references. The main advantage is that the algorithm is greatly simplified in relation to NVC, since it is much easier to find the closest level than the closest vector. In fact, the output voltage level selection is reduced to a unique simple expression per phase

$$\text{closest voltage level} = v_{aN} = V_{dc} f_{\text{round}} \tag{7}$$

where V_{dc} is the voltage difference between two levels (usually the dc-link voltage in CHB), which is used to normalize the phase output voltage reference v^*. The normalized value is then evaluated using the round function (or nearest integer function), which is defined such that $f_{\text{round}}\{x\}$ is the integer closest to x. Since this definition is ambiguous for half-integers, the additional convention is that half-integers are always rounded to even numbers, for example, $f_{\text{round}}\{1.5\} = 2$. This nearest integer multiplied by V_{dc} corresponds to the closest voltage level to the reference, and thus is generated by the inverter.

The operating principle is illustrated in Fig. 26(a) for the first quarter-cycle of a sinusoidal reference. Note that the maximum approximation error is $V_{dc}/2$. The implementation of the nearest voltage level generation is presented in Fig. 26(b). As can be seen in Fig. 26(a), the round function inherently produces only one commutation between two voltage levels and a maximum dv/dt of V_{dc}, unless the reference presents large step changes.

It is worth mentioning that this method is not a modulation technique, since there is no reference tracking

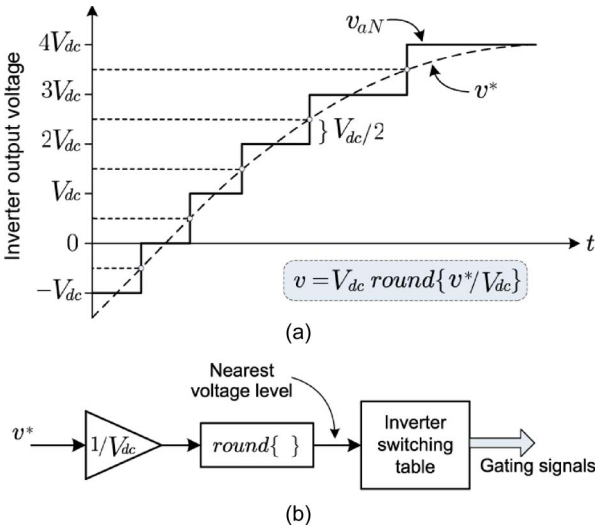

Fig. 26. ***Nearest level selection: (a) waveform synthesis and (b) control diagram.***

by time average synthesis between two levels. Instead, the stepped waveform is generated as an approximation to the reference. Although the voltage waveform is very similar to the one obtained with staircase modulation, it does not eliminate specific harmonics because it is not really a modulation. Therefore, this control method, like NVC, is not effective for converters with a reduced number of levels, since the approximation error becomes relevant. Hence it is aimed to be used in converters with a high number of levels to avoid important low-order harmonics at the ac side. The main advantage is its conceptual and implementation simplicity and the efficiency achieved with this method. An adaptive modulation method that solves this problem by introducing a duty-cycle calculation to NLC has been proposed [154], at the expense of a more advanced control algorithm.

It is also worth mentioning that there are other control algorithms that select the switching state and switching times of multilevel converters but are not a modulation or control stage dedicated to the converter; instead they are a direct consequence of the overall system controller. This is the case of direct torque control of ac motors, where the switching states and transitions are directly obtained from the torque and flux controller of the motor [155], [156]. Another method where the switching states and switching times are directly computed by the controller is finite control set model predictive control, which also has been applied to multilevel converters [157].

V. RECTIFIERS FOR MULTILEVEL INVERTERS

Multilevel inverters like NPC and FC require a medium voltage dc source [45], [46], while in CHB inverters, several isolated dc sources are needed [47]. To provide these dc voltages, different topologies of rectifiers can be used. Each proposed configuration provides different possibilities to cancel harmonics in the input current, minimizing the impact on the ac network.

These rectifiers can be divided into nonregenerative, i.e., diode-based and regenerative or active front-end (AFE) rectifier.

A. Nonregenerative Rectifiers

Three-phase full bridge diode-based rectifiers provide a low input energy quality due to the six pulse current, which has high harmonic content, especially low-order harmonics. However, when several of these rectifiers are used in combination with a multipulse transformer, it is possible to cancel out low-order characteristics harmonics and provide a nearly sinusoidal multipulse input current [21].

The basic configuration corresponds to the double bridge rectifier fed by a delta-delta-wye transformer, which is shown in Fig. 27. Each six-pulse rectifier generates characteristic current harmonics of the same amplitude but, due to the phase angle between the transformer secondaries, the fifth and seventh harmonics are canceled. This principle can be extended when more rectifiers are used, reducing or even eliminating a number of harmonics two times the number of diode rectifiers used. To produce a proper harmonic cancellation, the phase angle between secondaries must be $60^\circ/m$, where m is the number of rectifiers [60].

In NPC and FC inverters, the dc voltage is obtained using several diode rectifiers in series, producing a single dc source for the complete converter (for all three phases). Therefore, the power is equally distributed between each rectifier, and the current harmonics can be almost canceled. The number of necessary rectifiers in series will depend on the rated voltage of the dc-link.

When a CHB inverter is used, each individual rectifier is used to produce an isolated dc source for each H-bridge. Hence, the power delivered by each rectifier depends only

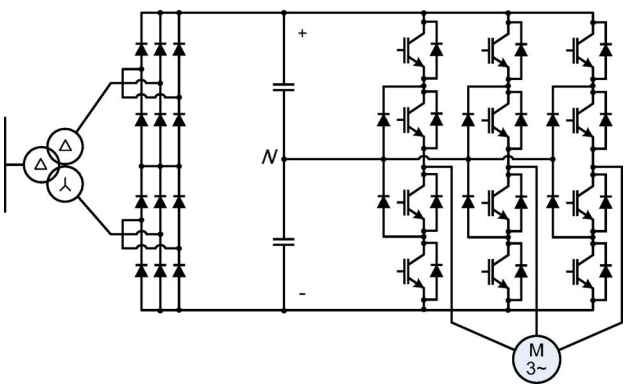

Fig. 27. ***Double diode-based rectifier in combination with a delta-wye transformer.***

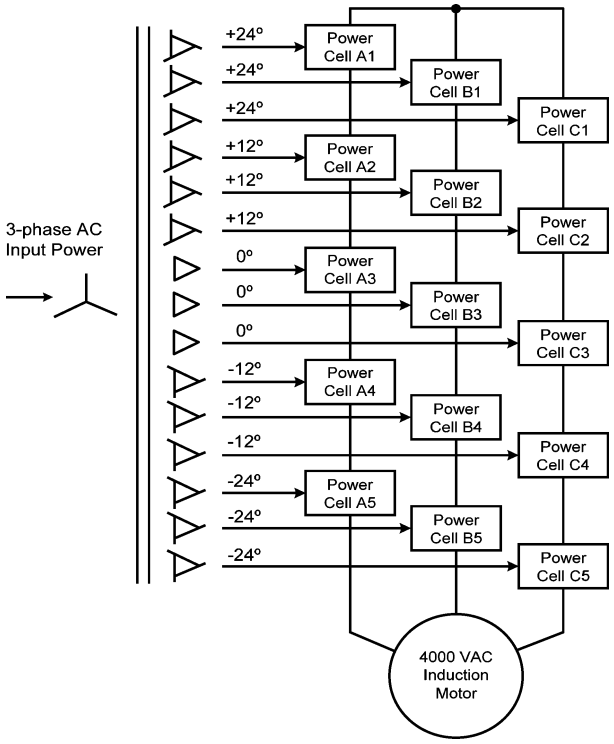

Fig. 28. ***Multipulse transformer feeding 11-level cascaded inverter.***

on the load of the corresponding phase. Therefore, to reduce harmonic distortion, the rectifiers are connected to the transformer secondaries in groups of three (one on each output phase) with the same angle displacement, as shown in Fig. 28.

Generally, each cell of a CHB inverter is fed by a three-phase diode rectifier (for nonregenerative applications), like the one shown in Fig. 29. Single phase rectifiers can also be used, reducing the number of components and simplifying the transformer design [77], but at the expense of an increase in the input current harmonics.

Diode rectifiers are directly affected by ac network disturbances, producing variations on the dc voltage [78]. Usually, the control scheme of the inverter can reject these perturbations, providing a stable energy to the load. However, when a controlled dc voltage is required, a controlled or semicontrolled thyristor-based rectifier can be used, as shown in Fig. 30, used with a flying capacitor inverter. In addition, with a controlled rectifier, it is possible to keep a constant dc voltage, protecting the dc capacitor from overvoltages and reducing the requirements of the inverter controller.

In general terms, multilevel converters using several rectifiers and a proper transformer configuration provide a good-quality input current. However, the main drawback of these rectifiers appears when regenerative loads are fed, reducing the efficiency of the system by introducing resistive chopper circuits to dissipate the extra energy entering the dc link. An alternative for this inefficient approach is the use of a regenerative rectifier.

B. Regenerative Rectifiers

Several loads like elevators, trains, and downhill conveyors need to regenerate energy back into the ac network. Power converters based on diode rectifiers do not provide regenerative operation, requiring a resistive chopper to handle this energy and reducing the overall efficiency [42].

Regenerative converters based on active rectifiers can take the energy provided by the load and put it back on the ac network, increasing the efficiency of the power-conversion system, especially when the load regenerates constantly, like downhill conveyors [41].

Replacing the diode rectifier and the transformer with the same inverter topology, a back-to-back configuration is obtained. These configurations are shown in Fig. 31 for an NPC inverter and Fig. 32 for an FC inverter. These rectifier configurations have been successfully implemented in regenerative conveyor in the mining industry [79] and wind energy conversion [80]. The main advantage of this scheme, besides its regenerative operation, is that the same hardware is required for both rectifier and inverter side. Only different control strategies are required. The rectifier control not only is used to control the dc link voltage but also is employed to control the input current at will, obtaining lower distortions than with the diode rectifier

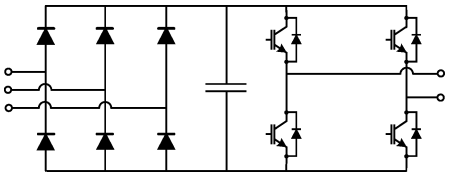

Fig. 29. ***Single phase rectifier based power cell.***

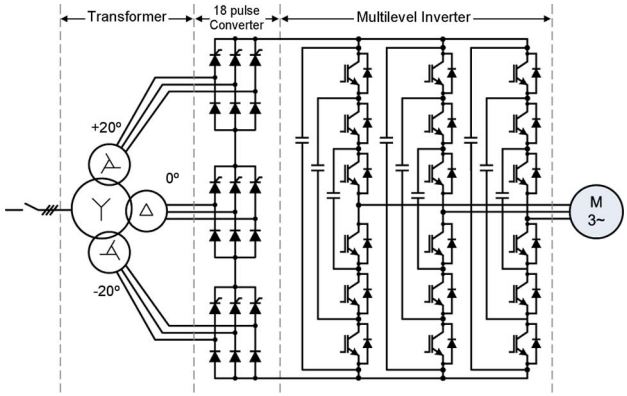

Fig. 30. ***Semicontrolled rectifier in combination with a 18-pulse transformer to provide a regulated dc voltage.***

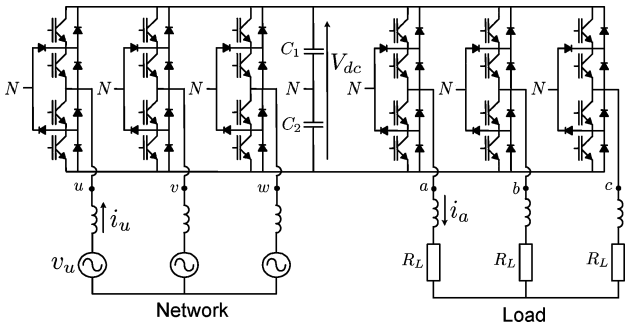

Fig. 31. *Back-to-back NPC configuration.*

with multipulse transformer. Moreover, since the input current can be controlled by the rectifier, there is no special need of winding angle shifts in the transformer, simplifying its design.

In CHB converters, the diode rectifier is replaced by a three-phase voltage source rectifier or AFE rectifier for each power cell, providing the regenerative operation as needed. However, the input transformer cannot be eliminated, because it is needed in order to provide the required isolated dc sources. Usually this AFE is a three-phase rectifier like the one shown in Fig. 33. On the other hand, several single-phase regenerative rectifier configurations have been proposed [81], in order to reduce switch and component count. Here, the transformer can also be simplified, since no winding angle shifts are necessary.

VI. OPERATIONAL AND TECHNOLOGICAL ISSUES

A. DC-Link Voltage Balance for NPC Inverters

The balance of the dc-link capacitor voltage is one of the most important concerns in NPC multilevel converters. Many control strategies to achieve this balance have been presented in the last years [82]–[94].

In general, most of these strategies use the well-known technique based on choosing between redundant state-space vectors. As was introduced in the SVM section, two state vectors are redundant if they are located in the same position of the α–β plane. For instance, switching state vectors $(0,-,-)$ and $(+,0,0)$ are redundant, as can be observed from Fig. 19. Therefore, redundant vectors generate the same phase-to-neutral load voltages, and hence there is no difference from the load point of view to use either of them. However, from the inverter point of view, the redundant space vectors have different effects on the dc-link capacitor voltages, and therefore they can be used for balance control.

By measuring the dc voltage unbalance (difference between capacitor voltages) and the sign of the load phase currents, it is possible to choose the redundant vector that tends to balance the dc voltages. This is always necessary for NPC topologies, where the dc-link unbalance is a common problem. FC inverters do have natural balancing when used with PS-PWM, although for other modulation methods or for a faster dc-link balance dynamics, the same concepts based on state redundancies can be applied. Traditional CHB inverters do not have voltage unbalance problems, since they are fed by independent dc sources. However, variations on the CHB, for example, where only one cell is fed by a dc source while the others are floating, also require this type of unbalance control algorithms [153].

It should be noticed that when increasing the number of levels of the converter, the number of redundant vectors in the control region increases overproportionally. In fact, the number of state vectors for an n_p-level converter is n_p^3, and the number of redundant vectors (NRV) can be determined using the expression

$$\mathrm{NRV} = n_p^3 - 1 - \sum_{i=1}^{n_p-1} 6i. \tag{8}$$

The increasing number of redundancies makes difficult the design of a criterion to choose the most convenient redundant vector to control the voltage unbalance. In

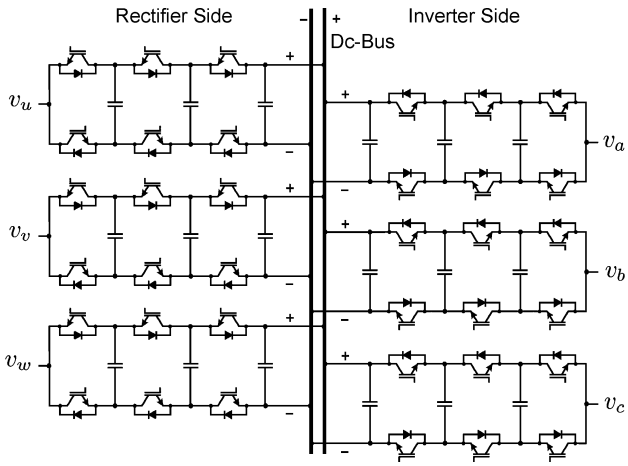

Fig. 32. *Back-to-back FC configuration.*

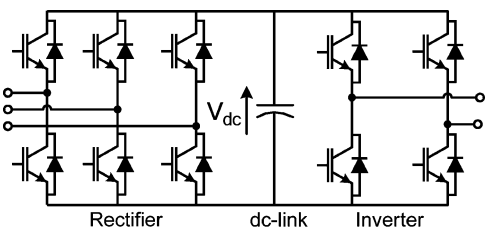

Fig. 33. *Three-phase AFE rectifier-based power cell.*

addition, sometimes the dc voltage balance in multilevel converters cannot be achieved depending on the modulation index and the power factor of the load [95].

Moreover, even if the dc voltages can be controlled around their desired values, additional low-frequency harmonics appear in the dc voltages, which can affect the modulator performance. This problem is not exclusive to multilevel inverters; it is common to all voltage source inverters and has direct relation with the dc-link capacitance value, the rectifiers' input frequency, and the inverters' output frequency. Some recent modulation strategies have been presented in order to minimize the oscillations of the dc voltages in multilevel converters. These strategies are capable of reducing the unbalance and oscillations of the dc voltages at the expense of increasing the power semiconductors' switching frequency [92]–[94]. Other modulation methods take into account the dc voltage unbalance using feedforward strategies to compensate the oscillations within the modulation stage, generating a precompensated output voltage that cancels out the distortion produced by these low-frequency components [96]–[99].

In conclusion, the balance of the dc voltages of NPC multilevel converters has been an important research drive over the last decades. Nowadays, NPC converters have an important industrial presence in medium-voltage drives, and hence this issue can be considered as a solved problem for three-level inverters.

B. Multilevel Converter Modeling

Modeling and simulation of multilevel converter systems are fundamental tasks for their analysis and design process. In addition to the problems related to conventional power-converter systems, the modeling of multilevel converters presents new challenges that the engineer has to overcome, mainly due to the more complex power circuit and more available switching states.

Due to the wide range of topologies and operating principles available in multilevel converters, several modeling approaches have been derived. However, all of them take into account the fact that the converter periodically switches among a finite set of different switching states that lead to different transitory power circuits. In [100], a detailed and systematic classification of models for dc–dc power-electronic converters can be found. Since most modeling techniques for three-phase multilevel converters have been derived from those applied to dc–dc converters, this classification can be considered as a reference for the variety of models that can be found. The description of this wide range of models is out of the scope of this paper, so only the most relevant and recently reported ones will be introduced in this section. Fig. 34 shows the main modeling techniques used to analyze, design, and simulate multilevel converters. In addition, the figure shows the order in which each model is deduced from the previous one.

1) Detailed Switching Models: The use of powerful and advanced circuit simulation software packages as SPICE or SABER for power-electronic converters has been widely reported. The simulation results, when carried out successfully, gives very detailed information about the behavior of the power converter, but this modeling simulation technique has some serious drawbacks.

1) Good user-defined models for semiconductor switches are needed to get feasible results [101]–[103].
2) A very realistic circuit characterization is needed to avoid convergence problems and to obtain a stable simulation [104], [105].
3) Due to the fact that those software packages are designed for circuit simulation, integration in the model of control systems or modulators is possible only with low-complexity systems [106], [107], being almost impossible for complex control schemes and advance modulation techniques.

2) Simplified Piece-Wise Switching Model: Due to the switching action, which is common on power electronics circuits and hence on multilevel converters, the system periodically switches among a finite set of different circuit topologies. Electrical analysis of each configuration can be made, obtaining a set of differential equations that describe the dynamics of the converter for every switching state. For the compactness of the system equations to be derived, one switching function can be defined for each possible configuration of the switches. The switching function takes value "1" when the switch states correspond to that switching function and value "0" in any other case.

With the aid of switching functions and considering ideal switches (negligible commutation times and saturation voltages), every converter topology can be represented by a state equation model of the system given by

$$\frac{dx}{dt} = Ax + Bu \tag{9}$$

where x are the chosen system variables, u is the input vector, and A and B matrix elements are the switching functions and linear element parameter values.

Usually this modeling approximation is used under idealized conditions, but similar state-space models are not hard to obtain for more elaborate, less idealized, and

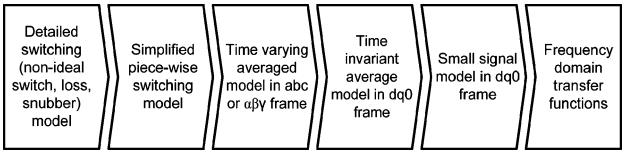

Fig. 34. ***Most common modeling techniques in multilevel converters.***

different topologies, for instance, capacitor equivalent series resistance, switch conduction losses, and saturation voltages. Simulations carried out with these models include the switching behavior of the circuit, so the ripple on currents and nonsinusoidal magnitudes can be analyzed. On the other hand, the controller is hard to derive from these models, and only some control techniques, such as sliding mode control (bang bang), can be directly applicable.

3) Time-Varying Averaged Models in a–b–c or α–β–γ Planes: The generalized state-space averaging method [108], [109] is a widely used tool for large signal dynamic modeling of power converters. The method is based on the fact that a waveform $x(t)$ can be approximated on the interval $(t-T, t]$ to any desired accuracy by the Fourier series

$$x(t) = \sum_{k=-n}^{k=n} \langle x \rangle_k(t) e^{jk\omega t} \tag{10}$$

where $\omega = 2\pi/T$ and

$$\langle x \rangle_k(t) = \frac{1}{T} \int_{t-T}^{T} x(\tau) e^{-jk\omega t}\, d\tau. \tag{11}$$

In (11), $\langle x \rangle_k(t)$ is the kth complex coefficient of the Fourier series expansion and n is an integer. If n approaches infinity, the approximation error becomes zero. In most cases, it suffices to consider only a few terms (one or two harmonics), but sometimes higher order harmonics are necessary to correctly model the dynamics of the system magnitudes [110], [111]. The application of this method to the state-space model is based on the following two important properties of the Fourier coefficients:

$$\begin{aligned} \frac{d}{dt}\langle x \rangle_k(t) &= \left\langle \frac{d}{dt} x \right\rangle_k(t) - jk\omega \langle x \rangle_k(t) \\ \langle xy \rangle_k(t) &= \sum_{n=-\infty}^{n=\infty} \langle x \rangle_{k-n}(t) \langle y \rangle_n(t). \end{aligned} \tag{12}$$

Applying those properties, both sides of the state-space equation can be expanded to any desired number of terms to find the dynamic of the time evolution of every signal with the desired degree of accuracy.

The generalized state-space averaging method has been applied to different multilevel converter topologies: for NPC [112], [113], FC [110], [111], and CHB [114]. It must be noticed that all these contributions use carrier-based PWM modulation strategies in order to obtain an analytical representation of the switching functions and, in this manner, achieve the application of the method. This is a serious drawback since other modulation strategies, as SVM, cannot be directly integrated in the model to achieve the application of the averaging method. To solve this limitation, instead of averaging the converter state equations, the characteristics or waveforms associated with each of the components in the converter can be directly averaged. This approach is used in [115] and [116] for three- and five-level NPC converters, respectively, where, due to the characteristics of this topology, an additional approximation in the switches is necessary to obtain a unique averaged circuit valid all over the range of existence of the control inputs.

The idea behind the circuit averaging is to work on the schematic, replacing the switches (nonlinear elements) by equivalent voltage or current sources. Since the averaged circuit still fulfils Kirchhoff's laws, once the switches have been replaced by the corresponding sources, the model of the converter can be developed directly by circuit analysis techniques. In [117], this averaging method is applied to a five-level CHB. Modeling methods have also been developed for the α–β–γ plane [115], [118].

4) Time-Invariant Averaged Models in dq0 Frame: Previous methods considered large-signal time-varying models, since ac quantities are time-varying even in steady state. From the control design point of view, it would be more suitable to have time-invariant models. Considering a balanced sinusoidal system, without harmonics, it can be transformed into the $dq0$ rotating reference frame [110], in which the ac system variables appear fixed. In this way, the model equations will correspond to time-invariant systems. However, usually nonlinear models are obtained; hence nonlinear control techniques such as feedback linearization [119], nonlinear quadratic optimal control [120], or neural networks [121] should be considered for controller design.

5) Small Signal Model in dq0 Frame: The modeling techniques described previously provide models that are time-varying or, in most cases, nonlinear. Assessing stability, designing and evaluating controllers with nonlinear models is usually difficult and requires application of specific and complex control techniques, as has been stated in the previous section. In addition, the application of nonlinear controllers is not systematic, and each system configuration must be studied in order to accommodate the technique to the model characteristics.

Small signal analysis is crucial to evaluate nominal operating conditions, with the linearization being the most common systematic and generally successful approach to obtain the small signal model of the converter. The linearization makes sense when applied to time-invariant models, so the small signal model is usually obtained from the averaged time invariant in $dq0$ reference frame. In [122] and [114], a detailed description of the small signal

models for a multilevel FC and CHB can be found, respectively.

C. Multilevel Inverter Fault-Tolerant Operation

There is a growing interest from industry to reduce stop times and increase availability through system monitoring, fault detection, fault diagnosis, and fault-tolerant operation. This can result in cost reduction, increased productivity, and even safety improvements. This is a challenging task, not easy to achieve with traditional power converters. Instead, multilevel converters (particularly FC and CHB inverters) have several characteristics that make it possible: they have modular and scalable structures and have redundant switching states, as seen previously. Several contributions of fault detection and tolerant operation for the FC, CHB, and even for the NPC have been reported [123]–[136].

In power converters, the failure types can be dc-link short-circuit to ground, dc-link capacitor bank short-circuit, open circuit damage of switches, short-circuit damage of switches, line-to-line short-circuit at load terminals, and single line to ground fault at machine terminals. All these kinds of failures are mostly related to the power semiconductors, the gate drivers, and the dc-link capacitors.

To be able to achieve fault-tolerant operation, it becomes necessary to have knowledge about the type of fault and where it has occurred. Therefore, fault detection and fault diagnosis are required. A straightforward fault-detection mechanism is to measure currents and voltages across all the components. This alternative is very precise but not a cost-effective solution, considering the amount of components available in a multilevel converter. Another fault-detection scheme relies on the output voltages and current measurements, thus reducing the number of necessary sensors, but the detection dynamics depends on the load characteristics [123]. Another alternative fault-detection method, used in NPC inverters to detect open circuit faults, is to sense the pole voltages [124]. The pole voltage includes information of switching states in the NPC inverter, concerned by the dc-link but not affected by the load. During abnormal operating conditions, the pole voltage is determined by the direction of the phase current and the switching state for each phase. In this condition, it is necessary to discriminate whether the outer or inner switch is the faulty one and bypassed it using auxiliary switches [124]. The previous discrimination can be done comparing the pole voltage with the switching pattern. If the voltage remains in zero when a switching pattern is applied, the direction of the current defines which of the outer switches has failed. On the other hand, if the current remains at zero when a switching pattern is applied, the sign of the pole voltage defines which inner switch has failed.

In [125]–[128], the characteristic high-frequency harmonics produced by FS-PWM are used to detect a faulty power cell in FC and CHB converters. Using

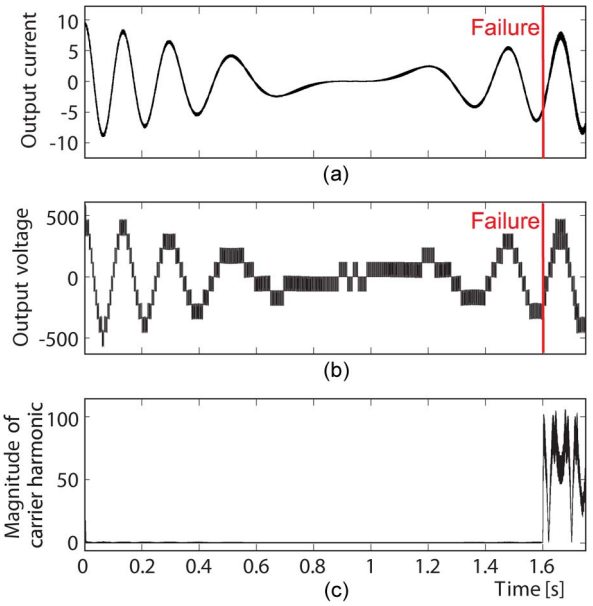

Fig. 35. ***Fault detection in a CHB: (a) load current, (b) inverter output voltage, and (c) fault detection by monitoring the amplitude of the f_{cr} component.***

PS-PWM, the carriers of frequency f_{cr} for each cell are shifted in such a way that no f_{cr} component should appear in the output voltage. However, under fault condition, the magnitude of the phasor related with the faulty cell changes; then a component at frequency f_{cr} appears in the output voltage. Once the presence of the component at f_{cr} has been detected, the angle of the resulting phasor is calculated. This angle gives information about which one is the faulty cell. Thus, by only measuring the three output voltages of the converter (only three sensors), a fault can be detected instead of using, for example, 24 measurements to detect semiconductor malfunction in a three-phase five-level CHB. Fig. 35 shows this fault-detection method when a fault has occurred; t = 1.6 s [128] in a closed-loop system operation.

Once a fault has been detected, the power circuit can be reconfigured, isolating the defective part. This is why it can be more easily achieved for FC and CHB, since they are modular in structure.

For the NPC, more hardware will be needed in order to provide sufficient flexibility to isolate a defective part of the circuit. In Fig. 36, two approaches of additional hardware are highlighted in different color. The one on the right is an additional NPC inverter leg connected through triacs to all the phases; hence the one experiencing a fault can be isolated and replaced. This solution can be found in more detail along with other reconfigurations for the NPC in [137]. The solution shown on the left in Fig. 36 is based on an additional FC inverter leg with its output connected to the neutral point of the NPC. This additional leg can be used to control the dc-link voltage and provides the extra

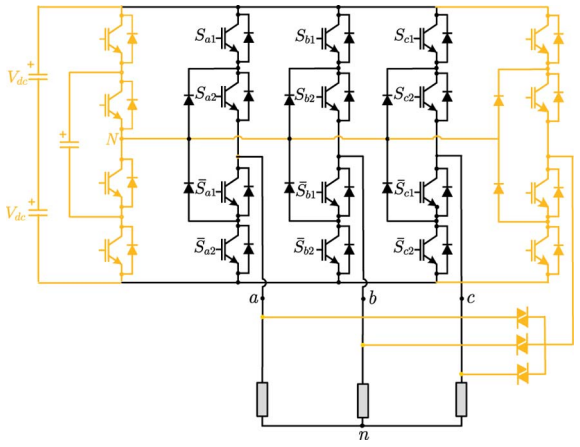

Fig. 36. *Two alternatives of modifications to the NPC topology for fault operating capability: (a) with additional FC inverter leg and (b) with additional NPC inverter leg.*

hardware necessary for fault-tolerant operation. More details on this solution can be found in [136].

In [132] and [133], fault-tolerant operation of CHB is analyzed. A switch is added in each power cell of a CHB, as shown in Fig. 37, in order to bypass the cell in case of failure. Hence the converter will reduce its output voltage in the phase where the cell has been bypassed, leading to unbalanced voltages, although it will continue operating. Nevertheless, this unbalance can be corrected in two ways: bypassing the same amount of cells in all phases of the converter (this will reduce the total power delivered by the converter) or by changing the angle between the references of each phase, in such a way that the line voltages are balanced. This solution can be appreciated in Fig. 38, where the phase voltage of an 11-level (five power cells per phase) CHB is presented, with two bypassed cells in phase c and one in phase a. In Fig. 38(a), the failure cells are only bypassed, producing an unbalanced output voltage. In Fig. 38(b), the reference voltage for each output phase is changed in order to balance the line-to-line voltage and maximize its value. Results for this method are shown in Fig. 39. Note how the change in the angles introduced for the references makes them look unbalanced; instead, the line–line voltage and load currents appear completely balanced.

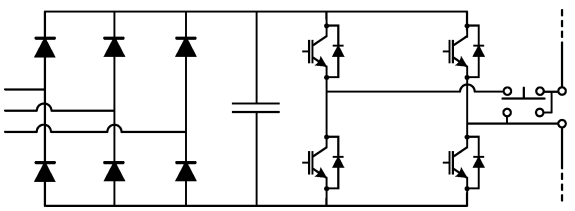

Fig. 37. *CHB power cell for fault-tolerant capability.*

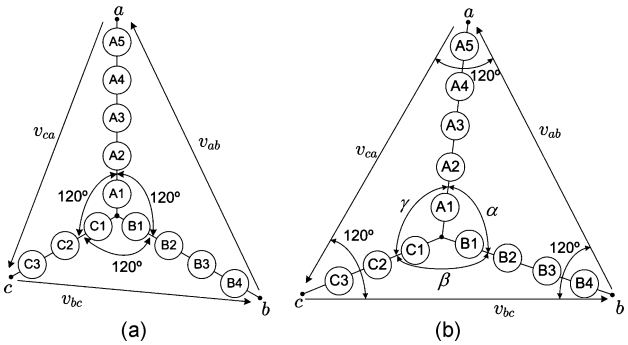

Fig. 38. *Phase and line voltages for an 11-level five-cell CHB converter with two faulty cells in phase c and one in phase a. (a) Cells are bypassed an unbalanced operation is obtained. (b) Cells are bypassed and the references have been changed in angle, achieving balanced operation.*

VII. MULTILEVEL CONVERTER APPLICATIONS

As mentioned earlier, multilevel converters have found an important market penetration in high-power medium-voltage applications, where the power range and power-quality limitations of classic topologies justifies their use. In this section, some well-established and other multilevel converter applications under development are presented. They are organized by field of application.

A. Energy and Power Systems

Grid-connected systems, such as flexible ac transmission systems (FACTs), regenerative converters, and renewable energy to grid systems, to name a few, share a main development drive: power quality and efficiency. And

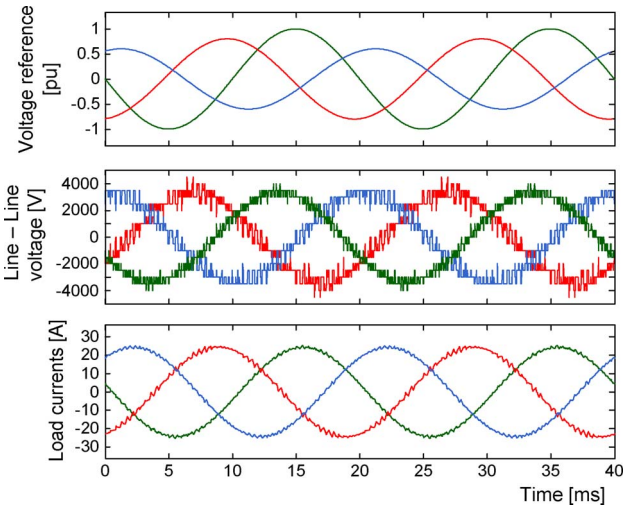

Fig. 39. *Fault-tolerant operation of an 11-level five-cell CHB converter with two faulty cells in phase c and one in phase a: (a) unbalanced references, (b) balanced line–line voltages, and (c) load currents.*

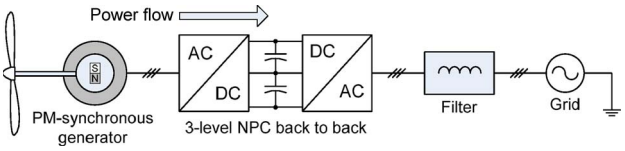

Fig. 40. ***Three-level NPV back-to-back for wind energy conversion.***

because several of these applications are going higher in power levels, it is no wonder that multilevel converters have attracted attention as a convenient solution. Nowadays, the integration problem is one of the main concerns of renewable energy providers because new grid codes related to this topic have been presented in recent years and are now coming into effect. This has motivated research and development in multilevel converter technology for grid connection of renewable energy sources [32]. In particular, wind energy conversion benefits in terms of efficiency of larger wind turbines that today can reach up to 5 MW. Therefore, multilevel topologies have been proposed, mainly NPC back-to-back configurations [32], [138], [139], such as the one in Fig. 40. Note that the ac–dc/dc–ac converter corresponds to the one shown in Fig. 31.

Photovoltaic (PV) power-conversion systems are not yet in the multilevel power rate range. Nevertheless, there are some photovoltaic farms reaching levels of several tens of megawatts, and it is expected to increase with photovoltaic technology development and cost reduction. Here multilevel converters can also become relevant, since PV strings can be used as dc sources for multilevel topologies. Since there is no need for a rectifier stage, the multilevel power circuit is greatly reduced. In addition, the multilevel converter can provide control for both maximum power tracking and input power factor. Moreover, it reduces the need for a filter, can improve efficiency (lower switching frequencies can be applied), can eliminate the need for step-up transformers, or boost elevator circuits if enough PV sources can be connected in series. Several works using CHB connected to the grid have been reported for PV power conversion [32]. Fig. 41 shows the configuration analyzed in [140] and [141].

On the other hand, an actual problem of the electrical grid is the power-distribution control and management. In this case, FACTs have been introduced as the solution in order to enhance the controllability and the power-transfer capability of the network. Among the many different technologies covered by FACTs, the most interesting one for multilevel converters is in distributed energy applications, where the development of active filters (AFs), static compensators (STATCOMs), dynamic voltage restorers (DVRs), and unified power flow controllers (UPFCs) can provide instantaneous and variable reactive power in response to grid voltage transients, enhancing the grid voltage stability [142]–[145]. These devices (AF, STATCOMs, DVRs, and UPFCs) are currently gaining importance due to the harmonic spectrum requirements from the energy providers and the requirement of riding through the voltage sags imposed by the grid codes all over the world. As examples, the diagram of a three-level diode-clamped converter working as a STATCOM and a scheme of a multilevel converter working as a UPFC are shown in Figs. 42 and 43, respectively; more details can be found in [142]. Other applications include utility adapters, for example, to connect a three-phase grid of 50 Hz and a single-phase grid of 16 2/3 Hz for railway application [146].

B. Production

Multilevel converters can be found in almost any medium-voltage high-power motor drive application, having found widespread presence in the petrochemical industry (pumps and compressors), cement industry (high power fans), metal industry (steal rolling mills), and

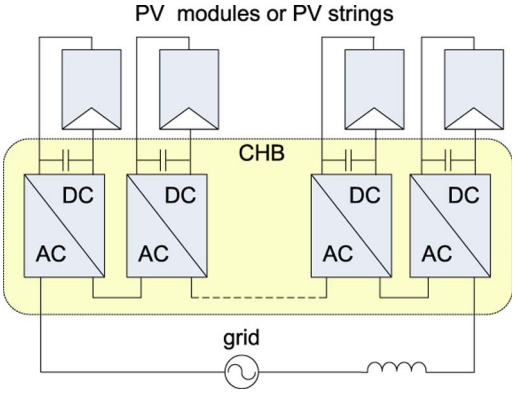

Fig. 41. ***Grid connection of PV system using CHB.***

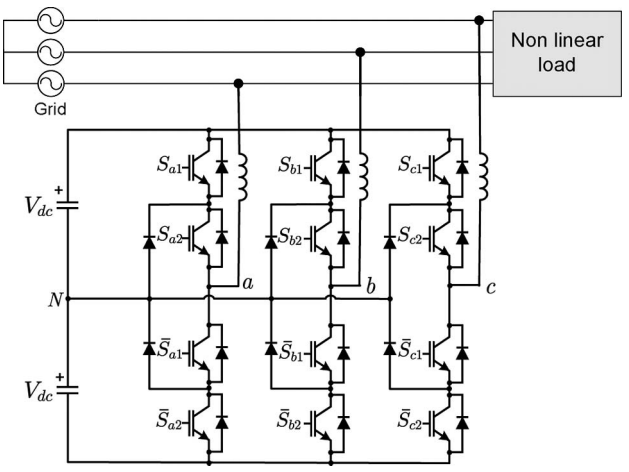

Fig. 42. ***STATCOM based on a three-level diode-clamped topology.***

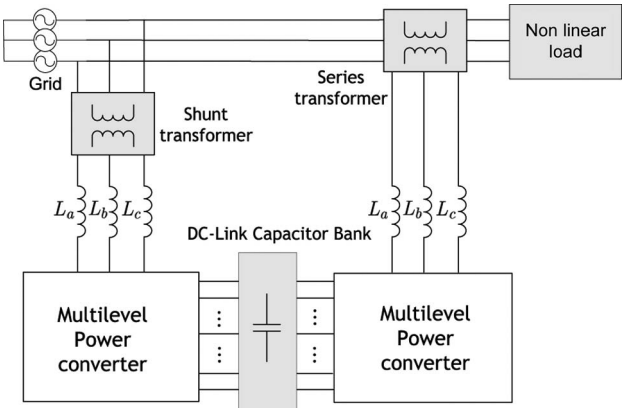

Fig. 43. ***UPFC based on multilevel converter topologies.***

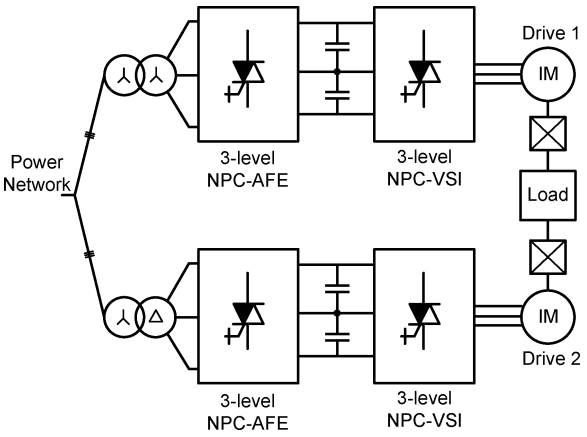

Fig. 45. ***Conveyor motor drive scheme.***

mining industry (copper grinding mills and conveyors for ore transportation), among others. The latter is exposed in the next section.

1) Regenerative Conveyors: Downhill conveyors are used in the mining industry as an alternative to transport the ore produced in the mine to another mining process. Fig. 44 shows an example of a downhill conveyor located in a Chilean mining facility [41]. The system operates almost continuously regenerating, requiring a power drive that allows this operating condition in order to improve overall efficiency.

The conveyor is designed to transport 5800 [ton/h] of mineral. The mine stock pile is located at 1307 [m] above the concentrator plant level. The average inclination is 11% and can reach 24% at some places.

The total path is divided in three sections of different lengths: 5905 [m], 5281 [m], and 1467 [m]. Each section has a motor drive in a configuration shown in Fig. 45, where two ac–dc–ac drives feed induction motors that control the conveyor by means of two gearboxes. The delta-delta-wye transformer connection achieves 12-pulse operation, improving the input current quality.

Each ac–dc–ac drive is composed of a three-level active front-end NPC rectifier connected in a back-to-back configuration with a three-level NPC inverter. Each single drive has a power of 2500 kW. Both sides are implemented using gate turnoff thyristors (GTOs) as power semiconductors. The AFE is modulated using an SHE modulation technique to achieve low switching frequency, allowing to eliminate low-order harmonics (11th and 13th) not eliminated by the transformer connection [79]. The main features of this drive configuration are [147] and [148]:

- fully regenerative operation;
- extremely low input current harmonic content;
- adjustable input power factor.

C. Transportation

Multilevel converters have an important presence in state-of-the-art high-power transportation systems such as ship propulsion and high-speed train traction. Large ship propulsion, above 25 MW, has mainly been dominated by cycloconverters and load commutated inverters. However, in recent years, there has been an important market penetration of NPC and CHB topologies for this application.

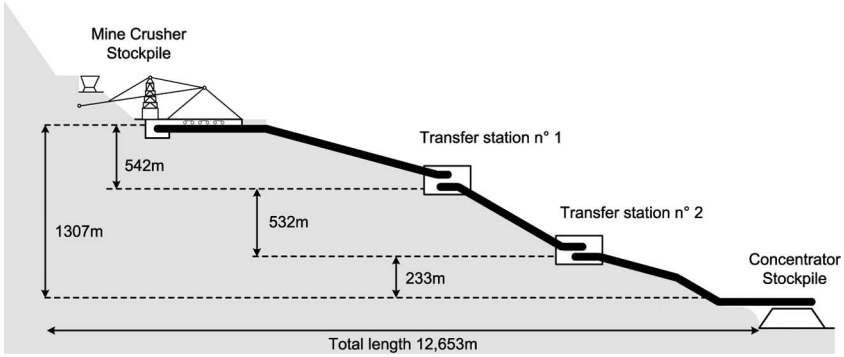

Fig. 44. ***Downhill conveyor system example.***

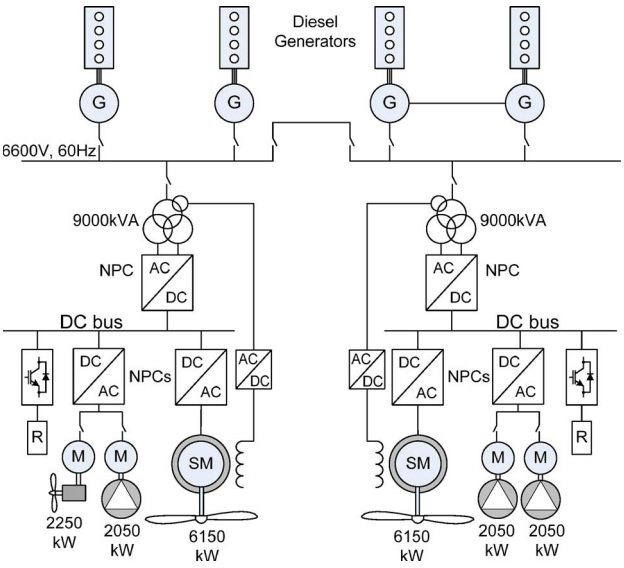

Fig. 46. ***Tanker propulsion power system.***

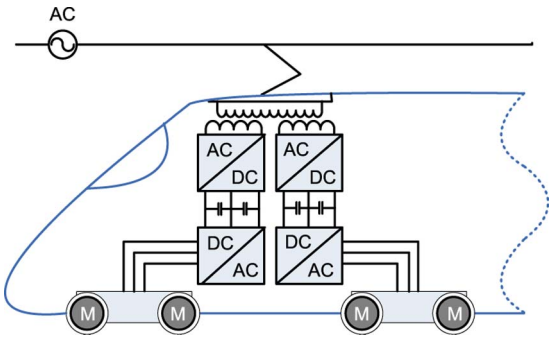

Fig. 47. ***High-speed train traction system using two NPC back-to-back converters.***

In Fig. 46, the power and propulsion plant for a tanker with a twin screw, redundant electrical propulsion system is shown. Two commercial NPC converters drive a 6.15 MW motor drive each. The tanker uses a multimotor system in which several motors are fed by the same converter, for example, to drive the pumps for cargo loading and unloading, since cargo pumps and propulsion normally will not be used simultaneously, reducing the overall cost of the system.

One of the applications where multilevel technology is considered as the state-of-the-art power-conversion system is high-speed railway traction. The main reason is that high-speed trains are driven by higher fundamental frequencies (up to 400 Hz) and demand high dynamic performance and efficiency. To generate voltages of such frequencies with traditional two-level converters and keep good dynamic performance will necessarily involve very high switching frequencies, and hence losses (including expensive and bulky cooling systems). Multilevel converters not only can reduce the transformer by operating at higher voltages but also can deliver good power quality for the catenaries and motors (less need of filters) and operation with lower switching frequencies while keeping dynamic performance. The use of back-to-back configurations also permits bidirectional power flow, enabling regenerative braking so the energy can be fed back to the catenaries. Because of the back-to-back necessity, and the fact that the transformer for CHB is too bulky, the preferred multilevel topologies used for this application are the FC [149] and NPC [25], [150]. Fig. 47 shows a simplified schematic of a state-of-the-art locomotive powered by two NPCs in back-to-back configuration in which each one powers one bogey containing four motors each.

Another very attractive application of multilevel converters in transportation is magnetic levitation, or maglev. An example is the Transrapid system.[1, 2] [151], [152]. Maglev systems do not have traditional rotating motors as regular trains; instead they use linear motors, specifically, long stator linear synchronous motors. The system is composed of a propulsion system (rather than traction in this case) and a levitation system. The purpose of the first one is to produce horizontal movement of the train. It is composed of the stator placed on the guideway and the "rotor" which consists of magnets on the vehicle and is placed on the vehicle. The rotor magnets also have a lateral part called the guidance magnet that is in charge of keeping the train on the guideway. On the other hand, the levitation system is also performed by the stator's attracting the rotor magnets and charge of suspending the rotor in the air, eliminating friction that is present in traditional rotating machine. Thus, when the long stator windings are supplied with three-phase current, a traveling electromagnetic field is created instead of the rotating magnetic field of a conventional electric motor. This traveling field interacts with the support magnets of the rotor producing the horizontal thrust. The speed can be controlled in the same way as in rotational machines by adjusting the frequency and amplitude of the stator voltage, which acts accordingly on the travelling magnetic field. By shifting the phase angle of this field, the motor can accelerate or brake. Since there is no friction, a very high percentage of the energy can be fed back to the grid, improving overall efficiency of the system.

The levitation system is fed by onboard batteries, which are recharged through linear generators integrated into the support magnets while travelling.

The high dynamic performance needed by this application, the need for regenerative braking, and the power level of the application make multilevel back-to-back converters an attractive solution. In fact, the

[2]See http://www.thyssenkrupp-transrapid.de/ and http://www.transrapid.de/.

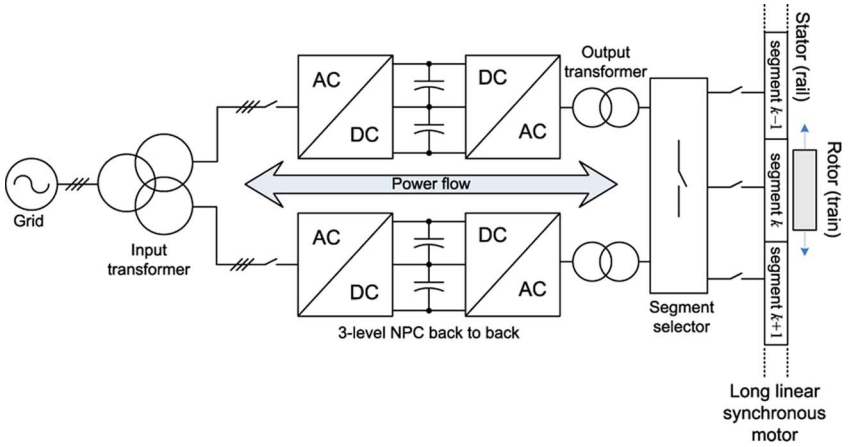

Fig. 48. ***Maglev train long linear synchronous motor multilevel drive system.***

Transrapid uses NPC back-to-back converters to control the propulsion system, as shown in the simplified diagram of Fig. 48. The only difference with the topology shown in Fig. 3 is that it includes asymmetric snubber circuits [151]. It should be noticed that only one segment of the linear stator where the train is crossing is energized; therefore, an additional segment selector is needed.

Initially the Transrapid used GTO devices, which are nowadays replaced by integrated gate commutated thyristor power semiconductors. Because of the high speeds achieved by the train (430 km/h), higher fundamental frequencies are necessary, which, independently of the modulation method that is used, will require a water-cooled refrigerating system for the power semiconductors due to the high switching frequency and nominal power rating of the drive.

There are currently two Transrapid systems operating in the world: the 31.5 km long test facilities in Emsland, TVE, Germany, and a commercial 30 km segment connecting the Long Yang Road subway station with the Pudong International Airport in Shanghai, China. The last one features 12 converter units of 15.6 MVA each.

VIII. CONCLUSION

Multilevel converters have matured from being an emerging technology to a well-established and attractive solution for medium-voltage high-power applications. Three topologies and several modulation methods have found industrial application. Initially, the higher power rates together with the improved power quality have been the major market drive and trigger for research and development of multilevel converters. However, the continuous development of technology and the evolution of industrial applications will open new challenges and opportunities that could motivate further improvements to multilevel converter technology. ■

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