



Academic year 2022-2023 (Even Sem)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Date	11 JULY 2023	Maximum Marks	50
Course Code	22ES24C	Duration	90 Min
Sem	II Semester	Test-1	
PRINCIPLES OF ELECTRONICS ENGINEERING			

Sl. No.	Questions	M	BT	CO
1a.	Draw the circuit diagram of a Full wave Bridge rectifier circuit with filter and explain its operation along with suitable waveforms.	6	2	1
b.	In an amplifier, the output power is 1.5 watts at 2 kHz and 0.3 watt at 20 Hz, while the input power is constant at 10 mW. Calculate the difference in decibel gain between 20 Hz to 2 kHz.	4	2	2
2a.	In a Zener regulator circuit, Design the value of R so that circuit performs satisfactorily under all the given conditions. Given Pd(max) =6W Izmin =10mA, Vz=12V Vin varies from 22V to 28V RL varies from 50Ω to 500Ω.	6	3	3
b.	Bring out any four differences between Avalanche breakdown and Zener breakdown.	4	1	2
3a.	A full wave bridge rectifier using ideal diodes is supplied from the secondary of a 10:1 transformer, whose primary is connected to 220V, 50Hz main supply. The output of the rectifier is connected to a load resistance of 220Ω in parallel with a capacitor filter C. Calculate the value of C required so that the ripple factor is 3%. Also determine: i) The dc output voltage ii) The peak to peak ripple voltage iii) The load regulation	6	3	3
b.	Write a brief note on the three regions of operation of a bipolar junction transistor.	4	2	1
4a.	Three stages are cascaded with 0.05V _{P-P} providing 150 V _{P-P} output. If the voltage gain of first stage is 20 and the input to the third stage is 15 V _{P-P} . Find the following. i) Overall gain in dB. ii) Voltage gain of 2 nd and 3 rd stages. iii) Voltage gain of each stage in dB.	6	2	3
b.	Explain the working principle of LED and Photodiode.	4	2	2
5a.	Draw the circuit diagram of a single stage RC coupled amplifier. With the	6	1	1



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	help of frequency response, discuss the effect of capacitors in each region.			
b.	Draw the block diagram of a regulated DC power supply and explain the function of each block.	4	1	2

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	16	16	18	-	14	24	12	-	-	-

Academic year 2022-2023 (Odd Sem)

DEPARTMENT OF Electronics and Communication Engineering			
Date	25/02/2023	Maximum Marks	60
Course Code	22ES14	Duration	120 Mins
Sem	I Semester	CIE2	
ELEMENTS OF ELECTRONICS ENGINEERING			

Instructions to candidates:

- Part A must be answered within the first two pages of manuscript.
- Assume the suitable data for missing values

PART-A		M	BT	CO
1	The Slew rate of an Op-Amp is 3V/μsec with a peak value of voltage as 2V. Calculate the maximum output frequency so that the output is not distorted.	1	2	2
2	If one of the input to a 2-input EX-NOR gate is connected to 0, then it can be used to _____	1	1	1
3	The canonical sum of product form of the function $y(A,B) = A + B$ is _____	1	2	2
4	Prove that $AB + BC + B\bar{C} = AB + C$	1	3	2
5	The gain of a voltage follower is _____	1	1	1
6	An op-Amp has a differential gain of 86dB and Common mode gain of 20dB. The CMRR in dB is _____	1	2	3
7	The minimum number of NAND gates required to realize XOR gates is _____	1	2	1
8	State the necessary and sufficient conditions to obtain sustained oscillations	2	1	1
9	In a 3 variable K-map, if all the cells contain 1's then the output is _____	1	1	1
PART-B				
1.a	Explain the operation of RC phase shift oscillator with a neat diagram and also mention the gain equation.	6	2	2
b	Prove that the stability of the gain of an amplifier improves with negative feedback by a factor $(1+A\beta)$ where A is the open loop gain of the amplifier and β is the feedback factor.	4	3	2
2a	Simplify the logic expression using K map and implement the logic circuit using NAND Gate. $F = \sum m(0,1,2,3,,5,7,8,9,,10,12,13)$	6	4	3
2b	List at least four important characteristics of an ideal op-amp and indicate their typical values for a general purpose commercial op-amp.	4	1	1
3a	Simplify the following expressions: i. $Y = (A + B)(A + \bar{B})(\bar{A} + B)$ ii. $Y = XY + XYZ + XY\bar{Z} + \bar{X}YZ$	5	3	2
b	Design an adder circuit using an op-amp to obtain an output expression. $V_0 = 2(0.1 V_1 + 0.5 V_2 + 20 V_3)$ where V_1, V_2, V_3 are the inputs. Assume the value of feedback resistor as 10KΩ.	5	4	4
4a	Define Slew rate and CMRR with necessary expressions	4	1	1
b	An amplifier has a gain of 50 dB. The bandwidth of 250KHz, distortion of 12%, an input impedance of 30KΩ, and an output impedance of 2KΩ. If the voltage series negative feedback of 2.9% is given to this amplifier, calculate the gain, input impedance, output impedance, bandwidth, and distortion of the amplifier with negative feedback.	6	4	3



Academic year 2022-2023 (Odd Sem)

5a	Write the truth table for SUM and CARRYOUT of a full adder. From the truth table, obtain the logic expressions for the same and then realize the full adder using 2 half adders.	6	3	3
5b	Draw the circuit of an inverting amplifier and explain the working of the same with suitable expressions	4	3	3

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Quiz	Max Marks	5	4	1	-	5	4	1	-	-	-
	Test	Max Marks	8	15	22	5	8	6	19	17	-	-

Course Code: 22ES14C

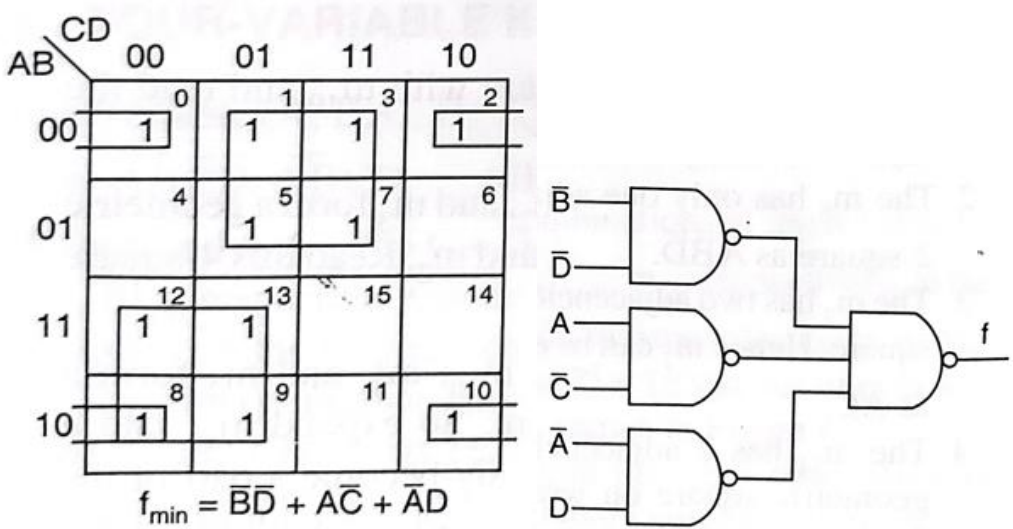
Course Title: Principles of Electronics Engineering

Semester: I

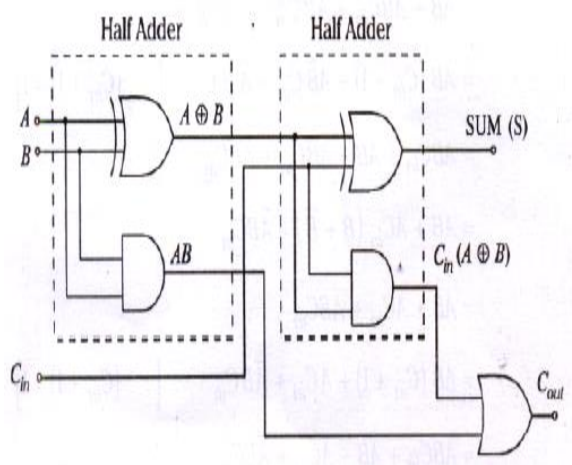
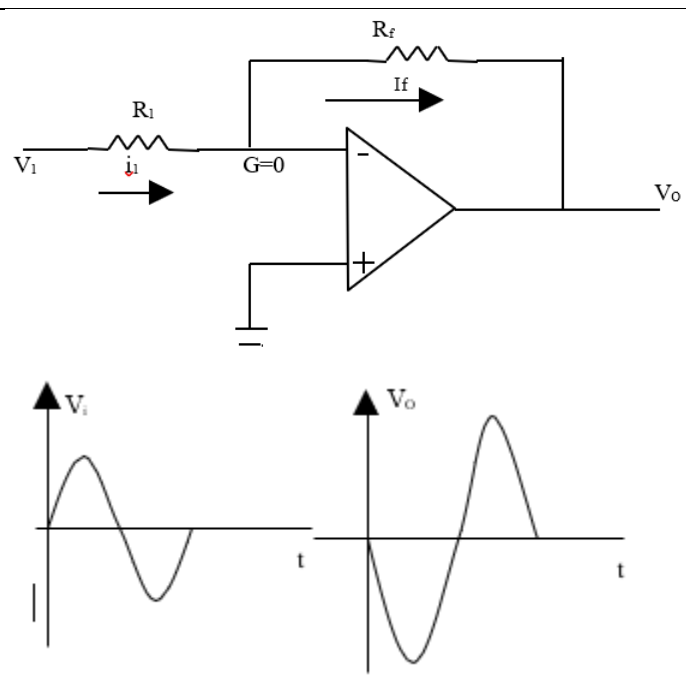
SCHEME & SOLUTION

Sl.No	Solution with Mark split-up	Marks allotted
1	$SR = \frac{dV_o}{dt} \text{ volts}/\mu \text{ sec}$ $SR = f_{\max} 2 \pi V_m$ $F = 238.7 \text{ KHz}$	01
2	Not	01
3	$AB + AB' + A'B.$	01
4	$AB + BC + \bar{B}C = AB + C$ $AB + C(B + \bar{B}) = AB + C$	01
5	1	01
6	<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;"> $CMRR = \frac{A_d}{A_c}$ </div> 4.3 dB	01
7	4	01
8	<ol style="list-style-type: none"> 1. The loop gain is equal to one in absolute magnitude, which means that $\beta A = 1$ 2. The phase shift through the loop is either zero or an integer multiple $\angle \beta A = 2\pi n, n = 0, 1, 2, \dots$ 	02
9	1	01

Sl. No.	Solution with Mark split-up	Marks
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	<p>This shows that magnitude of the relative change in gain $\left \frac{dA_f}{A_f} \right$ is reduced by the factor βA compared to that without feedback $\left(\left \frac{dA}{A} \right \right)$.</p>																															
2.a	 <p>$f_{\min} = \bar{B}\bar{D} + A\bar{C} + \bar{A}D$</p>	4+2																														
2.b	<table border="1"> <thead> <tr> <th>Parameter</th><th>Ideal</th><th>Typical or Practical Value</th></tr> </thead> <tbody> <tr> <td>Voltage Gain $[A_v]$</td><td>∞</td><td>2×10^5</td></tr> <tr> <td>Output Impedance</td><td>0</td><td>75Ω</td></tr> <tr> <td>Input Impedance</td><td>∞</td><td>$2M\Omega$</td></tr> <tr> <td>Input Offset</td><td>0</td><td>2mV</td></tr> <tr> <td>CMRR</td><td>∞</td><td>90dB</td></tr> <tr> <td>Slew Rate</td><td>∞</td><td>$0.5V/\mu s$</td></tr> <tr> <td>Bandwidth</td><td>∞</td><td>1MHz</td></tr> <tr> <td>PSRR</td><td>0</td><td>$30\mu V/V$</td></tr> <tr> <td>Input Bias Current</td><td>0</td><td>80nA</td></tr> </tbody> </table> <p>To mention any Four</p>	Parameter	Ideal	Typical or Practical Value	Voltage Gain $[A_v]$	∞	2×10^5	Output Impedance	0	75Ω	Input Impedance	∞	$2M\Omega$	Input Offset	0	2mV	CMRR	∞	90dB	Slew Rate	∞	$0.5V/\mu s$	Bandwidth	∞	1MHz	PSRR	0	$30\mu V/V$	Input Bias Current	0	80nA	4
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3.a	$Y = (A + B)(A + \bar{B})(\bar{A} + B)$ $= AB$ $Y = XY + XYZ + XY\bar{Z} + \bar{X}YZ$ $Y = Y[X + Z]$	<p>2.5</p> <p>2.5</p>																														
3.b	$V_o = \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$ <p>$R_1=50K\Omega$, $R_2=10K\Omega$ and $R_3=250\Omega$</p> <p>Design</p>	<p>1</p> <p>3</p> <p>1</p>																														
4.a	slew rate is the maximum rate at which amplifier output can change in volts per	2																														

	<div>microsecond (V/microsecond)</div> <div>$SR = \frac{\Delta V_o}{\Delta t} \quad V/\mu s \quad \text{with } t \text{ in } \mu s$</div> <div>Common Mode Rejection Ratio(CMRR): It is defined as “ The ratio of differential voltage gain to common-mode voltage gain”.</div> <div>$CMRR = \frac{A_d}{A_c}$</div>	2																																																		
4.b	<div>Gain=50/(1+1.45)=20.408</div> <div>Input impedance=30K*(1+1.45)=73.5KΩ</div> <div>Output impedance=2K/(1+1.45)=816.32Ω</div> <div>Bandwidth=250K*2.45=612.5KHz</div> <div>Distortion of the amplifier with negative feedback=4.89%</div>	6																																																		
5.a	<table><tr><th colspan="3">Inputs</th><th colspan="2">Outputs</th></tr><tr><th>A</th><th>B</th><th>C_{in}</th><th>Carry</th><th>Sum</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table> <div><div>Sum=$\overline{A} \overline{B} C_{in} + \overline{A} B \overline{C_{in}} + A \overline{B} \overline{C_{in}} + ABC_{in}$ $= \overline{A} [\overline{B} C_{in} + B \overline{C_{in}}] + A [\overline{B} \overline{C_{in}} + BC_{in}]$ $= \overline{A} [B \oplus C_{in}] + A [\overline{B} \oplus \overline{C_{in}}]$ $= A \oplus B \oplus C_{in}$</div><div>Carry = $\overline{A} B C_{in} + A \overline{B} C_{in} + AB \overline{C_{in}} + ABC_{in}$ $= \overline{A} B C_{in} + A \overline{B} C_{in} + AB (\overline{C_{in}} + C_{in})$ $= \overline{A} B C_{in} + A \overline{B} C_{in} + AB$ $= \overline{A} B C_{in} + A (\overline{B} C_{in} + B)$ $= \overline{A} B C_{in} + AB + AC_{in}$ $= B (\overline{A} C_{in} + A) + AC_{in}$ $= B (A + C_{in}) + AC_{in}$ $= AB + BC_{in} + AC_{in}$</div></div>	Inputs			Outputs		A	B	C _{in}	Carry	Sum	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	0	1	1	1	0	1	0	0	0	1	1	0	1	1	0	1	1	0	1	0	1	1	1	1	1	2
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		2
5.b	 $A_v = \frac{V_o}{V_i} = \frac{-R_f}{R_1}$ <p>Working</p>	<p>1</p> <p>1</p> <p>1</p> <p>1</p>

Signature (Digital) of course handling faculty

1. Dr. Abhay Deshpande
2. Dr. Sahana B
3. Prof. Sowmya Nag
4. Dr. Saba
5. Prof. Sindhu