RV Educational Institutions
RV College of Engineering
Autonomous Institution Affiliated to Visvesvaraya Technological University, Belagavi
Approved by AICTE, New Delhi

Academic year 2023-2024 (Odd Sem)

DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

Date	21st NOVEMBER 2023	Maximum Marks	50
Course Code	EC113AT	Duration	90 Min
Sem	I Semester	Test-1	
PRINCIPLES OF ELECTRONICS ENGINEERING			

Sl. No.	Questions	M	BT	CO
1a.	Draw the Input and output characteristics of a Common Emitter configuration and explain the three regions of a bipolar junction transistor.	6	2	1
b.	List any four differences between Avalanche and Zener breakdown.	4	2	2
2a.	In a Zener regulator circuit, Design the value of R so that circuit performs satisfactorily under all the given conditions. Given Pd(max) =6W Izmin =5mA, Vz=12V Vin varies from 14V to 24V R_L varies from 500Ω to 1KΩ.	6	3	3
b.	Draw the block diagram of a regulated DC power supply and explain the function of each block.	4	1	2
3a.	A full wave bridge rectifier is supplied from the secondary of a transformer, whose primary is connected to 200sin314t main supply. The output of the rectifier is connected to a load resistance of 220Ω in parallel with a capacitor filter C. Calculate the value of C required so that the ripple factor is 3%. Also determine: i) The dc output voltage ii) The peak to peak ripple voltage iii) The load regulation	6	3	3
b.	An amplifier having a power gain of 17dB delivers a power output of 40W to a load of 1KΩ. Calculate i) the input power needed and ii) the input voltage needed, if the voltage gain of the amplifier is 38dB.	4	2	1
4a.	Draw the circuit of a full wave bridge rectifier with filter circuit and explain its operation. Also sketch the waveform of the voltage across the load.	6	2	3
b.	Three amplifier stages are cascaded with individual gains 10dB,10dB and 2 dB respectively. The input to the third stage is 10V.Find i) Overall gain in dB ii) Calculate the input and output voltages of the cascaded three stage amplifier.	4	2	2

5a.	Draw the circuit diagram of a single stage RC coupled amplifier. With the help of frequency response, discuss the effect of capacitors in each region.	6	1	1
b.	Explain the working principle of LED and Photodiode.	4	1	2

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	16	16	18	-	14	24	12	-	-	-

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430

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Academic year 2023-2024 (Odd Sem)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Date	28th DECEMBER 2023	Maximum Marks	50
Course Code	EC113AT	Duration	90 Min
Sem	I Semester	Test-2	
PRINCIPLES OF ELECTRONICS ENGINEERING			

Sl. No.	Questions	M	BT	CO
1a.	Explain the operation of RC phase shift oscillator with a neat diagram and also mention the gain equation.	6	2	2
b.	Prove that the stability of the gain of an amplifier improves with negative feedback by a factor (1+Aβ) where A is the open loop gain of the amplifier and β is the feedback factor.	4	3	2
2a.	An amplifier has a gain of 50 dB. Bandwidth of 250KHz, distortion of 12%, an input impedance of 30KΩ, and an output impedance of 2KΩ. If the voltage series negative feedback of 2.9% is given to this amplifier, calculate the gain, input impedance, output impedance, bandwidth, and distortion of the amplifier with negative feedback.	6	2	3
b.	Write any eight practical characteristics of an op-amp.	4	1	1
3a.	Design a summer circuit using 2 ideal op amp $V_0 = 2V_1 - 4V_2 + 6V_3 - 3V_4$. where V_1, V_2, V_3, and V_4 are the inputs. Assume the value of $R_f = 10K\Omega$.	6	4	4
b.	Draw the circuit of an inverting amplifier and explain the working of the same and derive the equation for output voltage.	4	3	3
4a.	Write the truth table for SUM and CARRYOUT of a full adder. From the truth table, obtain the logic expressions for the same and then realize the full adder using 2 half adders.	6	3	3
b.	Convert the following Numbers i) $(770)_8$ to Hexadecimal ii) $(10.11)_2$ to Decimal	4	2	2
5a.	Simplify the logic expression using K map and implement the logic circuit using NAND Gate. $F(A,B,C,D) = \sum m(0,2,5,7,8,10,13,15)$	6	4	3
b.	Simplify the following expressions and realize using Basic gates: i. $Y = AB + ABC + \bar{A}B + A\bar{B}C$ ii. $Y = XYZ + YZ + \bar{Z}$	4	2	2

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	4	18	22	6	4	20	14	12	-	-

Academic year 2023-2024 (Odd Sem)

DEPART MENT OF

ELECTRONICS & COMMUNICATION ENGINEERING

Date	23 Jan 2024	Maximum Marks	50
Course Code	**EC113AT**	Duration	90 Mins
Sem	I Semester	CIE 3-Improvement Test	

PRINCIPLES OF ELECTRONICS ENGINEERING

Sl.No	QUESTION	M	BT	CO
1	a. Explain the working of each block in Superheterodyne receiver. b. Sinusoidal carrier signal of frequency 1MHz, amplifier 4V and power of 1KW is amplitude modulated by a sinusoidal signal with a frequency of 10KHz. The depth of modulation is 70%. Determine (a) side band frequencies (b) Bandwidth (c) Total Power of modulated wave (d) Amplitude of the side bands.	6 4	1 2	2 3
2	a. Draw the block diagram of digital communication system and explain each block. b. List any four needs for modulation.	6 4	3 3	1 3
3	a. Calculate fm, fc, Vc, m, bandwidth and P_t for the amplitude modulated wave given by S(t)= 20[1+0.6sin3140]sin31.4*10^6t with P_c=2kW. b. List any 4 differences between AM and FM.	6 4	2 2	3 1
4	a. With a block diagram of computer system explain the salient features of microprocessor. b. Differentiate RISC and CISC architecture.	5 5	3 3	1 1
5	Explain and list the differences of the following: i. Harvard and Von- Neumann architecture. ii. Microprocessor and microcontroller.	 5 5	 3 3	 1 2

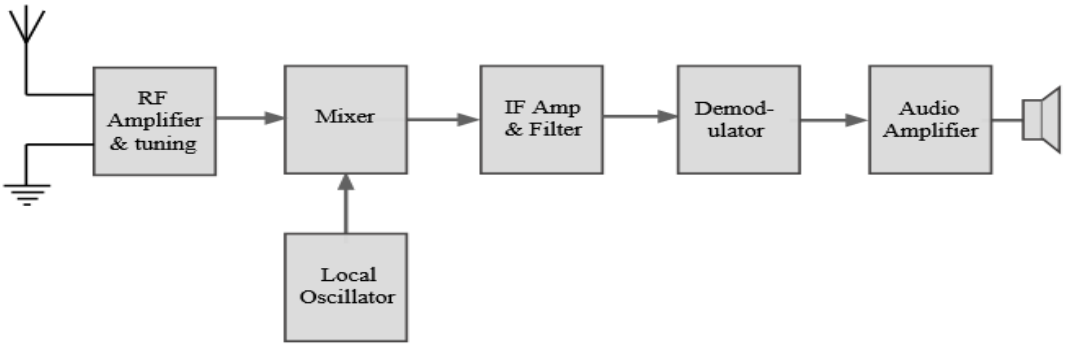
Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	25	11	14	-	6	14	30	-	-	-

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

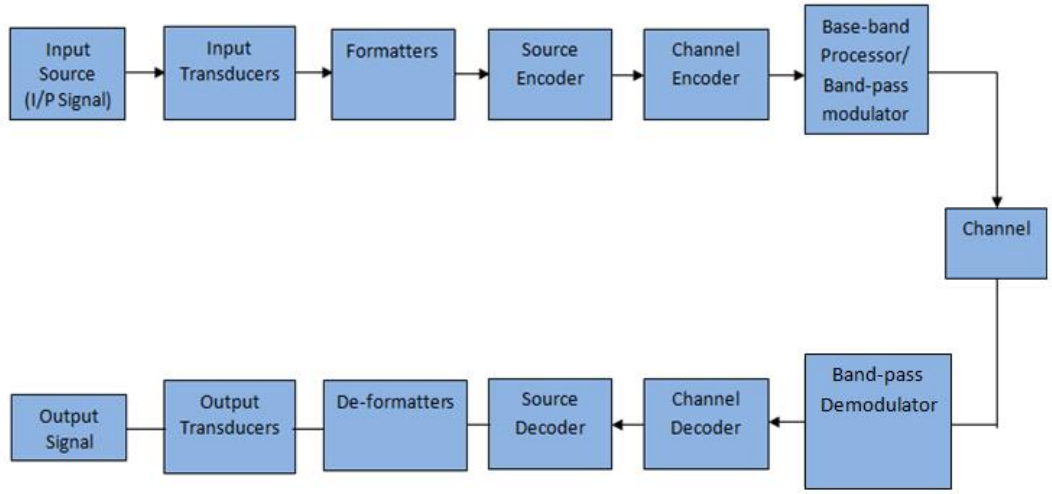
Test 3- Improvement Test

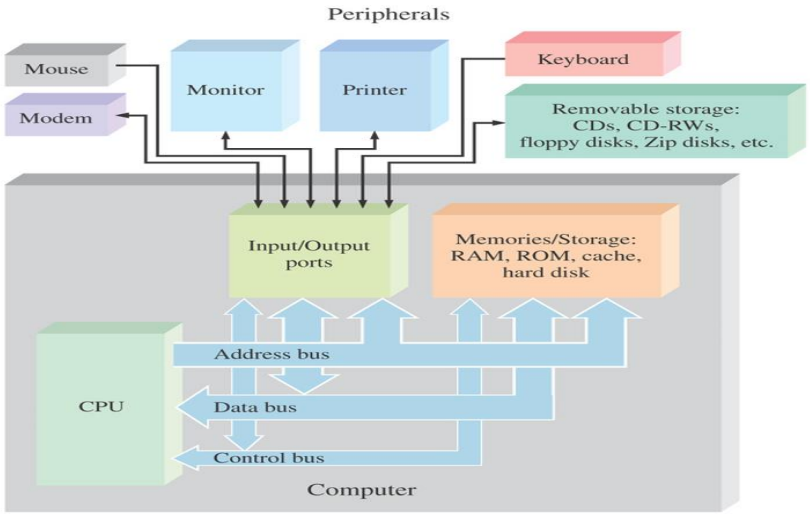
Course Code: EC113AT
Course Title: Principles of Electronics Engineering
Semester: I

SCHEME & SOLUTION

Sl.No	Solution with Mark split-up	Marks allotted
1a.	 **Diagram-2M** **Explanation-4M**	6
b.	a) f_{USB} = 1.01MHz f_{LSB} = 990kHz ----(1M) b) BW = $2f_m = 2 \times 10kHz = 20kHz$ ----(1M) c) Pt = 1.245kW ----(1M) d) Amplitude of side bands $= \frac{MVc}{2} = \frac{(0.7)(4)}{2} = 1.4V$ ----(1M)	4

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

2a.	 **Diagram-2M** **Explanation-4M**	6
b.	Practical Antenna length Operating Range Allows adjustments in Bandwidth Improves Quality of Reception Avoids mixing of the signals Allows multiplexing of the signal **Any 4 Points with explanation-1*4=4M**	4
3a	S(t)= 20[1+0.6Sin3140t]Sin31.4*10^6t. On Comparing with the $v = Vc \sin(2\pi fct + m \sin 2\pi\ fm\ t)$ $f_{c=}$ 4.99MHz **-1M** f_m=499.74Hz **-1M** Vc=20 Volts μ= 0.6 **-1M** Bandwidth=999.48Hz **-1M** P_t=2.36kW **-1M**	6
b.	<table><tr><th>**AMPLITUDE MODULATION**</th><th>**FREQUENCY MODULATION**</th></tr><tr><td>Amplitude of the carrier varies while its frequency remain constant</td><td>Frequency of the carrier varies while its Amplitude remain constant</td></tr><tr><td>Modulation index can have values from 0 to 1 only</td><td>Modulation index is much greater than one</td></tr><tr><td>AM has only two side bands</td><td>FM has infinite side bands</td></tr><tr><td>BW is twice the highest modulating frequency</td><td>BW is much larger than AM</td></tr></table>	4

	Susceptible to noise	More immune to noise		
	Range: 500KHz to 3MHz	Range: 88MHz to 108M Hz		
	AM covers long distances	FM covers short distance		
	Propagation is by ground waves and sky waves	Propagation is by space waves		
	Requires less complex and less expensive equipment	Requires more complex equipment		
4a.	 Core/CPU/ALU Address bus Data bus Control signals **Diagram-1M** **Explanation-4M**		5

b	**CISC** • More number of instructions • Instructions are complex to understand. • Hardware support for many instructions (More silicon Usage) A programmer can achieve the desired functionality with a single instruction which in turn provides the effect of using more simpler single instructions in RISC • Clock cycles per instruction(CPI) is more. **RISC** • Lesser no. of instructions. • Instructions are Easier to understand. • Software support for many instructions/operations. (Less silicon usage) Programmer needs to write more code to execute a task since the instructions are simpler ones • Clock cycles per instruction(CPI) is less. **CISC** • Code density is more. • Less number of registers. • Memory to memory operations are supported. Load & store operations in a instruction • More number of addressing modes. • Variable length instructions. • Design of Pipelining is Complex. **RISC** • Code density is less. • More number of registers. • No memory to memory operations are supported. Load & store operations not in a instruction (So called as load-store architecture) • Less number of addressing modes. • Fixed length instructions. • Design of Pipelining is easier.	5
5	**Harvard and Von Neumann architecture.** It uses single memory space for both instructions and data. / It has separate program memory and data memory It is not possible to fetch instruction code and data / Instruction code and data can be fetched simultaneously Execution of instruction takes more machine cycle / Execution of instruction takes less machine cycle Uses CISC architecture / Uses RISC architecture Instruction pre-fetching is a main feature / Instruction parallelism is a main feature Also known as control flow or control driven computers / Also known as data flow or data driven computers Simplifies the chip design because of single memory space / Chip design is complex due to separate memory space Eg. 8085, 8086, MC6800 / Eg. General purpose microcontrollers, special DSP chips etc.	5
	Microprocessor and Microcontroller	5

	MP	MC	MP	MC	
	• A silicon chip representing a Central Processing Unit (CPU), which is capable of performing arithmetic as well as logical operations according to a pre-defined set of Instructions • It is a dependent unit. It requires the combination of other chips like Timers, Program and data memory chips, Interrupt controllers etc. for functioning	• A microcontroller is a highly integrated chip that contains a CPU, RAM, On Chip ROM/FLASH memory for program storage, Timer and Interrupt control units and dedicated I/O ports. • It is a self contained unit and it doesn't require external Interrupt Controller, Timer, UART etc. for its functioning	• Doesn't contain a built in I/O port. The I/O Port functionality needs to be implemented with the help of external Programmable Peripheral Interface Chips like 8255. • Targeted for high end market where performance is important • Most of the time general purpose in design and operation • Limited power saving options	• Most of the controllers contain multiple built-in I/O ports which can be operated as a single 8 or 16 or 32 bit Port or as individual port pins • Targeted for embedded market where performance is not so critical (At present this demarcation is invalid) • Mostly application oriented or domain specific • Includes lot of power saving	

Signature of course handling faculty

1. Prof. Sowmya Nag K
2. Prof. S Praveen
3. Dr. Saba Fahreen N S
4. Prof. Sindhu Rajendran
5. Dr. Avik Banerjee

EC113AT / 22ES14C / 22ES24C

USN | 1 | R | V | 2 | 3 | C | 0 | 0 | 4 | 2 |

RV COLLEGE OF ENGINEERING®

(An Autonomous Institution affiliated to VTU)

I / II Semester B. E. Regular / Supplementary Examinations Feb-2024

PRINCIPLES OF ELECTRONICS ENGINEERING

Time: 03 Hours *Maximum Marks: 100*

Instructions to candidates:

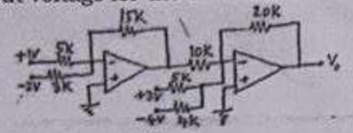
1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2 is compulsory. Answer any one full question from 3 and 4, 5 and 6, 7 and 8 & 9 and 10.

PART-A

1	1.1	In a regulated DC power supply the output voltage drops from $14V$ to $13.6V$ when the load current increases from no load to full load. The load regulation is _____%.	01
	1.2	The NPN transistor has $I_{CO} = 2nA$, $I_B = 0$, $V_{CE} = 4V$ and $I_C = 0.3\mu A$. The value of β = _____.	01
	1.3	The power gain of an amplifier is $20dB$. The input power required to obtain an output power of $100W$ = _____.	01
	1.4	In a NPN transistor if emitter base junction is forward biased and the collecter base junction is forward biased, then the transistor is working in _____ region.	01
	1.5	The lower cut off frequency of an RC coupled amplifier is $300Hz$. It has a voltage gain of 65 at $300Hz$. The mid frequency gain of the amplifier is _____.	01
	1.6	An amplifier having open loop gain of $60dB$ and closed loop gain of $40dB$. The amount of feedback in dB is _____.	01
	1.7	The main advantage of using a piezo electric crystal in oscillator circuit is to obtain _____.	01
	1.8	An op-amp has a differential gain of $86dB$ and common mode gain of $20dB$. The $CMRR$ in dB is _____.	01
	1.9	Output impedance _____ by applying negative feedback.	01
	1.10	Convert $(536)8 = Hexadecimal(\ )16$.	01
	1.11	Find the right hand side of the Boolean expression $AB + \bar{A}C + BC$ = _____.	01
	1.12	The minimum number of $NAND$ gates required to realize XOR gates is _____.	01
	1.13	Convert the given number $(6FE4)16$ to binary.	01
	1.14	An audio signal of $2kHz$ is used to amplitude modulate the carrier of $600kHz$. The bandwidth required is _____.	01
	1.15	The value of intermediate frequency in super heterodyne receiver is _____.	01
	1.16	Given the modulation indices as $m1 = 0.4$, $m2 = 0.3$ and $m3 = 0.5$. Calculate the total modulation index.	01
	1.17	The total power of an AM transmitter is $2400W$ and carrier power is $2000W$. The modulation index of an AM transmitter is _____%.	01

1.18		In *LDR* sensor, if the intensity of light applied is more, its resistance value _____.	01
1.19		The principle of operation of *LVDT* is based on the variation of _____.	01
1.20		What kind of waves does the Ultrasonic Sensor work on?	01

PART-B

2	a	Draw the block diagram of a DC power supply and explain the function of each block.	04
	b	Design the Zener Regulator for the given specifications: V_{in} varies from $12V$ to $18V$ R_L varies from 100Ω to $1K\Omega$ $V_z = 6V$ $I_z(\min) = 6mA$ $P_d(\max) = 1164mW$	06
	c	Draw the circuit diagram of a single stage *RC* coupled amplifier. With the help of frequency response, discuss the effect of capacitors in each region.	06
3	a	Draw the circuit of a non-inverting amplifier using an $op-amp$ and derive the expression for the gain of non-inverting amplifier.	06
	b	An amplifier has a gain of $60dB$, bandwidth of $30kHz$, distortion of 15%, input impedance of $5K\Omega$ and an output impedance of $1K\Omega$. If voltage series negative feedback of 3.9% is given to the amplifier, calculate the gain, input impedance, output impedance, amount of feedback, bandwidth and distortion of the amplifier with negative feedback.	06
	c	List two conditions for Barkhausen criteria and draw the circuit for *RC* phase shift oscillator. Determine the frequency of oscillations given $R = 450\Omega$ and $C = 0.2\mu F$.	04
		OR	
4	a	Draw the circuit of an integrator using an op-amp and derive the expression for the output voltage.	04
	b	Mention six advantages of negative feedback. Also prove that gain stability of an amplifier with negative feedback improves by a factor of $(1 + A\beta)$ compared to that of the amplifier without feedback, where A is open loop gain and β is the feedback factor.	06
	c	Determine the output voltage for the circuit shown in Fig. 4.c  Fig. 4.c	06
5	a	State and prove Demorgan's theorem.	04
	b	Write the truth table for "*SUM*" and "*CARRYOUT*" of a full adder. From the truth table, obtain the logic expressions for them. From these expressions, realize the full adder using logic gates.	06
	c	Perform the following: i) Convert the number $(5062)_{10}$ to the binary system. ii) Convert $(380)_{10}$ to the hexadecimal number system. iii) Convert the binary number $(11001011)_2$ to the decimal number system.	06
		OR	
6	a	Write the logic circuit for $EX-OR$ gate and realize it using minimum number of *NOR* gates.	04
	b	Draw the truth table for "*SUM*" and "*CARRYOUT*" of a half adder. From the truth table, obtain the logic expressions and realize the half adder using only *NAND* gates.	06
	c	$Y(a,b,c,d) = \Sigma(4,6,12,13,14,5,7,10)$ simplify the above suing K-map and realize Y using basic gates.	06
7	a	List any four differences between *AM* and *FM*.	04
	b	Draw the block diagram of digital communication system and explain the function of each block.	06
	c	The output of an *AM* transmitter is given by $V_{AM}(t) = 50(1 + 0.6\cos 12560t)\sin 628 \times 10^4 t$, determine: i) The sideband frequencies. ii) Modulation index and bandwidth. iii) The total power in the AM wave given the carrier power is $2KW$.	06
		OR	
8	a	Write any four differences between *RISC* and *CISC*.	04
	b	With the help of a block diagram representation, describe Super heterodyne receiver.	06
	c	In an *AM* signal, $S(t) = 50(1 + 0.5\sin 12560t)\sin 31.4 \times 10^5 t$, find the total power, sideband frequencies, power in each sideband, if the load impedance is 50Ω. Also sketch the frequency spectrum and indicate the values.	06
9	a	List any four differences between sensor and transducer.	04
	b	Explain the working of Ultrasonic sensor and mention any two applications of Ultrasonic sensor.	06
	c	With a neat diagram explain the working of Hall effect transducer.	06
		OR	
10	a	Explain the working of *LVDT* considering all the three cases.	08
	b	Explain the following: i) Humidity sensor ii) *LDR*.	08