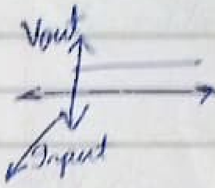
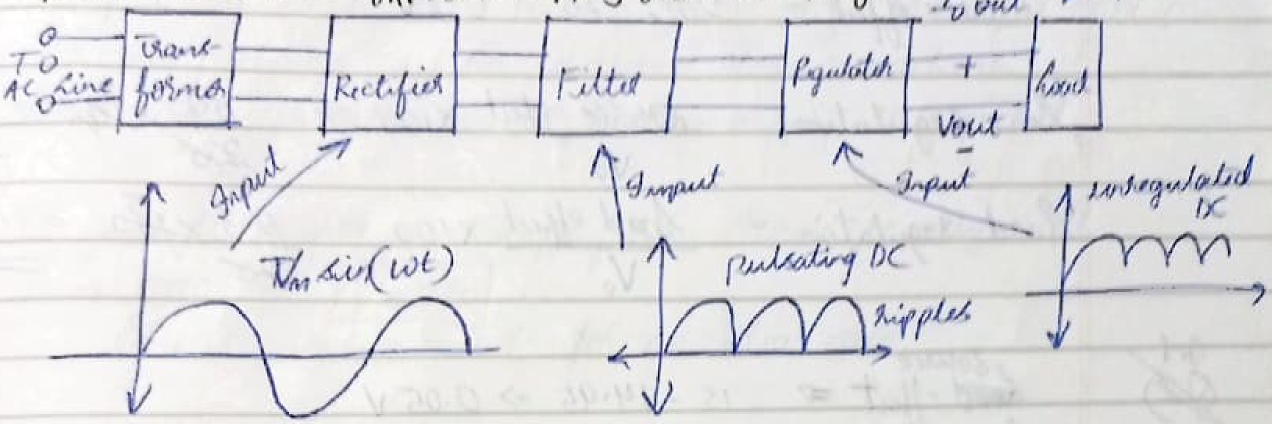
ESC - Electronics Eng

5M // Regulated Power Supply



Q) Explain each block of regulated power supply with neat diagram



→ Domestic => 220V, 50Hz
→ Output of transformer is A.C
→ Rectification is convertion of AC to DC
→ Output of Rectifier is pulsating DC (only +ve reference)
→ Filter is a simply a capacitor put in parallel to rectifier
→ Output of filter is unregulated DC
→ Input of regulator is unregulated DC & output is pure constant DC
→ Input AC is line supply & output is called load.

Power Supply Performance Parameters

→ Regulation is change in parameter
→ The tolerance value can be ± 10% variation in AC supply for line voltage.

1M/2M **Source effect** => Change in ΔV_0 due to change in line voltage

$\boxed{\text{source effect} = \Delta V_0 \text{ for a } 10\% \text{ change in } V_s}$

1M/2M Quiz **Line Regulation** source effect expressed as a % of DC output V_0.

$\boxed{\text{Line regulation} = \frac{\text{source effect}}{V_0} \times 100}$

~~For good~~

Imp Q1)
$\Delta V_0 = 0.3\,V$
~~ΔV_0 new = 0.2V~~ Source effect = 0.2V
10% increase is source effect
Load effect = 20 - 19.7 = 0.3V
Source effect = 20.2 - 20 = 0.2 V

Line regulation = $\frac{\text{source effect}}{V_0} \times 100 \Rightarrow \frac{0.2}{20} \times 100 = \underline{1\%}$

Load regulation = $\frac{\text{load effect}}{V_0} \times 100 \Rightarrow \frac{0.3}{20} \times 100 = \underline{1.5\%}$

Imp Q2)
Source effect ⇒ 15 - 14.95 ⇒ 0.05 V
Load effect ⇒ 15 - 14.9 ⇒ 0.1 V

Load regulation = $\frac{\text{Load effect}}{V_0} \times 100 = \frac{0.1}{15} \times 100 \Rightarrow \frac{2}{3}\%$

Line regulation = $\frac{\text{source effect}}{V_0} \times 100 = \frac{0.05}{15} \times 100 \Rightarrow \frac{20 \times 5}{3 \cdot 100}$
$= \underline{0.66\%}$

5M
Regulated Power Supply Theory

(i) Transformer → It helps to step up/step down the AC voltage for the desired output. AC voltage is connected to primary of the transformer.

(ii) Rectifier → Input of rectifier is AC voltage & the output is pulsating DC. Pulsating DC is unidirectional voltage containing large varying component called ripples.

(iii) Filter → Input of filter is pulsating DC and the output is unregulated DC. Filter is used to reduce the ripple content & make it smoother. But still, the output contains some ripples.

(iv) Regulator → Input of regulator is unregulated DC & the output is pure DC. Load can be connected to regulator. Regulator makes

the dc output voltage not only smooth but also ripple free.
It keeps the DC voltage constant under variable input condition

Line Voltage

Input to unregulated power supply (Rectifier circuit) is 230V AC
It may change under different load conditions.
A ± 10% variation in AC voltage supply is expected

Note// For good DC ~~output~~ power supply ΔV_o should be very small.
Ideal case → $\boxed{\Delta V_o = 0}$.
∴ Line Regulation = 0% for an ideal case

Load effect

The output voltage change (ΔV_o) due to load current change I_{Lmax}

$$\boxed{\text{Load effect} = \Delta V_o \text{ for } \Delta I_{Lmax}}$$

Load Regulation

Load effect expressed as a % of the output voltage (V_o)

$$\boxed{\text{Load Regulation} = \frac{\Delta V_o \text{ for } \Delta I_{Lmax}}{V_o} \times 100}$$

Note// DC output voltage (V_o) is a func of load current.

$$\boxed{I_{Lmax} \uparrow \propto \frac{1}{V_o \downarrow}}$$

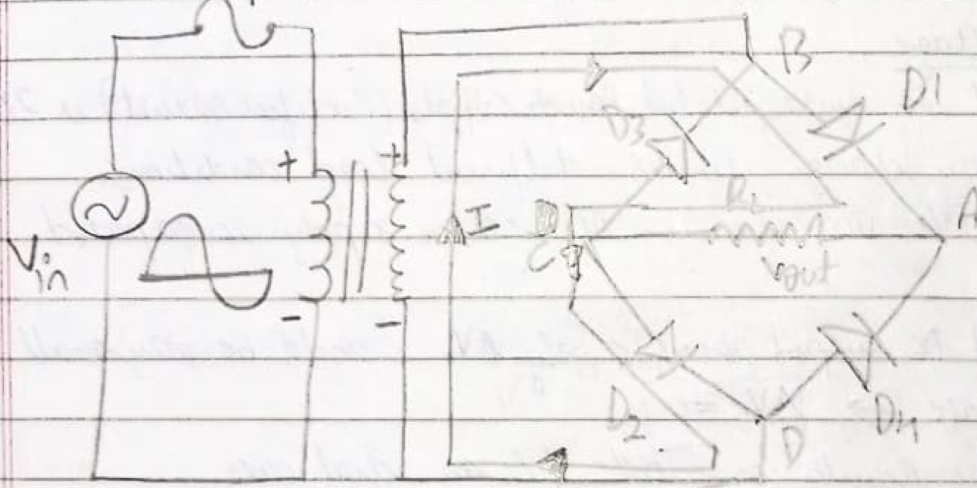
Rectification - Application of Diodes

Types of Rectifiers

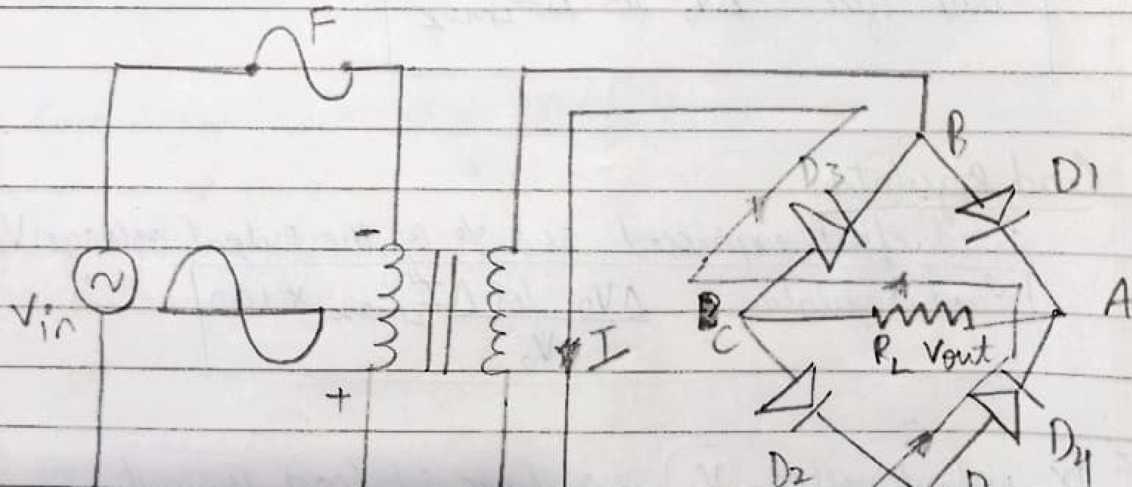
(X) (i) Half wave
(ii) Full-wave.
→ (X) 2 diodes & centre tap transformer
→ 4 diodes & ordinary transformer diodes

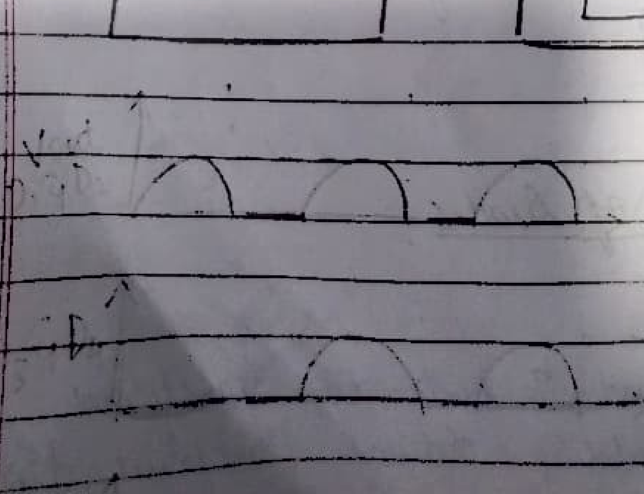
8M Bridge Rectifier

(i) During (+ve) Half cycle

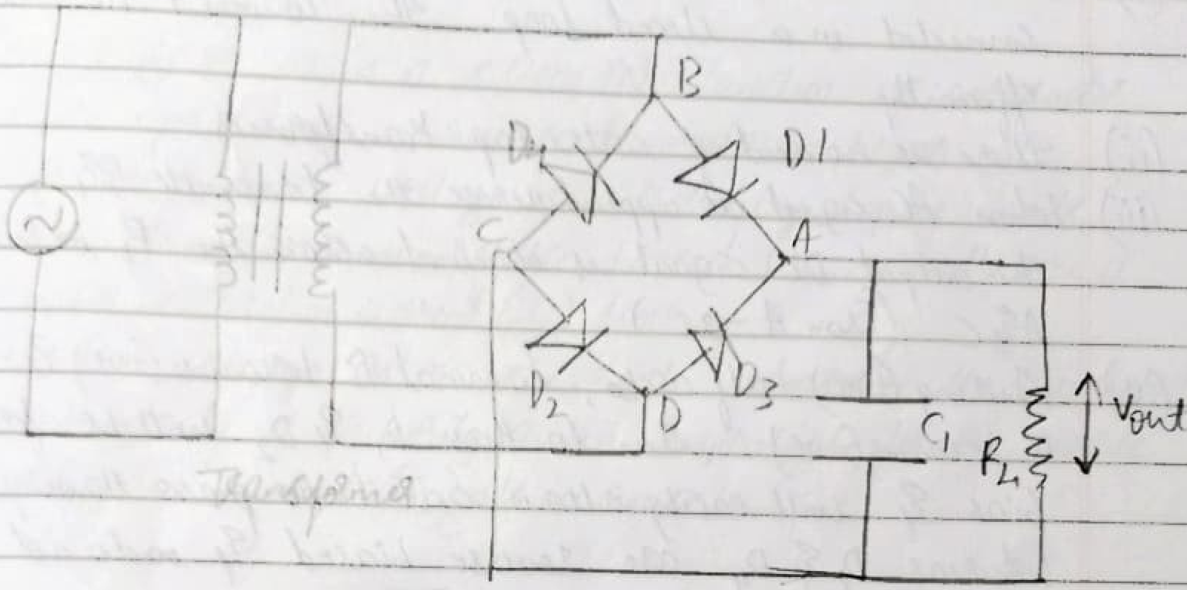


(ii) During (-ve) Half-cycle

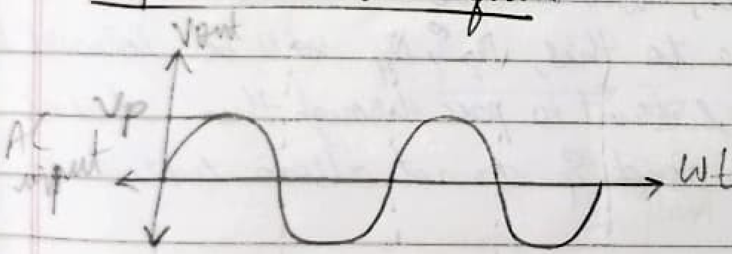


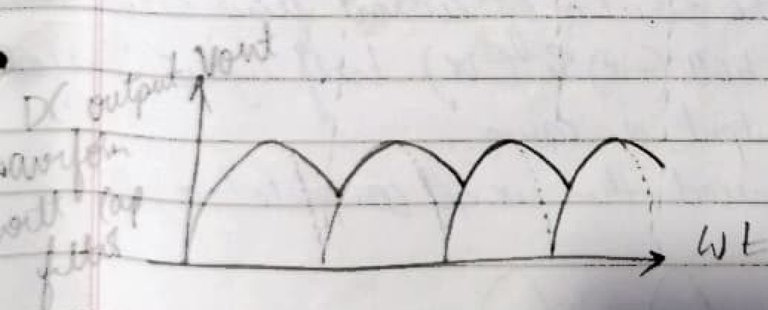


Bridge Rectifier with filter



Output wave with filter





Working Of Bridge Rectifier

(i) Four diodes D_1, D_2, D_3, D_4 & load Resistance R_L are connected in a closed loop. They converted AC → DC very efficiently.

(ii) There is no need of centre tap transformer

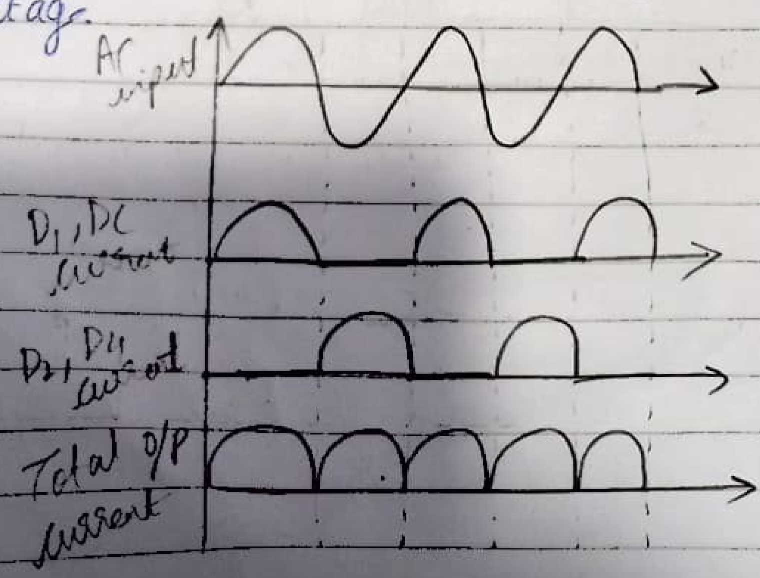
(iii) When AC signal is applied across the terminals B & D, the output DC signal is obtained across the R_L between terminals A & C (From A → C)

(iv) During (+ve) half cycle, terminal B becomes (+ve) & terminal D becomes (−ve). Due to this D_1 & D_2 will be forward bias & will easily allow current to pass through them whereas D_3 & D_4 are reverse biased & do not allow current to pass through them.

(v) During (−ve) half cycle, terminal D becomes (+ve) & terminal B becomes (−ve). Due to this, D_3 & D_4 will be forward biased & will easily allow current to pass through them whereas D_1 & D_2 are reverse biased & do not allow current to pass through them.

(vi) We can observe that the direction of current flow across ~~load~~ R_L is same during both (+ve) & (−ve) half cycles. Therefore the polarity of DC output is same.

(vii) If the diodes are reversed then we get complete (−ve) DC voltage.



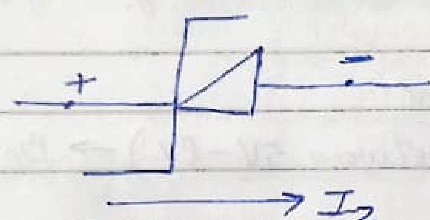
5M/4M

Zener Diode

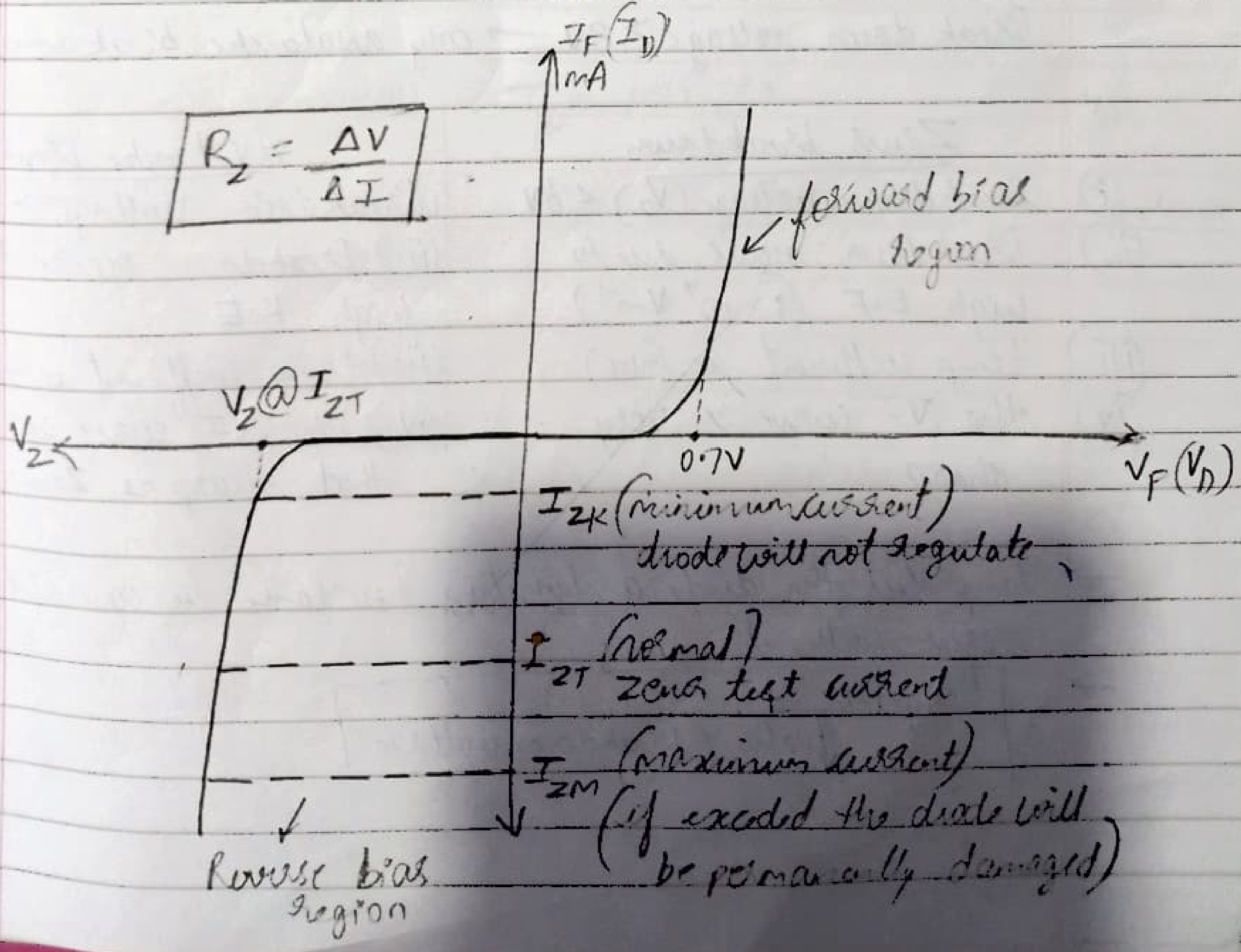
Q) Diff betw Zener breakdown & Avalanche breakdown?

Zener diode → it is a silicon PN-Junction semiconductor diode operated op in reverse breakdown region

- The break down voltage is controlled by doping levels.
- When the Junc is reverse biased we normally see a reverse saturation current (I_S) flowing.
- As the voltage across the diode increases in the reverse bias the velocity of minority carrier responsible for the reverse saturation current (I_S) als increase.



$$\boxed{R_Z = \frac{\Delta V}{\Delta I}}$$



Characteristics of Zener diode

(i) The breakdown will occur in reverse bias.
(ii) The reverse saturation current will flow until the reverse voltage applied is less than the reverse breakdown voltage
(iii) When the reverse voltage > reverse breakdown voltage current changes drastically.
(iv) At reverse voltage, current through zener diode increases rapidly.
(v) The sharp change from low value to large value of current in reverse charac is called Zener knee. of the curve
(vi) The reverse biased voltage at which break down occurs is called Zener break down voltage (V_z).

Breakdown Mechanisms

Break down voltage (between 5V – 8V) → Both avalanche & Zener mechanisms

Break down voltage > 8V → only avalanche break down

Zener breakdown	Avalanche breakdown
(i) Breakdown voltage (V_z) < 6V	(i) Break down voltage > 6V
(ii) Breakdown occurs due to high E.F ($3 \times 10^7 \, Vm^{-1}$)	(ii) Breakdown occurs due to high K.E
(iii) temp coefficient is (-ve)	(iii) temp coefficient is (+ve)
(iv) The VI curve is very sharp	(iv) The VI curve is not that sharp as Zener

→ To protect the diode a limiting Resistance is connected in series with it

→ $\boxed{\text{temp} \uparrow \propto \frac{1}{\downarrow \text{value of breakdown voltage}}}$

Q1) $R_L = 2000\ \Omega$ $\quad V_{rms} = 200V$ (We multiply ($\sqrt{2}$) because its in 2nd transformer)
$C = 500 \times 10^{-6} F$
$r = ?$

(i) $r = \frac{1}{4\sqrt{3} f C R_L} \times 100 \Rightarrow \frac{1}{4\sqrt{3} \times 50 \times 500 \times 10^{-6} \times 2000} \Rightarrow \frac{1}{4\sqrt{3} \times 25 \times} \times 100 = \cancel{0.577\%}\ 0.288\%$

(ii) DC output voltage $\Rightarrow \left(\frac{V_M}{1 + \frac{1}{4\sqrt{3} f C R_L}} \right) \Rightarrow \left(\frac{200 \cdot \sqrt{2}}{1 + 0.00288} \right) \Rightarrow 281.98 V$

(iii) $r = \frac{V_{ac}}{V_{dc}} \Rightarrow V_{ac} = r \cdot V_{dc} \Rightarrow \frac{0.288}{100} \times 281.98 \Rightarrow 0.812 V$

(iv) $I_{dc} = \frac{V_{dc}}{R_L} \Rightarrow \frac{281.98}{2000} = 0.1409 A$

(v) (%) Regulation $\Rightarrow \frac{1}{4 fCR_L} \times 100 = 0.5\%$

Q2) $V_{rms} = 230V$, $f = 50 Hz$ $\quad I_{dc} = 10 \times 10^{-3} A$.

Ripple factor $< 1\%$ $\qquad \boxed{\text{Ripple factor} = \frac{\text{Regulation}}{\sqrt{3}}}$

$\frac{1}{4\sqrt{3} fCR_L} < \frac{1}{100}$

$4\sqrt{3} fCR_L > 100$

$C > \frac{\cancel{100}\,25}{R_L f \cancel{4} \sqrt{3}} \Rightarrow \boxed{C > \frac{25}{R_L f \sqrt{3}}}$

$\because I_{dc} = \frac{V_{dc}}{R_L}$

since Ripple factor < 0.01

$V_{dc} = \left(\frac{V_M}{1 + \sqrt{3} r} \right) \Rightarrow \left[\frac{230 \cdot \sqrt{2}}{1 + \sqrt{3} r} \right] \Rightarrow \left[\frac{230 \cdot \sqrt{2}}{1 + \sqrt{3} \cdot (0.01)} \right] \Rightarrow \left(\frac{325.27}{1.01732} \right)$

$V_{dc} = 319.73 V$

$R_L \Rightarrow \frac{V_{dc}}{I_{dc}} = \frac{319.73}{10 \times 10^{-3}} \Rightarrow \underline{31.973 \times 10^{2}\ \Omega}$

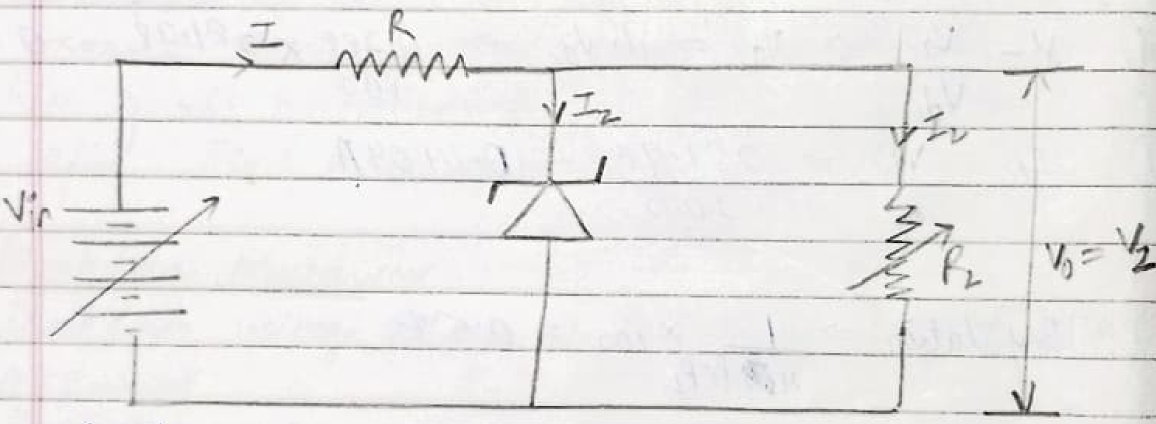
$$C \geq \frac{25}{R_L f \sqrt{3}} \Rightarrow C > \frac{25}{31.973 \times 10^{2} \times 50 \times \sqrt{3}}$$

$$C > \frac{25 \times 10^{-3}}{5 \times 31.973 \times \sqrt{3}}$$

$$C > 0.090 \times 10^{-3} F$$

$$\boxed{C > 90 \mu F}$$

Design of Zener Regulator



Case 1

$V_{in} = V_{in(max)}$, $I = I_{max}$, $R = R_{min}$, $I_z = I_{z(max)}$,
$I_L = I_{L\,min}$

$$\boxed{R_{min} = \frac{V_{in(max)} - V_z}{I_{z(max)} + I_{L(min)}}}$$

Case 2

$V_{in} = V_{in(min)}$, $I = I_{min}$, $R = R_{max}$, $I_z = I_{z\,min}$, $I_L = I_{L(max)}$

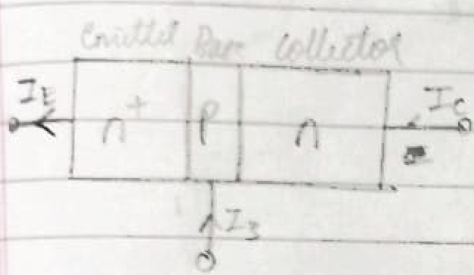
$$\boxed{R_{max} = \frac{V_{in(min)} - V_z}{I_{z(min)} + I_{L\,max}}}$$

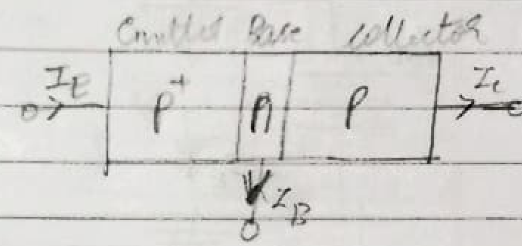
Calc (R) such that zener should operate bet^{n} $I_{z(min)} - I_{z(max)}$

Bipolar Junction Transistors

Transistor

It is a 3- layer semiconductor device consisting of either two n-type & one p-type layer of material / two p-type and one n-type of material.





Doping conc $\Rightarrow E > C > B$

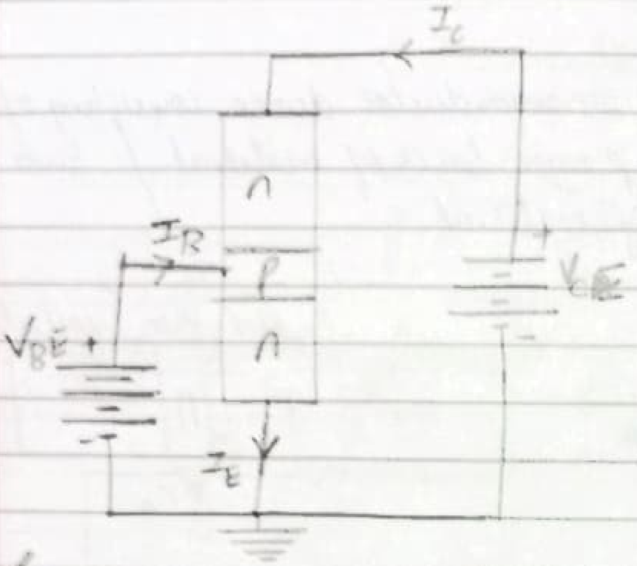
Width $\Rightarrow C > E > B$

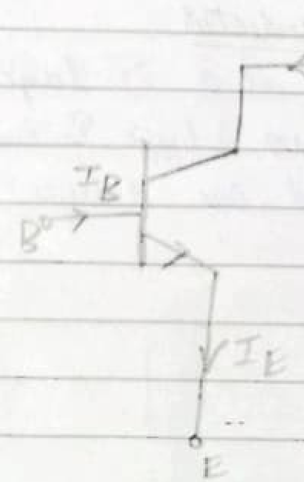
- There are two Junctions J_1 & J_2
- Application of BJT $\Rightarrow$ T.V, mobile, Radio

Region of Operation

J_1	J_2	Region
FB	FB	closed switch, Saturation
FB	RB	Amplifier, Active
RB	FB	Inverter, Reverse active
RB	RB	Open switch, cut off

Common emitter configuration



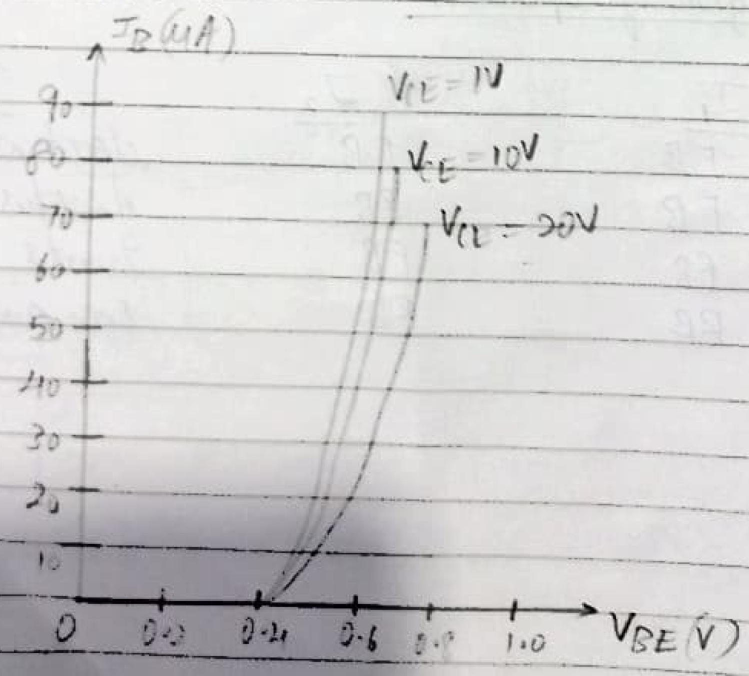


Input charac

(i) V_{CE} is kept constant & V_{BE} is ~~recorded~~ varied ~~of value~~ & value of I_B is recorded.

(ii) When V_{BE} is fixed, I_B decreases with ↑ in V_{CE}

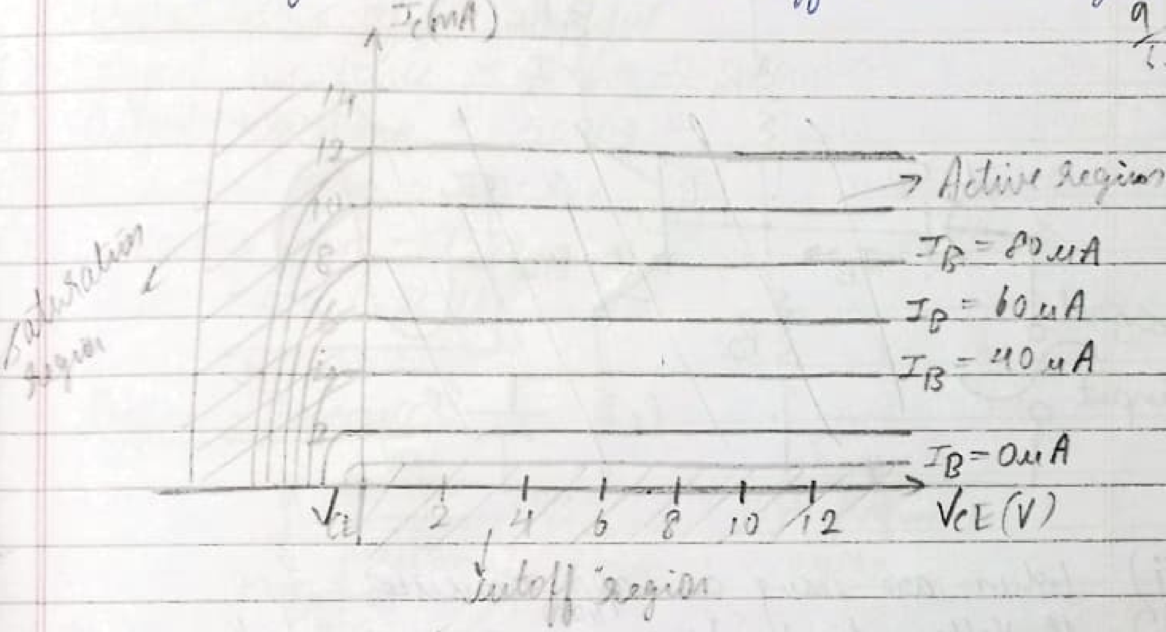
(iii) This is because, the depletion region across collector-base widens with ↑ in V_{CE}



$\frac{t_c - 0}{100} = \frac{t_f - 32}{180}$

Output characteristics

(i) Relationship betw input current (I_C) & input voltage (V_{CE}).
(ii) The regions of interest are active, cutoff, saturation regions.



Formulae

$50 < \beta < 400$

$\boxed{\beta = \dfrac{I_C}{I_B}}$ (d_c)

When emitter is open, $I_C = I_C(\text{major}) + I_{CO}(\text{minority})$

$\boxed{I_{CEO} = \dfrac{I_{CBO}}{1-\alpha}}$ $\boxed{\alpha = \dfrac{I_C}{I_E}}$

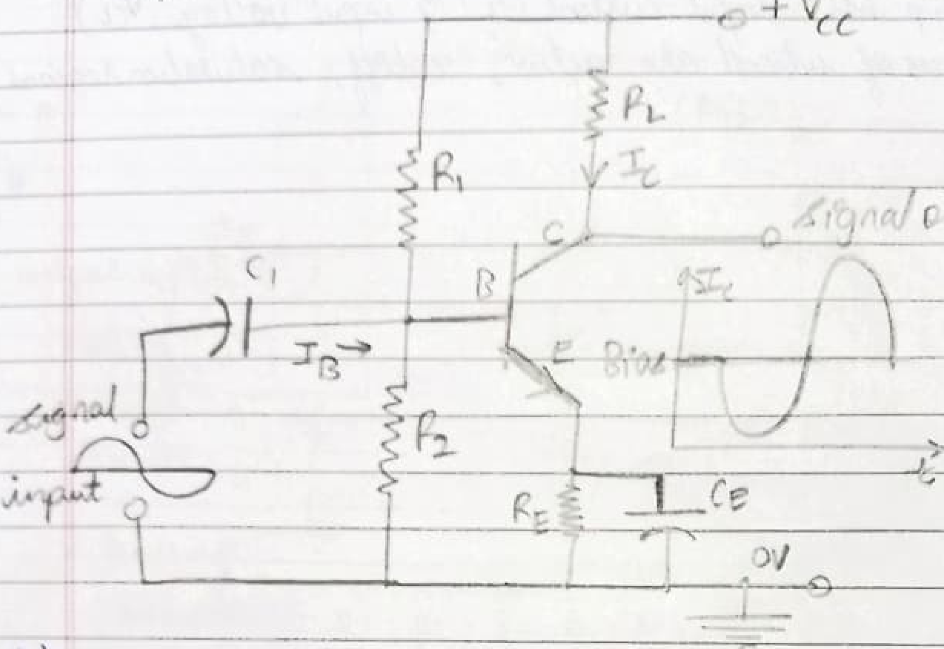
$\boxed{\alpha = \dfrac{\beta}{\beta+1}}$ $\boxed{\beta = \dfrac{\alpha}{1-\alpha}}$ $\boxed{I_E = (\beta+1) I_B}$

Imp (iii) Cutoff region → When J_1 & J_2 are both reverse biased, the region obtained is cutoff region. In the graph, the region right of V_{CE} & below $I_B = 0\,\mu A$ is called cutoff region

Imp (iv) Saturation region → When J_1 & J_2 are both forward biased, the region obtained is saturation region. Here, the curves merge & fall towards the origin. In this region, I_C is almost independ of I_B.

Imp

Single Staged RC Coupled Amplifier (~~Negative feedback amplifier~~)



(i) When are using an npn transistor

(ii) Voltage divider biasing (VDB) is necessary to keep the Q-point exactly at the centre of the load line so that ~~so that~~ we can use the transistor for amplification purposes

(iii) R_1, R_2 & R_E for the (VDB)

(iv) C_1 couples the input to the base terminal of & C_E (Emitter bypass capacitor) bypasses the emitter current to the ground.

(v) V_{CC} is a constant DC voltage input

$$\beta = \frac{I_C}{I_B} \qquad I_C = \beta I_B \qquad \boxed{I_C \propto I_B}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad (1)$$

(vi) During +ve half cycle of V_{in}, $I_B \uparrow$, thereby increasing $I_C \uparrow$ so in Eq (1), as $I_C \uparrow$, $V_{CE} \downarrow$ because V_{CC} is a constant voltage input

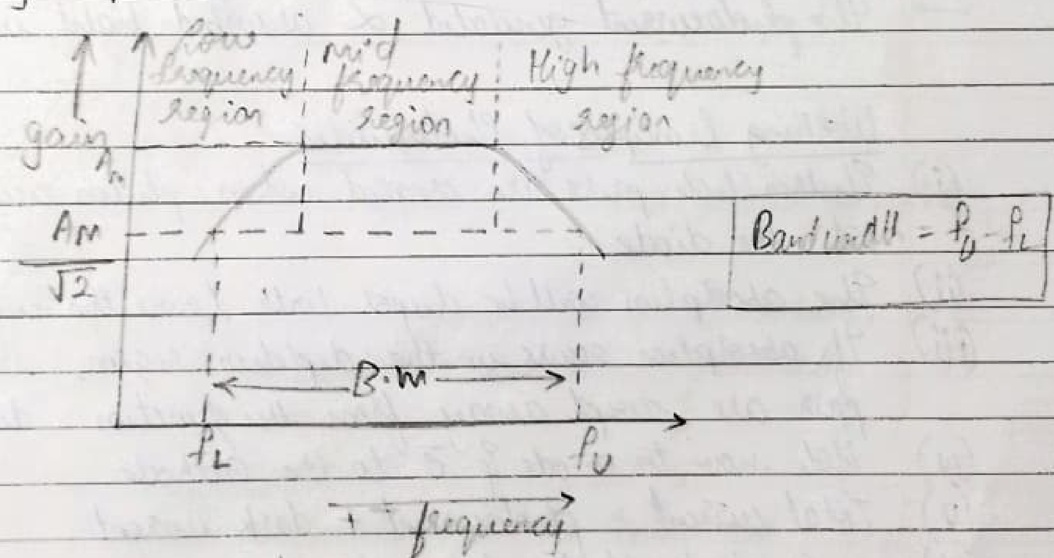
(vii) During −ve half cycle of V_{in}, $I_B \downarrow$, thereby decreasing I_C ($I_B \propto I_C$) so, in Eq (1), as $I_C \downarrow$, $V_{CE} \uparrow$.

(viii) The output voltage is amplifide by a factor β, but, we will get a 180° phase shift.

Characteristics of CE amplifier

(i) Input resistance = 1000 Ω - 2000 Ω
(ii) Output resistance = 50,000 Ω
(iii) Current gain = 50-300 I_o/I_i
(iv) Voltage gain - 1500 V_o/V_i
(v) Phase reversal is 180°

Frequency response



(i) Low-frequency region the voltage gain ↑, Mid frequency region the voltage gain is constant & in high frequency region voltage gain ↓
(ii) f_L & f_H are called Half Power frequencies.
(iii) They are called half power points because the gain drop to 70.7% of max value.

Photo Diode

→ It is a light detector, which involves conversion of light into voltage / current.

Components of Photodiode are
(i) Built-in lenses
(ii) Optical filters
(iii) Small / Large surface areas.

→ It is a semi-conductor device with a p-n junction & an intrinsic layer between p & n layers.
→ The photocurrent generated $\propto$ absorbed light intensity.

Working Principles of Photodiodes
(i) Electron-hole pairs are created when photon energy > 1.1eV hit the diode
(ii) The absorption will be deeper with lower the energy of photon.
(iii) If absorption occurs in the depletion region, the hole-electron pair are swept away from the junction, due to built in E.F
(iv) Hole move to anode & $\bar{e}$ to the cathode.
(v) Total current = photocurrent + dark current
(vi) Sensitivity of the device $\propto \dfrac{1}{\text{dark current}}$

Modes of Operation of Photodiode
(i) Photovoltaic Mode
(ii) Photoconductive mode
(iii) Avalanche mode.

(i) <u>Photovoltaic ~~cell~~ mode</u>

(a) Also called Zero bias mode.
(b) voltage is generated by illuminated photo diode
(c) It provides a very small dynamic range & non-linear dependence of the voltage produced

(ii) <u>Photo conductive mode</u>

(a) This mode is usually used in reverse bias
(b) Reverse voltage increases the width of depletion region which thereby ↓ ~~res~~ response time & capacitance of junction
(c) It is very fast & exhibits electronic noise

(iii) <u>Avalanche mode</u>

(a) Operated at high reverse bias condition
(b) This multiplies avalanche breakdown to each photo-generated $\bar{e}$-hole pair
(c) ~~As~~ This results in internal gain within the photodiode, which increases the responsivity of the device gradually

<u>Applications of Photodiodes</u>

Bar code, scanner, camera, safety Equipment.

Derivation of Negative feedback

(6M) Adv of negative feedback amplifiers

Zener diode

working of Photo diode & LED

multistage amplifier

negative feedback amplifiers → derivation → Adv

All numericals

Light Emitting diode LED

(i) ~~Two~~ It is a two lead semiconductor light source
(ii) It is a p-n junction that emits light when activated
(iii) Within the device, energy is released in the form of photons (Electroluminescence)

Adv of LED over Incandescent bulbs

(i) Smaller size
(ii) Lower energy consumption
(iii) Longer lifetime
(iv) Faster switching

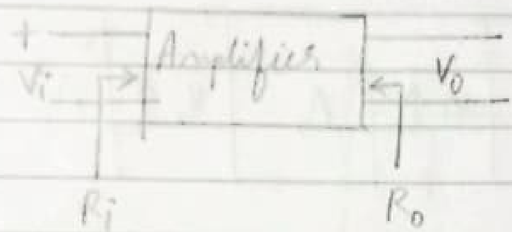
Applications of LED

(i) General lighting
(ii) Advertising
(iii) Traffic signal
(iv) Headlights of cars, trucks etc

Working of LED

(i) Light emitted by LED include red, yellow, orange & green. These lights emitted have lower bandwidth.
(ii) It has high power to light conversion efficiency. Its efficiency is 50 times of tungsten lamp
(iii) Response of LED is about 0.1 micro sec.
(iv) Here, the p-n junc emits light when energy is applied to it
(v) Within the p-n junc, ē move from n-region to p-region & recombine with holes. Free ē are in conduction band whereas holes are in valence band. Energy of holes is less than that of ēs. The ~~energy~~ light energy is ~~dissipated~~ ~~emitted~~ emitted in the form of heat & light.

Amplifier



It is an electronic circuit that magnifies the amplitude of input signal without any distortion

Voltage gain of amplifier (A_V)

Ratio of output voltage to input voltage

$$\boxed{A_V = \frac{V_0}{V_i}}$$

Current gain of Amplifier (A_i)

Ratio of output ~~voltage~~ current to input current

$$\boxed{A_i = \frac{I_0}{I_i}}$$

Power gain on Amplifier ($\cancel{\frac{P_0}{P_i}}$) (A_P)

$$\boxed{A_P = \frac{P_0}{P_i} \Rightarrow \frac{V_0 I_0}{V_i I_i}}$$

Decibel Power & voltage ~~gain~~, current gain

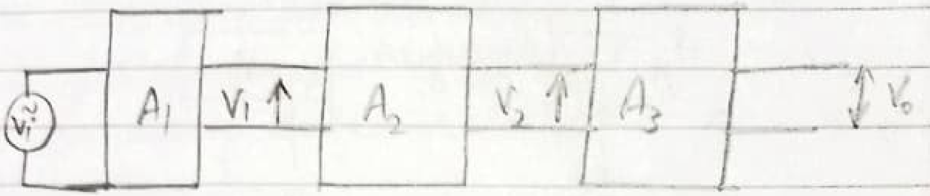
Decibel voltage gain $(A_V)dB = 10 \log\left(\frac{V_0^2}{V_i^2}\right) = 20 \log\left(\frac{V_0}{V_i}\right)$

Decibel current gain $(A_i)dB = 10 \log\left(\frac{I_0^2}{I_i^2}\right) = 20 \log\left(\frac{I_0}{I_i}\right)$

Decibel Power gain $(A_P)dB = 10 \log\left(\frac{P_0}{P_i}\right) \Rightarrow 10 \log\left(\frac{V_0 I_0}{V_i I_i}\right)$

Also, $P_0 = \frac{V_0^2}{R_L}$, $P_i = \frac{V_i^2}{R_i}$ $\therefore$ $\frac{P_0}{P_i} = \frac{V_0^2}{R_L} \times \frac{R_i}{V_i^2} \Rightarrow \boxed{\frac{P_0}{P_i} = \left(\frac{V_0}{V_i}\right)^2 \text{ if } R_L = R_i}$

Need for cascading of Amplifiers



Cascading is the ~~pross of~~ process of connecting the same type of amplifiers back to back in series, to get much more magnitude ~~vo~~ voltage output / current output

Need for cascading

(i) To transfer the ac output of one stage to the input of another stage

(ii) DC conditions of one stage do not mix with the other stages

$A_{V_1} = \frac{V_1}{V_i}$, $A_{V_2} = \frac{V_2}{V_1}$, $A_V = A_{V_1} \cdot A_{V_2}$

$$\boxed{A_V = A_{V_1} \cdot A_{V_2} \cdots A_{V_n}} \quad \boxed{A_V = \frac{V_o}{V_i}}$$

Voltage gain in decibels is

$$(A_V)\,dB = 20 \log \left(\frac{V_o}{V_i}\right)$$

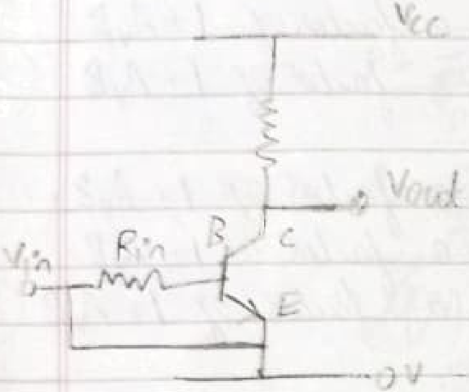
$$\Rightarrow 20 \log (A_V)$$

$$\Rightarrow 20 \log (A_{V_1} \cdot A_{V_2} \cdots A_{V_n})$$

$$\Rightarrow 20 \log (A_{V_1}) + 20 \log (A_{V_2}) + \cdots + 20 \log (A_{V_n})$$

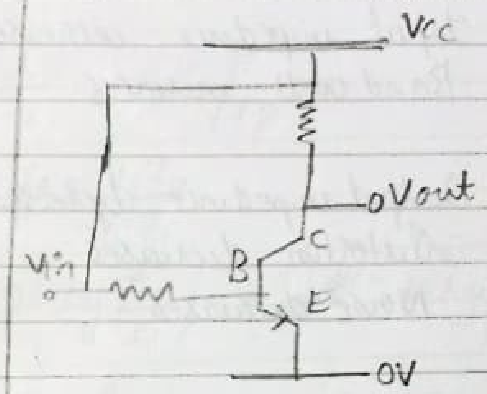
$$\boxed{(A_V)\,dB = A_{V_1}\,dB + A_{V_2}\,dB + \cdots + A_{V_n}\,dB}$$

BJT transistor as open switch



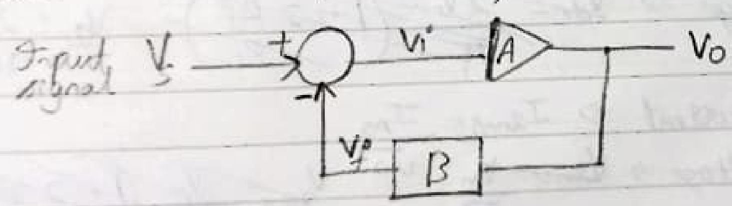
(i) Input & Base are grounded
(ii) $V_{BE} < 0.7V$
(iii) Base emitter junc is reverse biased
(iv) Transistor is fully off
(v) $V_{out} = V_E = 1$

BJT transistor as closed switch



(i) Input & Base are connected to V_{cc}
(ii) $V_{BE} > 0.7V$
(iii) Base emitter junc is forward biased
(iv) Transistor is fully ON
(v) $V_{out} = V_{CE} = 0$

Negative Feed-back (derivation)



$$A_v = \frac{V_o}{V_s} = \frac{V_o}{V_i}$$

$\boxed{V_i = V_s - V_f}$ principle of -ve feedback

$$V_o = A_v V_i \Rightarrow A_v (V_s - V_f) \Rightarrow A_v V_s - A_v V_f$$

$$\Rightarrow A_v V_s - A(\beta V_o)$$

$$(1 + \beta A_v) V_o = A_v V_s$$

$$\boxed{A_f = \frac{V_o}{V_s} = \frac{A_v}{1 + \beta A_v}}$$

6M Advantages of negative feed back amplifiers

(i) Input impedance increases by a factor of $1+A_vB$
(ii) Band width increases by a factor of $1+A_vB$
(iii) Output impedance decreases by a factor of $1+A_vB$
(iv) Distortion decreases by a factor of $1+A_vB$
(v) Noise decreases by a factor of $1+A_vB$

(vi) Stability of the gain improves by a factor of $1+A_vB$

Unit 1 all calculation formulae

1) Source effect, load effect (subtraction)
2) Line regulation, load regulation (% calc)

3) DC load current $\Rightarrow I_{dc} = \frac{2I_m}{\pi}$

4) DC load voltage $\Rightarrow \cancel{V_{dc} = \frac{2V_m}{\pi}\left(1+\frac{2R_f}{R_L}\right)}$ $V_{dc} = \frac{2V_m}{\pi\left(1+\frac{2R_f}{R_L}\right)}$

5) RMS load current $\Rightarrow I_{rms} = \frac{I_m}{\sqrt{2}}$

6) RMS load voltage $\Rightarrow \cancel{V_{rms} = \frac{V_m}{\sqrt{2}}}$ $\cancel{V_{rms} = \frac{V_m}{\sqrt{2}}\left(1+\frac{2R_f}{R_L}\right)}$ $V_{rms} = \frac{V_m}{\sqrt{2}\left(1+\frac{2R_f}{R_L}\right)}$

7) Regulation $= \frac{2R_f}{R_L}$

8) Efficiency of rectification $\Rightarrow \eta = \frac{0.812}{1+2\frac{R_f}{R_L}}$

9) Ripple factor = 0.483

10) $\gamma = \frac{1}{4\sqrt{3}fCR_L}$, $\gamma = \frac{V_{ac}}{V_{dc}}$

11) Load regulation $= \frac{1}{4fCR_L}$

12) $V_{dc} = \frac{V_m}{1+\frac{1}{4fCR_L}}$

13) $R_{min} = \dfrac{V_{in(max)} - V_Z}{I_{z(max)} + I_{Lmin}}$ $\quad R_{max} = \dfrac{V_{i(min)} - V_Z}{I_{Z(min)} - I_{L(max)}}$

14) $\alpha = \dfrac{I_C}{I_E}$, $\beta = \dfrac{I_C}{I_B}$, $\beta = \dfrac{\alpha}{1-\alpha}$, $\alpha = \dfrac{\beta}{1+\beta}$

15) $A_V = \dfrac{V_o}{V_i}$, $A_i = \dfrac{I_o}{I_i}$, $A_P = \dfrac{P_o}{P_i} = \dfrac{V_o I_o}{V_i I_i}$

16) $(A_V)dB = 20 \log\left(\dfrac{V_o}{V_i}\right)$, $(A_i)dB = 20 \log\left(\dfrac{I_o}{I_i}\right)$, $(A_P)dB = 10 \log\left(\dfrac{P_o}{P_i}\right)$

$\dfrac{P_o}{P_i} = \dfrac{V_o^2}{R_L} \times \dfrac{R_i}{V_i^2} \Rightarrow \left(\dfrac{V_o}{V_i}\right)^2$ if $R_L = R_i$

17) $(A_V)dB = A_{V_1}(dB) + A_{V_2}(dB) + A_{V_3}(dB) + \cdots + (A_{V_n})dB$

18) $A_f = \dfrac{V_o}{V_s} = \dfrac{A_V}{1+\beta A_V}$