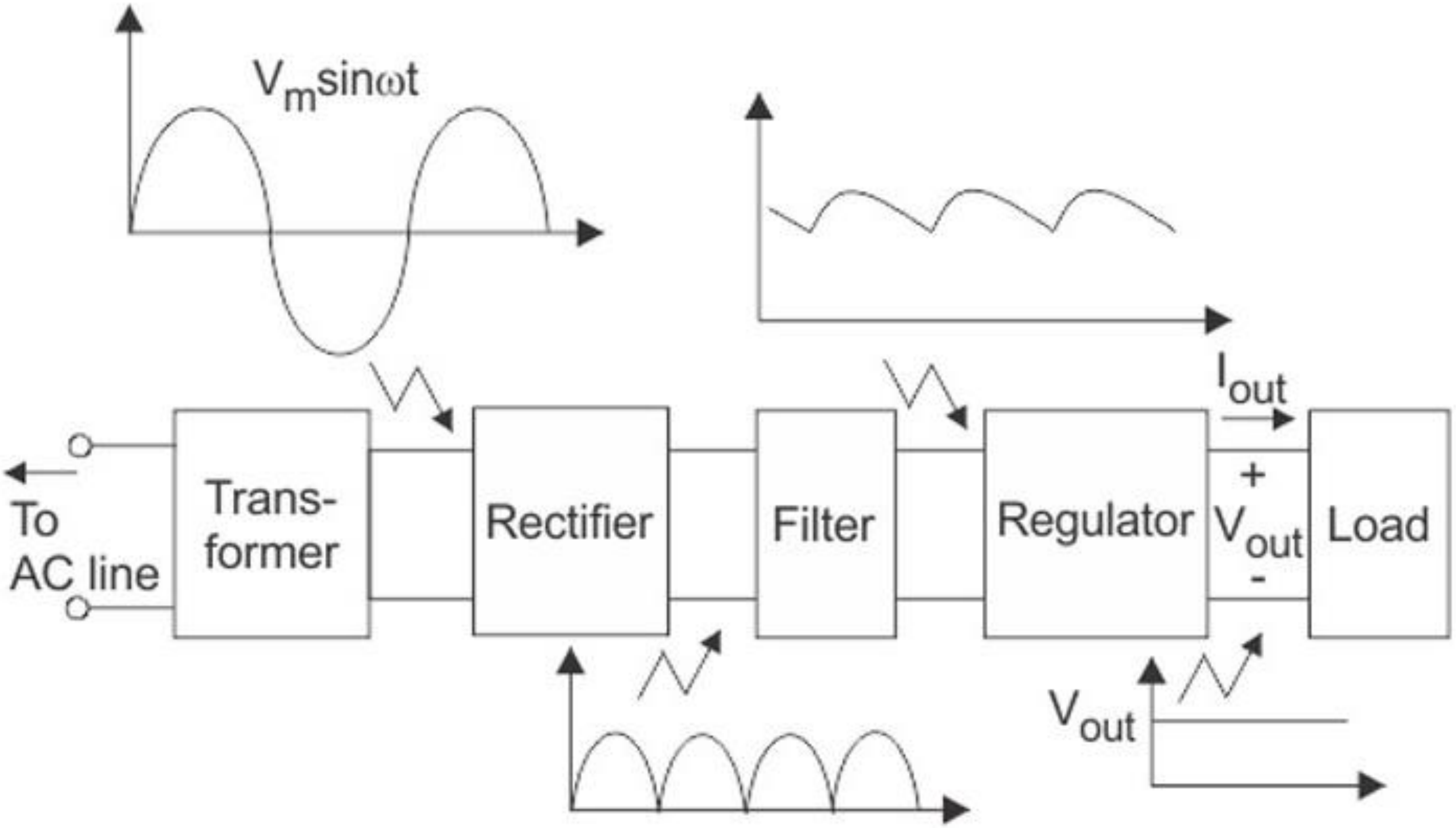
PRINCIPLES OF ELECTRONICS ENGINEERING

UNIT 1

REGULATED POWER SUPPLY: Block Diagram, Bridge Rectifier with filter, Zener diode as Voltage Regulator, Photo diode, LED.

AMPLIFIERS: CEAmplifier with and without feedback, Multistage amplifier, BJT as a switch, Cutoff and Saturation modes.

REGULATED POWER SUPPLY



POWER SUPPLY PERFORMANCE PARAMETERS:

The DC output voltage in a DC Supply varies due to two parameters.

1. Line Regulation
2. Load Regulation

Definitions:

Line Voltage: The input to the unregulated power supply i.e 230V-50Hz AC supply. A +/- 10% variation in the AC supply voltage Vs is common.

Source Effect: The change in output voltage ΔV_0 due to a change in the line voltage.

Source Effect= $\Delta V0$ for a 10% change in Vs

Line Regulation: The source effect expressed as a % of DC output voltage V_0

Line Regulation = =(ΔV_0 for a 10% change in Vs)/V_0 x100

For a good DC power supply, ΔV_0 should be very small. Line Regulation is 0% for an ideal case.

POWER SUPPLY PERFORMANCE PARAMETERS(CONT..,)

Load Effect: The output voltage change ΔV_0 due to the load current change $I_{lmax.}$

$$\text{Load Effect} = \Delta V0 \text{ for } \Delta I_{Lmax}$$

load Regulation: The change in the regulated output voltage when the load current is changed from minimum (no load) to maximum (full load).

"The load effect expressed as a percentage of the output voltage V_0"

$$\text{Load regulation} = (\Delta V_0 \text{ for } \Delta I_{Lmax.})/V_0 \times 100$$

NUMERICALS:

P1: The output Voltage of a DC power supply changes from 20V to 19.7V when the load is increased from 0 to maximum. The Voltage also increases to 20.2V when AC supply increased by 10%. Calculate

i. Load and source Effect

ii. Load and Line Regulation

SOLUTION

Load Effect: ΔV_0 (no load to full load=20-19.7=0.3V

Source Effect: ΔV_0 for a 10% change in Vs=20.2-20=0.2V

Load Regulation: (Load Effect/V_0)*100=(0.3/20)*100=1.5%

Line Regulation: (Source Effect/V_0)*100=(0.2/20)*100=1%

NUMERICALS(CONT.,)

P2: A DC power supply drops from 15V to 14.95V when the AC source voltage falls by 10%. The output also falls from 15V to 14.9V when the load is increased from 0 to maximum. Calculate

i. Load and source Effect

ii. Load and Line Regulation

SOLUTION

Load Effect: ΔV_0 (no load to full load=15-14.9=0.1V

Source Effect: ΔV_0 for a 10% change in V_s=15-14.95=0.05V

Load Regulation: (Load Effect/V_0)*100=(0.1/15)*100=0.66%

Line Regulation: (Source Effect/V_0)*100=(0.05/15)*100=0.33%

RECTIFIER- APPLICATION OF DIODES

A device that converts alternating current into direct current

Types of rectifiers

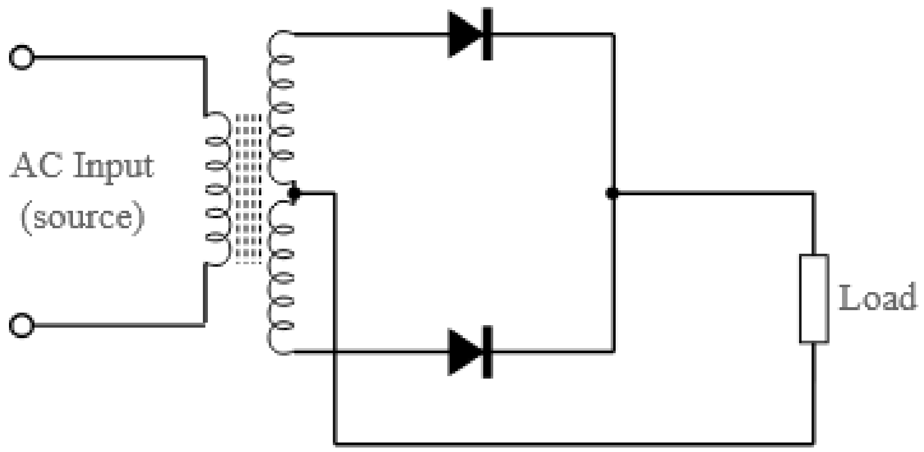
i. Half Wave Rectifier

ii. Full Wave Rectifier

- 2 diodes and a centre tapped transformer
- 4 diodes and an ordinary transformer diodes

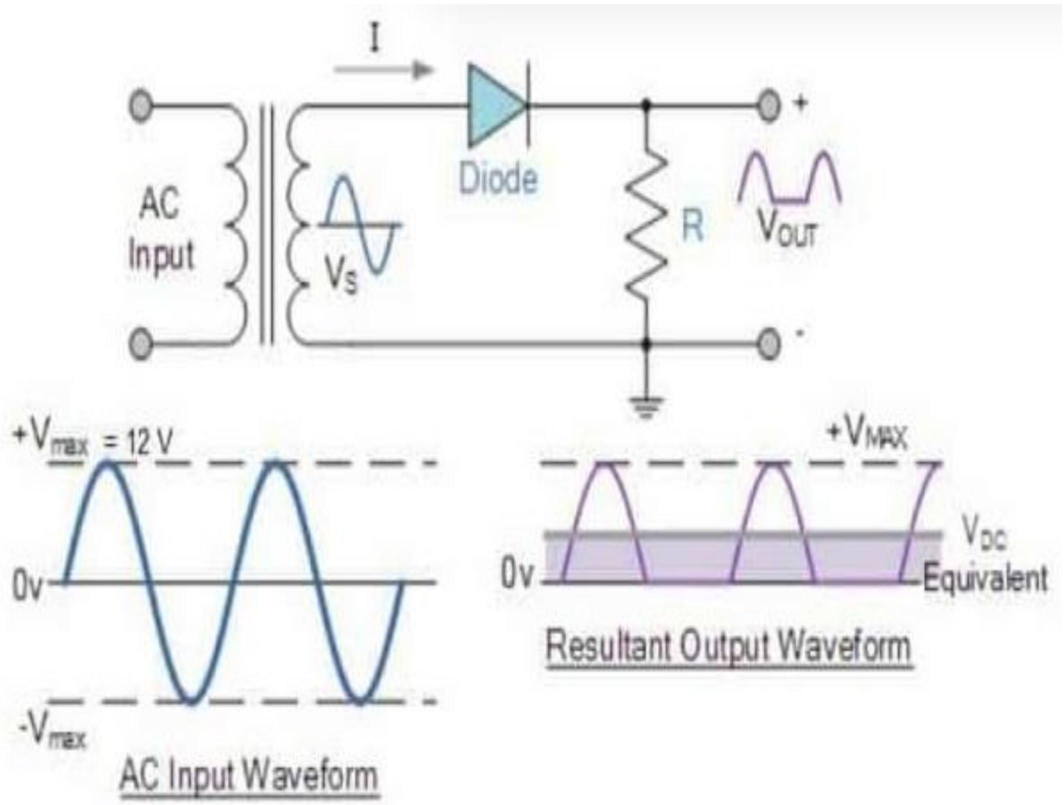
RECTIFIER

Full Wave Rectifier

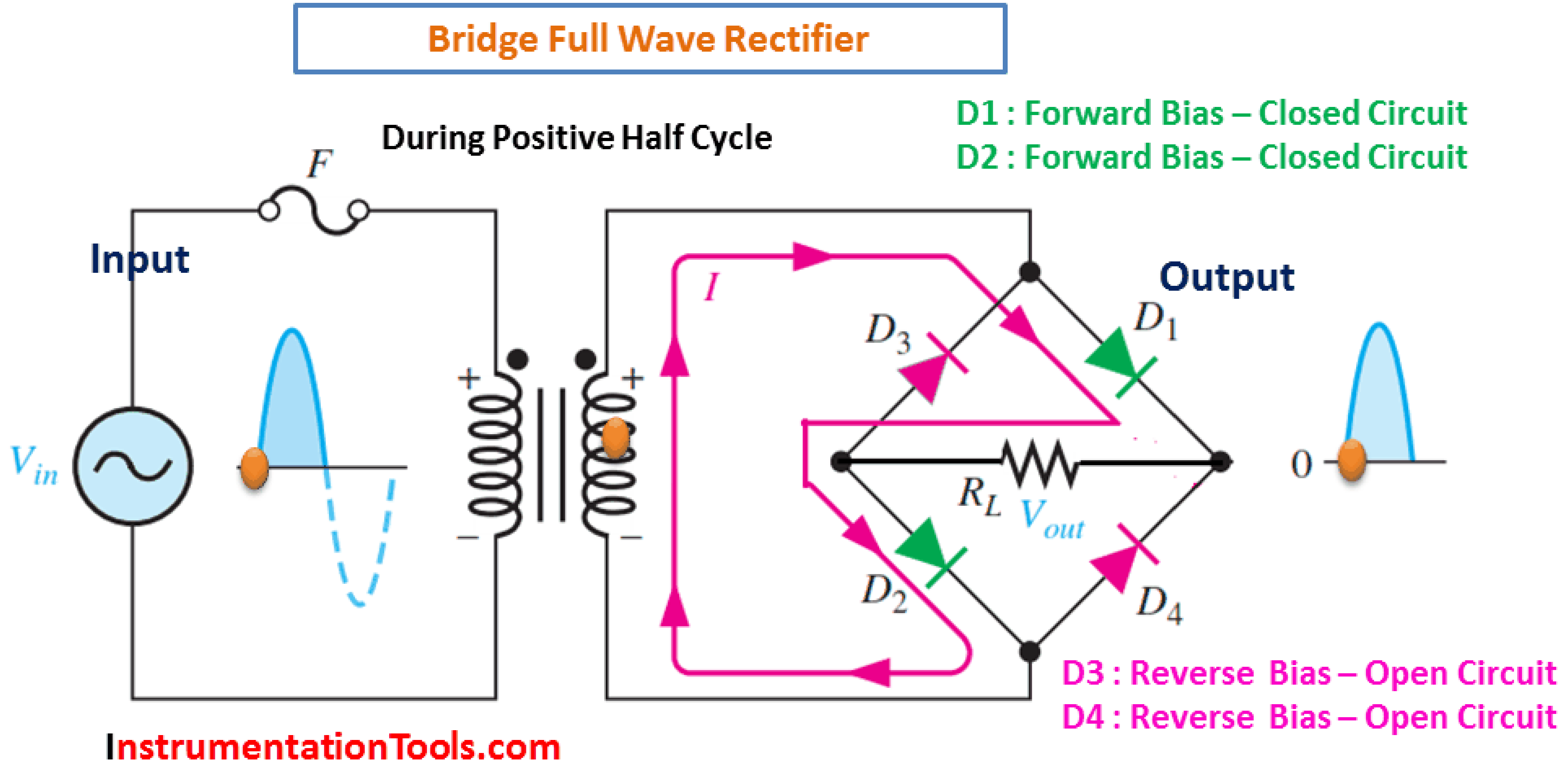


Full wave rectifier using two diodes and a centre tapped transformer

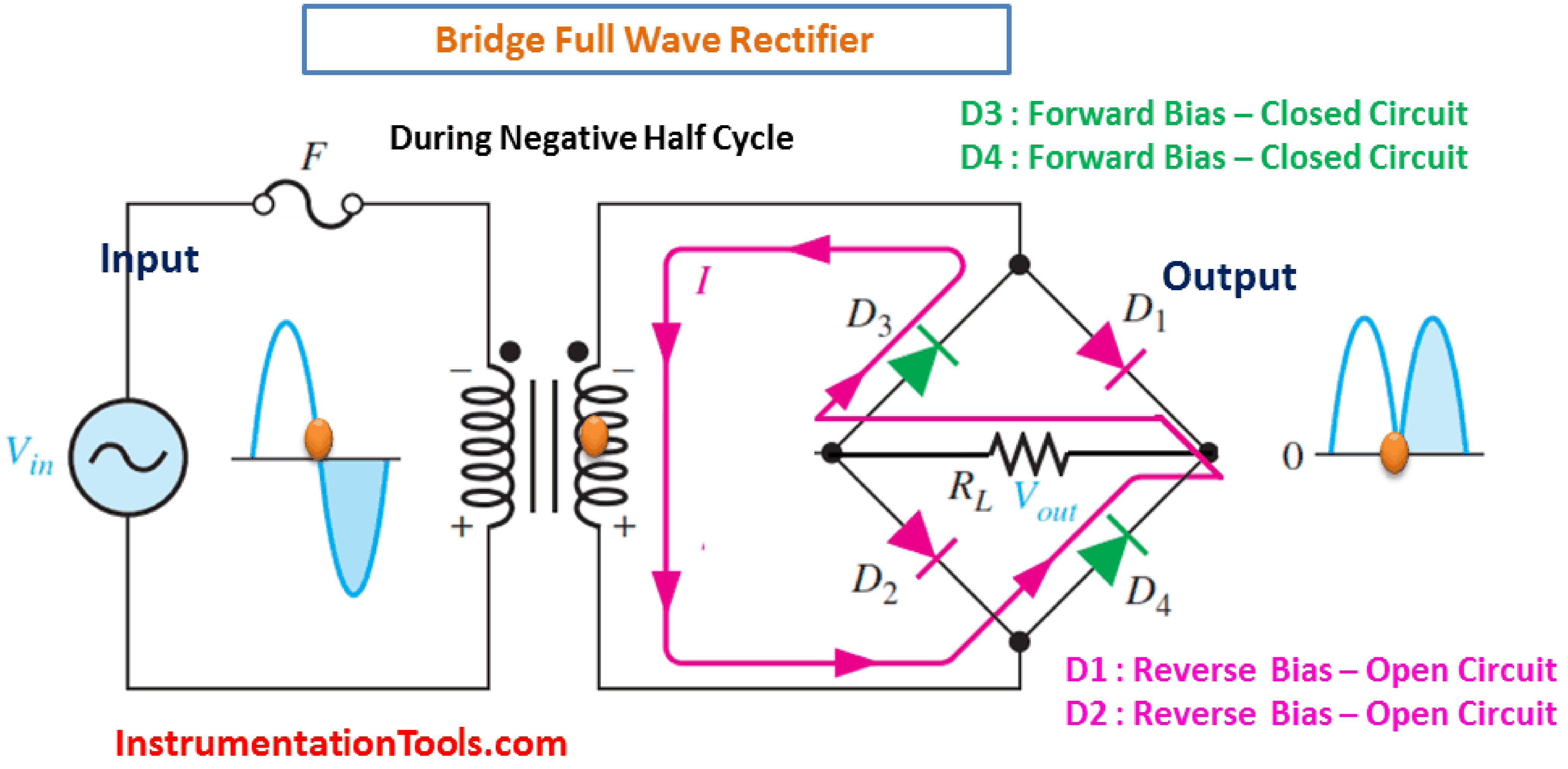
Half Wave Rectifier



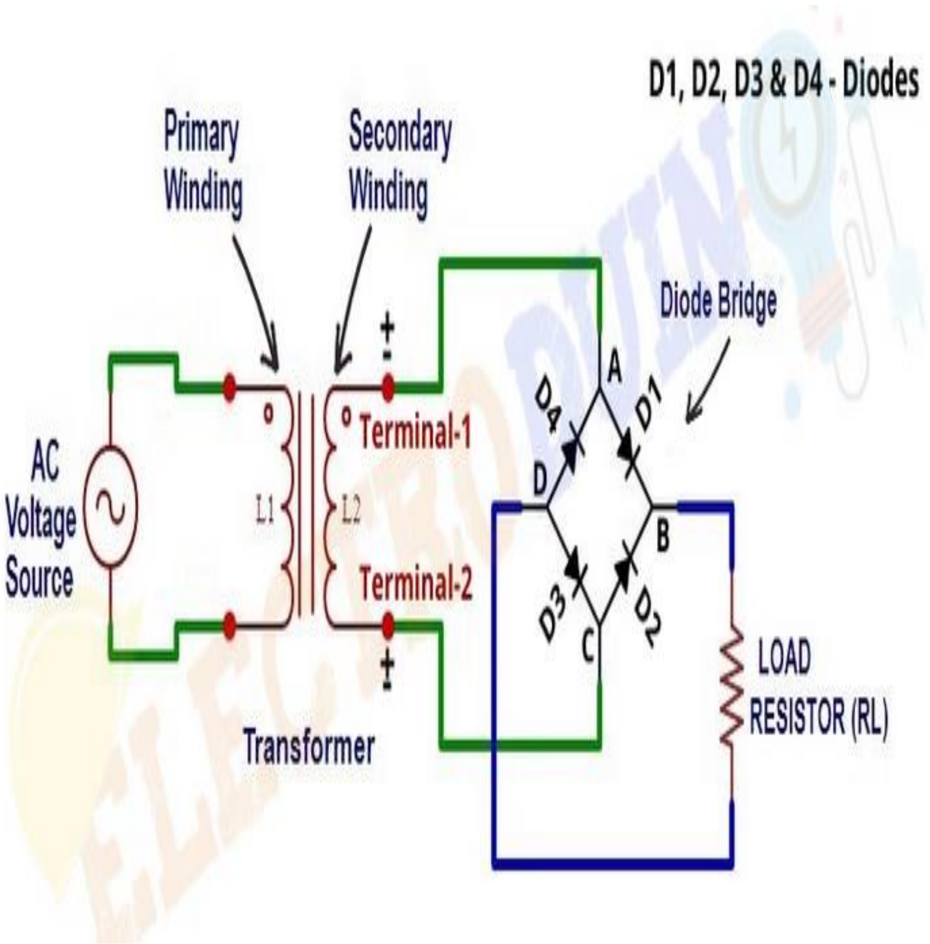
BRIDGE RECTIFIER- 4 DIODES AND AN ORDINARY TRANSFORMER



BRIDGE RECTIFIER- 4 DIODES AND AN ORDINARY TRANSFORMER



Without Filter



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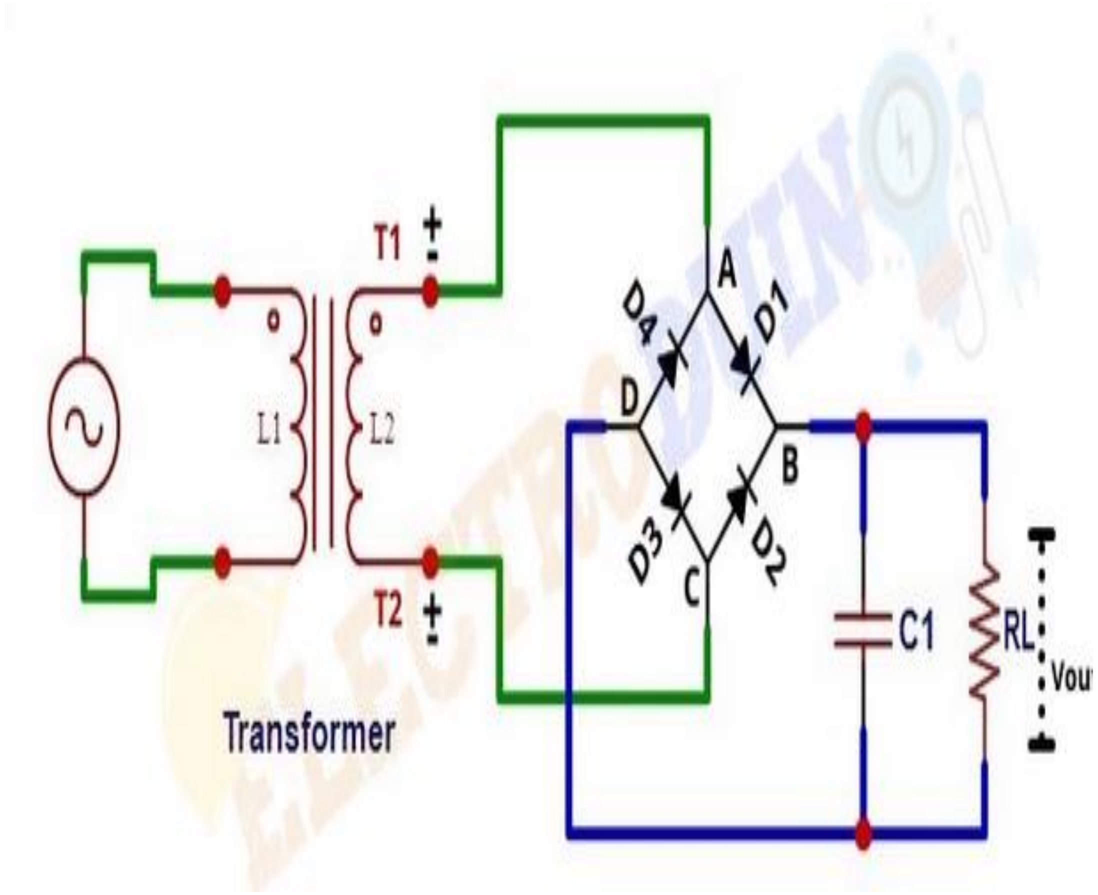
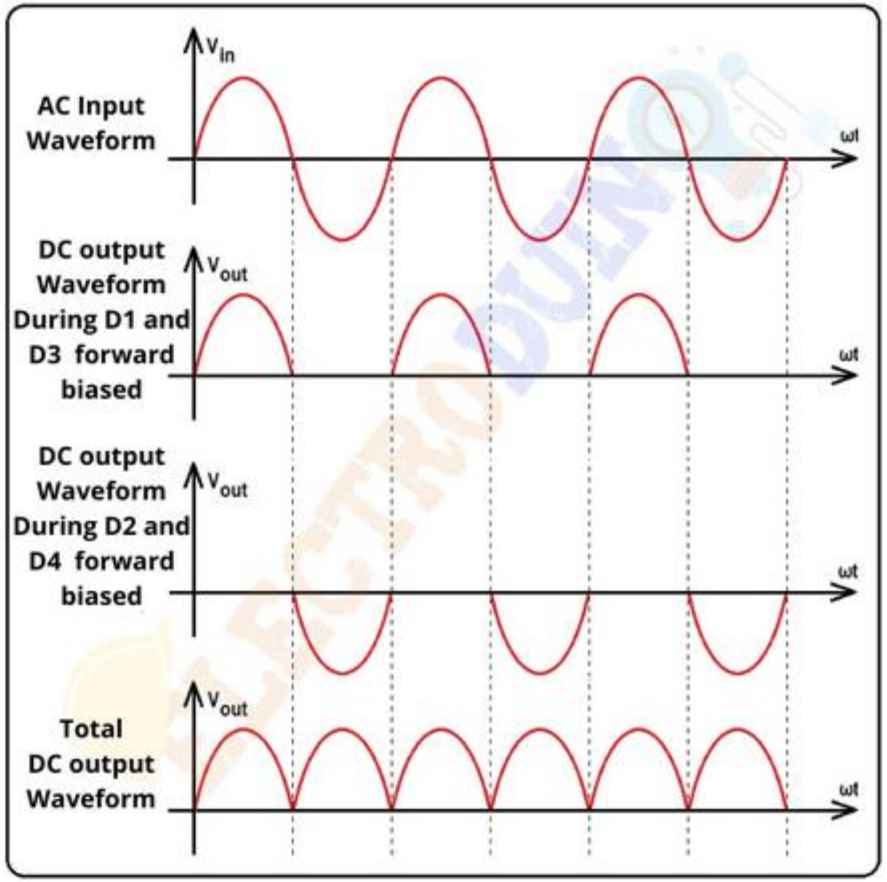
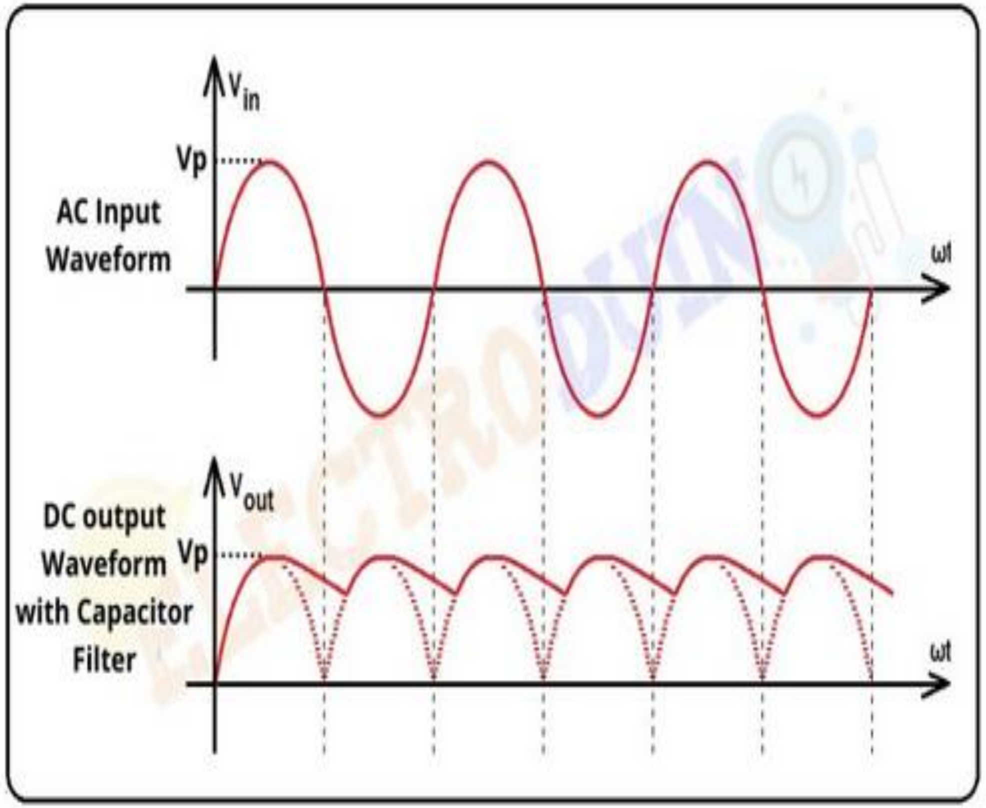


Without Filter



DC Output Waveform

With Filter



DC output Waveform with Capacitor Filter

EQUATIONS

$V_2 - i_o R_f - i_o R_f - i_o R_L = 0$

$i_o = V_2/(2R_f + R_L)$

WKT $V_2 = V_m \sin\omega t$

$i_o = V_m \sin\omega t /(2R_f + R_L)$

$i_o = I_m \sin\omega t$

where $I_m = V_m/(2R_f + R_L)$

$\gamma = 1/4\sqrt{3} fCR_L$

$V_{dc} = V_m/(1 + 1/4fCR_L)$

Load regulation $= 1/4fCR_L$

Sl. No.	Parameter	Equation
1	DC Load Current	$I_{dc} = 2 I_m/\pi$
2	DC Load Voltage	$V_{dc} = 2V_m/\pi\ (1+2 R_f/R_L)$
3	RMS Load Current	$I_{rms} = I_m/\sqrt{2}$
4	RMS Load Voltage	$V_{rms} = V_m/\sqrt{2}\ (1+2 R_f/R_L)$
5	Regulation	$2 R_f/R_L$
6	Effiency of rectification	$\eta = 0.812/1+2 R_f/R_L$
7	Ripple factor	0.483
8	PIV	V_m

PROBLEMS ON FWBR

P1: A Full wave bridge rectifier supplies a load of2K ohms. The AC voltage applied is 200V at secondary of transformer. If a capacitor of 500μF is connected across the load, Find i) Ripple Factor ii) DC Output Voltage iii) Ripple voltage on capacitor iv) DC Load Current v) % of Regulation.

Sol. i) Ripple Factor= $\frac{1}{4\sqrt{3}fcR_L} = \frac{1}{4\sqrt{3}*50*500\mu*2K}$ *100=0.29%

ii) $V_{DC} = \frac{V_m}{\left(1+\frac{1}{4fcR_L}\right)} = \frac{200*\sqrt{2}}{\left(1+\frac{1}{4*50*500\mu*2K}\right)}$ =281.43V

Iii) $\gamma = \frac{V_{ac}}{V_{dc}} = V_{ac}$=0.0029*281.43=0.816V

Iv) $I_{DC} = \frac{V_{dc}}{R_L} = \frac{281.43}{2K} = 0.1407A$

V) % of Regulation = $\frac{1}{4fcR_L}$ *100=0.5%

$\gamma = 1/4\sqrt{3}fCR_L$

$V_{dc} = V_m/(1+1/4fCR_L)$

Load regulation $=1/4fCR_L$

P2: In a Full wave bridge rectifier with capacitor filter the load current from the circuit operating from 230V, 50Hz is 10mA. Estimate the value of Capacitor to keep the Ripple Factor less than 1%.

Sol. $V_m = \sqrt{2} * V_2$=325.27V--------- Maximum peak value in one half of secondary

Ripple Factor=$\frac{1}{4\sqrt{3}fcR_L} < 0.01$

$4\sqrt{3}fcR_L$>100

C> $\frac{100}{4\sqrt{3}fR_L}$

γ =1/4√3fCRL

Vdc=Vm/(1+1/4fCRL)

Load regulation=1/4fCRL

To Find R_L

$V_{DC} = \frac{V_m}{\left(1+\frac{1}{4fcR_L}\right)}$= $\frac{230*\sqrt{2}}{(1+\sqrt{3}\gamma)}$=319.73V

$R_L = \frac{V_{dc}}{I_{DC}} = \frac{319.73}{10m} = 31.97Kohm$

Thus C> $\frac{100}{4\sqrt{3}fR_L}$ = 9 µF

ZENER DIODE

DESIGN OF ZENER REGULATOR

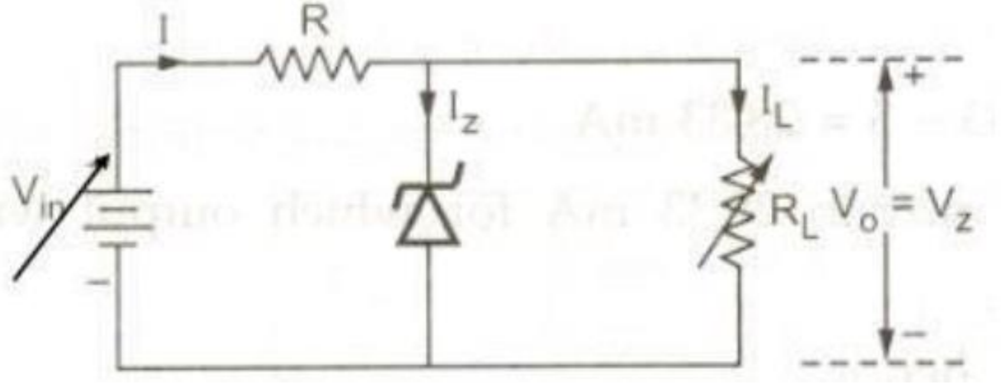


Fig: when both voltage and load are varying

- V_{in} varies between $V_{in(min)}$ to $V_{in(max)}$ and the load current I_L varies from $I_{L(min)}$ to $I_{L\,(max)}$
- $V_0=V_z$

- To find $I_{L\,(max)}=V_z/R_{l(min)}$ & $I_{L\,(min)}=V_z/R_{l(max)}$
- Using KCL, $I=I_z+I_L$ But $I=V_{in}-V_z/R$
- Thus, $V_{in}-V_z/R= I_z+I_L$
- $R= V_{in}-V_z/I_z+I_L$

Case i:

When $V_{in}=V_{in(max)}$ then $I=I_{max}$, $R=R_{min}$, $I_Z=I_{z(max)}$, $I_L=I_{L(min)}$

Thus,

$$\mathbf{R_{(min)}= V_{in(max)}-V_z/I_{z(max)}+I_{L(min)}}$$

Case ii:

When $V_{in}=V_{in(min)}$ then $I=I_{min}$, $R=R_{max}$, $I_Z=I_{z(min)}$, $I_L=I_{L(max)}$

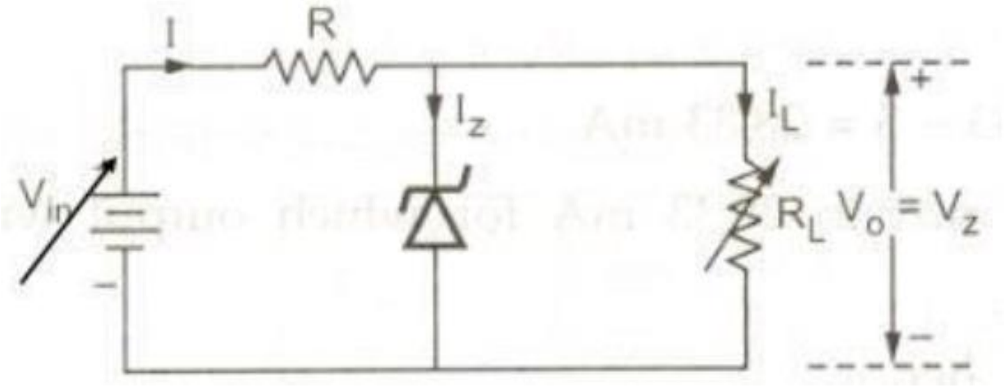
Thus,

$$\mathbf{R_{(max)}= V_{in(min)}-V_z/I_{z(min)}+I_{L(max)}}$$

PROBLEM 1

In the Zener Regulator Circuit design the value of R so that circuit performs satisfactorily under all the given conditions.

V_{in}=22 to 28V, V_z=12V, R_L=50 to 500 Ohm, I_{zmin}=10mA, P_{dMax}=6W.



Sol. To find $I_{L\ (max)}=V_z/R_{l(min)}=12/50=0.24A$

$I_{L\ (min)}=V_z/R_{l(max)}=12/500=0.024A$

Also, $P_{dMax}=V_{z*}I_{zmax}$=Izmax=6/12=0.5A

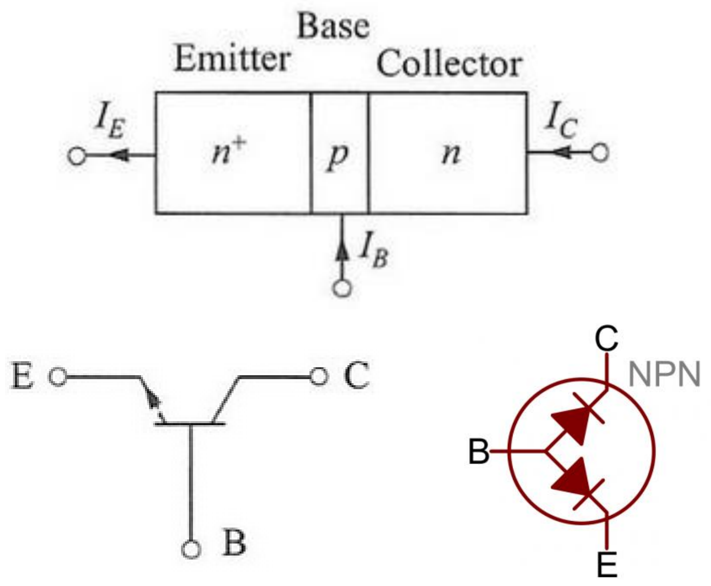
To find R_{min}, $\mathbf{R_{(min)}= V_{in(max)}-V_z/I_{z(max)}+I_{L(min)}=28-12/0.5+0.024=30.53\ Ohm}$

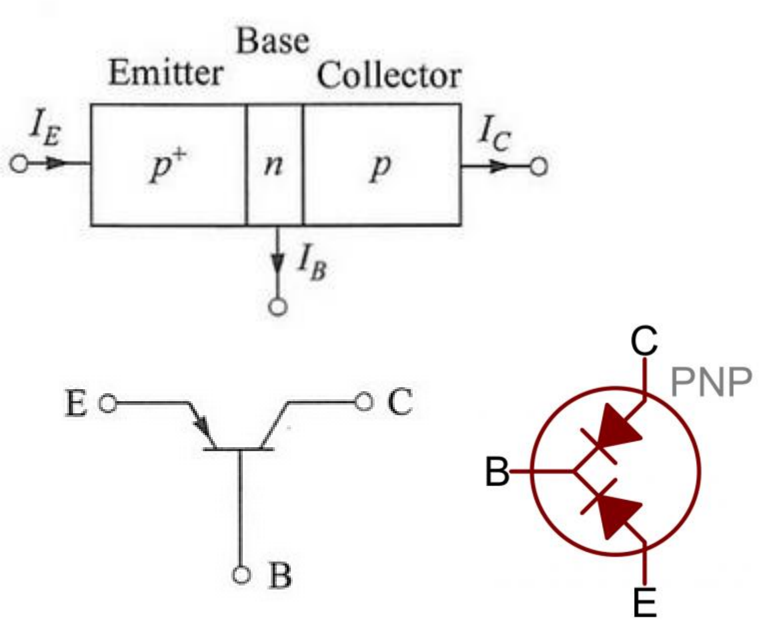
To find R_{max}, $\mathbf{R_{(max)}= V_{in(min)}-V_z/I_{z(min)}+I_{L(max)}=22-12/10m+0.24=40\ Ohm}$

BIPOLAR JUNCTION TRANSISTORS

Co-inventors of the first transistor at Bell Laboratories in 1947: Dr. William Shockley, Dr. John Bardeen and Dr. Walter H. Brattain.

The transistor is a three-layer semiconductor device consisting of either two n- and one p-type layers of material or two p- and one n-type layers of material.





It is 3 terminal device - E for emitter --supplies the charge carriers, C for collector- function is to collect charge carriers and B for base.

Doping Concentration: E>C>B

Width of 3 terminals: C>E>B

BIPOLAR JUNCTION TRANSISTORS.,

Bipolar- holes and electrons participate in the injection process into the oppositely polarized material.

Junction-J_1 & J_2

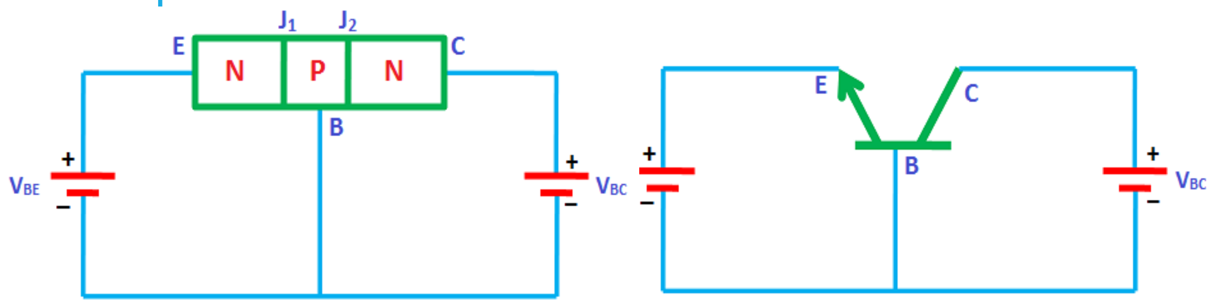
Transistor → transfer + resistor.

Applications of BJT – Televisions, Mobile phones, Computers, Radio transmitters, Audio amplifiers

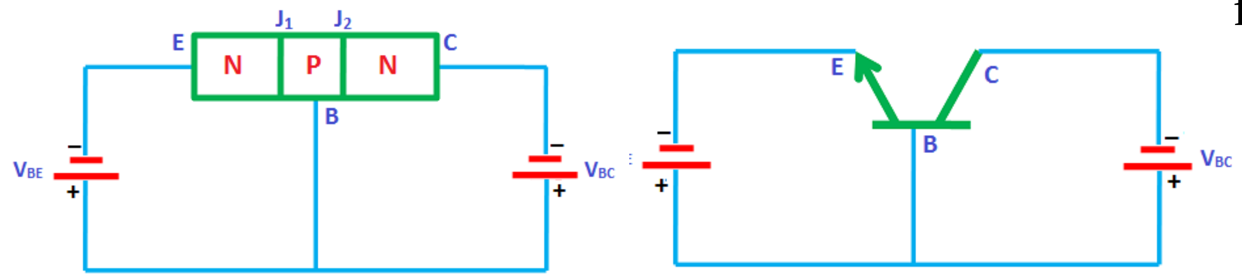
Regions of Operation:

J_1	J_2	Region
FB	FB	Closed Switch, Saturation
FB	RB	Amplifier, Active
RB	FB	Inverter, Reverse Active
RB	RB	Open Switch, Cut off

REGIONS OF OPERATION:



Cutoff mode



Saturation mode

Cutoff mode : Both the junctions of the transistor (emitter to base and collector to base) are reverse biased..

No current flows through the device. Hence, no current flows through the transistor. Therefore, the transistor is in off state and acts like an open switch.

The cutoff mode of the transistor is used in switching operation for switch OFF application.

Saturation mode: Both the junctions of the transistor (emitter to base and collector to base) are forward biased.

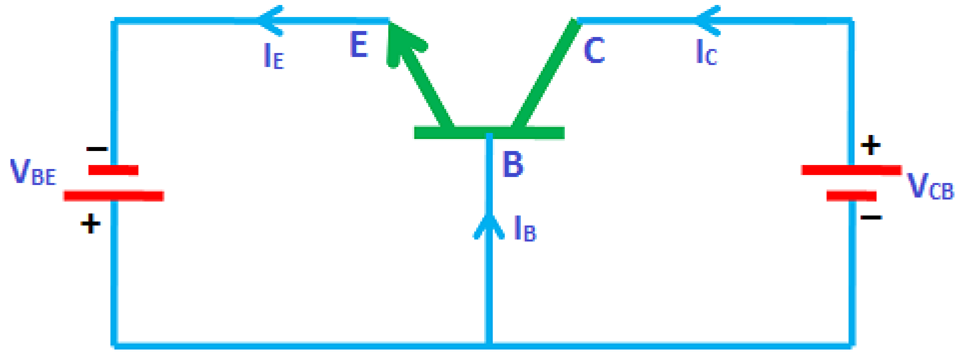
Current flows through the device. free electrons (charge carriers) flows from emitter to base as well as from collector to base. As a result, a huge current will flow to the base of transistor.

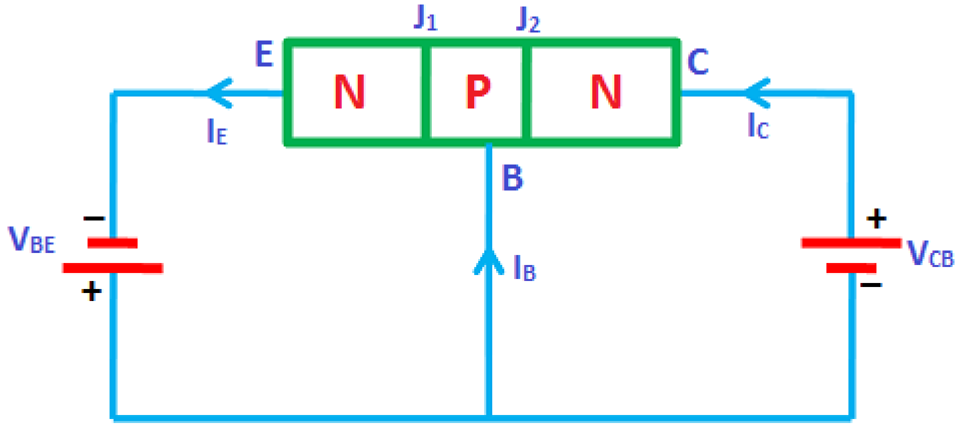
Therefore, the transistor in saturation mode will be in on state and acts like a closed switch.

The saturation mode of the transistor is used in switching operation for switch ON application.

Thus by operating the transistor in saturation and cutoff region, the transistor can be used as an ON/OFF switch.

REGIONS OF OPERATION:



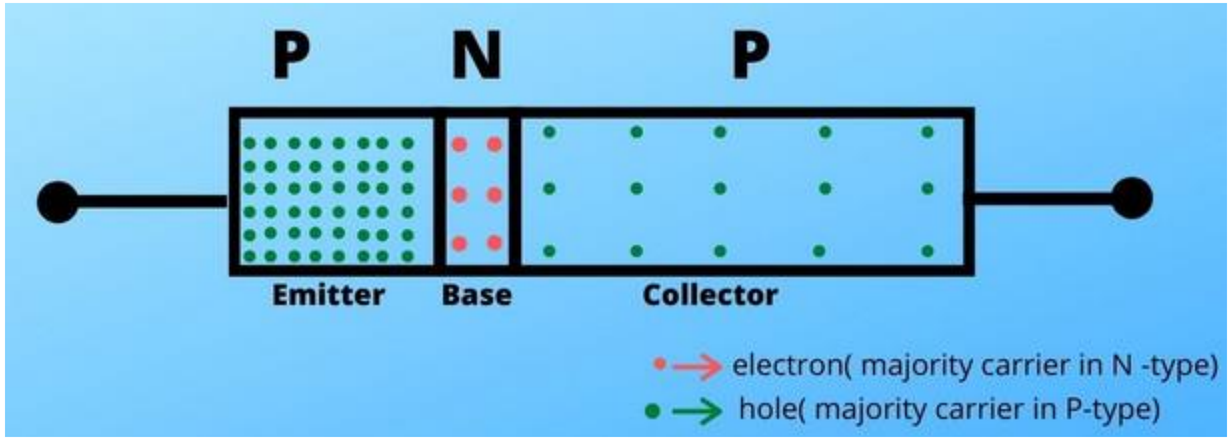


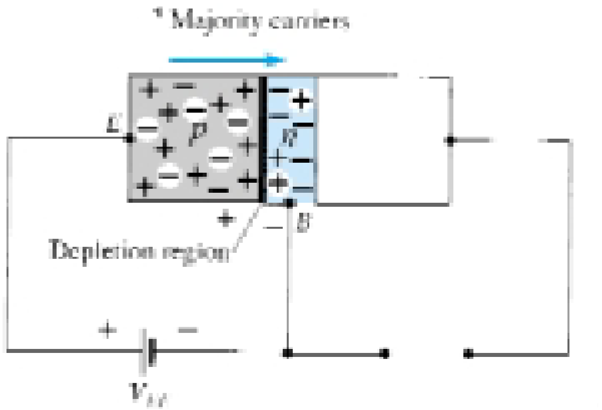
Active mode

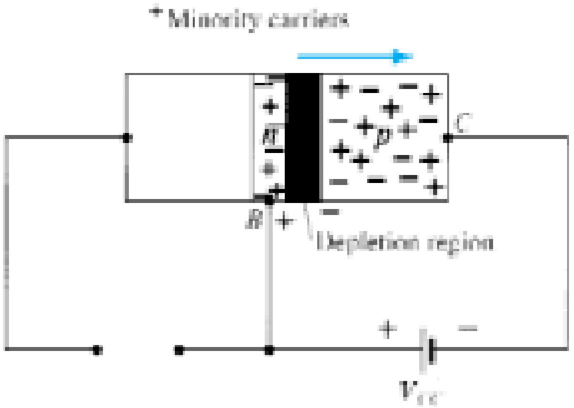
Active mode: One junction (emitter to base) is forward biased and another junction (collector to base) is reverse biased.

The active mode of operation is used for the amplification of current.

WORKING OF PNP TRANSISTOR







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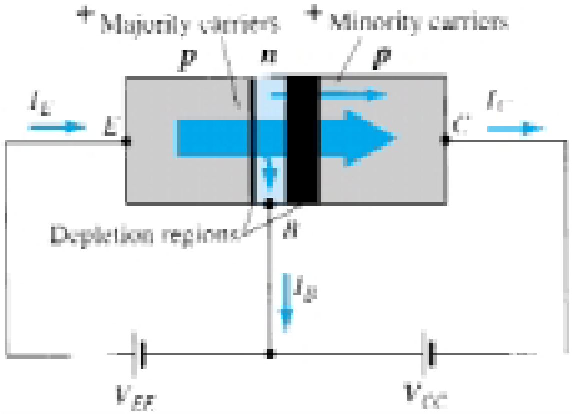


CONT.,

Applying Kirchhoff's current law to the transistor,

$$\boxed{I_E = I_C + I_B}$$

The collector current, is comprised of two components—the majority and minority carriers. The minority-current component is called the leakage current I_{CO}.

$$\boxed{I_C = I_{C_{majority}} + I_{CO_{minority}}}$$

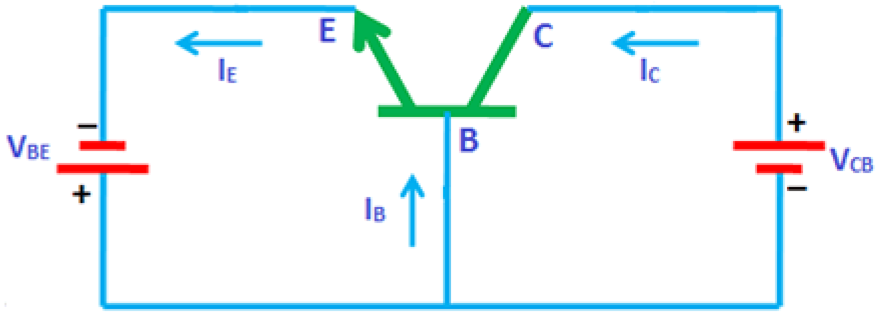
I_C is measured in milliamperes, while I_{CO} is measured in microamperes or nanoamperes.

V_{BC} is increased to such an extent where Base region reduces so much that J_2 and J_1 would merge giving I_B=0----Early Effect/Base Width Modulation.

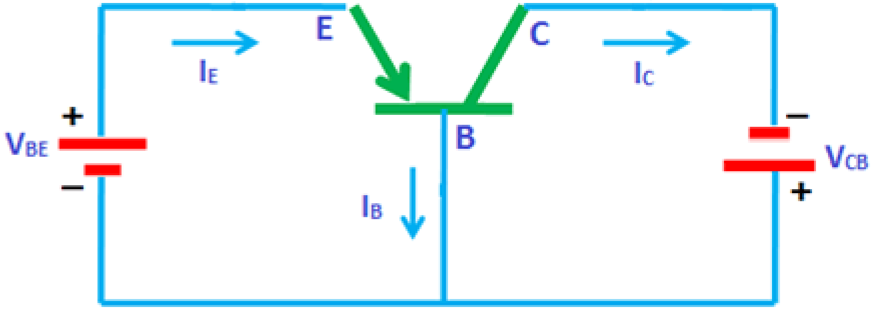
$I_E \approx I_C$

The effect of increase in Reverse voltage reducing the base width is known as BWM or EF

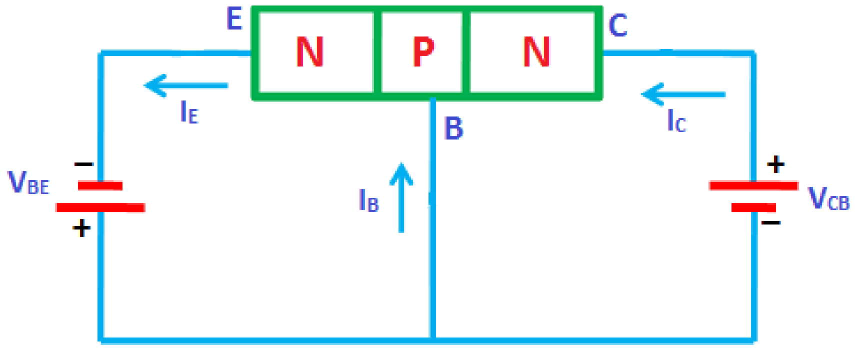
COMMON-BASE CONFIGURATION



NPN Transistor



PNP transistor



The input signal is applied between the emitter and base terminals while the corresponding output signal is taken across the collector and base terminals.

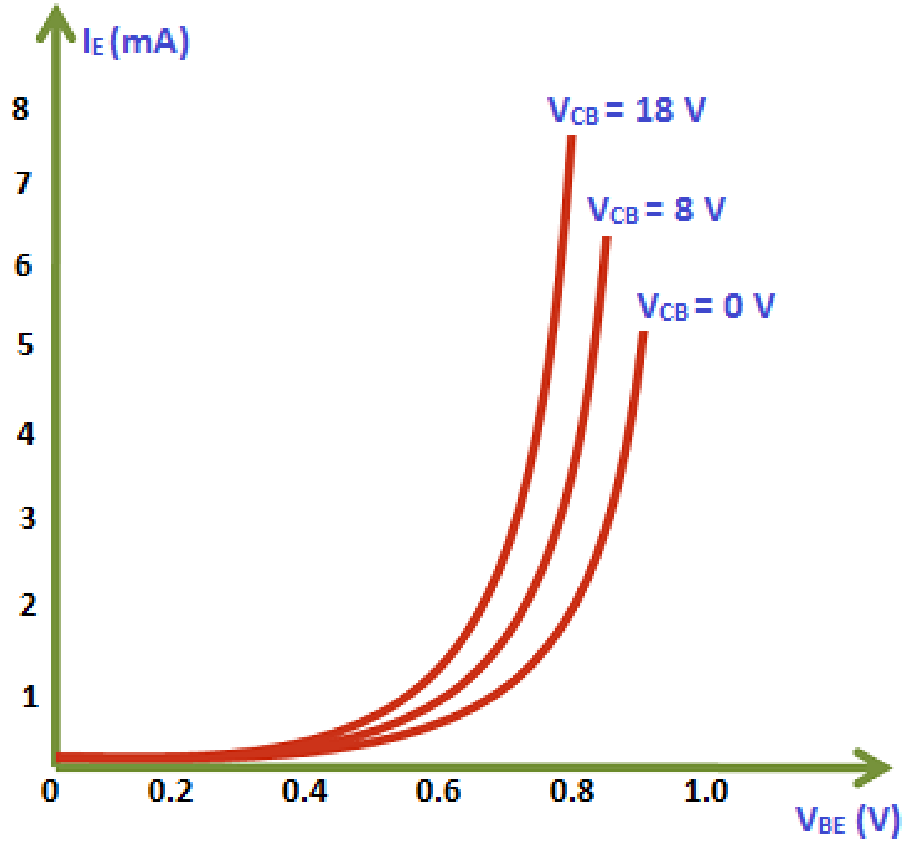
Thus the base terminal of a transistor is common for both input and output terminals and hence it is named as common base configuration.

Two set of characteristics:

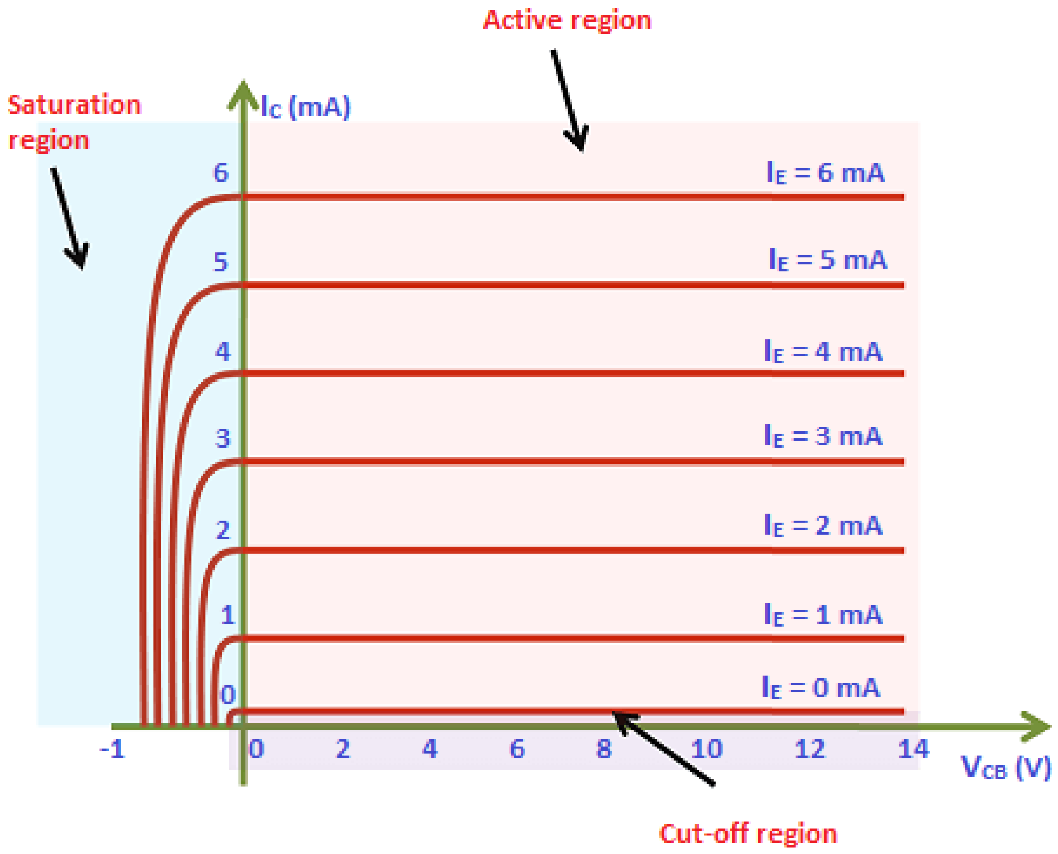
i. Input characteristics - relationship between input current (I_E) and the input voltage (V_{BE})

ii. Output characteristics -relationship between input current (I_c) and the input voltage (V_{CB})

CONT.,



I/p characteristics CB configuration



O/P characteristics CB configuration

CONT.,

Alpha(α)- In the dc mode the levels of IC and IE due to the majority carriers are related by

Alpha typically extends from 0.90 to 0.998

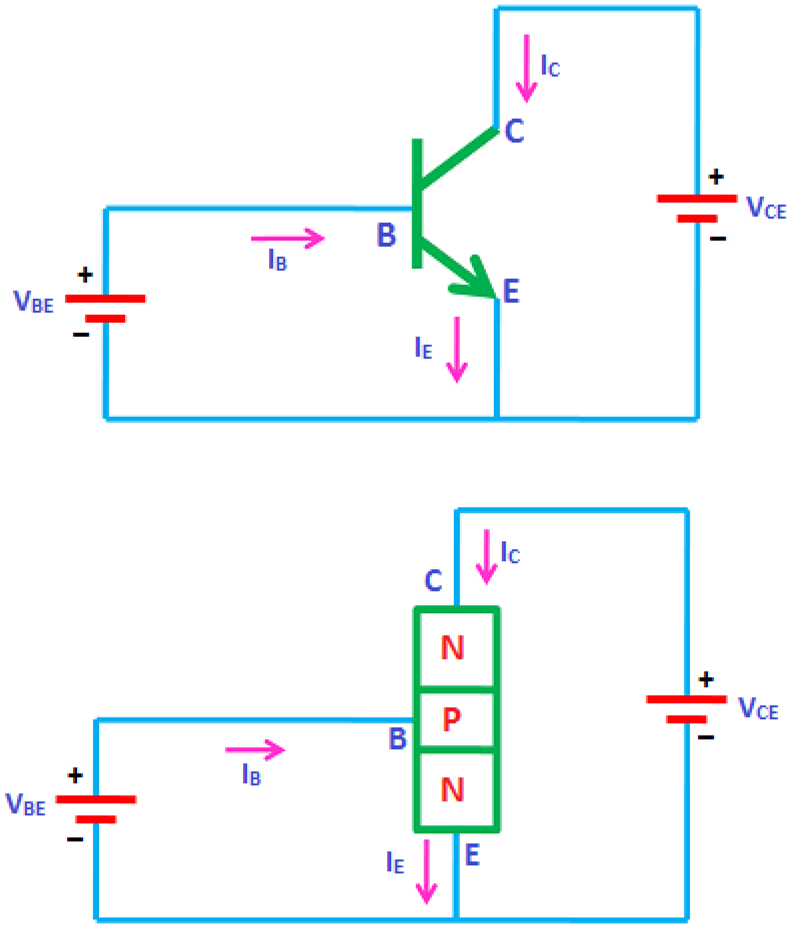
$$\alpha_{dc} = \frac{I_C}{I_E}$$

When emitter is open then

$$I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}$$

$$I_C = \alpha I_E + I_{CBO}$$

COMMON-EMITTER CONFIGURATION



Common emitter configuration

Used when large current gain is needed.

The supply voltage between base and emitter is denoted by V_{BE} while the supply voltage between collector and emitter is denoted by V_{CE}

Input current or base current is denoted by I_B and output current or collector current is denoted by I_C

Two set of characteristics:

i. Input characteristics - relationship between input current (I_B) and the input voltage (V_{BE})

ii. Output characteristics -relationship between input current (I_c) and the input voltage (V_{CE})

CONT.,

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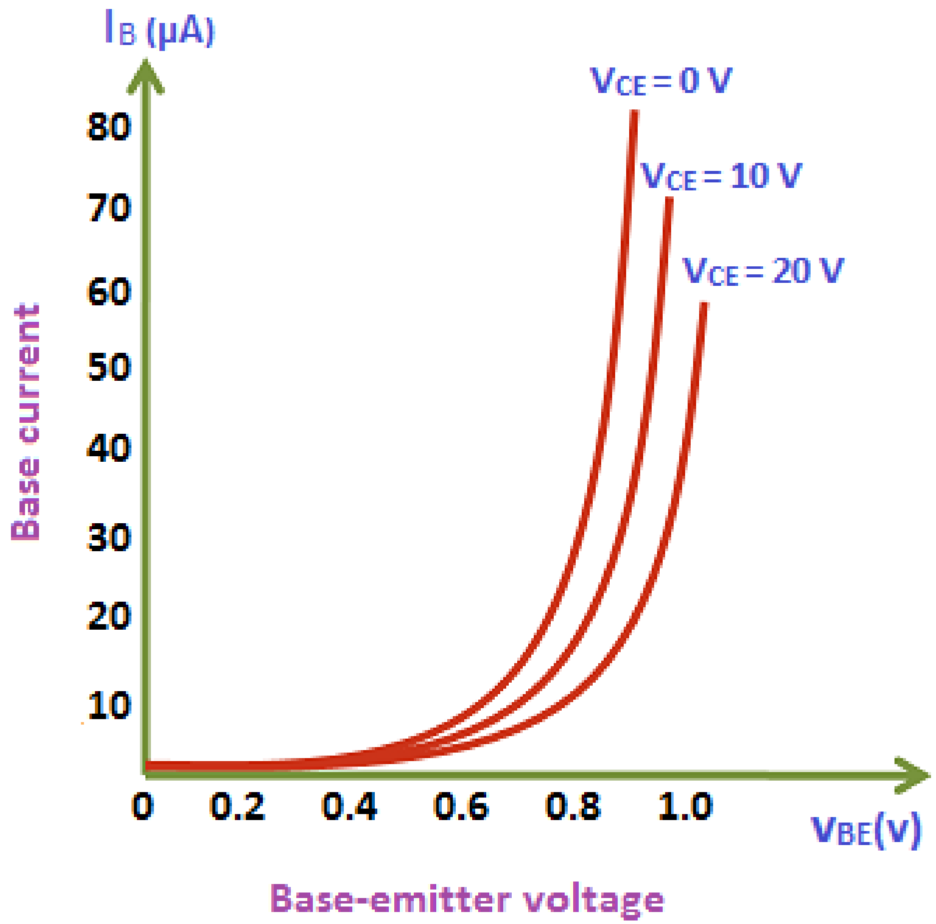
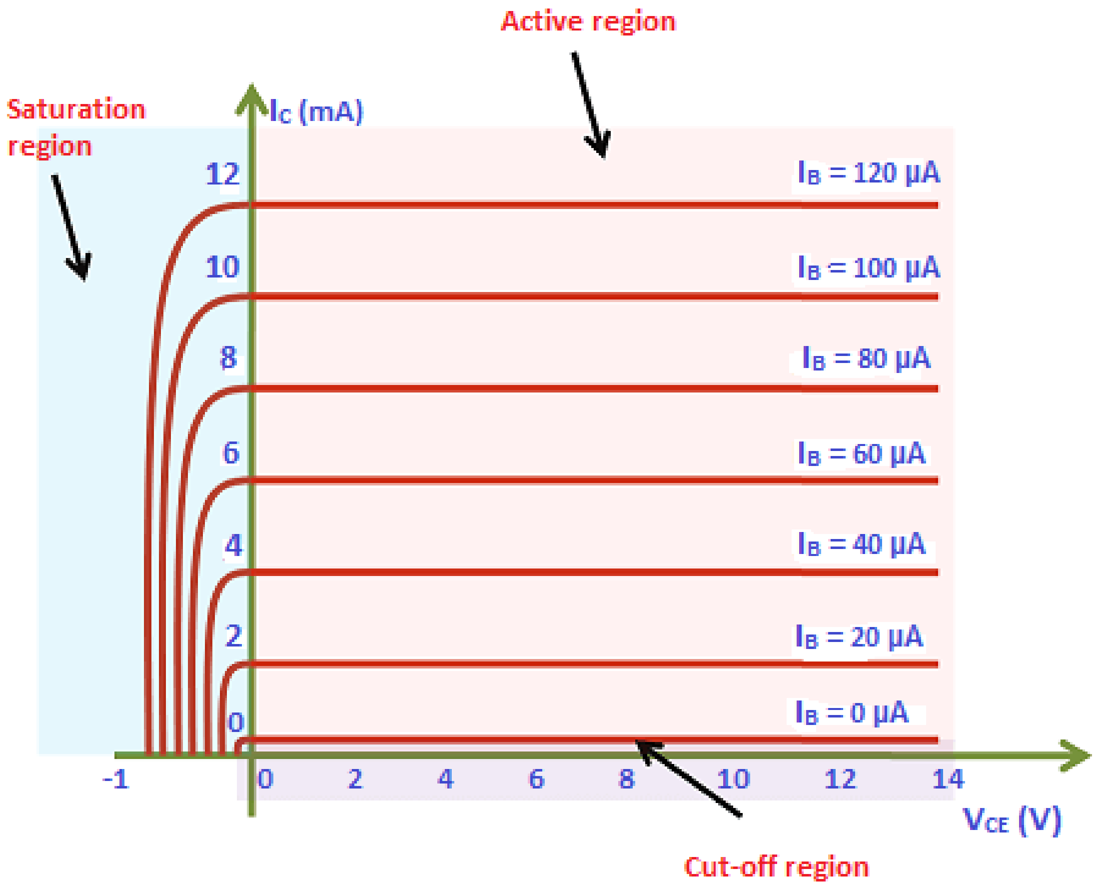


I/P characteristics CE configuration



O/P Characteristics CE Configuration

CONT.,

Beta(β)- In the dc mode the levels of IC and IE due to the majority carriers are related by

Beta typically extends from 50 to over 400

$$\beta_{dc} = \frac{I_C}{I_B}$$

When emitter is open then

$$I_C = I_{C_{majority}} + I_{CO_{minority}}$$

$$I_C = \alpha I_E + I_{CBO}$$

$I_C = \alpha(I_C + I_B) + I_{CBO}$

$(1-\alpha)I_C = \alpha I_B + I_{CBO}$

$(1-\alpha)I_C = \alpha I_B + I_{CBO}$

$I_C = \alpha I_B/(1-\alpha) + I_{CBO}/(1-\alpha)$

$$I_{CEO} = \left.\frac{I_{CBO}}{1-\alpha}\right|_{I_B = 0\ \mu A}$$

RELATIONSHIP B/W A & B

WKT $$I_E = I_C + I_B$$

Divide by I_c

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

$$\boxed{\alpha = \frac{\beta}{\beta + 1}}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$$

$$\frac{1}{1 - \alpha} = \beta + 1$$

$$I_{CEO} = (\beta + 1)I_{CBO}$$

$$\boxed{I_{CEO} \cong \beta I_{CBO}}$$

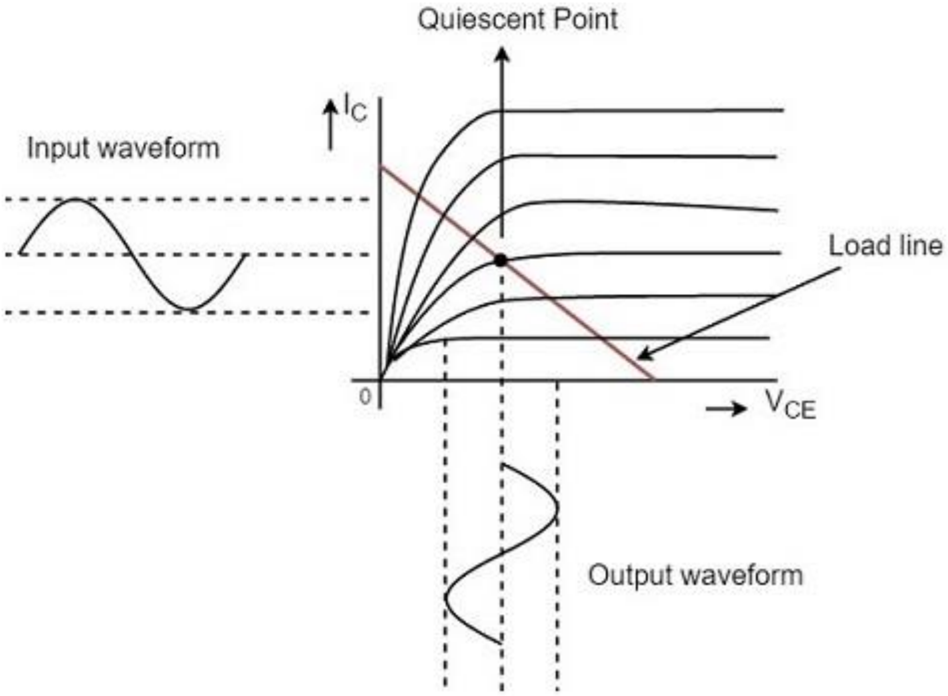
$$\boxed{I_C = \beta I_B}$$

$$I_E = I_C + I_B$$

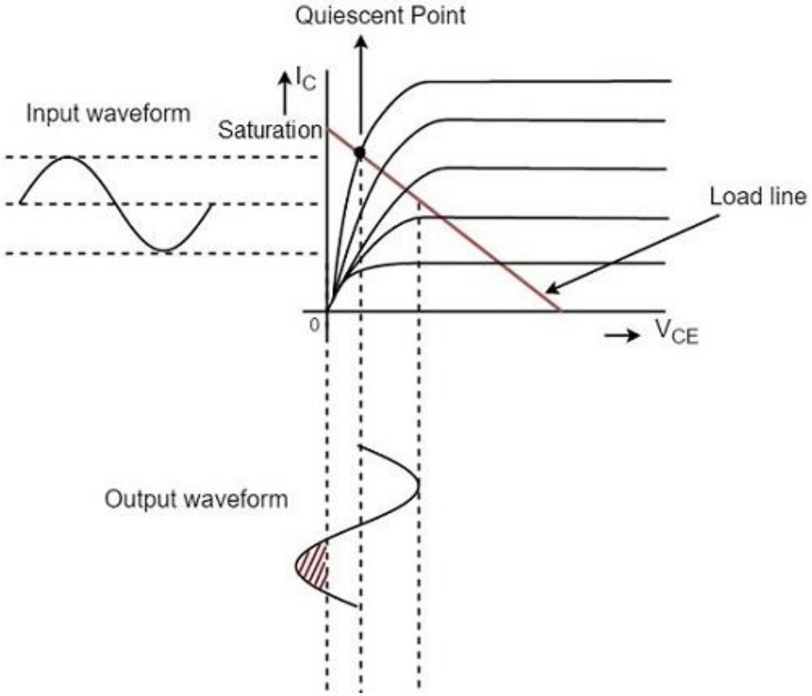
$$= \beta I_B + I_B$$

$$\boxed{I_E = (\beta + 1)I_B}$$

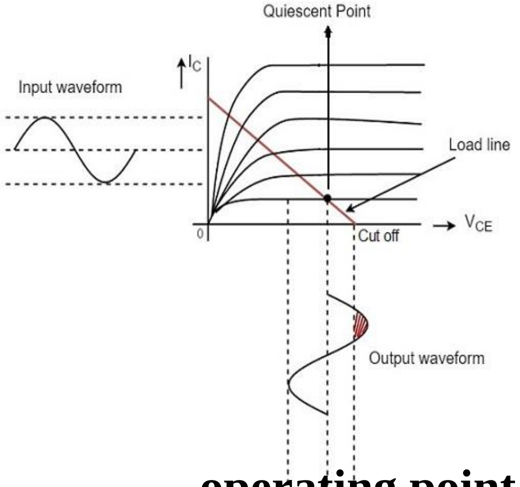
FOR AMPLIFICATION



Operating point is in the middle of active region

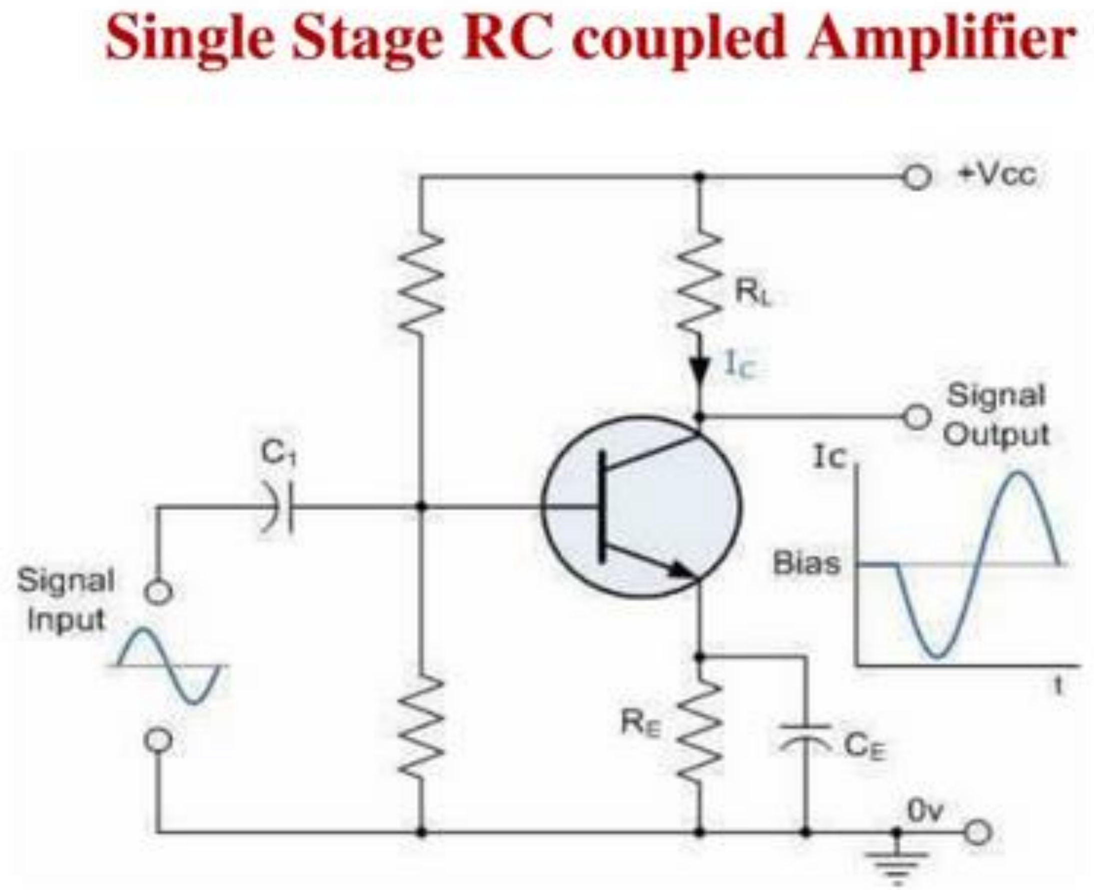


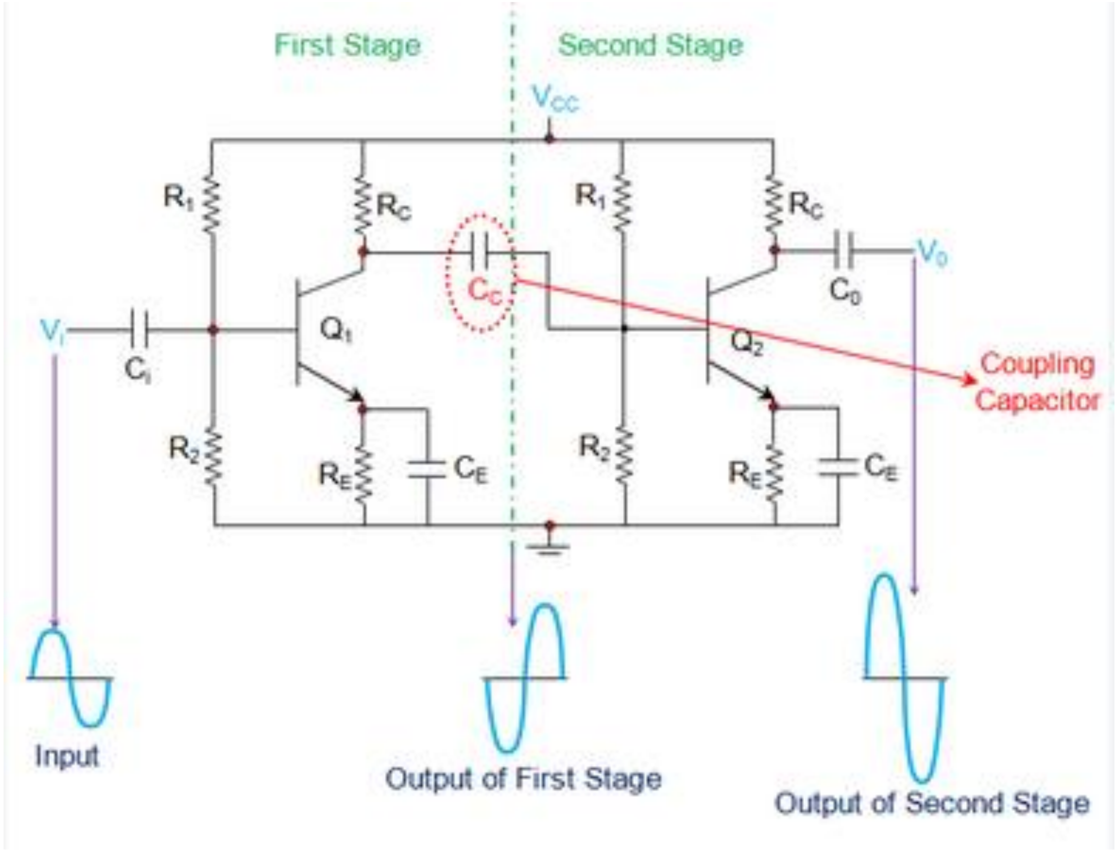
operating point is considered near saturation point



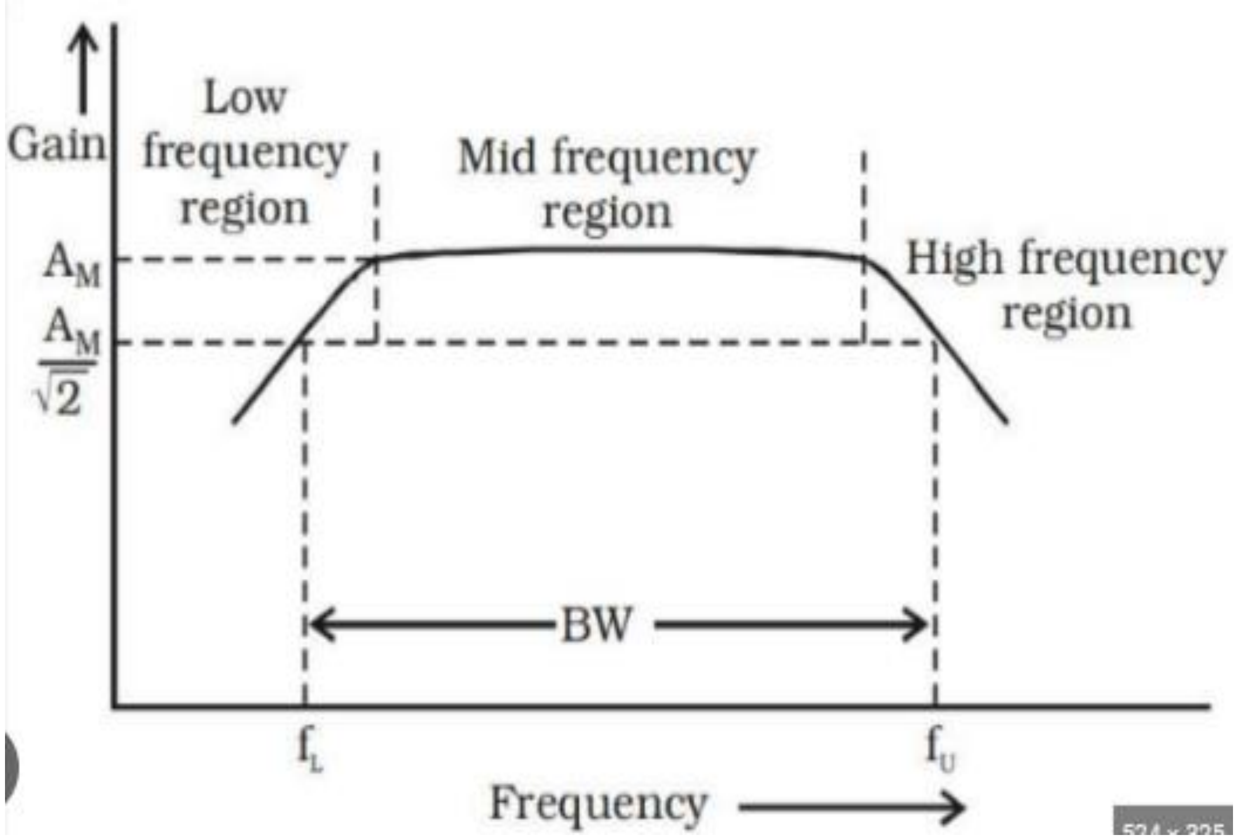
operating point is considered near cutoff point

SINGLE STAGE AND 2 STAGE RC COUPLED AMPLIFIER





FREQUENCY RESPONSE



Bandwidth:

Specifies range of frequencies over which the gain does not deviate more than 70.7% of maximum gain at the mid freq range.

f_H and f_L are referred as Half Power Frequencies.

They are called Half Power points because the gain or output voltage drops to 70.7% of maximum value.

PROBLEMS:

Three amplifiers of voltage gain 20 dB, 26dB and 32dB are cascaded to obtain an output voltage of 2V. Calculate the input voltage required.

$$A_{dB}=A_{1dB}+A_{2dB}+A_{3dB}=20+26+32=78dB$$

$$A_{dB}=20\log(V_0/V_i)=78$$

$$20\log(2/V_i)=78$$

$$V_i=0.25mV$$

An Amplifier having a power gain of 17dB delivers a power output of 40W to a load of 1K Ohm. Calculate i)The input power needed and ii)Input voltage needed, if the voltage gain of amplifier is 38dB.

Sol. $A_{dB}=10\log(P_0/P_i)=17$

$P_i=0.79W$

Voltage gain$=20\log(V_0/V_i)=38$------1

Find V_0 using P_0 of 40W

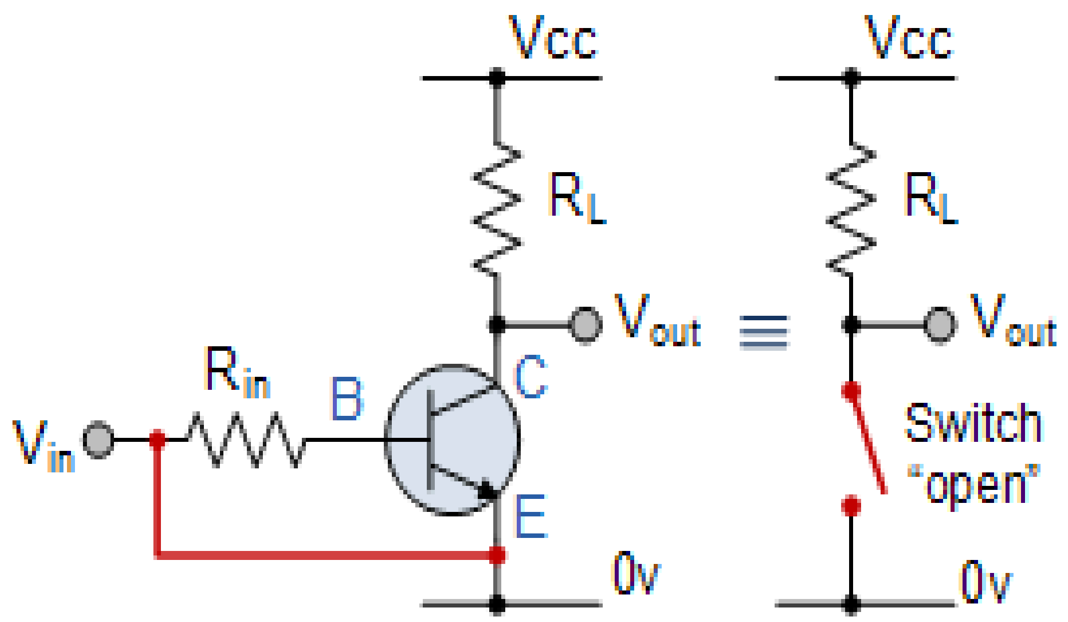
$P_o=v_o^2/R_l=40$

$V_o=200V$--------2

Substituting 2 in 1

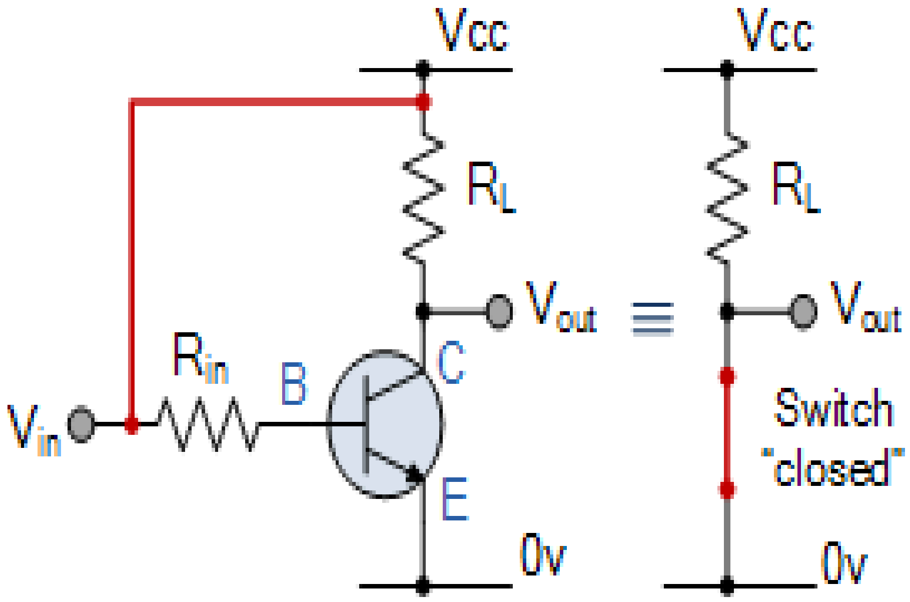
$V_i=2.51V$

TRANSISTOR AS SWITCH



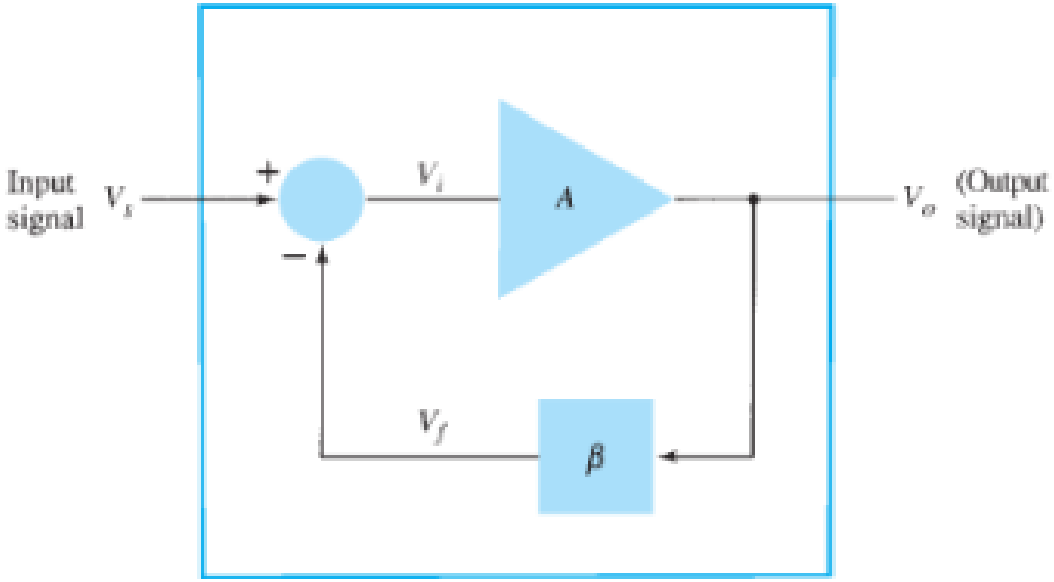
- The input and Base are grounded (0v)
- Base-Emitter voltage $V_{BE} < 0.7v$
- Base-Emitter junction is reverse biased
- Base-Collector junction is reverse biased
- Transistor is "fully-OFF" (Cut-off region)
- No Collector current flows ($I_C = 0$)
- $V_{OUT} = V_{CE} = V_{CC} =$ "1"
- Transistor operates as an "open switch"

TRANSISTOR AS SWITCH



- The input and Base are connected to V_{CC}
- Base-Emitter voltage $V_{BE} > 0.7v$
- Base-Emitter junction is forward biased
- Base-Collector junction is forward biased
- Transistor is "fully-ON" (saturation region)
- Max Collector current flows ($I_C = Vcc/R_L$)
- $V_{CE} = 0$ (ideal saturation)
- $V_{OUT} = V_{CE} =$ "0"
- Transistor operates as a "closed switch"

NEGATIVE FEEDBACK:



Feedback amplifier

Gain with feedback:

$$A = \frac{V_o}{V_s} = \frac{V_o}{V_i}$$

$$V_i = V_s - V_f$$

$$V_o = AV_i = A(V_s - V_f) = AV_s - AV_f = AV_s - A(\beta V_o)$$

$$(1 + \beta A)V_o = AV_s$$

$$\boxed{A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}}$$

ADVANTAGES OF NEGATIVE FEEDBACK AMPLIFIERS:

Input impedance increases by a factor of $1+A\beta$

Output impedance decreases by a factor of $1+A\beta$

Bandwidth increases by a factor of $1+A\beta$

Distortion decreases by a factor of $1+A\beta$

Noise decreases by a factor of $1+A\beta$

Stability of the gain improves by a factor of $1+A\beta$