Unit - 3

~~Binary Number Systems~~
Boolean Algebra

George Boole (1854)
Also called Switching Algebra.

Laws of Boolean Algebra

$\bar{0} = 1$

$\bar{1} = 0$

If $x = 0$, $\bar{x} = 1$

If $x = 1$, $\bar{x} = 0$

$\bar{\bar{x}} = x$

$x \cdot 0 = 0$

$x \cdot 1 = 1$

$x \cdot x = x$

$x \cdot \bar{x} = 0$

$x + 0 = x$

$x + 1 = 1$

$x + x = x$

$x + \bar{x} = 1$

$x + xy = x(1+y) = x$

$x + \bar{x}y = x + xy + \bar{x}y = x + y(x+\bar{x}) = x + y$

Logic Gates

They are digital circuits that take in 1/more input signals to produce one output signal.
The input/output signals are either low/high voltage.

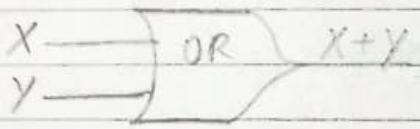
Logical divisions → AND, OR, NOT gate.

OR Gate

It takes in two/more input signals to produce one output signals. It performs logical additions. If both inputs are high, the output is also high.

$$Z = X + Y$$

Symbol



Truth table

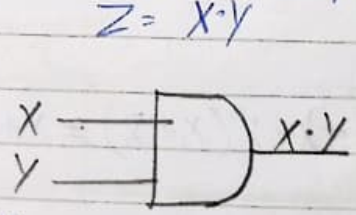
X	Y	X+Y
0	0	0
0	1	1
1	0	1
1	1	1

AND gate

It takes in two/more input signals to produce one output signal. It performs logical multiplication. If either of the two inputs it low, the output signal is also low.

$$Z = X \cdot Y$$

Symbol



Truth Table

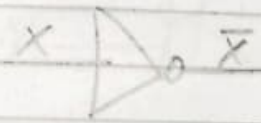
X	Y	X·Y
0	0	0
0	1	0
1	0	0
1	1	1

NOT Gate

It is also called inverter. It performs complementation. It converts one logic level to another logic level. It takes in one input signal & produces one output signal.

$$X \longrightarrow \overline{X}$$

Symbol



Truth Table

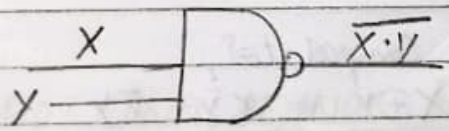
X	$\overline{X}$
0	1
1	0

NAND Gate

It takes in two/more input signals to produce one output signal. When all inputs are low, the output produced is high.

$$Z = \overline{X \cdot Y}$$

Symbol



Truth table

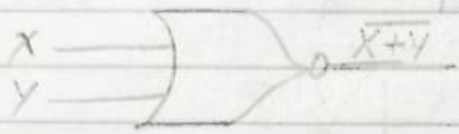
X	Y	$X \cdot Y$	$\overline{X \cdot Y}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

NOR Gate

It takes in two/more input variables to produce one output
If all inputs are low, the output is high

$$Z = \overline{X+Y}$$

Symbol



Truth table

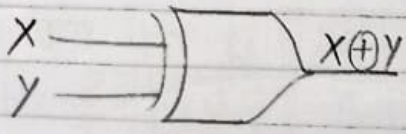
X	Y	X+Y	$\overline{X+Y}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

XOR Gate / EX-OR gate

It takes in two/more input signals to produce one output signal. The output is high when any one of the input is High.
Also called inequality Comparator.

$$Z = X \oplus Y = X\bar{Y} + \bar{X}Y$$

Symbol



Truth table

X	Y	X⊕Y
0	0	0
0	1	1
1	0	1
1	1	0

XNOR gate / Ex-NOR gate

It takes in two/more input signals to produce one output signal. When all inputs are low, the output is high.

$$Z = X \odot Y$$

Symbol

Truth Table

X	Y	X⊙Y
0	0	1
0	1	0
1	0	0
1	1	1

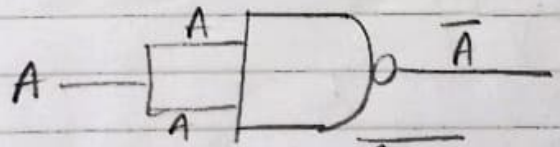
$X \odot Y = \bar{X}\bar{Y} + XY$

Universal gates

NAND & NOR are called Universal gates, because with their help we can realise AND, OR, NOT gates / combination of these gates.

Q. Realise NOT, AND, OR, XNOR & XNOR Gates with NAND Gate

(i) NOT Gate realisation with NAND Gate



$\bar{A} \cdot A$

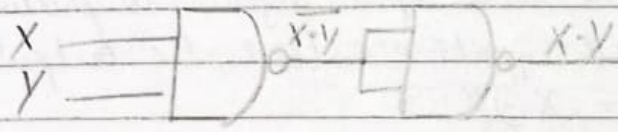
$\bar{A} + \bar{A}$ De-morgan's theorem

$\bar{A}$ Idempotence law

$X + YZ = (X+Y)(X+Z)$

$Y + \bar{Y}(X\bar{Z}) = (Y+\bar{Y})(Y+X\bar{Z})$

(ii) AND Operation with NAND gate



$\overline{X \cdot Y}$ NAND $\overline{X \cdot Y}$

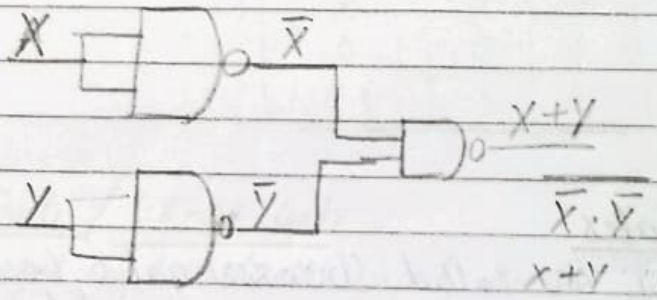
$\overline{X \cdot Y}$ AND $\overline{X \cdot Y}$

$(\overline{X \cdot Y}) \cdot \overline{X \cdot Y}$

$\overline{X \cdot Y}$ Idempotent law

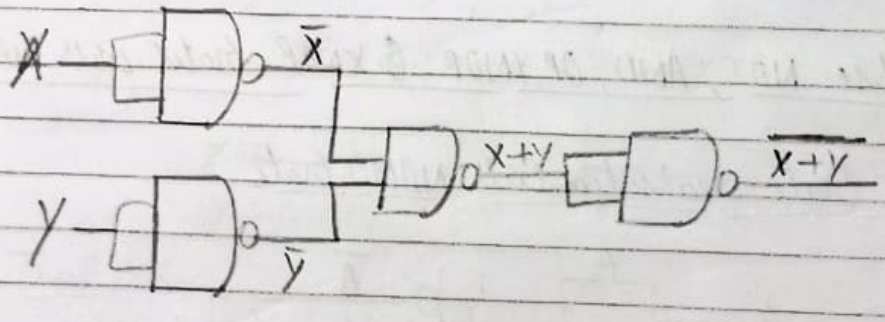
$X \cdot Y$ Involution law

(iii) OR Operation with NAND gate

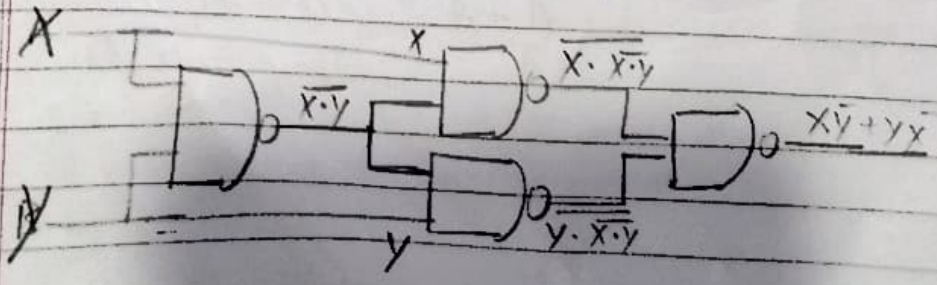


$X+Y$ De-Morgan's law.

(iv) NOR Operation with NAND gate

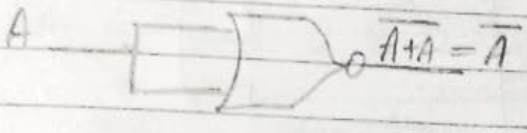


(v) Realise XOR gate with NAND gate

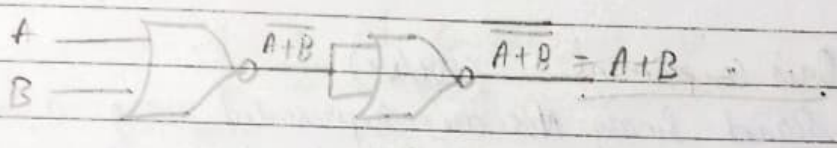


Prob Realise NOT, OR, AND, XOR, XNOR using NOR gate

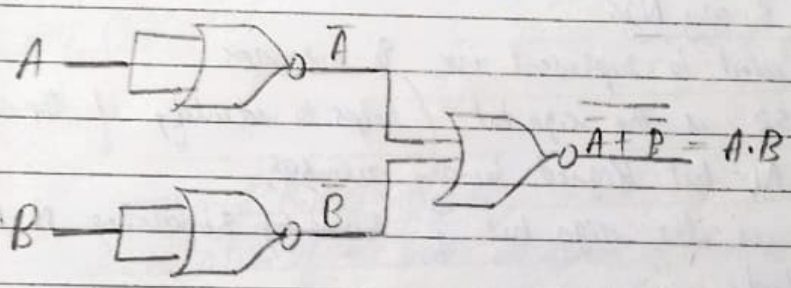
(i) Not gate realisation with NOR gate



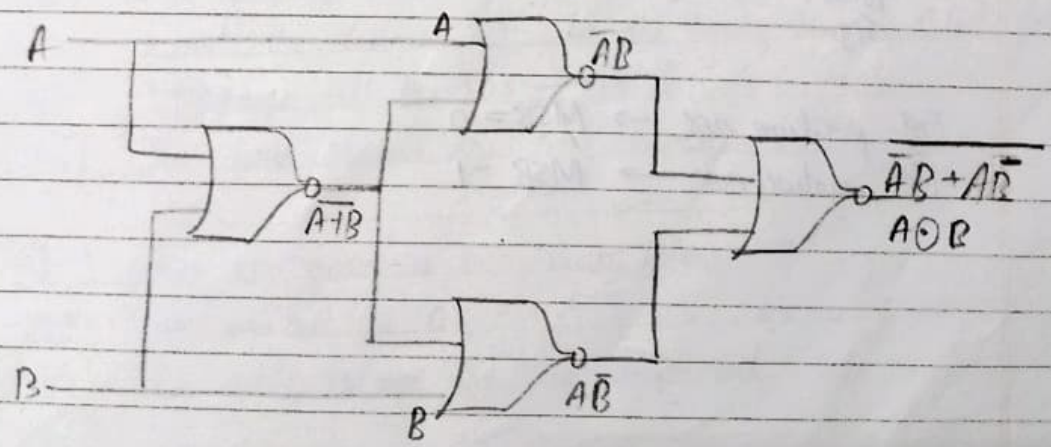
(ii) OR gate realisation with NOR gate



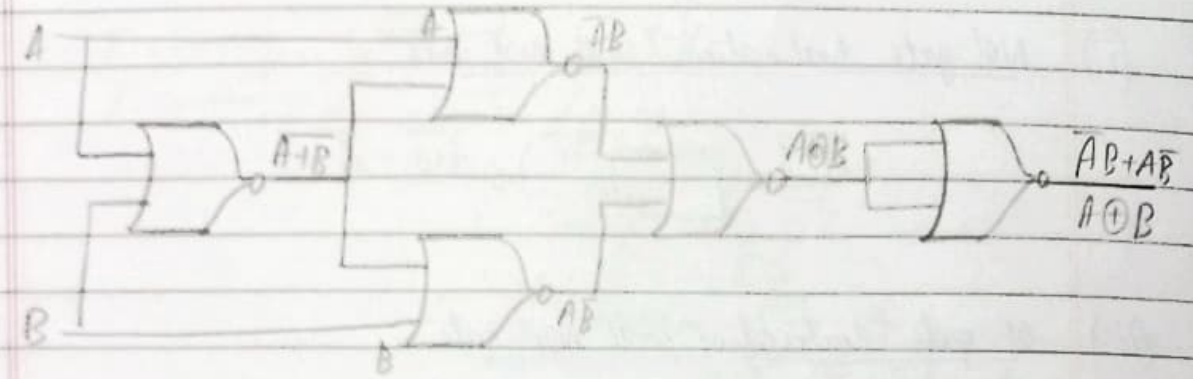
(iii) AND gate realisation with NOR gate



(iv) Ex-NOR gate realisation with NOR gates



(v) Ex of realization with NOR gate



2's compliment (+ve/-ve)

Signed Binary Nos are represented using Sign Magnitude form, 1's compliment & 2's compliment

Signed Binary Nos

→ It is used to represent +ve & -ve nos.
→ The MSB is the sign bit. (helps to identify if the no. is +ve/-ve).
→ For a N-bit signed binary number, MSB is the sign bit & remaining N-1 bit represent magnitude

Eg. 1 0 1 0 1 1 0 0
↓ ← Magnitude
MSB Sign

* For positive nos. → MSB = 0
For negative nos → MSB = 1

Signed Magnitude form

Eg-1) +34 represent in 8 bit form (1 byte form).

2	34
2	17 → 0
2	8 → 1
2	4 → 0
2	2 → 0
	1 → 0

0 0 1 0 0 0 1 0

MSB ← Magnitude →

Eg-2) -34 represent in 8 bit form.

1 0 1 0 0 0 1 0

MSB ← Magnitude →

Eg-3) +0, 8 bit → 0 0 0 0 0 0 0 0

-0, 8 bit → 1 0 0 0 0 0 0 0

1's Complement Representation

→ Representation of +ve no is same as that of signed Mag form.

Steps for obtaining 1's complement of a number

(a) When No. given is in Decimal No system →

(i) Convert the decimal No into the binary No. in 8 bit format

(ii) Interchange all the 0's → 1's & 1's → 0's

(iii) You will obtain the one's compliment

(b) When No given is in binary form, →

(i) Interchange all the 0's → 1's & 1's → 0's

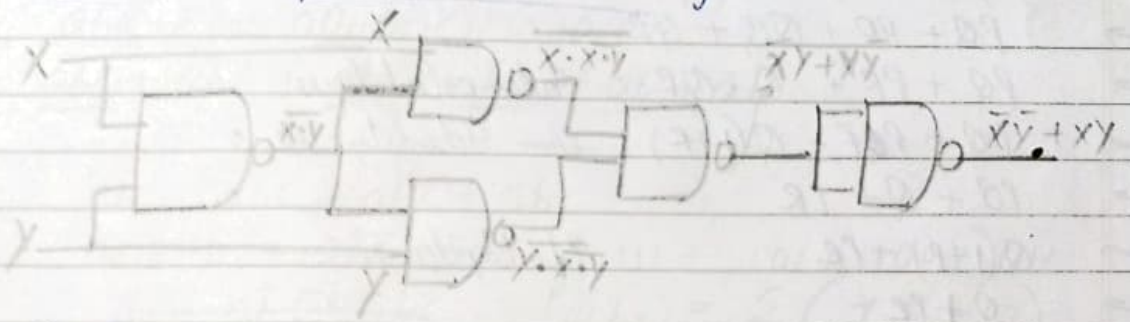
(ii) You will obtain the one's compliment

(c) When Number given is in any other No system →

(i) Convert the given No to decimal & finally to binary

(ii) Interchange all 0's → 1's & 1's → 0's

(vi) Realise XNOR Operation with NAND gate



Eg:) $(\bar{A}+B)(A+B)$ Simplify

→ $\bar{A}A + \bar{A}B + AB + BB$

→ $0 + \bar{A}B + AB + B$

→ $B(\bar{A}+A+1)$

→ $B(1+1)$

→ $B(1) \Rightarrow 1$

Eg:) $f(X,Y,Z) = \bar{X}Y + Y\bar{Z} + YZ + X\bar{Y}\bar{Z}$ Simplify

$\bar{X}Y(Z+\bar{Z}) + (X+\bar{X})Y\bar{Z} + (X+\bar{X})YZ + X\bar{Y}\bar{Z}$

$\bar{X}YZ + \bar{X}Y\bar{Z} + XY\bar{Z} + \bar{X}Y\bar{Z} + XYZ + \bar{X}YZ + X\bar{Y}\bar{Z}$

$\bar{X}YZ + \bar{X}Y\bar{Z} + XY\bar{Z} + XYZ + X\bar{Y}\bar{Z}$

$\bar{X}YZ + \bar{X}Y\bar{Z} + XY(\bar{Z}+Z) + X\bar{Y}\bar{Z}$

$\bar{X}YZ + \bar{X}Y\bar{Z} + XY(1) + X\bar{Y}\bar{Z}$

$\bar{X}Y\cdot(Z+\bar{Z}) + XY + X\bar{Y}\bar{Z}$

$\bar{X}Y + XY + X\bar{Y}\bar{Z}$

$Y(\bar{X}+X) + X\bar{Y}\bar{Z}$

$Y + X\bar{Y}\bar{Z}$

↓ absorption law

$Y + X\bar{Z}$

Q-3) $F(P,Q,R) = (P+Q)(Q+R)$ simplify

→ $PQ + PP + QQ + QR$

→ $PQ + PR + Q + QR$ Idempotent law

→ $PQ + PQR + Q(1+R)$ Identity law

→ $PQ + Q + PR$

→ $Q(1+P) + PR$ Identity law.

→ $Q + PR$

Q-4) $f(x,yz) = \bar{X}\bar{Y}Z + YZ + XZ$ simplify

$\bar{X}\bar{Y}Z + (X+\bar{X})YZ + X(Y+\bar{Y})Z$

$\bar{X}\bar{Y}Z + XYZ + \bar{X}YZ + XYZ + X\bar{Y}Z$

$\bar{X}\bar{Y}Z + XYZ + \bar{X}YZ + X\bar{Y}Z$

$\bar{X}\bar{Y}Z + YZ(X+\bar{X}) + X\bar{Y}Z$

$\bar{X}\bar{Y}Z + YZ + X\bar{Y}Z$

$\bar{Y}Z(\bar{X}+X) + YZ$

$\bar{Y}Z + YZ$

$Z(\bar{Y}+Y) = Z$

Q-5) $f(A,B,C) = (A\bar{B}(C+BD) + \bar{A}\bar{B})C$ Simplify

→ $(A\bar{B}C + A\bar{B}BD + \bar{A}\bar{B})C$

→ $A\bar{B}C \cdot C + \bar{A}\bar{B}C$

→ $A\bar{B}C + \bar{A}\bar{B}C$

→ $\bar{B}C(A+\bar{A}) \rightarrow \bar{B}C$

Eg-6) $f(a,b,c) = a\bar{b} + a\bar{c} + bc$ Simply

→ $a\bar{b}(c+\bar{c}) + a(b+\bar{b})\bar{c} + (a+\bar{a})bc$

→ $a\bar{b}c + a\bar{b}\bar{c} + abc + a\bar{b}c + abc + \bar{a}bc$

→ $abc + a\bar{b}c + a\bar{b}\bar{c} + \bar{a}bc$

→ $a(b+\bar{b})c + a\bar{b}\bar{c} + \bar{a}bc$ 111 + 101 + 100 + 011

→ $ac + a\bar{b}\bar{c} + \bar{a}bc$ $f(a,b,c) = \Sigma(7,5,4,3)$

→ $ac + \bar{a}(bc) + a\bar{b}c$

→ $ac + a$

Boolean Algebra

→ Boolean Algebra also called as Switching Algebra / logical Algebra is used to analyse & simplify digital circuits

→ It deals with logical operations & binary variables

Terminologies

(i) **Sum term**

It is the combination of multiple variables & logical OR operator

Eg. $X + Y$, $\bar{X} + \bar{Y}$

(ii) **Product term**

It is the combination of multiple variables & logical AND operator

Eg: $X \cdot Y$ &, $\bar{X} \cdot \bar{Y}$

(iii) **SOP** → logical OR of multiple product terms

Eg. $XY + \bar{X}Y + X\bar{Y} + \bar{X}\bar{Y}$

(iv) **POS** → logical AND of multiple sum terms

Eg. $(X+Y)(\bar{X}+Y)(X+\bar{Y})(\bar{X}+\bar{Y})$

Minterm →
It is a product term consisting of all literals, with/without compliment to make a Boolean expression.

Maxterm →
It is a sum term consisting of all literals, with/without compliment to make a Boolean expression

Canonical SOP
Complete set of minterms that are defined when output is logic '1' / true
Eg- $f(X,Y) = XY + \bar{X}Y + X\bar{Y} + \bar{X}\bar{Y}$

Canonical POS
Complete set of maxterms that are defined when output is logic '0' / False
Eg- $f(X,Y) = (X+Y)(\bar{X}+Y)(X+\bar{Y})(\bar{X}+\bar{Y})$

Laws of Boolean Algebra

Name	AND form	OR form
Identity law	$1 \cdot A = A$	$0 + A = A$
Null law	$0 \cdot A = 0$	$1 + A = 1$
Idempotent law	$A \cdot A = A$	$A + A = A$
Complimentary law	$A \cdot \bar{A} = 0$	$A + \bar{A} = 1$
Commutative law	$AB = BA$	$A + B = B + A$
Associative law	$(AB)C = A(BC)$	$(A+B)+C = A+(B+C)$
Distributive law	$A + BC = (A+B)(A+C)$	$A(B+C) = AB + AC$
Absorption law	$A(A+B) = A$	$A + AB = A$
De-Morgan's law	$\overline{AB} = \bar{A} + \bar{B}$	$\overline{A+B} = \bar{A} \cdot \bar{B}$

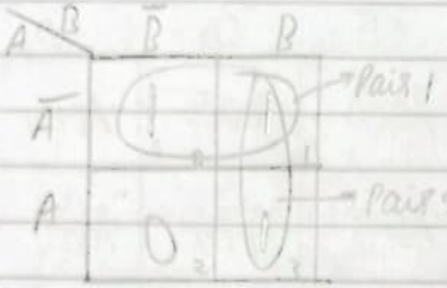
K-Map

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	$\bar{A}\bar{B}\bar{C}\bar{D}$ 0	$\bar{A}\bar{B}\bar{C}D$ 1	$\bar{A}\bar{B}CD$ 3	$\bar{A}\bar{B}C\bar{D}$ 2
$\bar{A}B$	$\bar{A}B\bar{C}\bar{D}$ 4	$\bar{A}B\bar{C}D$ 5	$\bar{A}BCD$ 7	$\bar{A}BC\bar{D}$ 6
AB	$AB\bar{C}\bar{D}$ 12	$AB\bar{C}D$ 13	$ABCD$ 15	$ABC\bar{D}$ 14
$A\bar{B}$	$A\bar{B}\bar{C}\bar{D}$ 8	$A\bar{B}\bar{C}D$ 9	$A\bar{B}CD$ 11	$A\bar{B}C\bar{D}$ 10

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	$\bar{A}\bar{B}\bar{C}$ 0	$\bar{A}\bar{B}C$ 1	$\bar{A}BC$ 3	$\bar{A}B\bar{C}$ 2
A	$A\bar{B}\bar{C}$ 4	$A\bar{B}C$ 5	ABC 7	$AB\bar{C}$ 6

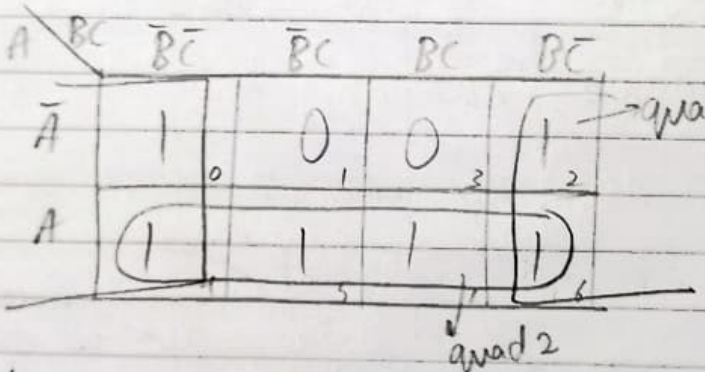
A \ B	$\bar{B}$	B
$\bar{A}$	$\bar{A}\bar{B}$ 0	$\bar{A}B$ 1
A	$A\bar{B}$ 2	AB 3

Q1) Solve $Y = \bar{A}\bar{B} + \bar{A}B + AB$



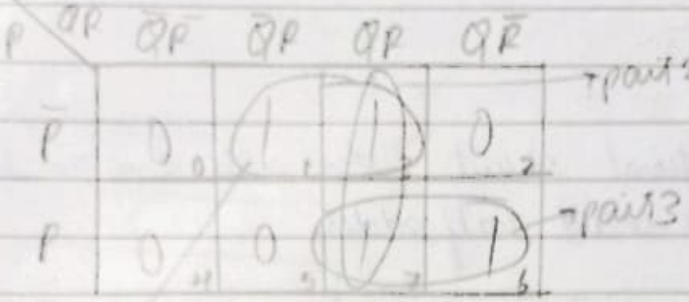
minterm expansion for Pair 1 $\Rightarrow m_0 + m_1$
Reduced expression for pair 1 $\Rightarrow \bar{A}$
minterm expression for pair 2 $\Rightarrow m_1 + m_3$
Reduced expression for pair 2 $\Rightarrow B$
final reduced expression is $\Rightarrow Y = \bar{A} + B$

Q2) Solve $\Rightarrow Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC$



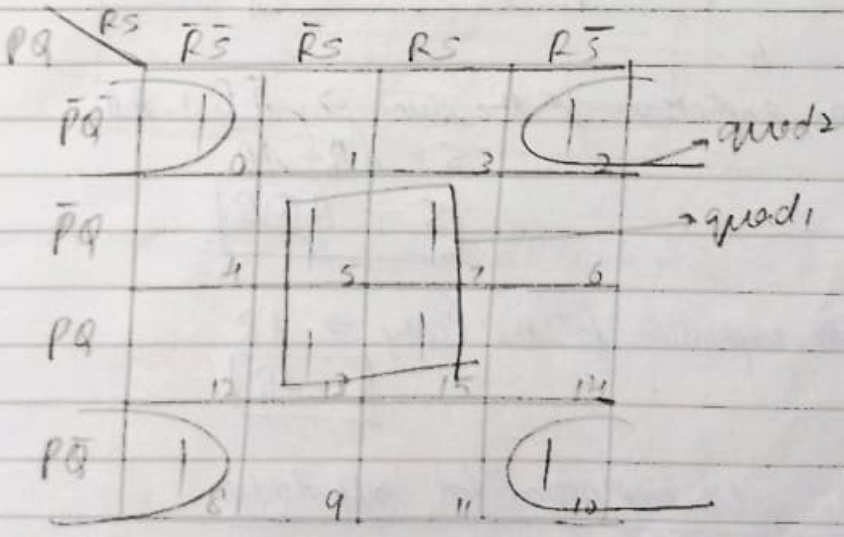
minterm expansion of quad 2 $\Rightarrow m_4 + m_5 + m_7 + m_6$
reduced expression for quad 2 $\Rightarrow A$
minterm expansion of quad 1 $\Rightarrow m_0 + m_2 + m_4 + m_6$
Reduced expression for quad 1 $\Rightarrow \bar{C}$
final reduced expression is $\Rightarrow Y = A + \bar{C}$

Q3) Solve $Z = \Sigma P,Q,R\ (1,3,6,7)$



minterm expansion of pair 1 => $M_1 + M_3$
reduced expression for pair 1 => $\bar{P}R$
minterm expansion for pair 2 => $M_3 + M_7$
reduced expression for pair 2 => QR
minterm expansion for pair 3 => $M_6 + M_7$
reduced expression for pair 3 => PQ.
final reduced expression is => $Z = PQ + QR + \bar{P}R$

Q4) $f(P,Q,R,S) = \Sigma(0,2,5,7,8,10,13,15)$.



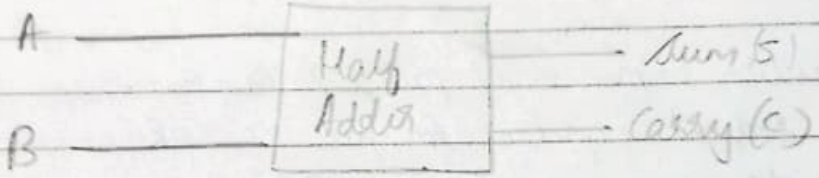
final expression => $QS + \bar{Q}\bar{S}$

classmate
Date
Page

Combinational Circuits

Half Adder

A combinational circuit which adds two one-bit binary numbers is called half adder.



Truth table for Half adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Boolean expression for the sum $\Rightarrow \bar{A}B + A\bar{B}$

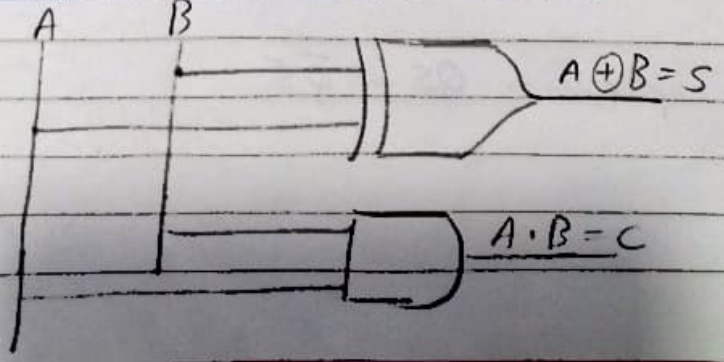
$$S = \bar{A}B + A\bar{B}$$

$$\boxed{S = A \oplus B}$$

Boolean expression for the carry $\Rightarrow AB$

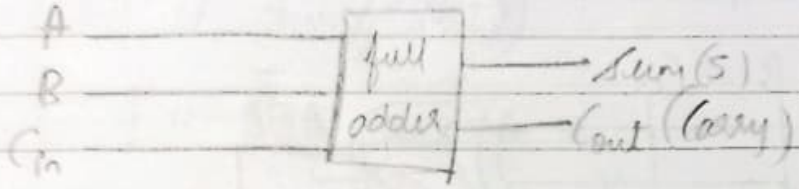
$$\boxed{C = AB}$$

Logic gates expression for half Adder



Full adder

A combinational logic circuit which performs the addition of three bits – two significant bits & one carry bit is called a full adder



Truth table for full adders

A	B	C_{in}	Sum	(carry out)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean expression for the sum $\Rightarrow \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$

$\Rightarrow C_{in}(\bar{A}\bar{B} + AB) + \bar{C}_{in}(\bar{A}B + A\bar{B})$

$\Rightarrow C_{in}(A \odot B) + \bar{C}_{in}(A \oplus B)$

$\Rightarrow C_{in}\overline{(\bar{A}B + A\bar{B})} + \bar{C}_{in}(A \oplus B)$

$\Rightarrow C_{in}\bar{X} + \bar{C}_{in}X$

$\Rightarrow C_{in} \oplus \bar{X}$

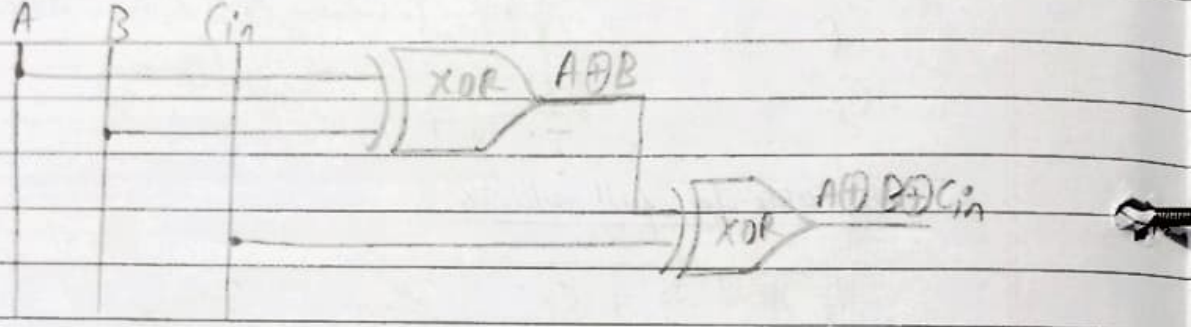
$S \Rightarrow C_{in} \oplus A \oplus B$

Boolean expression for carry out $\rightarrow \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in}$

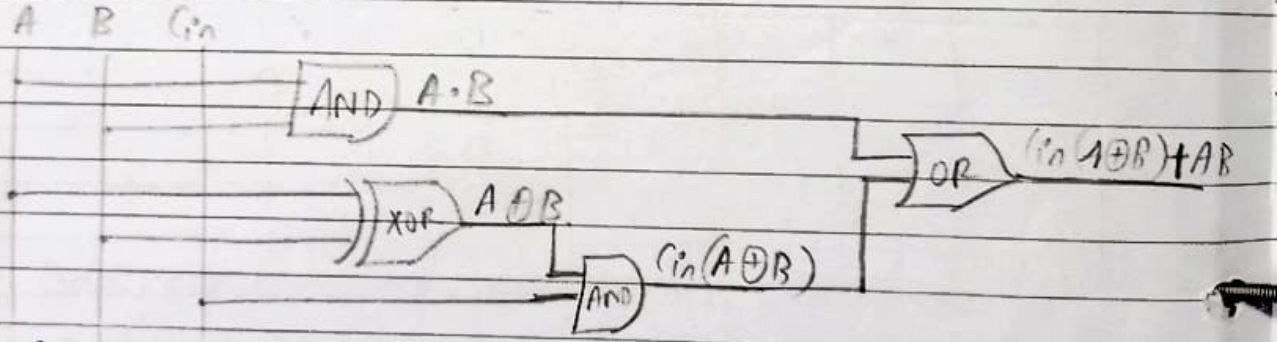
$\Rightarrow C_{in}(\bar{A}B + A\bar{B}) + AB(\bar{C}_{in} + C_{in})$

$\Rightarrow C_{in}(A \oplus B) + AB$.

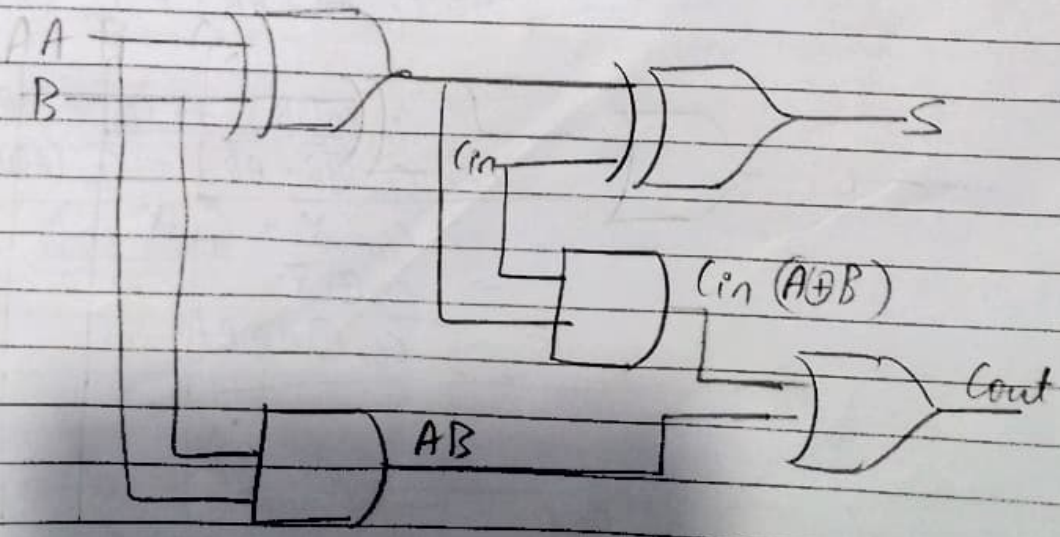
Logic gate expression for sum



Logic gate expression for Carry out



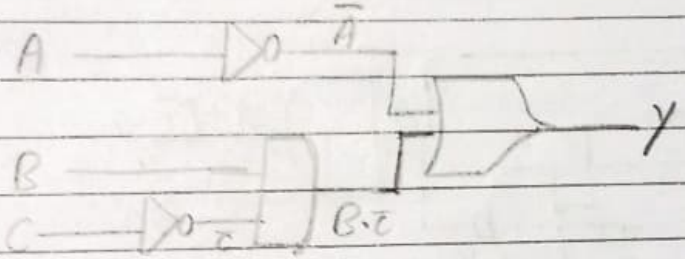
Realise full adder with half adder



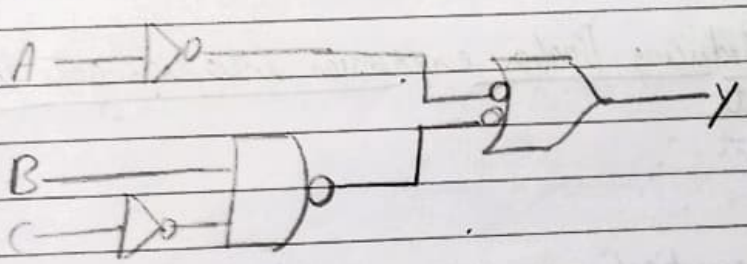
Q.P Steps for reducing Boolean expression in logic gates format with NAND gate

$Y = \bar{A} + B\bar{C}$

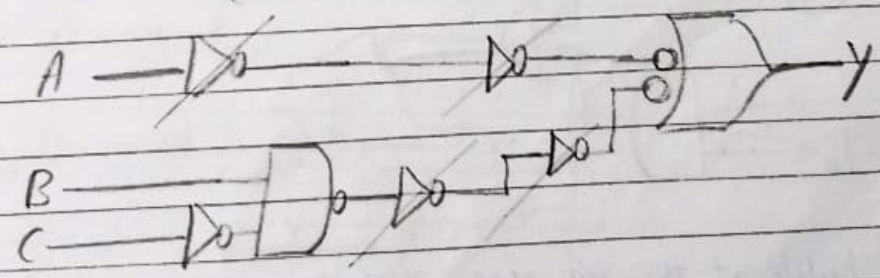
Step1 Implement given boolean expression in terms of basic gates of AOI (And, OR, Inverter (NOT)).



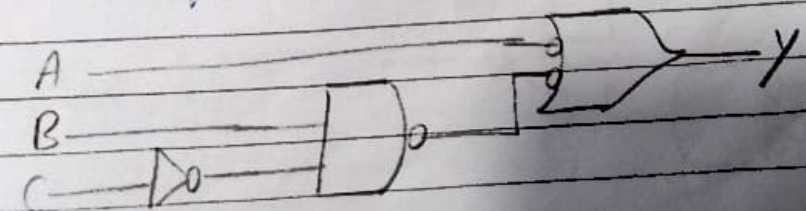
Step-2 Apply bubble to O/P of AND gate & Input of OR gate



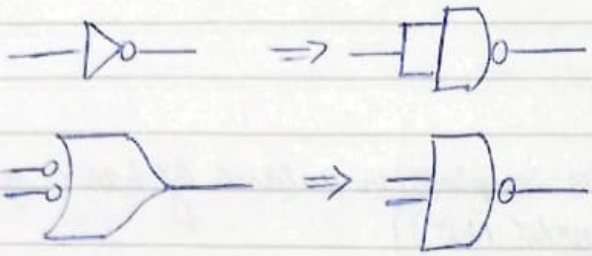
Step3 Apply ~~not gat~~ NOT gate at places where bubbles have been inserted. (Do not erase the added bubbles).



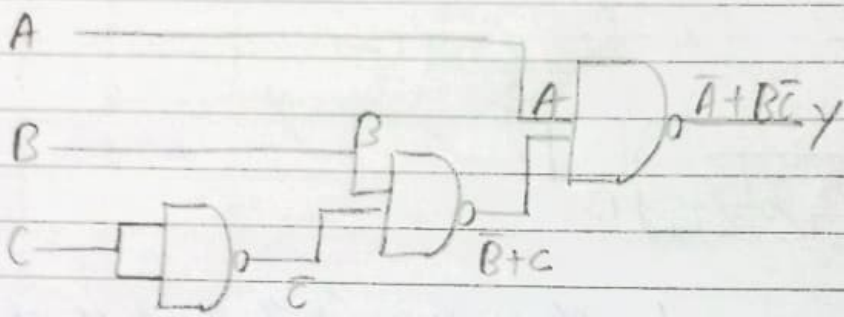
Step-4 Look out for double inverters & cancel extra NOT gates



Step-5 Replace NAND equivalent to →



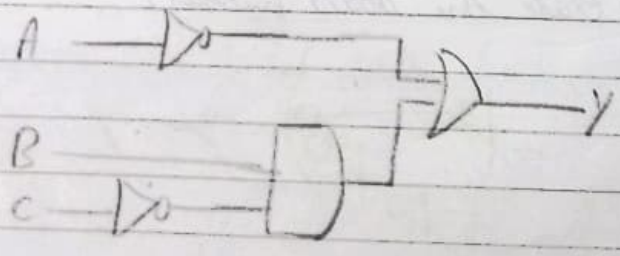
(De-Morgan's theorem)



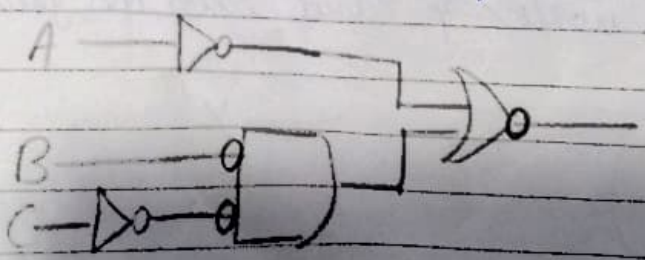
Ans/ Steps to for reducing Boolean expression into logic gate format with NOR gate

$Y = \bar{A} + B\bar{C}$

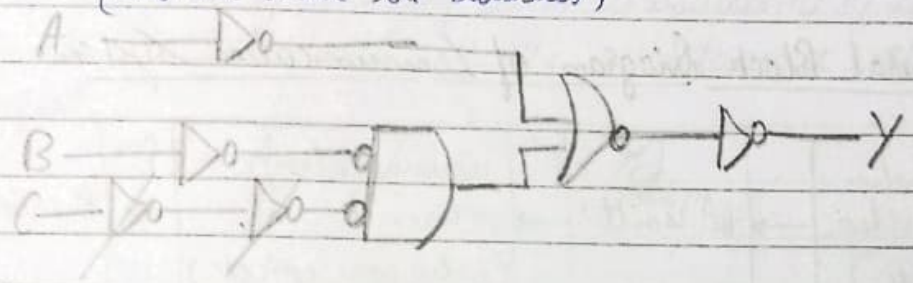
Step-1 Implement given boolean expression in terms of AOI (AND, OR, Inverter (NOT)).



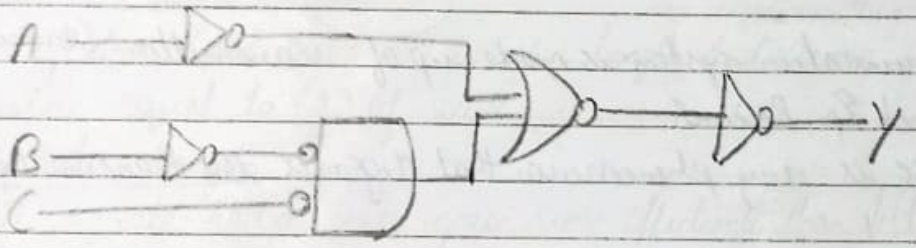
Step-2 Apply bubble at the o/p of OR gate & i/p of AND gate.



Step-3 Apply NOT gate replace of bubble were have applied (Do not erase the bubbles)



Step-4 Look out for Double inverters & cancel extra NOT gates



Step-5 Replace NOR equivalent to →