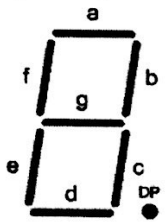
Sardar Vallabhbhai National Institute of Technology

B.Tech. II (CO) 3rd Semester, 2012

Subject: Digital Circuits

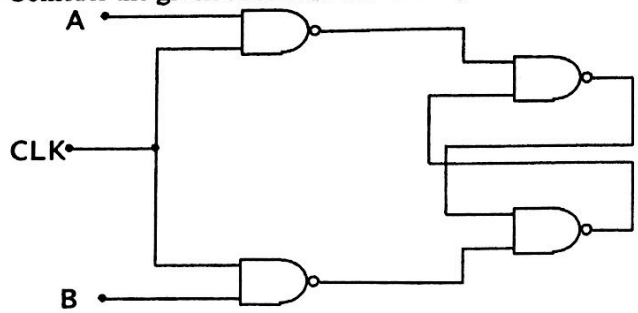
End Sem Exam (Dec-2012)

Max. Marks-50 **Time 2:00 Hr**

Q.1	A Circuit receives a 4- bit Excess-3 code. Find a minimal SOP function for the circuit to detect the decimal nos. 0, 1, 4, 6, 7 and 8. And implement the same using only 2 input NAND gates. **OR** Design a decimal arithmetic unit with a 9's complements Circuit with two selection variables V1 and V0 and two BCD digits A and B. The unit should have four arithmetic operations which depend on the value of selection variables as shown below. (Note: Using Binary Parallel Adder IC) V1 V0 OUTPUT 0 0 A+9's complement of B 0 1 A+B 1 0 A+10's complement of B 1 1 A+1(add 1 to A)	**(05)**
Q.2	a) Realize given Boolean function F (W, X, Y, Z)= Σ M(1,2,4,5,9,11,13,14,15) using single 8X1 MUX (no enable i/p, selection lines S2 S1 S0= W X Y). b) Construct a 5 X 32 Decoder with four 3X8 Decoders and one 2X4 Decoder (Consider all decoders with Active High I/P , O/P and Enable logic).	**(03)** **(02)**
Q.3	Redefine the carry propagate and carry generate as follows: $P_i = A_i + B_i$ $G_i = A_i B_i$ Show that the output carry and output sum of a full-adder becomes: $C_{i+1} = (C_i'G_i' + P_i')' = G_i + P_i C_i$ $S_i = (P_iG_i') \oplus C_i$	**(05)**
Q.4	Hexadecimal-to-seven-Segement decoder is a combinational circuit that accepts hexadecimal digits (0-9 and A-F) in binary (4-bit) and generates appropriate outputs for selection of segments in a display indicator used for displaying a hexadecimal digits. Consider logic 1 required to glow particular segment. Find the functions for a, b, d, e segments using K Map. 	**(05)**
Q.5	Design a Binary multiplier that multiplies a 4-bit number $B = b3b2b1b0$ by a 3-bit number $A = a2a1a0$ to form the product $C = c6c5c4c3c2c1c0$. This can be done with 12 Gates and two 4-bit parallel adders. The AND gates are used to form the products of pairs of bits. For example, the product of a0 and b0. The partial product formed by AND gates are summed with the parallel adders.	**(05)**

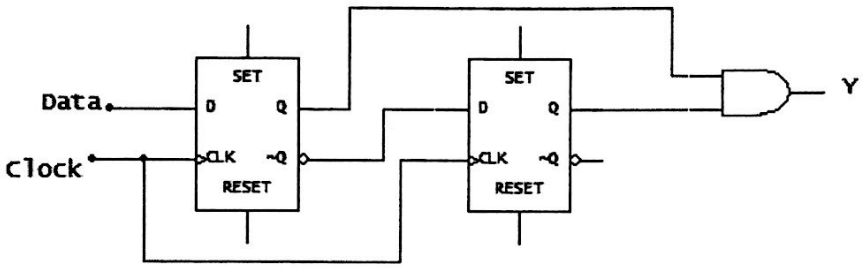
Q.6 **Answer the following Questions:-** **(05)**

1. Consider the given circuit. In this circuit, the race around



[a] does not occur
[b] Occurs when CLK = 0
[c] Occurs when CLK = 1 and A = B = 1
[d] Occurs when CLK = 1 and A = B = 0

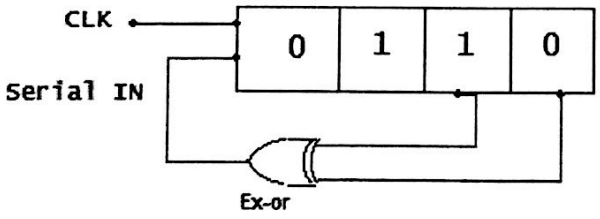
2. When the output Y in the circuit below is "1", it implies that data has



[a] Changed from "0" to "1"
[b] Changed from "1" to "0"
[c] Changed from in either direction
[d] Not changed

3. The present output Q_n of an edge triggered JK flipflop is logic 0. If J = 1, then Q_n+1
[a] cannot be determined [b] will be logic 0 [c] will be logic 1 [d] will race around

4. The initial contents of the 4 bit serial-in-parallel-out, right-shift, Shift Register shown in figure is 0110.After three clock pulses are applied, the contents of the Shift Register will be

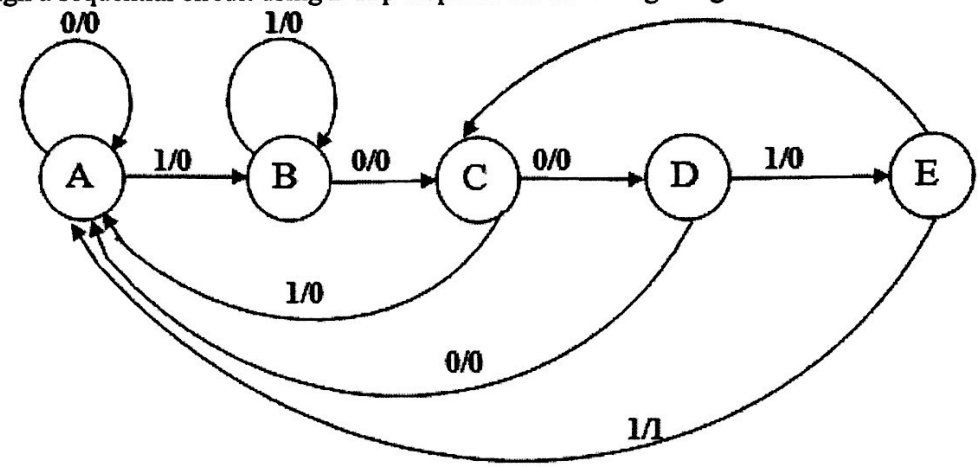
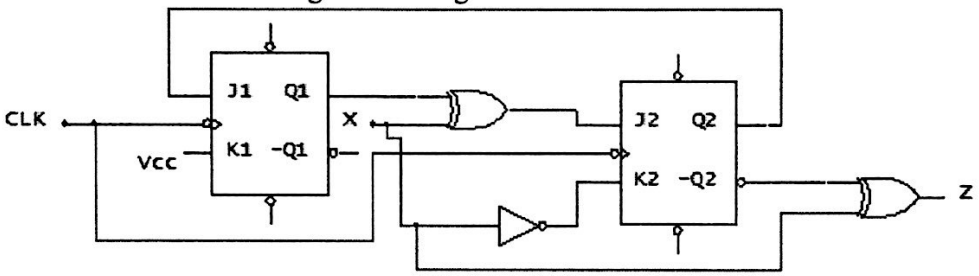


[a] 0000 [b] 0101 [c] 1010 [d] 1111

5. A 4 bit modulo-16 ripple counter uses JK flipflops. If the propagation delay of each FF is 50 ns, the maximum clock frequency that can be used is equal to:
[a] 20 MHz [b] 10 MHz [c] 5 MHz [d] 4 MHz

6. State True or False:- **(02)**

i) Synchronous data transfer requires less circuitry than asynchronous.
ii) The CLK input will affect the flip-flop output only when active transition of the control input occurs.

Q.7	Explain 4 bit twisted ring counter using D flip-flops with neat logic diagram & waveforms. How can you prevent lock-out condition?	(08)
Q.8	Design a sequential circuit using D flip-flops for the state diagram given: 	(05)
Q.9	Obtain the state table & diagram for the given circuit: 	(05)