Computer Engineering Department

B.Tech.2nd Year, Semester: 3rd

Digital Circuits

End Semester Exam- Dec 2011

Time: 2 Hour **Max. Marks: 50**

Note: Design the circuits neatly wherever required.

Assume necessary data wherever required.

Q.1	Given inputs $A_3 A_2 A_1 A_0$. We are required to produce outputs $B_3 B_2 B_1 B_0$, where B=A for A<10 & B=A- 4 for A≥ 10 . Design &draw the logic circuit.	05
Q.2	i) Design 4 line to 2 line priority encoder. Provide an extra O/P E to indicate that at- least one i/p is equal to 1. ii) Implement 4- bit even parity checker using MUX	05
Q.3	Design the circuit necessary to drive a seven- segment display when driven with an Excess-3 code BCD input. Assume that the display requires an active low input to turn on the LED segment. i) Construct the truth table and simplify the output equations. ii) Draw the logic diagram.	07
Q.4	Design an arithmetic circuit with two selection variables, s1 & s0, that generates the following arithmetic operations that generates the following arithmetic operations. Draw the logic diagram of one typical stage.	06

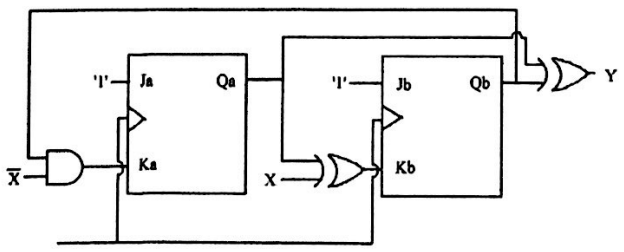
S1	S0	Cin=0	Cin =1
0	0	F= A+B	F= A+B+1
0	1	F= A	F= A+1
1	0	F= B'	F= B'+1
1	1	F= A+B'	F= A+B'+1

OR

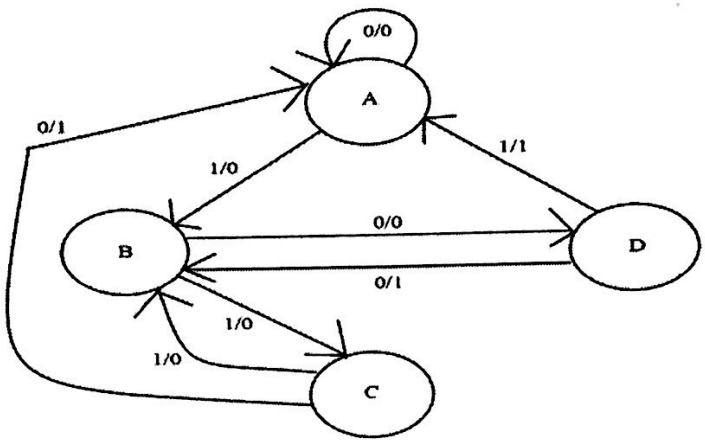
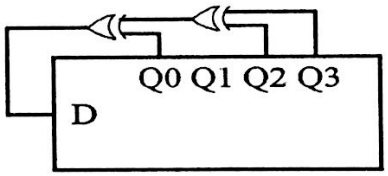
A staircase light is controlled by two switches, one is at the top of stairs &other is at the bottom of the stairs.

a) Make truth table for this system
b) Write logic expression in SOP form
c) Realize the circuit using AOI logic
d) Realize the circuit using minimum number of
i) NAND gates ii) NOR gates

Q.5	Derive state table and state diagram for mealy sequential circuit shown below.	06



Where X input, Y output, CLK clock

Q.6	Design a counter that counts the decimal digits according to the 2, 4, 2, 1 code. Use T-flip flops.	06
Q.7	Design a 3-bit counter using T- flip flop that has a repeated sequence of six states 000-001-010-100-101-110. Give the state table & state diagram. **OR** Design a clocked sequential machine using T-flip flop for the following state diagram. Use state reduction if possible.  	08
Q.8	A 4-bit shift register which shift one bit to the right at every clock pulse is initialize to values 1000 form Q0, Q1, Q2, Q3. The D input is derived from Q0, Q2 & Q3 through two EX-OR gates as shown below : a) Write 4-bit values (Q0, Q1, Q2, Q3) after each clock pulses clock pulses till the pattern (1000) reappears on Q0 Q1 Q2 Q3 b) To what value shift register be initialized so that the pattern 1001 occurs after 1st clock pulse  	07