Computer Engineering Department

B. Tech. 2nd Year, Semester: 3rd

Digital Circuits

Mid Semester Exam- Oct 2013

Time: 1 Hour **Max. Marks: 30**

Note: All Questions are Compulsory.

Design the circuits neatly wherever required.

Sufficient data has been provided, if required assume by your side.

Q.1 i) Generate the 12 bit even parity Hamming code for 10001011 and at receiver side if code word is 011100110110.find the correct message for odd parity system. **01**

ii) Perform subtraction using 9's complement method **01**

a) 20 - 1000 b) 3570 - 2100

iii) For weighted code 4,4,3,-2 for the decimal digits, determine all possible tables so that 9's complement of each decimal digit is obtained by changing 1's to 0's and 0's to 1's. **02**

iv) Using 8 bit signed arithmetic perform subtraction using 2's complement method **01**

a) + 68 - 108 b) + 32 - 49

Q.2 i) If A'B + CD' = 0 then prove that **02**

AB + C'(A' + D') = AB + BD + B'D' + A'C'D

ii) Reduce Expression using Boolean Theorems (mention the Theorem applied)

a) (A' + B' + D') (A' + B+ D') (B+C+D) (A+ C') (A+C'+D) = A'C'D + ACD'+BC'D' **02**

b) (A'+B+C') (A' +B+D+E) (C+D) **02**

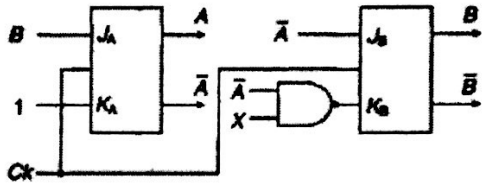
Q.3 A corporation having 100 shares entitles the owner of each share to cast one vote at the share- holder's meeting. Assume that A has 40 shares, B has 30 shares, C has 20 shares, D has 10 shares. A two third majority is required to pass a resolution in a share holder's meeting. Each of these four men has a switch which he closes to vote YES and opens to vote NO for his percentage of shares. When the resolution is passed the output LED must be ON. Derive a truth table for the output function and give the sum of product equation for it. Also represent the function using NAND- NAND logic. **04**

P.T.O

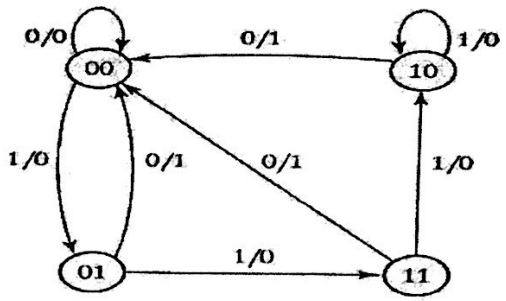
Q.4 Simplify the Boolean Expression using Mc-Clusky Method **04**
F (A, B, C, D, E, F, g) = Σ(20,18,38,39,52, 60, 102,103,127)
Represent the function using NOR-NOR logic.

Q.5 For the sequential circuit shown in Figure below find **04**
(a) The state table,
(b) The state diagram

For 2 bit output AB and 1 bit input X



Q.6 Design sequential circuit for the given state diagram. **04**



Q.7 Reduce the number of states in a following state table and tabulate reduced state table for 1 bit input X. Starting from state A determine output sequence for input sequence 10010. The rightmost bits are applied first. **03**

Present state	Next State		Output	
	X=0	X=1	X=0	X=1
A	B	C	0	0
B	D	E	0	0
C	F	G	0	0
D	H	I	0	0
E	J	K	0	0
F	L	M	0	0
G	N	P	0	0
H	A	A	0	0
I	A	A	0	0
J	A	A	0	1
K	A	A	0	0
L	A	A	0	1
M	A	A	0	0
N	A	A	0	0
P	A	A	0	0