Computer Engineering Department

B. Tech. 2nd Year, Semester: 3rd

Digital Circuits

Mid Semester Exam- Sept 2012

Time: 1 Hour **Max. Marks: 30**

Note: All Questions are Compulsory.

Design the circuits neatly wherever required.

Sufficient datas have been provided, if required assume by your side.

Q.1 A) simplify each of the following expression using one of the theorems and state the theorem used. 02

a) (V'W+X)' (V'W+X+Y+Z)

b) (V'+W'X) (V'+W'X+Y'Z)

c) (W'+X)YZ'+(W'+X)'YZ'

d) (V'+U+W)(WX+Y+UZ')+ (WX+Y+UZ')

B) Octal Subtraction using sign 7's complement and 8's complement method 02

(a) 1240.70-565.25 (b) 520.50-1250.66

C) Expand to get maxterms and minterms: 02

(a) x(x+y')(x'+y+z) (b) (w+x')(w'+x'+y)(w+y+z) 01

D) Write function in both SOP & POS form & draw circuits for both the cases.

(a) F=∏(0,2,8,9,10,11)+d(12,13,14)

Q.2 A Flow rate Sensing device used on a liquid transport pipeline functions as follows. The device provides a 5-bit output where all five bits are zero if the flow rate is less than 10 gallons per minute. The first bit is 1 if the flow rate is at least 10 gallons per minute; the first and second bits are 1 if the flow rate is at least 20 gallons per minute; the first, second and third bits are 1 if the flow rate is at least 30 gallons per minute and so on. The five bits represented by logic variables A, B, C, D and E are used as inputs to a device that provides two outputs Y and Z. 03

a) Write an equation for the output Y if we want Y to be 1 iff the flow rate is less than 30 gallons per minute.

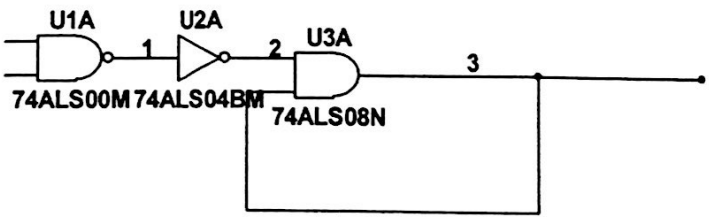
b) Write an equation for the output Z if we want Z to be 1 iff the flow rate is at least 20 gallons per minute but less than 50 gallons per minute.

K-Map is required for the mentioned problem.

Q.3 For each of the following functions find minimum SOP solution using QUINE Mc-CLUSKEY method: 05

f (a,b,c,d,e)=∑m(0,2,3,5,7,9,11,13,14,16,18,24,26,28,30)

Q.4 i) Determine that given circuit in figure is a part of combinational logic or sequential logic with appropriate justification. 03



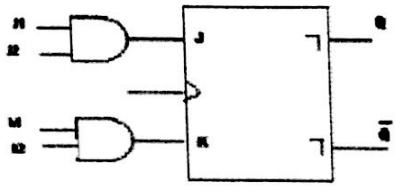
ii) "If a clock skew is minimal, flip-flop must be operate reliably."State True/False with appropriate justification.

iii) What is the difference between state table and excitation table?

Q.5 For a given 100 MHz clock signal, derive a circuit using D flip-flop to generate 50 MHz & 25 MHz clock signal. Draw a timing diagram for all three clock signal. Assuming reasonable delays. 04

Q.6 The following serial data applied to flip flop shown in figure. Determine the resulting serial data that appears on Q output. Assume there is one clock pulse for each bit time. Assume that Q is initially 0. The rightmost bits are applied first. 04

J1= 1 0 1 1 0 1 1 0 K1= 1 0 0 1 0 1 1 0 J2= 1 1 0 1 1 0 0 1 K2= 1 1 0 1 1 0 1 1



Q.7 Design a sequential circuit using J K flip-flop whose state table is given below: 04

Present State A1	A2	Input X	Next State A1	A2	Output Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1