S.V.NATIONAL INSTITUTE OF TECHNOLOGY,SURAT-7
B.Tech. II (EL), 4TH Sem.
MID SEM EXAMINATION, MARCH-2012
ELECTRONIC-II

MARKS: 30

TIME: 1 Hours

Instruction: (i) Assume necessary data wherever required.
(ii) Figure to the right indicates marks.

Q-1 ***Attempt Any Four*** **(08)**

(a) Find the octal equivalent of $(2F.C4)_{16}$ and the hex equivalent of $(762.013)_8$. **(02)**

(b) Perform BCD Addition of $(4965)_{10} + (3472)_{10}$ **(02)**

(c) It is proposed to construct an eight-input NAND gate using only two-input AND gates and two-input NAND gates. Draw the logic arrangement that uses the minimum number of logic gates. **(02)**

(d) The following Boolean expression. **(02)**
X = BE + B'DE' is a simplified version of the expression
A'BE + BCDE +BC'D'E +A'B'DE' + B'C'DE'
Are they any don't care conditions? If so what are they?

(e) Find the minimum Sum of product and product of Sum forms for the following. **(02)**
B'CD' + AB'D' + AB'C + A'BD + A'B'C'D'

Q-2 Design an eight-bit adder–subtractor circuit using four-bit binary adders, type number 7483, and quad two-input EX-OR gates, type number 7486. **(04)**

Q-3 ***Attempt Any TWO*** **(06)**

(a) Implement the four Boolean functions listed using three half adder circuits, **(03)**
$D = A \oplus B \oplus C$, $E = A'BC + AB'C$, $F = ABC' + (A' + B')C$, $G = ABC$

(b) Design a combinational circuit to check for even parity of four bits. A logic-1 output is required when the four bits do not constitute an even parity **(03)**

(c) Using the tabular method, obtain the minimal expression in SOP formate for **(03)**
F = ∏M (1, 2, 3, 4, 5) + d (10, 11, 12, 13, 14, 15)

Q-4 ***Attempt The Following*** **(12)**

(a) What are the different ways of triggering the flip-flops ? Generate the triggering pulse using appropriate logic circuits by using the delay time of logic gates and also draw the relevant timing waveforms. **(04)**

(b) Consider a J-K flip-flop (J-K' flip-flop to be more precise) where an inverter has been wired between the external K' input and the internal K input. Draw the logic circuit of it. With the help of a characteristic table, write the characteristic equation for this flip-flop. **(04)**

(c) A 100 kHz clock signal is applied to a J-K flip-flop with J = K = 1 . **(02)**
(i) If the flip-flop has active HIGH J and K inputs and is negative edge triggered, determine the frequency of the Q and Q' outputs.
(ii) If the flip-flop has active LOW J and K inputs and is positive edge triggered, what should the frequency of the Q and Q' outputs be? Assume that Q is initially '0'.

(d) In the case of a presettable, clearable J-K flip-flop with active HIGH J and K inputs and active LOW PRESET and CLEAR inputs, what would the Q output logic status be for the following input conditions, assuming that Q is initially '0', immediately after it is clocked? **(02)**
(i) J = 1, K = 0, PRESET=1, CLEAR= 1 (ii) J = 1, K = 1, PRESET= 0, CLEAR = 1
(iii) J = 0, K = 1, PRESET=1, CLEAR= 0 (iv) J = 0, K = 0, PRESET= 0, CLEAR = 1