Chapter1: General-purpose I/Os ports (GPIO)

Hardware : Discovery stm32f4, SoC Stm32f40vg

Reference : RM0090 reference manual (DM00031020.pdf)

Contact : Mustapha.hamdi@insat.rnu.tn

Institut national des sciences appliquées et de technologie

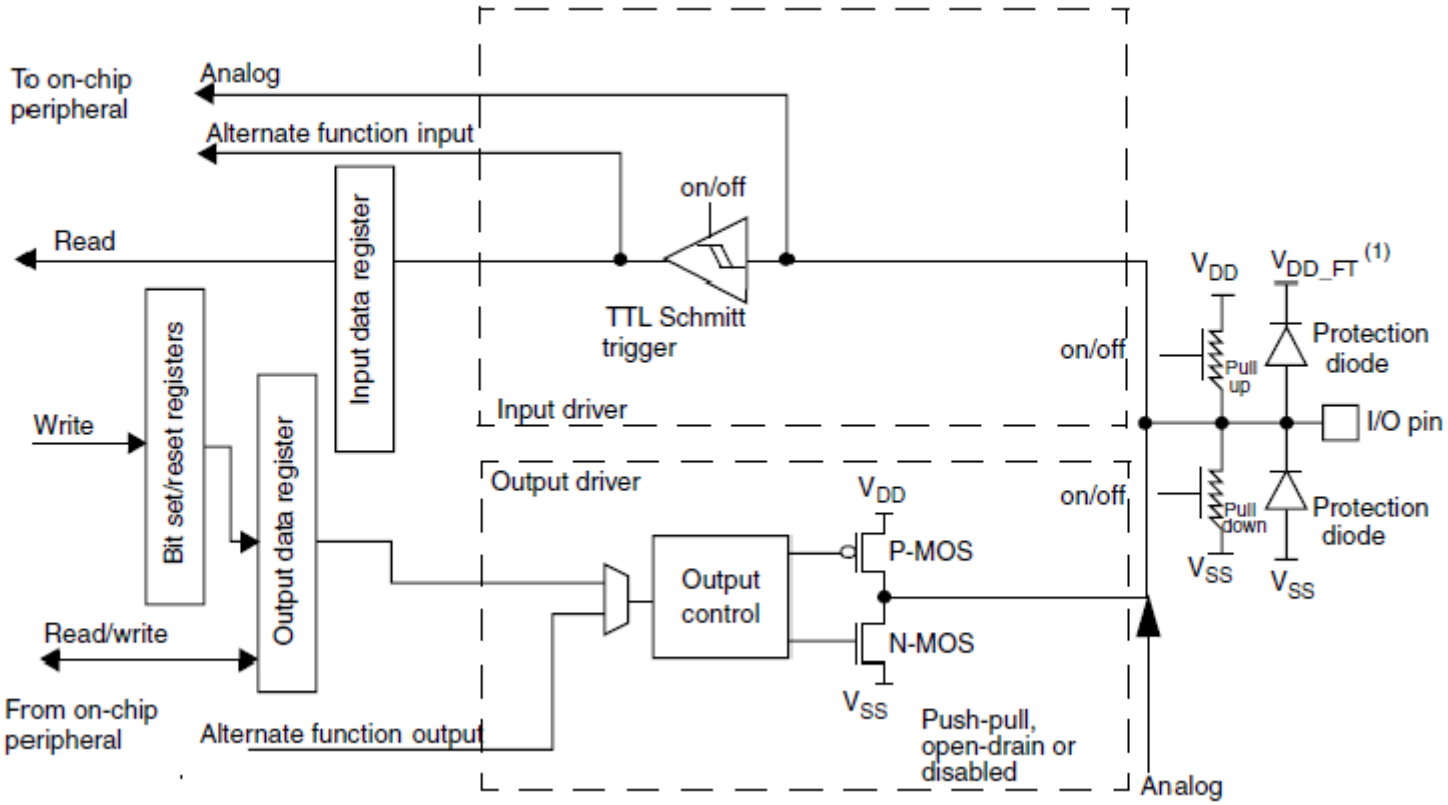
المعهد الوطني للعلوم التطبيقية والتكنولوجيا

insat

Powered by STM32

General-purpose I/Os (GPIO)

GPIO electronic schematic:



RM0090 reference manual, chapter 6.3, page 270, Fig 13

Contact : Mustapha.hamdi@insat.rnu.tn

GPIO Low Layer

General-purpose I/Os (GPIO)

Each general-purpose I/O port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR and GPIOx_PUPDR), two 32-bit data registers (GPIOx_IDR and GPIOx_ODR), a 32-bit set/reset register (GPIOx_BSRR), a 32-bit locking register (GPIOx_LCKR) and two 32-bit alternate function selection register (GPIOx_AFRH and GPIOx_AFRL).

GPIO modes :

Input (reset state)
General purpose output mode
Alternate function mode
Analog mode

Contact : Mustapha.hamdi@insat.rnu.tn

GPIO Low Layer

GPIO Used Registers: SoC stm32f407vg

RM0090 Reference manual (DM00031020.pdf) , General-purpose I/Os (GPIO) page 269

Peripheral clock enable register — AHB1ENR 32bits

Port mode register — MODER 32bits

Port output type register — Typer 32bits

Output speed register — OSPEEDER 32bits

Port output data register — IDR/ODR 16 bits

GPIOx

Contact : Mustapha.hamdi@insat.rnu.tn

GPIO Low Layer

6.3.10 RCC AHB1 peripheral clock register (RCC_AHB1ENR)

Address offset: 0x30

Reset value: 0x0010 0000

Access: no wait state, word, half-word and byte access.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reser-ved	OTGHS ULPIEN	OTGHSEN	ETHMACPTPEN	ETHMACRXEN	ETHMACTXEN	ETHMACEN	Res.	DMA2DEN	DMA2EN	DMA1EN	CCMDATARAMEN	Res.	BKPSRAMEN	Reserved	
	rw	rw	rw	rw	rw	rw		rw	rw	rw			rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			CRCEN	Res.	GPIOKEN	GPIOJEN	GPIOIEN	GPIOHEN	GPIOGEN	GPIOFEN	GPIOEEN	GPIODEN	GPIOCEN	GPIOBEN	GPIOAEN
			rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1

Enable GPIO D
(1<<3);

DM00031020.pdf Page 180

Contact : Mustapha.hamdi@insat.rnu.tn

GPIO Low Layer

8.4.1 GPIO port mode register (GPIOx_MODER) (x = A..I/J/K)

Address offset: 0x00

Reset values:

- 0xA800 0000 for port A
- 0x0000 0280 for port B
- 0x0000 0000 for other ports

32 bits register

Each pin requires two bits for mode configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODER15[1:0]		MODER14[1:0]		MODER13[1:0]		MODER12[1:0]		MODER11[1:0]		MODER10[1:0]		MODER9[1:0]		MODER8[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODER7[1:0]		MODER6[1:0]		MODER5[1:0]		MODER4[1:0]		MODER3[1:0]		MODER2[1:0]		MODER1[1:0]		MODER0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	**0**	**1**	rw	rw	rw	rw

Bits 2y:2y+1 **MODERy[1:0]:** Port x configuration bits (y = 0..15)

These bits are written by software to configure the I/O direction mode.

00: Input (reset state)
01: General purpose output mode
10: Alternate function mode
11: Analog mode

Pin 2: output mode

(1<<2*2) = (010000)$_2$

DM00031020.pdf Page 283

Contact : Mustapha.hamdi@insat.rnu.tn

GPIO Low Layer

Case study : GPIOD , pin 15 as output, output frequency: 50 MHz, Output 15:1

RCC->AHB1ENR |= (1<<3);

|=(1<<3)

Mode output, GPIOD->MODER |=(1<<2*15)

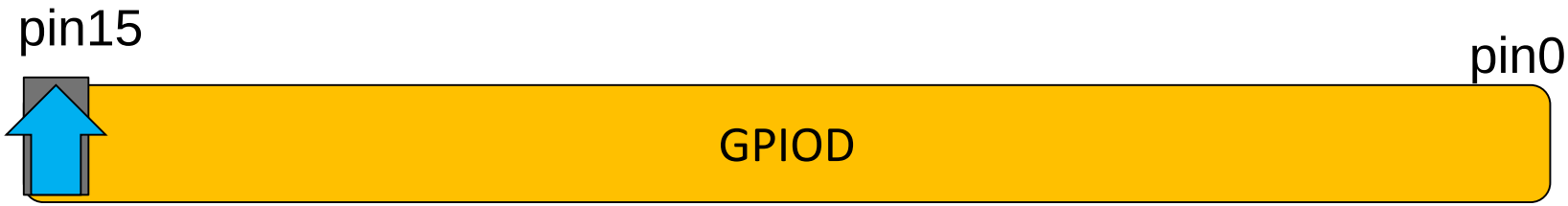
|=(1<<2*15)

Freq=50MHz, GPIOD->OSPEEDER

|=(2<<2*15)

Pin 15=1, GPIOD->ODER

|=(1<<15)



Contact : Mustapha.hamdi@insat.rnu.tn

GPIO Low Layer

Case study : GPIOD , pin 14 and 15 as output, Output :1

RCC->AHB1ENR |= (1<<3);

|=(1<<3)

output mode

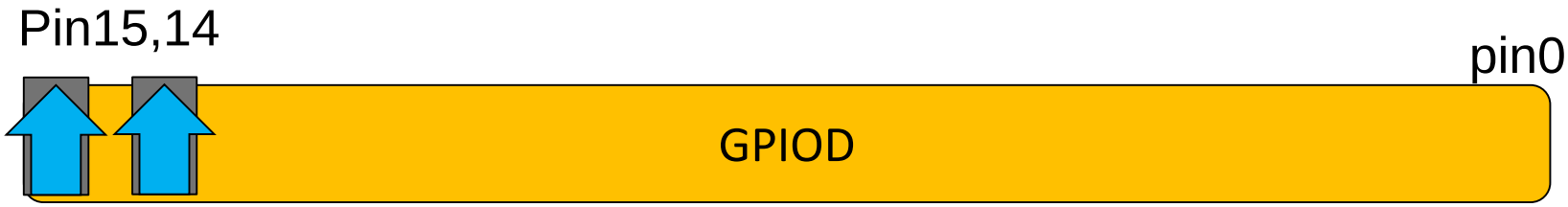
?

fpin15=50MHz,Fpin14=100

?

Pin 15=1, pin14=1

?



Mustapha.hamdi@insat.rnu.tn

Case study

RCC->AHB1ENR |= (1<<3);

|=(1<<3)

Mode output

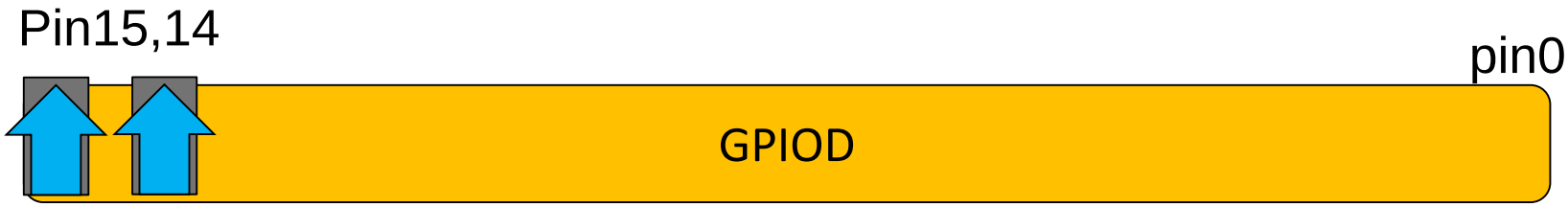
|=(1<<15*2)+(1<<14*2)

fpin15=50MHz,Fpin14=50MHz

|=(2<<15*2)+(2<<14*2)

Pin 15=1, pin14=1

|=(1<<15)+(1<<14)



Contact : Mustapha.hamdi@insat.rnu.tn

GPIO Low Layer

Low Layer Code :

By using Keil MDK,

Getting Started :

https://www.keil.com/product/brochures/uv4.pdf

Environnement Configuration :

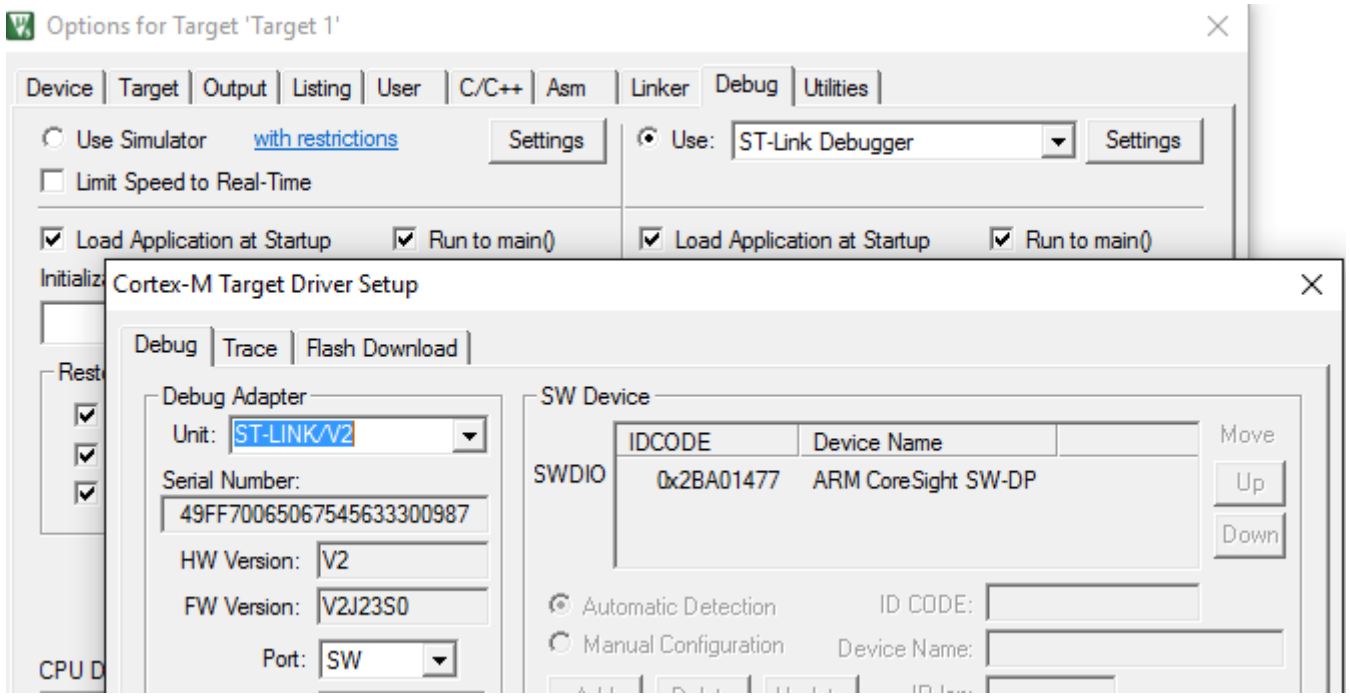
Manage Run-Time Environment

Software Component	Sel.	Variant	Version	Description
Board Support		STM32F429I-Disco	1.0.0	STMicroelectronics STM32F429I-Discovery Kit
CMSIS				Cortex Microcontroller Software Interface Components
CORE	☑		4.3.0	CMSIS-CORE for Cortex-M, SC000, and SC300
DSP	☐		1.4.6	CMSIS-DSP Library for Cortex-M, SC000, and SC300
RTOS (API)			1.0	CMSIS-RTOS API for Cortex-M, SC000, and SC300
CMSIS Driver				Unified Device Drivers compliant to CMSIS-Driver Specifications
Compiler				ARM Compiler Software Extensions
Device				Startup, System Setup
Startup	☑		2.1.0	System Startup for STMicroelectronics STM32F4 Series
STM32Cube Framework (API)			1.0.0	STM32Cube Framework
STM32Cube HAL				STM32F4xx Hardware Abstraction Layer (HAL) Drivers
File System		MDK-Pro	6.6.0	File Access on various storage devices
Graphics		MDK-Pro	5.30.0	User Interface on graphical LCD displays
Graphics Display				Display Interface including configuration for emWIN
Network		lwIP	1.4.1	Network lwIP Bundle
Oryx Embedded Middlware		Oryx Embedded Mi...	1.5.1	Middleware package(CycloneTCP, CycloneSSL and CycloneCrypto)
USB		MDK-Pro	6.6.10	USB Communication with various device classes
wolfSSL		wolfSSL	3.0.0	wolfSSL: SSL/TLS and Crypt Library

Contact : Mustapha.hamdi@insat.rnu.tn

GPIO Low Layer

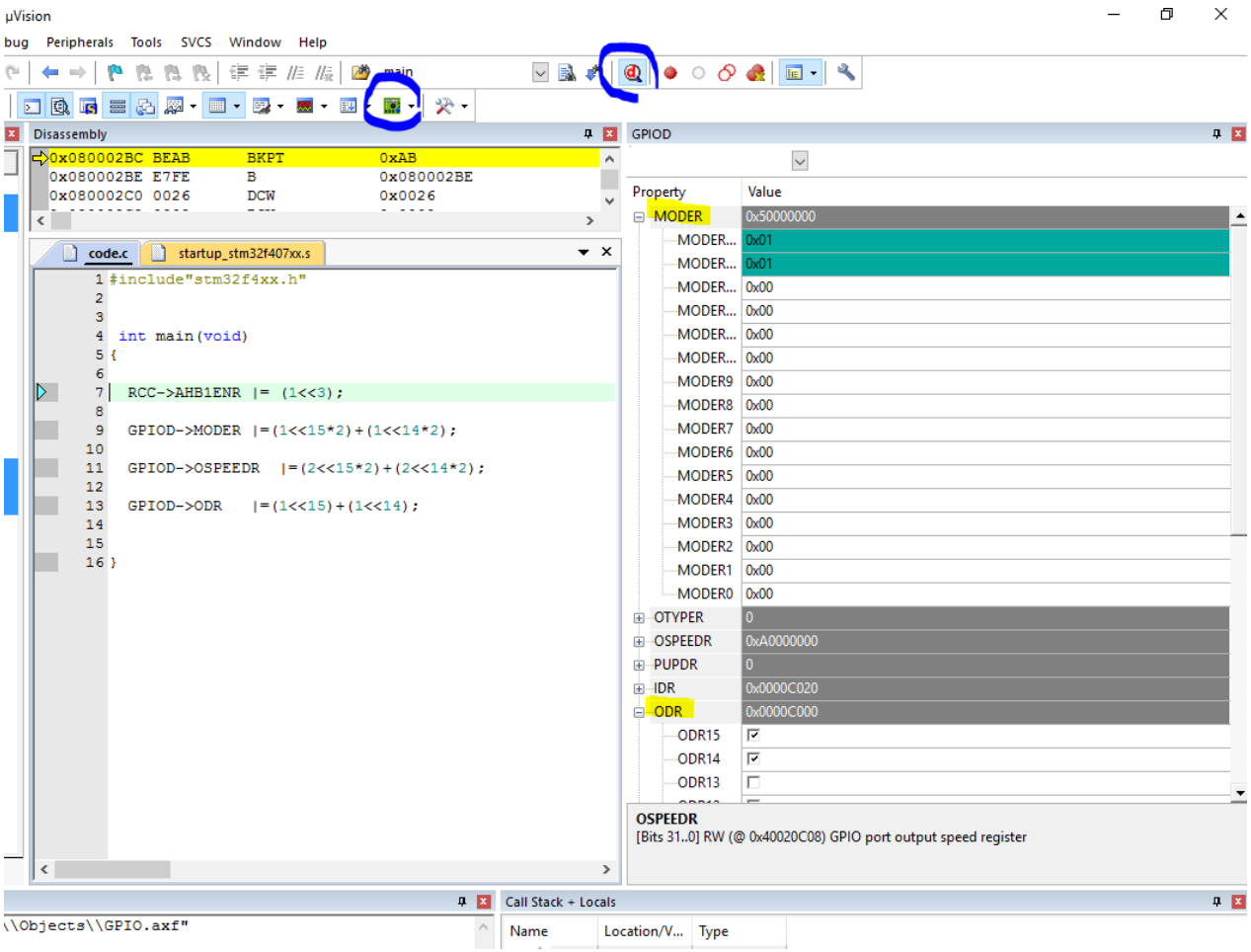
Debug and target configuration :



Contact : Mustapha.hamdi@insat.rnu.tn

GPIO Low Layer

Debug sessions



Program STM32F4 with stlink , then you should see led red and blue on because because our onboard **leds** are connected to GpioD 14 and 15

Contact : Mustapha.hamdi@insat.rnu.tn