Chapter2: Digital-to-analog converter (DAC)

Hardware : Discovery stm32f4, SoC Stm32f40vg

Reference : RM0090 reference manual (DM00031020.pdf)

Contact : Mustapha.hamdi@insat.rnu.tn

Institut national des sciences appliquées et de technologie, Tunisia

Powered by STM32

DAC Low Layer

- presentation
- DAC Registers
- Case study

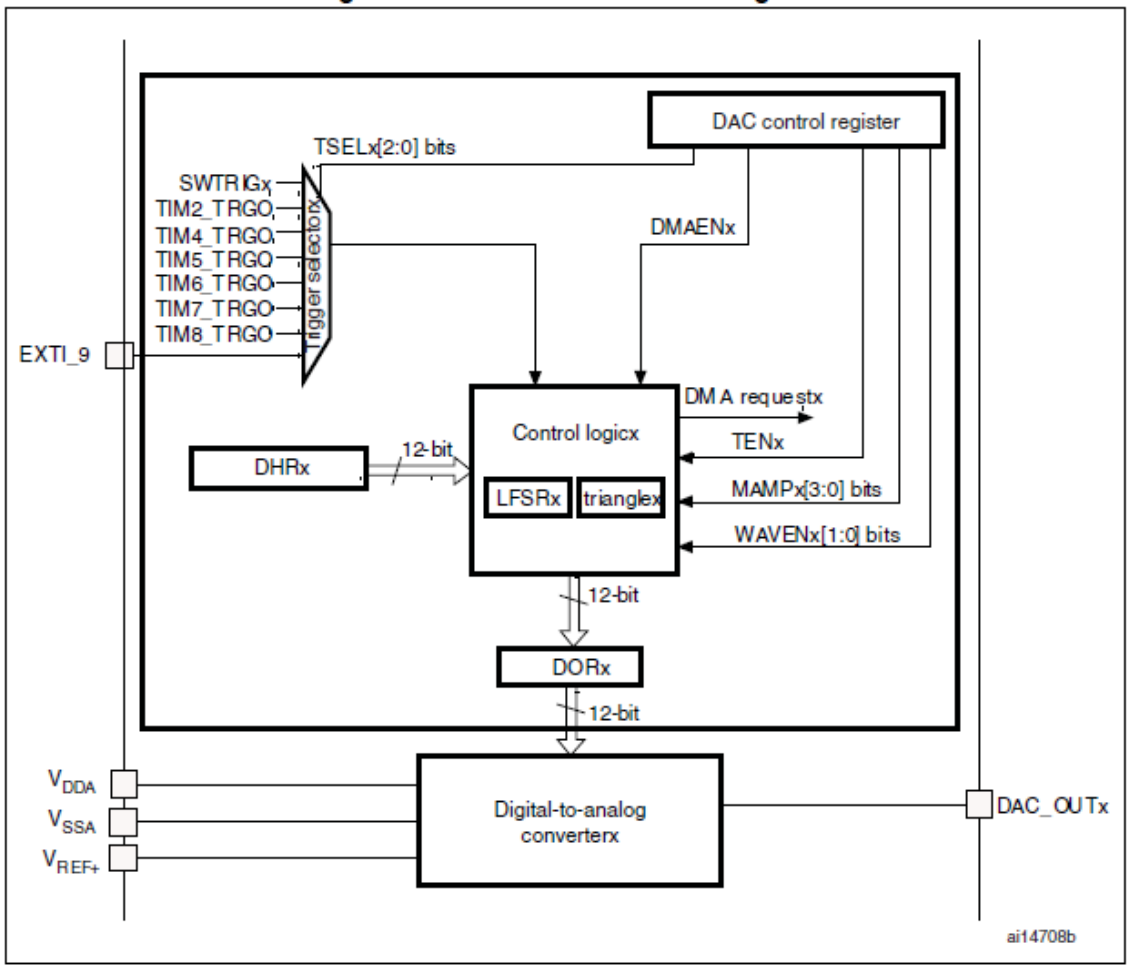
DAC Low Layer

The DAC module is a 12-bit, voltage output digital-to-analog converter. The DAC can be configured in 8- or 12-bit mode and may be used in conjunction with the DMA controller. In 12-bit mode, the data could be left- or right-aligned. The DAC has two output channels, each with its own converter.

Contact : Mustapha.hamdi@insat.rnu.tn

DAC Low Layer

Figure 64. DAC channel block diagram



Contact : Mustapha.hamdi@insat.rnu.tn

DAC Registers

DM00031020.pdf, page 448

Peripheral clock enable register
We should use Advanced
Peripheral Bus APB1 (42 MHz max)

APB1ENR

GPIO configuration

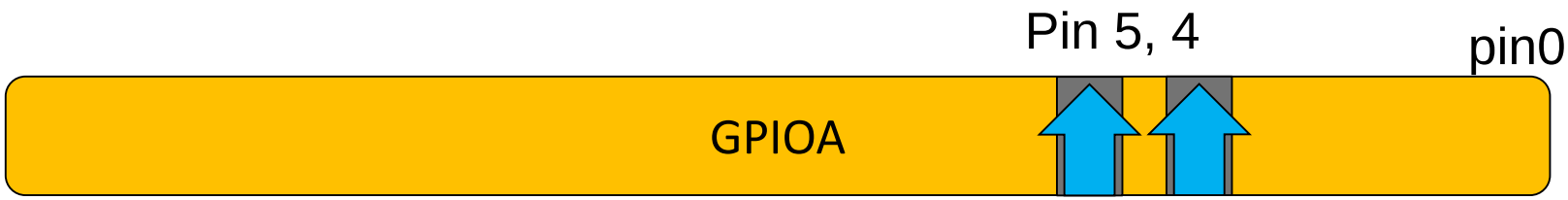
AHB1ENR, MODER

DAC control reg

CR

Data holding register 1 and 2

DHR12R1/R2



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DAC Low Layer

6.3.13 RCC APB1 peripheral clock enable register (RCC_APB1ENR)

Address offset: 0x40

Reset value: 0x0000 0000

Access: no wait state, word, half-word and byte access.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UART8 EN	UART7 EN	DAC EN	PWR EN	Reser-ved	CAN2 EN	CAN1 EN	Reser-ved	I2C3 EN	I2C2 EN	I2C1 EN	UART5 EN	UART4 EN	USART 3 EN	USART 2 EN	Reser-ved
rw	rw	rw	rw		rw	rw		rw	rw	rw	rw	rw	rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI3 EN	SPI2 EN	Reserved		WWDG EN	Reserved		TIM14 EN	TIM13 EN	TIM12 EN	TIM7 EN	TIM6 EN	TIM5 EN	TIM4 EN	TIM3 EN	TIM2 EN
rw	rw			rw			rw	rw	rw	rw	rw	rw	rw	rw	rw

Page 183, DM00031020.pdf

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DAC Low Layer

DAC->CR |=(1<<0)+(1<<16) = 0x00010001;

14.5.15 DAC register map

Table 76 summarizes the DAC registers. Activation de deux chaines de sortie

Table 76. DAC register map

Offset	Register name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	DAC_CR	Reserved		DMAUDRIE2	DMAEN2	MAMP2[3:0]				WAVE 2[2:0]		TSEL2[2:0]			TEN2	BOFF2	EN2	Reserved		DMAUDRIE1	DMAEN1	MAMP1[3:0]				WAVE 1[2:0]		TSEL1[2 :0]			TEN1	BOFF1	EN1
0x04	DAC_ SWTRIGR	Reserved																														SWTRIG2	SWTRIG1
0x08	DAC_ DHR12R1	Reserved																				DACC1DHR[11:0]											
0x0C	DAC_ DHR12L1	Reserved																				DACC1DHR[11:0]										Reserved	
0x10	DAC_ DHR8R1	Reserved																								DACC1DHR[7:0]							
0x14	DAC_ DHR12R2	Reserved																				DACC2DHR[11:0]											
0x18	DAC_ DHR12L2	Reserved																				DACC2DHR[11:0]										Reserved	

Mustapha.hamdi@insat.rnu.tn

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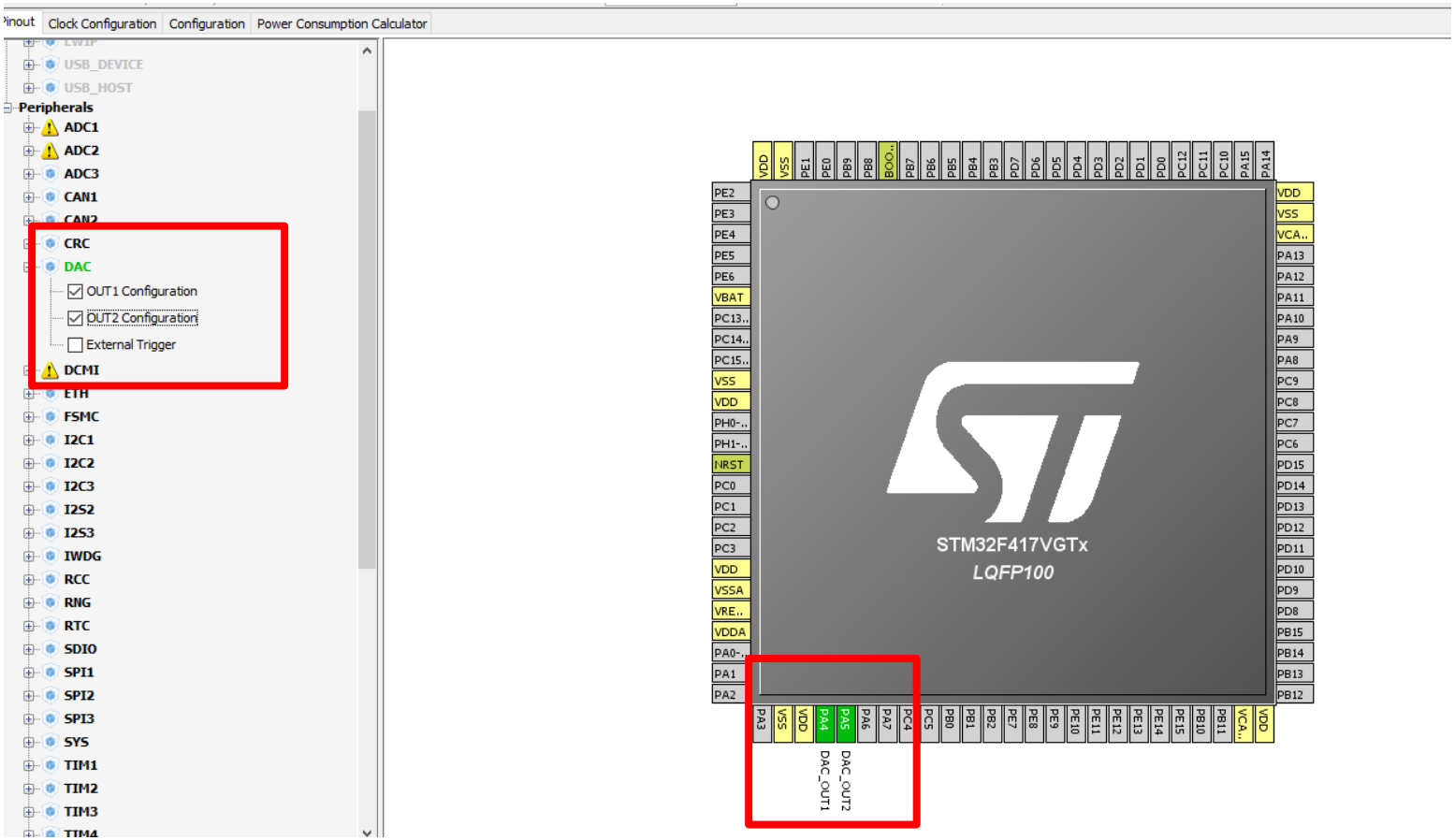
STM32CubeMX which is a graphical software configuration allows us to find DAC Pins output ; PA4 and PA5 as analog output :



Cubemx Link : http://www.st.com/en/development-tools/stm32cubemx.html

Mustapha.hamdi@insat.rnu.tn

DAC Low Layer

Case Study

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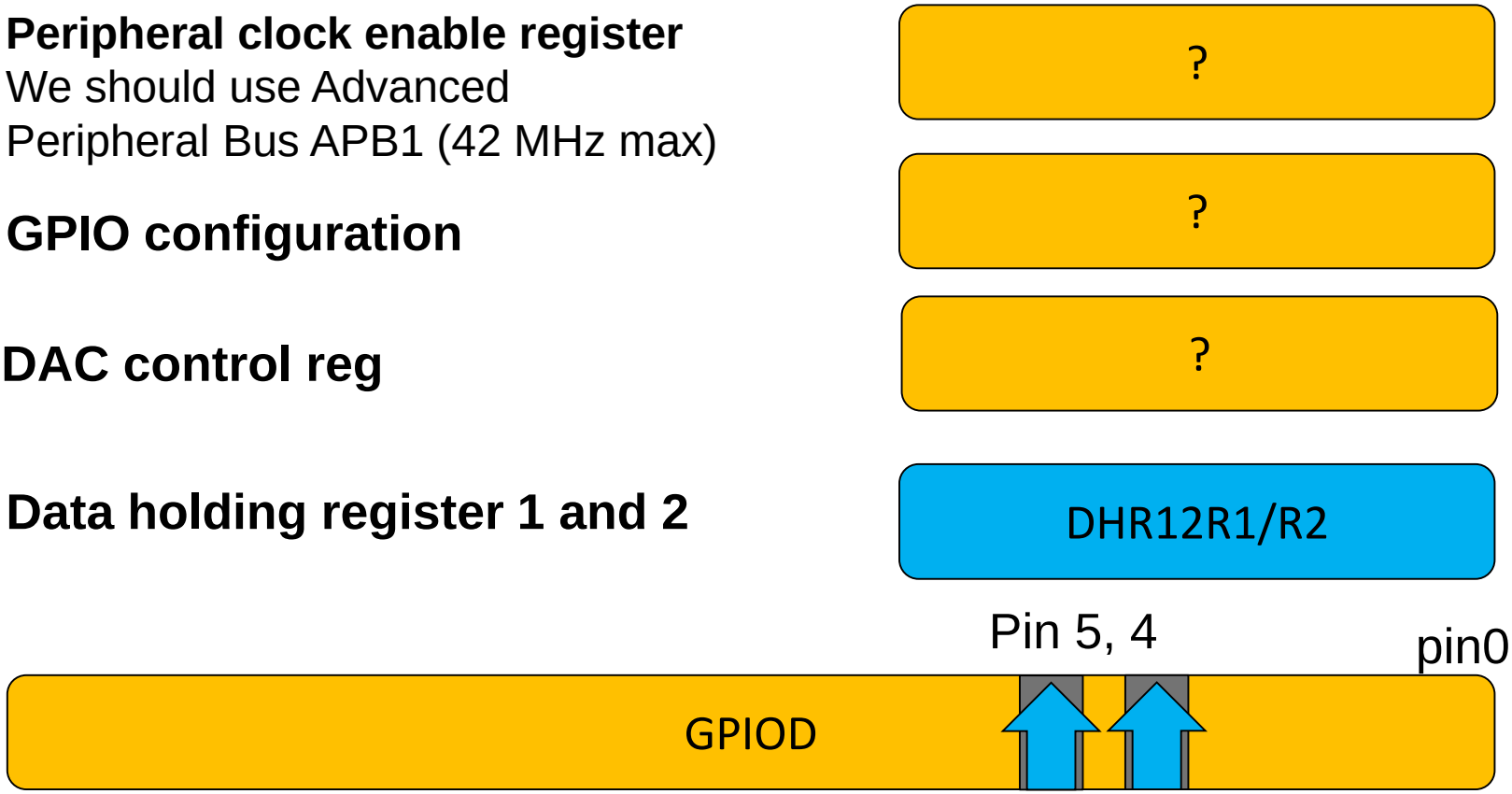
GPIO configuration

DAC control reg

Data holding register 1 and 2



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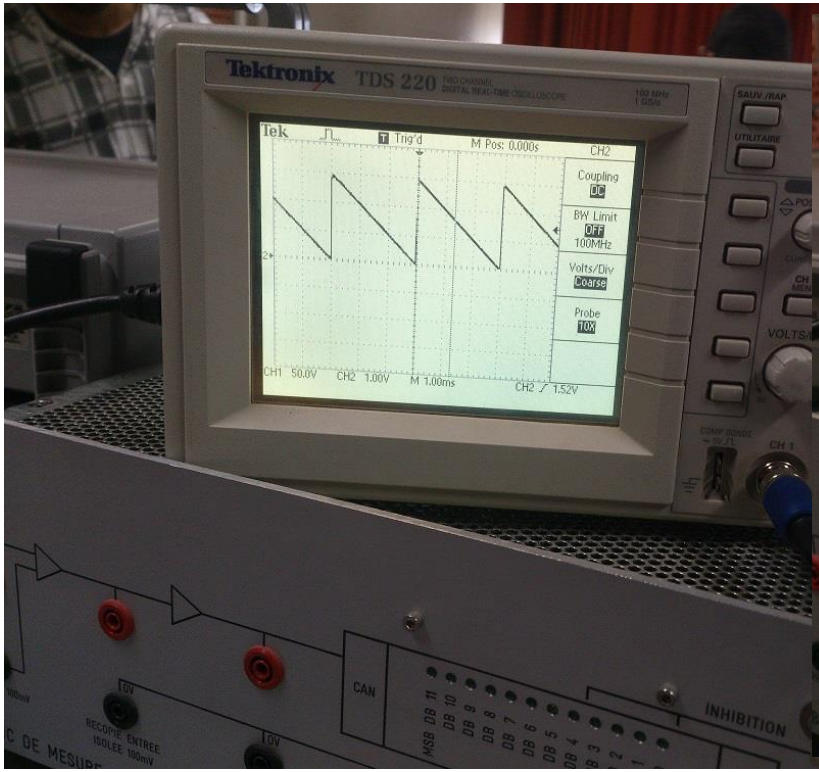
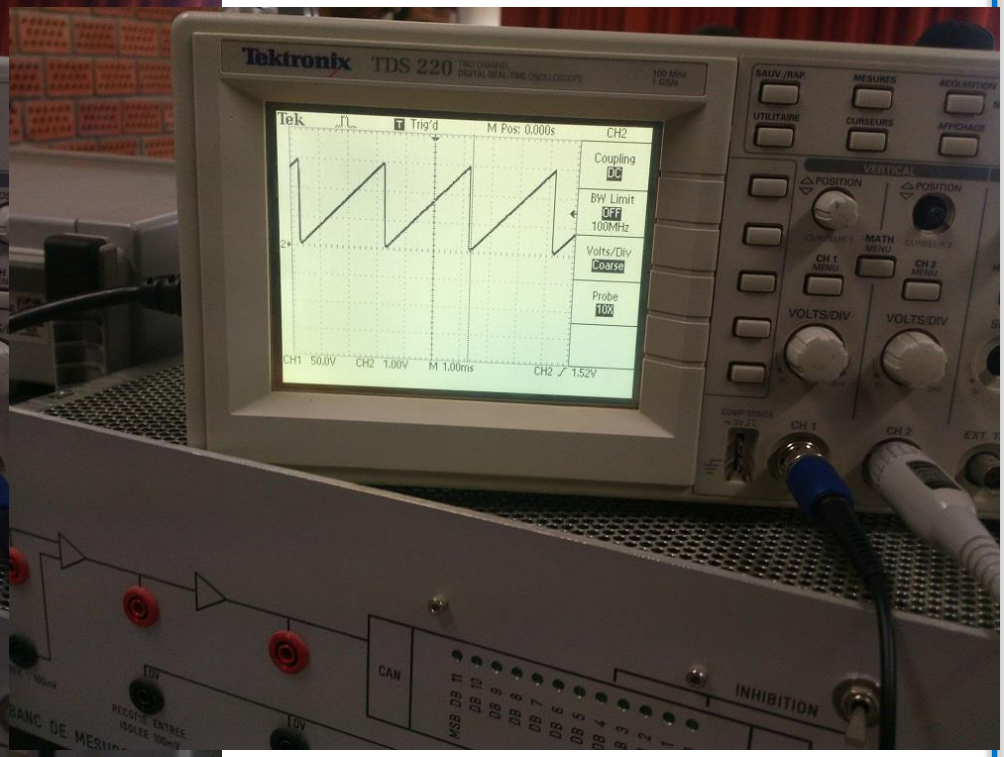
DAC Low Layer

solution please see attached code

DAC output :





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