BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

CSE306 (Computer Architecture Sessional), January 2019 Term
All Lab Sections, July 17, 2019

Specification for Floating Point Adder Simulation

In this assignment, you are required to design a floating point adder circuit which takes two floating points as inputs and provides their sum, another floating point as output. Each floating point will be 16 bits long with following representation:

Sign	Exponent	Fraction
1 bit	4 bits	11 bits

You have to implement your design in any simulator software of your choice. Please note that, if your chosen simulator does not provide support for 16 bit ALU, you can construct one by cascading number of smaller ALUs. Moreover, since construction of ALU is not major focus of this assignment, you can take help from the Internet or other sources (or even use someone else's implementation) for the 16 bit ALU part only. The rest of the circuit design and implementation must be done by yourselves.

Submission Guideline

- A submission link will be opened on Moodle for submitting your ALU simulation. Make a folder named *Bi_Gj* containing your simulation project files along with the soft copy of your Block Diagram and make a zip file for submission. Please ensure a single submission from each group.

Submission Deadline: For all lab groups: July 28, 2019 (Saturday) at 7.59am.