ELEC 5280 Homework 2

Due on March 24th, 2024 (Sun.). You must submit your homework online via Canvas.

Problem 1

The purpose of this exercise is to help you to understand the impact of parasitic resistance on the RF characteristics performance of a MOSFET. Using the **TSMC 22nm CMOS PDK (Cadence library name: tsmcN22)** provided (*see **[Tutorial]02 Homework 2 TSMC 22nm CMOS Characterization with Cadence**), simulate the NMOS model named "**nmos_rf_lvt_nw**" with W = 1 µm, L = 30 nm and number of fingers = 4, i.e., the total width = 4 µm, in Cadence. For 22nm process, you can use ideal inductors and capacitors to bias the device to set Vgs = 0.4 V and Vds = 0.5V. Perform a S-parameter simulation from **200 MHz to 200 GHz**.

Table 1. Equivalent circuit model components based on Y-parameters.

Circuit Model Component	Expression
Input Resistance	$R_{in} = R_e\left(\frac{1}{Y_{11}}\right)$
Output Resistance	$R_{out} = \frac{1}{R_e(Y_{22})}$
Input Capacitance	$C_{in} = \frac{\partial}{\partial\omega}\left[\frac{1}{\mathrm{Im}\left(\frac{-1}{Y_{11}}\right)}\right]$
Output Capacitance	$C_{out} = \frac{\partial}{\partial\omega}[\mathrm{Im}(Y_{22})]$
Transconductance	$g_m = \mathrm{Re}(Y_{21})$
Feedback Capacitance	$C_{fb} = \frac{\partial}{\partial\omega}[\mathrm{Im}(-Y_{12})]$

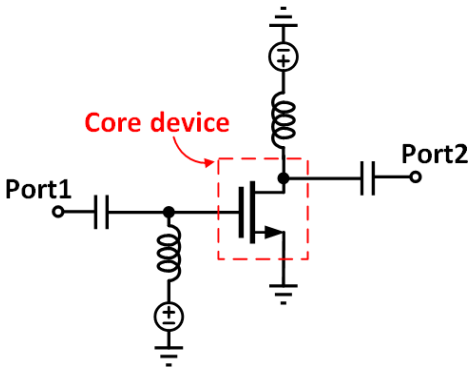

Figure 1. Test bench for an NMOS device.

a) Plot the six equivalent circuit model components listed in Table 1 over the specified frequency range. For the capacitance, you will need to use the derivative function in the Calculator in Spectre.
b) Plot minimum noise figure (in dB) over the specified frequency range.
c) Determine f_T from the simulation result (|h21|). (You may need to broaden the sweep range to, e.g., **800GHz**)
d) Determine f_{max} by extrapolating the maximum power gain (G_{max}). (You may need to broaden the sweep range to, e.g., **800GHz**)

Problem 2

In this problem, you will design a standard common-source Low Noise Amplifier (LNA) with source degeneration shown below using the **TSMC 22-nm CMOS process (tsmcN22)**. You are tasked with the design of the differential LNA begin by adapting the provided single-ended common-source LNA topology into a differential configuration. Next, you will evaluate two noise reduction techniques. The first method introduces C_d to decouple the input resonant circuit Q and Cgs. The second method reduces the noise contribution from the cascode device (M2) by increasing the impedance at node X at the center frequency. For transistors, use the RF transistor model 'nmos_rf_lvt_nw' of 'tsmcN22'. For capacitors, resistors and inductors, use ideal inductors of 'analogLib' named 'ind'.

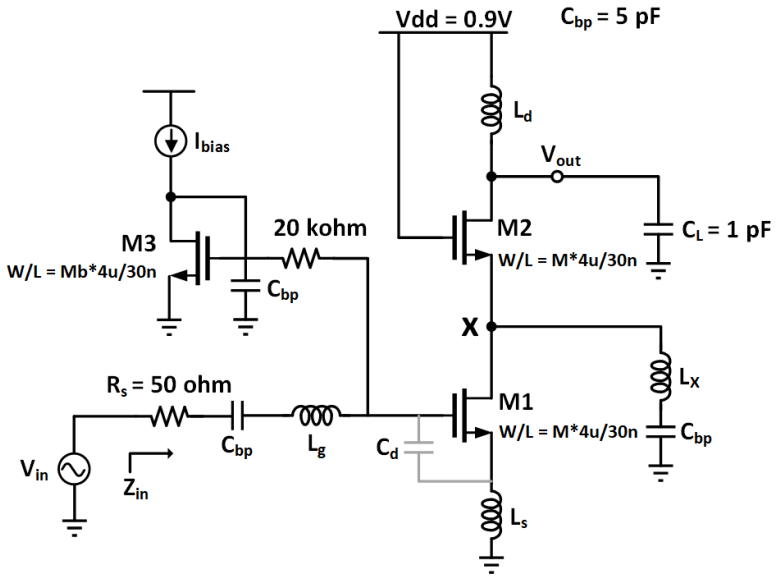

Figure 2. Schematic of a standard single-ended common-source LNA.

Specifications:

1. Input impedance matching: |S11| < −12 dB
2. Center frequency f_0 = 28 GHz
3. Voltage gain > 12 dB at f_0
4. Power consumption < 30 mW (the lower, the better) with Vdd =0.9 V
5. Noise figure < 5 dB
6. IIP3 > -15 dBm

Figure 2 presents the schematic of a single-ended common-source LNA. Your task is to modify this schematic into a differential topology. For tasks (e) to (i), you should make modifications without adding the capacitor Cd and the inductor Lx. For tasks (j) and (k), incorporate Cd into your design. Finally, for task (l), include Lx in the schematic.

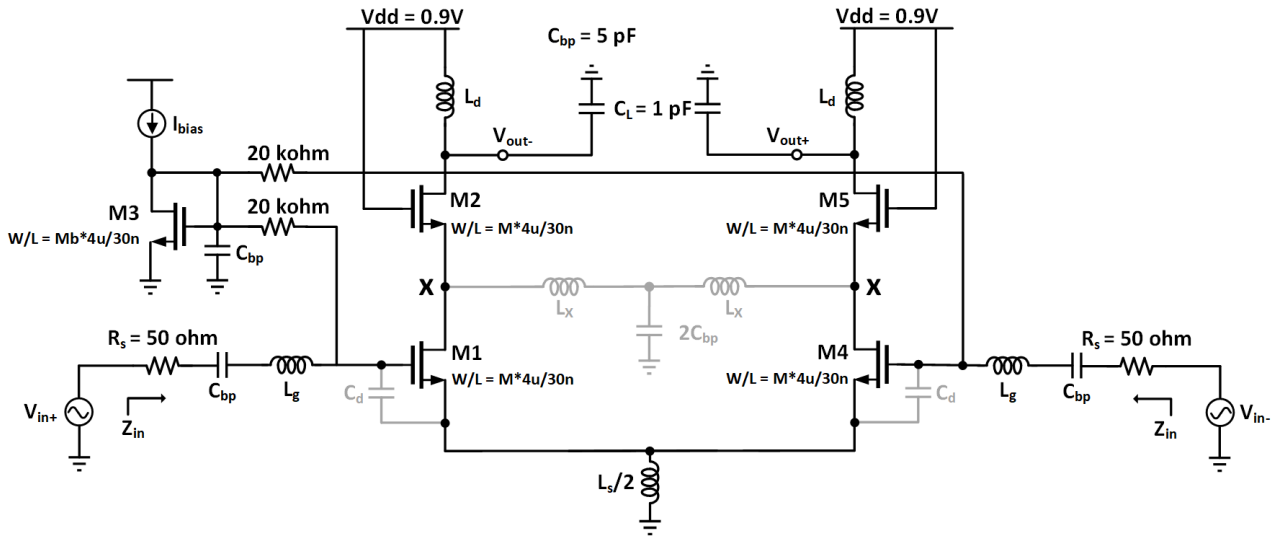

Figure 3. Schematic of the corresponding differential LNA.

a) Simulate the single transistor M1. Plot gm vs. I_{den1} (current density) and f_T vs. I_{den1} by sweeping I_{ds}, M1 with a fixed width, e.g., 4µm. (Hint: For 22nm transistors, minimum finger number is 4. To simplify calculations, we will standardize the finger width at 1µm. Therefore, the total width = M*finger width*finger number=M*4um)

b) Determine I_{bias} and M (Multiplier of M1 and M2) that gives the optimal f_T and gm for minimizing NF. What is resulting input resonant circuit Q? (For the size of transistor M3, Mb is typically very smaller than M, e.g., Mb=10%M)

c) Determine L_g and L_s using Cgs and f_T to provide the required input matching. Assume L_s and L_g have a Q of 15 at f_0, compute the series resistance value and include it in the simulation (use 'ind' and 'res' from 'analogLib').

d) Determine L_d such that the output node is tuned at f_0. Assume L_d have a Q of 15 at f_0, compute the series resistance value and include it in the simulation (use 'ind' and 'res' from 'analogLib').

e) Plot the gain (Vout/Vin), noise figure (NF) and input impedance (Zin) vs. frequency from 0.1 to 50 GHz.

f) Perform a PSS analysis at f_0 to determine the 1-dB compression of this LNA by sweeping the input port power.

g) Using PSS analysis, perform a two-tone test to determine the IIP3 of the LNA using signals at f_0 and f_0+800MHz. (Optional: You can use hb and PAC analysis to simulate the IIP3 again and compare results for **bonus credits**).

h) Using sp analysis, plot the K factor vs. frequency from 0.1 to 50 GHz. Comment on the stability of your designed LNA based on the simulation result.

i) Using sp analysis, plot noise circles with noise ranges from 1 dB to 10 dB and gain circles with gain ranges from 10 dB to 20 dB, both at f_0. Comment on the trade-off between gain and noise based on the circles.

j) Now, add C_d between the gate and source terminal of M1, plot NF at f_0 vs. C_d, make sure that you adjust L_g and L_s for each value of C_d to maintain the input matching at f_0. How much is the improvement in NF? What happened to the amplifier gain?

k) With the C_d and the L_g, perform a sweep of the input device width, is there a new optimal width that gives lower NF? If so, what is it and what is the NF?

l) Now, add L_x at the cascode node by first estimating the parasitic capacitance at node X. How much is the improvement in NF? What happened to the amplifier gain?

Hint:

In our design of a Low Noise Amplifier (LNA) using 22nm technology, we utilized two noise reduction techniques. The first is based on P. Andreani's method from the *IEEE TCAS-II* in 2001, which uses a capacitive load (Cd) to reduce the coupling between the Q factor of the input resonant circuit and the gate-source capacitance (Cgs). The second technique, proposed by H. Samavati in the *IEEE JSSC* in 2000, focuses on impedance enhancement.

While our design does not incorporate the latest advancements, such as the 65nm common-gate LNA by X. Wu presented at the *IEEE IWS* in 2019, or the 22nm FD-SOI two-stage LNA by Z. Zong from the *IEEE RFIC* Symposium in 2021, these cutting-edge designs represent potential future directions for enhancing our LNA design.

Reference Papers

[1] Thomas H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, 2nd Edition, 2004.
[2] X. Wu, M. Kalantari, D. H. Shin and C. Patrick Yue, "A 24-32GHz gm-boosted LNA with Triple Coupling Input Transformer for 5G Applications," 2019 IEEE MTT-S International Wireless Symposium (IWS), Guangzhou, China, 2019.
[3] Z. Zong et al., "A 39GHz T/R front-end module achieving 25.6% PAEmax, 20dBm Psat, 5.7dB NF, and −13dBm IIP3 in 22nm FD-SOI for 5G communications," 2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Atlanta, GA, USA, 2021.
[4] P. Andreani and H. Sjöland, “Noise Optimization of an Inductively Degenerated CMOS Low Noise Amplifier,” IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING, VOL. 48, NO. 9, SEPTEMBER 2001 835.
[6] H. Samavati, H. R. Rategh, T. H. Lee, “A 5-GHz CMOS Wireless LAN Receiver Front End,” IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 35, NO. 5, MAY 2000, pp.765.