Shuo **Feng**

B.Sc. Student · Integrated Circuit Design

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Education

SUSTech (Southern University of Science and Technology)

Shenzhen, China

B.S. in Microelectronics Science and Engineering

Aug. 2019 - PRESENT

- **Overall GPA:** 3.91 / 4.00 (Major GPA: **3.93** / 4/00, Ranking **2** / 78)
- **Relevant Coursework:** CMOS Analog Integrated Circuit Design *(99 / 100)*, Advanced Digital CMOS IC Design *(98 / 100)*, Analog Circuits *(98 / 100)*, Microprocessor Design *(98 / 100)*, VLSI Fabrication Technology *(95 / 100)*, Electronic Design Automation (EDA) Basics *(93 / 100)*, System-on-a-Chip Design *(93 / 100)*, Signals and Systems *(93 / 100)*, Engineering Electromagnetics *(97 / 100)*

Projects

High-Speed, Large-Swing Optical Modulator Driver with All-Pass Filter (APF) -Based Dynamic Bias and 2-Tap FFE

SUSTech, Shenzhen, China

Project Leader

Aug. 2022 - PRESENT

- Proposed a high-speed, large-output swing driver in **130-nm SiGe BiCMOS process**.
- Applied the breakdown voltage (BV) doubler topology with APF-based dynamic bias to improve the output swing and the bandwidth.
- Implemented a 2-tap fractional-spaced FFE to compensate for the insufficient bandwidth of optical modulators.

Large-Swing Breakdown Voltage (BV) Doubler Topology Drivers with Inductive-Peaking-Based Bandwidth Extension Techniques

SUSTech, Shenzhen, China

Project Leader

Mar. 2022 - PRESENT

- Gained expertise in inductive-peaking-based bandwidth extension techniques during design using **130-nm SiGe BiCMOS process**.
- Demonstrated the effectiveness of T-coils and three-end transformers in an electrical/optical (E/O) system where a Verilog-A model for Mach-Zehnder Modulator (MZM) with a 3-dB bandwidth of 35 GHz is used.
- Continuing to do research on the distributed output networks in transmitters (TXs).

Low-Power Consumption, High-Precision Relaxation Oscillation with Fully-on-Chip Voltage Reference and LDO Regulator

SUSTech, Shenzhen, China

Core Member

Mar. 2022 - July. 2022

- Developed a relaxation oscillation in **TSMC 180-nm CMOS process** with fully-on-chip voltage reference and LDO regulator.
- Simplified the logic control circuits to save power and chip area.
- Improved the delay compensation technique to make the proposed oscillator has minimized sensitivity to temperature variations.

High Output Voltage Swing Breakdown Voltage (BV) Tripler Topology Driver with Analog Multiplexer (AMUX)-based FFE

SUSTech, Shenzhen, China

Core Member

Jan. 2022 - PRESENT

- Participated in system design and verification in **130-nm SiGe BiCMOS process**.
- Confirmed of the validity of FFE stage for compensating the bandwidth.
- Finished the layout and post-simulation of partial blocks, and this work is supposed to be sent out for tapeout in August 2022.

Experience

Nanyang Technological University

NTU, Singapore

Exchange Ungergraduate Student

Jan. 2023 - May. 2023 (FUTURE)

- Received a recommendation for the Spring 2023 semester for the University Exchange Program (NTU).

Undergraduate Research, Communication Integrated Circuits and Systems Laboratory (Prof. Quan Pan)

SUSTech, Shenzhen, China

Researcher for <Wireline / Wireless high-speed communication ICs design>

Oct. 2021 - PRESENT

- Researched high-speed, large-swing optical transmitters with equalization techniques.
- Implemented optical modulator drivers that can transmit 160-Gb/s PAM-4 signals with 4-Vppd output voltage swing, and verified the proposed electrical driver by doing the co-simulations in an E/O system.

University of Oxford, Department of Computer Science, Academic Winter School *Oxford, United Kingdom*

Online Distance Learner of Oxford Study Abroad Programme *Jan. 2022*

- Obtained credit of course "Artificial Intelligence and Machine Learning" by engaging in 150 hours independent study and project work.

National University of Singapore (NUS), School of Computing *NUS, Singapore*

Project Leader in <Embedded part> *May. 2021 - July. 2021*

- Developed a smart system, "Smart Terrarium: Carp Yuelongmen", which connects the terrarium and customer by laptop server. The system is designed to monitor the condition of the mini-ecosystem and automatically adjust as well as notify the user.

Undergraduate Research, Energy-Efficient Integrated Circuit (EEIC) Laboratory (Prof. Chenchang Zhan) *SUSTech, Shenzhen, China*

Researcher for <Power management and energy harvesting ICs design> *Sept. 2020 - Oct. 2021*

- Studied low-power integrated circuit design methodology and gained practical experience in IC design.
- Researched on various topologies of low-dropout (LDO) regulators, as well as basic design ideas and circuit analysis of oscillators.

Publications & Patents

A 4-Vppd 160-Gb/s PAM-4 Optical Modulator Driver with All-Pass Filter-Based Dynamic Bias and 2-Tap FFE in 130-nm BiCMOS *Accepted for Presentation IEEE APCCAS 2022*

First Author *Aug. 2022*

- A high-speed, large-output swing driver with 2-tap feedforward equalizer (FFE) for optical modulators in 130-nm SiGe BiCMOS process.

A Large Output Swing Driver Circuit Design *National Intellectual Property Office*

Inventor *Sept. 2022*

- Application No.:202210504804.X
- This patent implements the breakdown voltage (BV) multiplier topology dynamic bias to avoid the breakdown of BJT transistors.

A Laborsaving Wire Pliers *National Intellectual Property Office*

Inventor *Apr. 2018 - Apr. 2020*

- Application No.:CN201820613788.7
- By pressing the pincer handle, the utility model can save effort for wire tensioning operation and subsequent tightening operation.

Honors & Awards

International

2022	**Finalist**, Consortium for Mathematics and Its Applications (COMAP), ICM Contest	*U.S.A*
2021	**1st Prize**, NUS Summer Workshop, Embedded System and Deep Learning	*Singapore*
2021	**Honorable Mention**, Consortium for Mathematics and Its Applications (COMAP), ICM Contest	*U.S.A*

Domestic

2022	**2nd Award**, China College IC Competition	*Fuzhou, China*
2021	**1st Class**, SUSTech 2021 Merit Student Scholarship	*Shenzhen, China*
2021	**Top 5**, SUSTech 2021 Jiang Bolong Scholarship	*Shenzhen, China*
2020	**1st Class**, SUSTech 2020 Merit Student Scholarship	*Shenzhen, China*

Leadership & Activities

2022	**Secretary**, SUSTech IEEE Student Branch	*Shenzhen, China*
2021	**Member**, SUSTech Shude College Women's Football Team	*Shenzhen, China*
2021	**Leader**, Huawei Developer Conference 2021	*Shenzhen, China*
2020	**Officer**, SUSTech, School of Microelectronics (SME) 2019 Grade Class Committee	*Shenzhen, China*
2020	**Director**, SUSTech Shude College Publicity Center	*Shenzhen, China*
2019	**Officer**, SUSTech Shude College STEAM+ Education	*Shenzhen, China*

Skills

Programming JAVA, Verilog, LaTex, Markdown, Python, Arduino, Linux

Tools Cadence, Silvaco, Quarters, Modelsim, Matlab, Visio, Origin, Multisim, Microsoft, TimeGen

Languages Chinese (native), English (fluent), Cantonese (basic)