A 4-V_{ppd} 160-Gb/s PAM-4 Optical Modulator Driver with All-Pass Filter-Based Dynamic Bias and 2-Tap FFE

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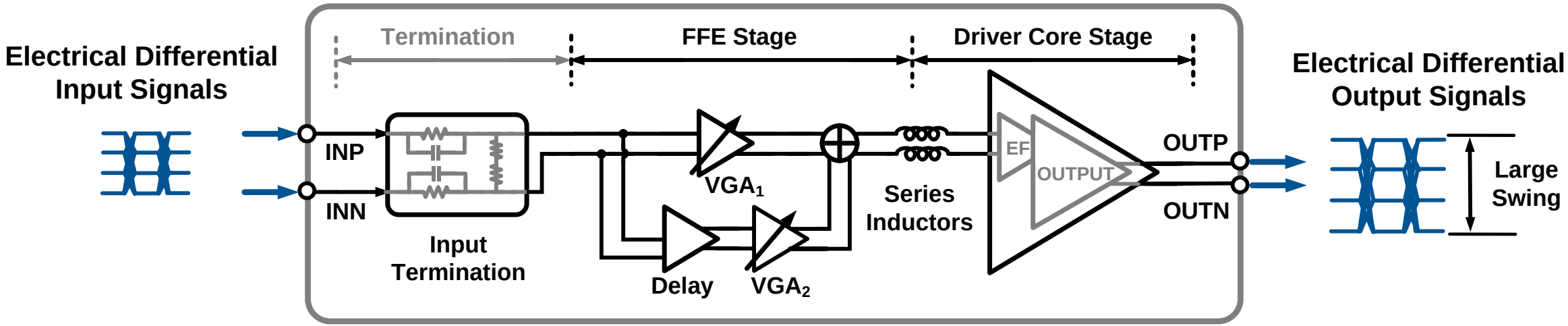
Driver Circuit Implementation

A 4-V_{ppd}160-Gb/s PAM-4 Optical Modulator Driver with All-Pass Filter-Based Dynamic Bias and 2-Tap FFE

- **Input Termination** (passive EQ, improve BW)
- **FFE Stage** (2-Tap, Re-configurable)
- **Driver Core Stage** (APF-based bias, BV Doubler)



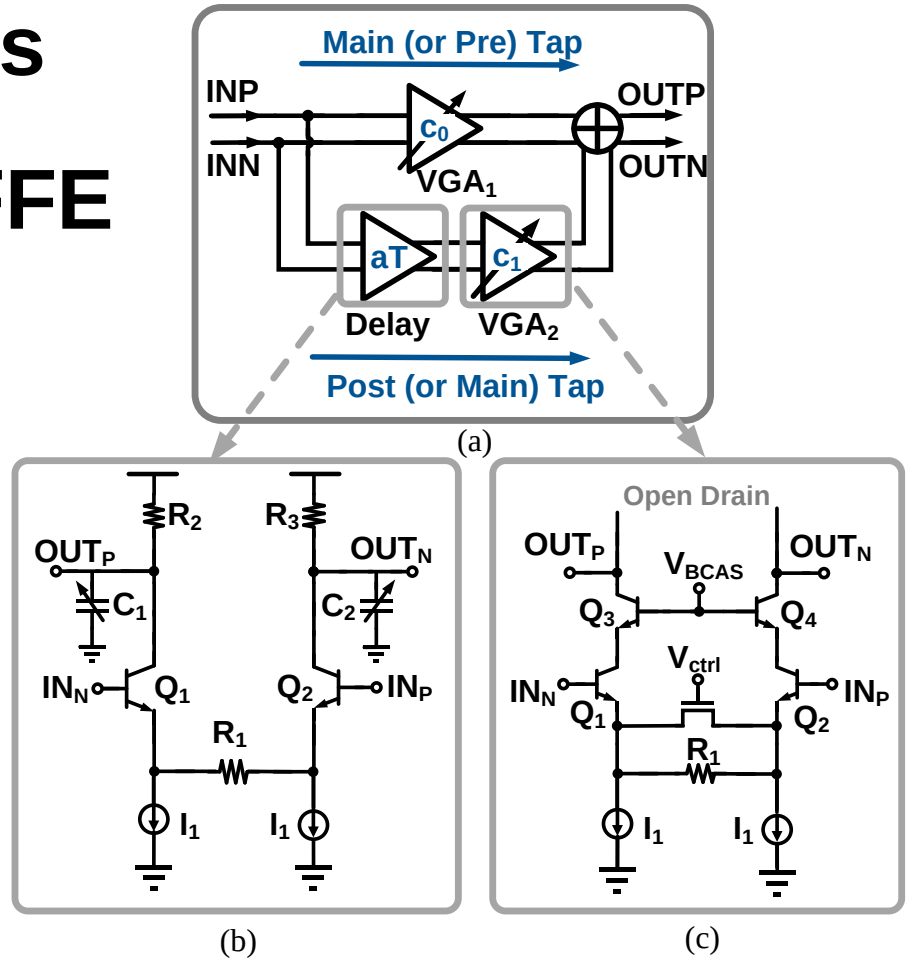
Block diagram of the proposed electrical driver.

Optical Modulator Driver with All-Pass Filter-Based Dynamic Bias and 2-Tap FFE

FFE Stage

- ☐1 Delay Cell
- ☐2 VGAs

The EQ stage incorporates a ① Fractional-Spaced ② 2-Tap FFE and can be ③ re-configurable.



(a) Block diagram of 2-tap fractional-spaced feed-forward equalizer (FFE). (b) Schematic of the delay cell. (c) Schematic of the variable-gain amplifiers (VGAs).

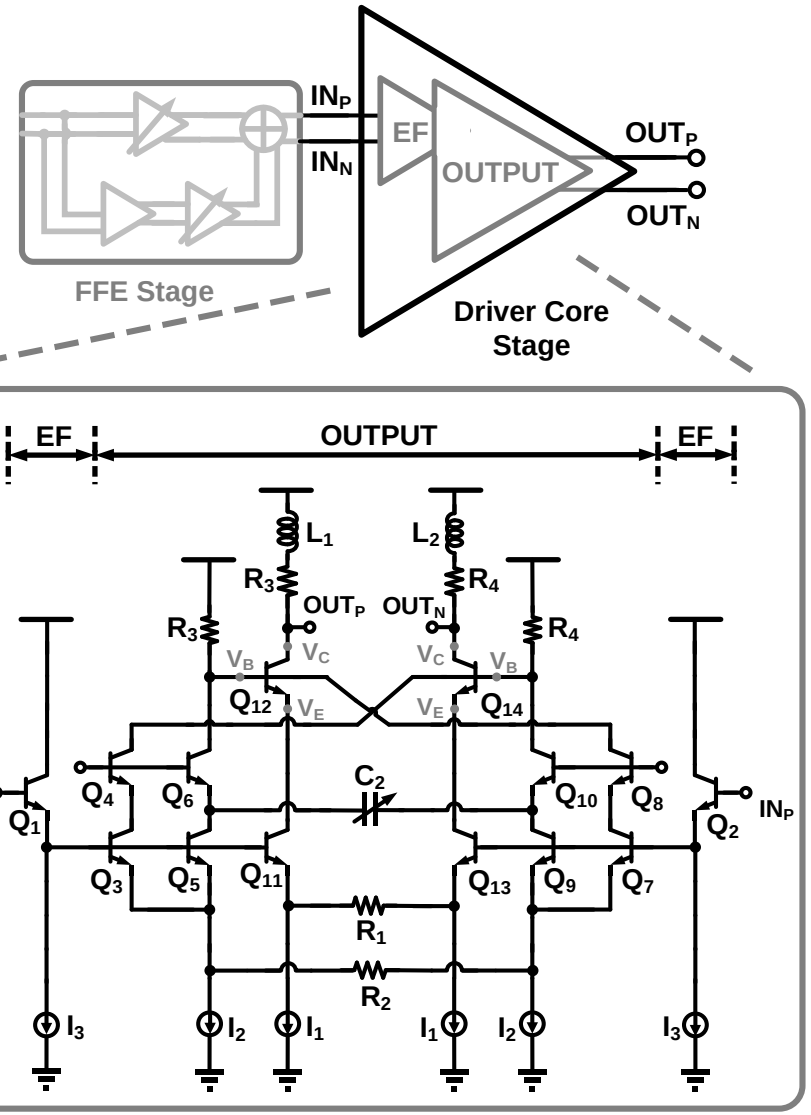
Driver Core Stage

Optical Modulator Driver with All-Pass Filter-Based Dynamic Bias and 2-Tap FFE

Driver Core Stage

- EF Stage
  - Buffer & DC common-mode level shifter
- Output Stage
  - APF-based bias circuit

$$H(j\omega\tau) = G \cdot \frac{1 - j\omega\tau}{1 + j\omega\tau} = G \cdot \left(\frac{2}{1 + j\omega\tau} - 1 \right)$$

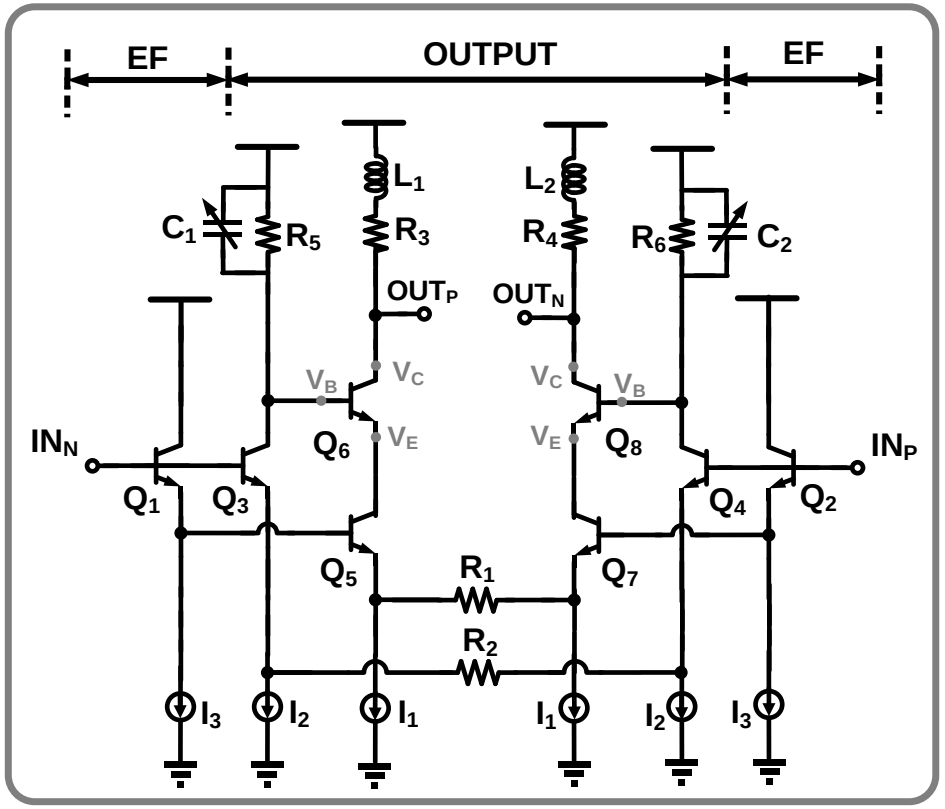


Schematic of the proposed BV doubler topology driver core with allpass filter (APF)-based bias.

Comparison Between LPF and APF Driver Core

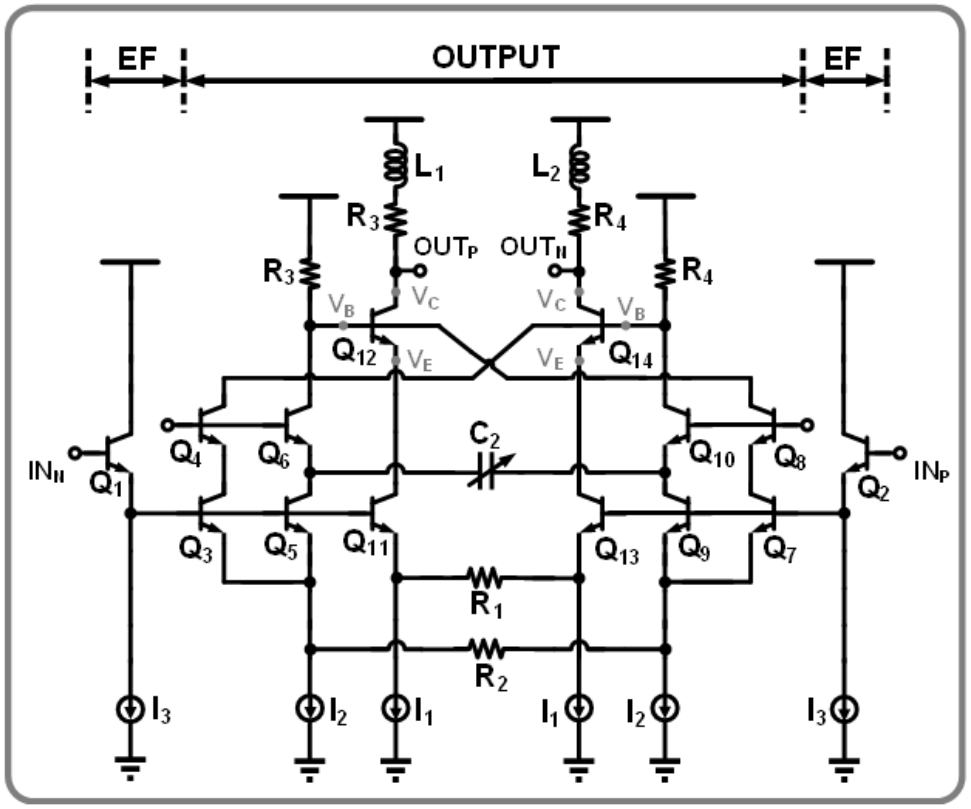
Output Stage: Dynamic Bias

- Conventional LPF-based dynamic bias



$$H(j\omega) = \frac{G}{1 + j\omega\tau}$$

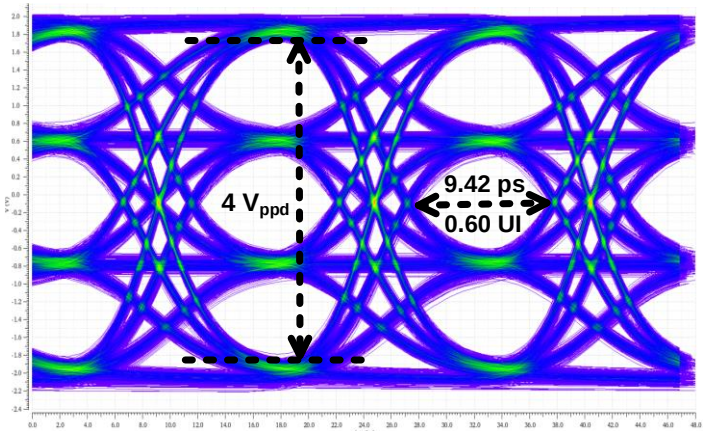
- Proposed APF-based dynamic bias



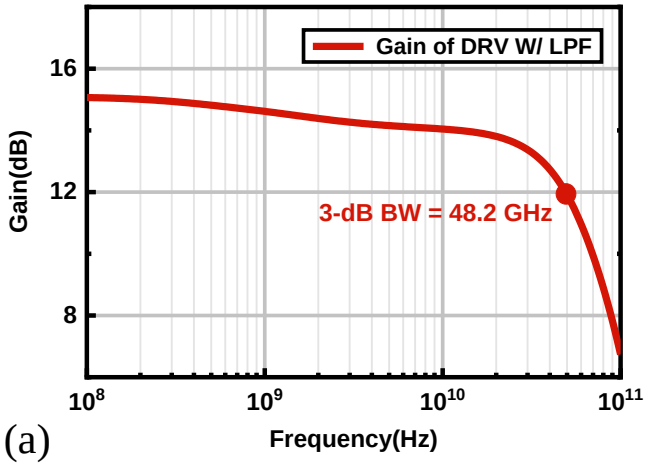
$$H(j\omega) = G \cdot \frac{1 - j\omega\tau}{1 + j\omega\tau} = G \cdot \left(\frac{2}{1 + j\omega\tau} - 1\right)$$

Comparison Between LPF and APF Driver Core

Simulation Results of the LPF-Based Bias Circuits

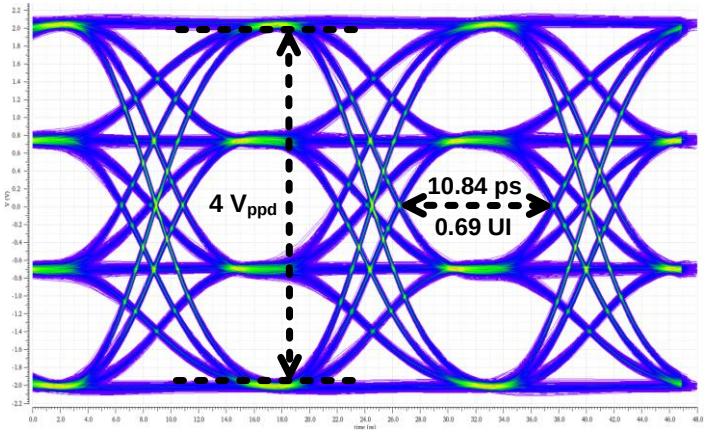


64-Gbaud PAM-4 Eye Diagram

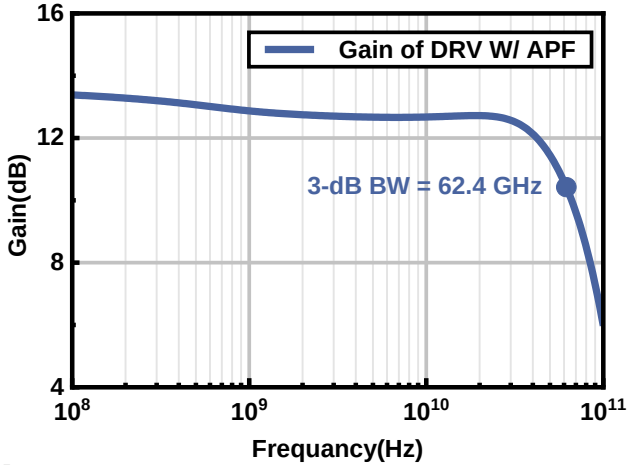


(a)

Simulation Results of the APF-Based Bias Circuits



64-Gbaud PAM-4 Eye Diagram



(b)

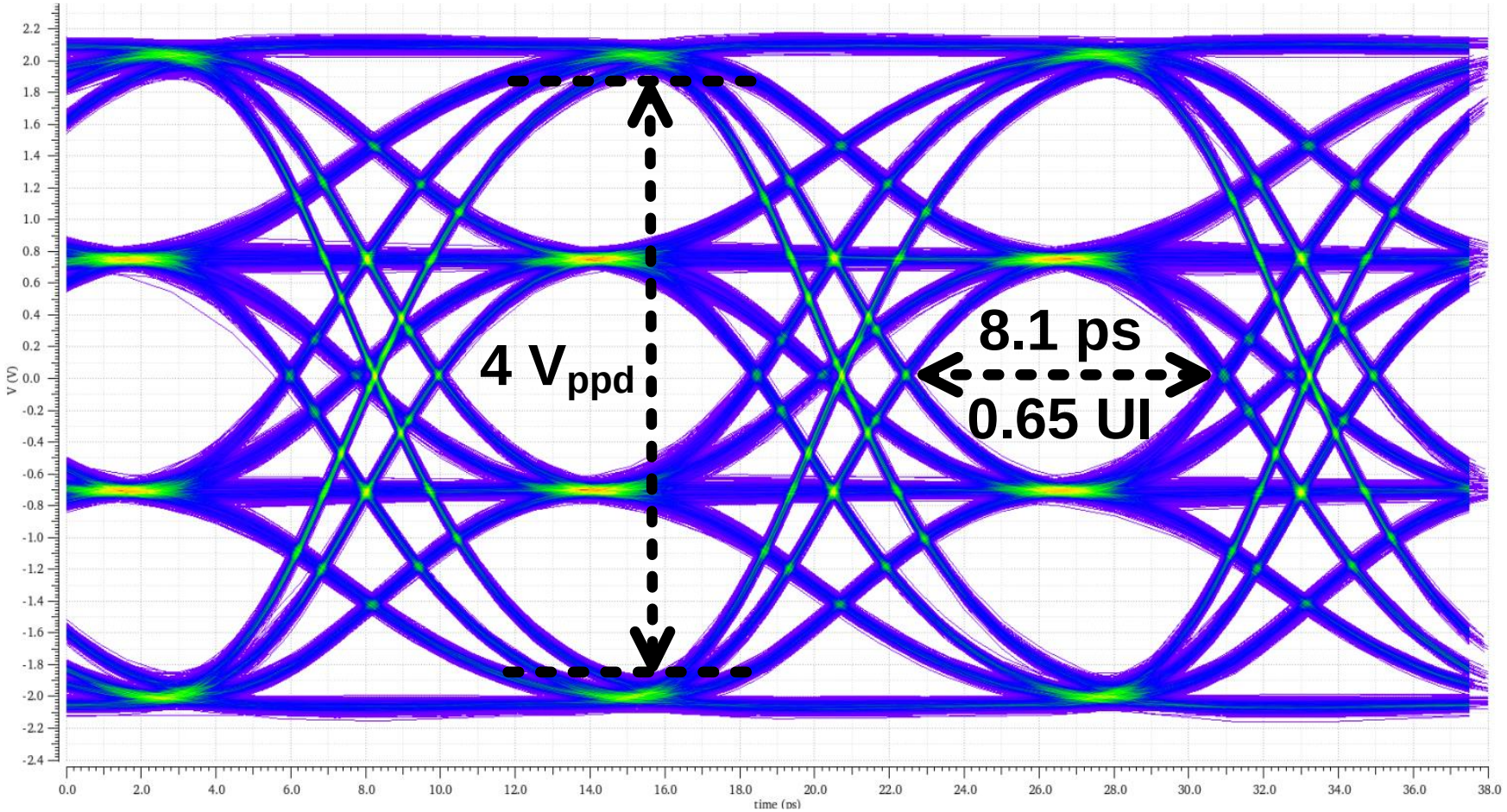
(a) 64-Gbaud PAM-4 eye diagram (left) and the frequency response (right) of the driver with LPF-based bias circuit.
(b) 64-Gbaud PAM-4 eye diagram (left) and the frequency response (right) of the driver with APF-based bias circuit.

Comparison Between LPF & APF versions

	LPF Version	APF Version
Bandwidth	48.2 GHz	62.4 GHz
Ratio of Level Mismatch	91.2%	95.1%
Eye Width	0.60 UI	0.69 UI
Power Consumption	Close Power Consumption	
Output Voltage	4 V_{ppd}	4 V_{ppd}

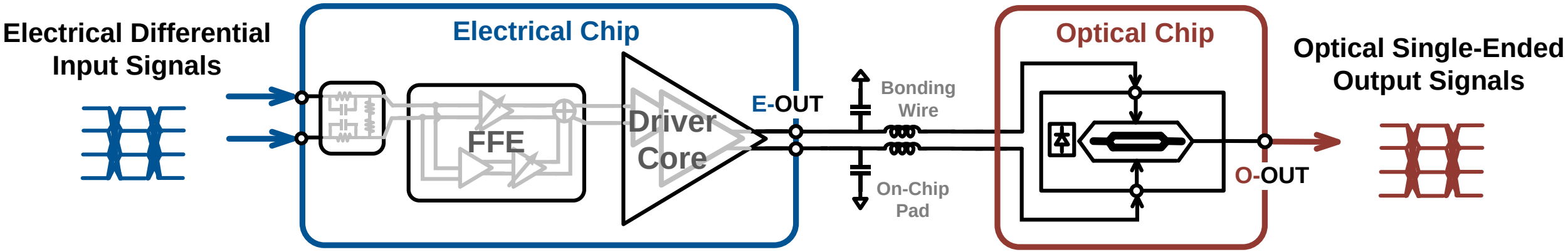
Simulation Result

80-Gbaud PAM-4 Eye Diagram of the Proposed Driver Core



80-Gbaud PAM-4 eye diagram of the proposed driver.

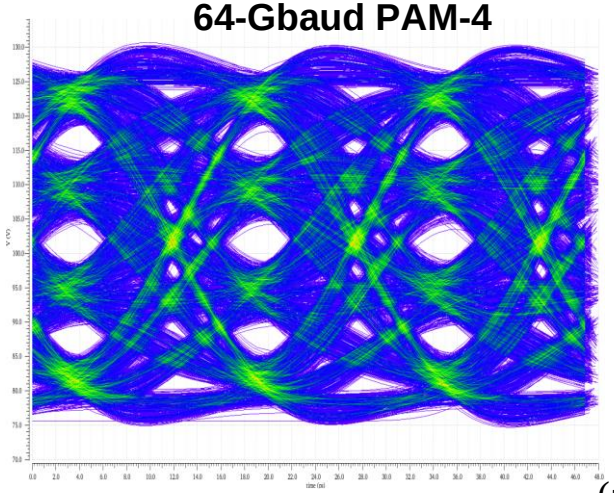
E/O System Simulation Results



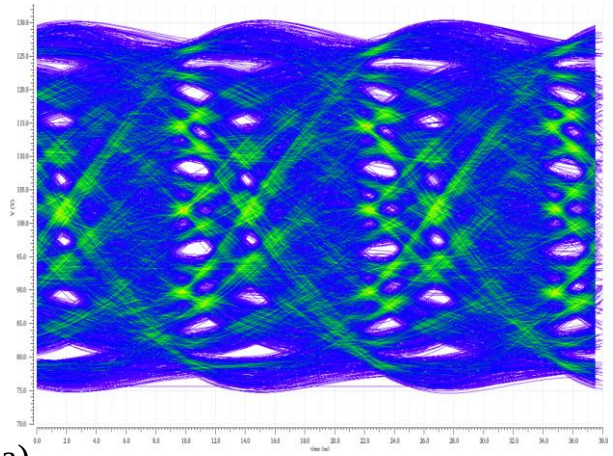
Electrical/optical (E/O) system with the proposed electrical driver and the optical MZM modulator.

System Optical Eye Diagram with FFE Turned off

64-Gbaud PAM-4



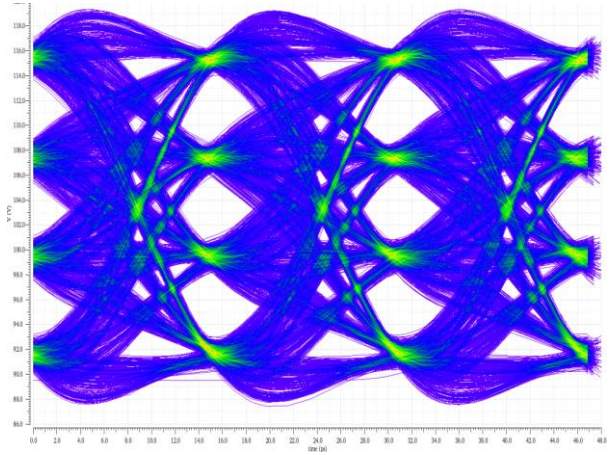
80-Gbaud PAM-4



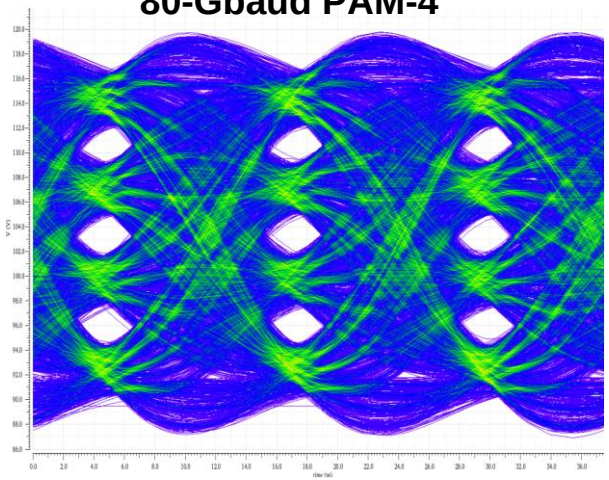
(a)

System Optical Eye Diagram with FFE Turned on

64-Gbaud PAM-4



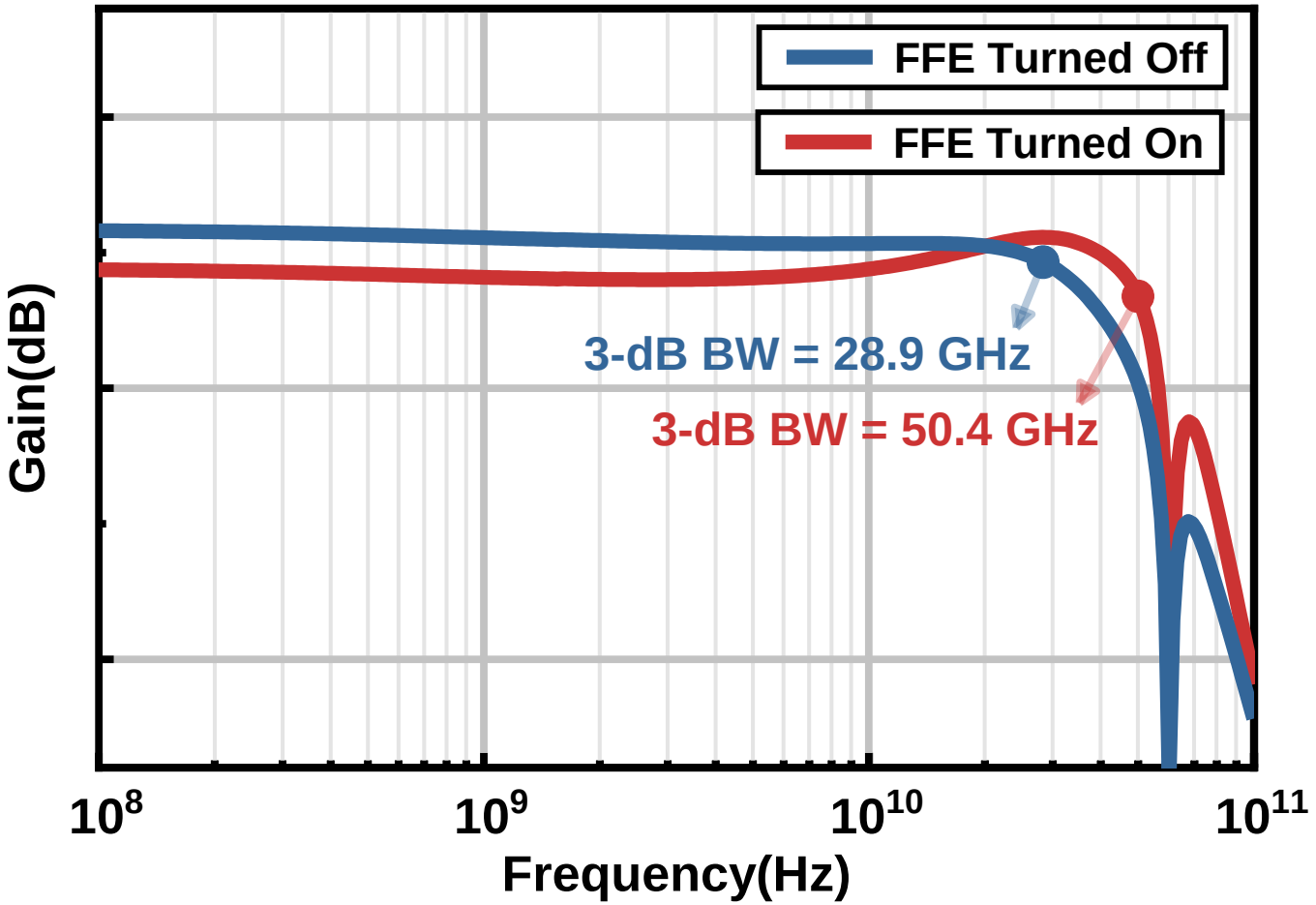
80-Gbaud PAM-4



(b)

(a) 64-Gbaud PAM-4 (left) and 80-Gbaud PAM-4 (right) E/O system optical eye diagram with FFE turned off. (b) 64-Gbaud PAM-4 (left) and 80-Gbaud PAM-4 (right) E/O system optical eye diagram with FFE turned on.

E/O System Simulation Results



Simulated frequency response of the E/O system with FFE turned off and turned on.

Comparison Table

SUSTech Southern University of Science and Technology

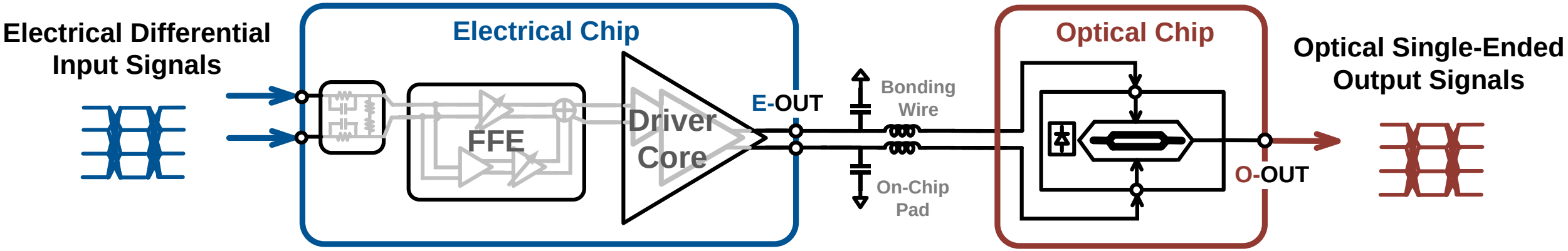
Comparison Table with State of The Art

	[1]	[2]	[3]	[4]	[5]	This Work
Technology	130-nm SiGe BiCMOS	250-nm InP DHBT	55-nm SiGe BiCMOS	55-nm SiGe BiCMOS	65-nm CMOS	130-nm SiGe BiCMOS
Differential Output Swing (V)	2.4 @PAM-4	1.8 @PAM-4	4.8 @PAM-4	4.4 @PAM-4	1.5 @PAM-4	4 @PAM-4
Electrical BW (GHz)	> 40	67	57.5	> 70	48	62
E/O BW (GHz)	40	N.A.	N.A.	N.A.	43	50.4
Data Rate (Gb/s)	552 @ DP-16QAM	112 @ PAM-4	128 @ PAM-4	128 @ PAM-4	640 @ DP-32QAM	160 @ PAM-4
Gain @ 1 GHz	20-30	1-11	12.8	20	13-22.5	13.4
Power (W)	4	0.84	0.82	1.1	0.9	1.15 (driver core: 0.99)

Some Thinking

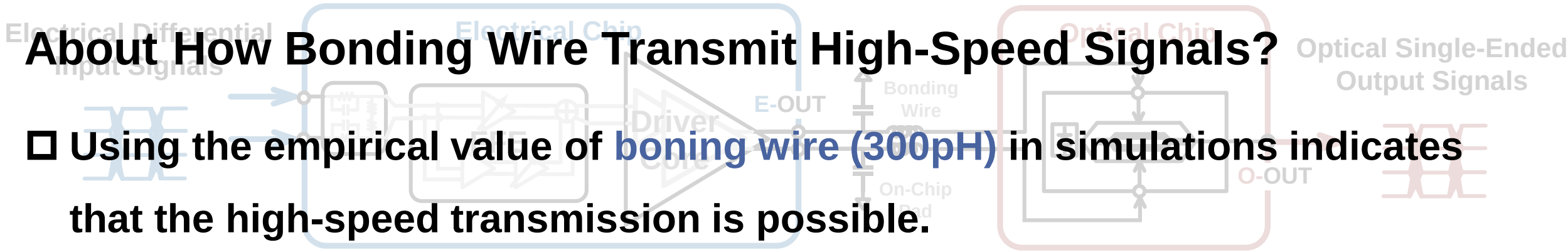
Some Re-Thinking about the Issues Mentioned Last Week

About How Bonding Wire Transmit High-Speed Signals?



Electrical/optical (E/O) system with the proposed electrical driver and the optical MZM modulator.

Some Thinking



About How Bonding Wire Transmit High-Speed Signals?

- Using the empirical value of boning wire (300pH) in simulations indicates that the high-speed transmission is possible.
- Make the wire as short as possible such as by PCB digging slots, so that the electrical chip and MZM optical chip the same height.
- The bonding wire will actually cause the bandwidth reduction, which can be compensated by EQ (FFE) stage.
- In the future, use relatively more advanced packaging methods such as flip chip.

Reference

[1] A. H. Ahmed, A. E. Moznine, D. Lim, Y. Ma, A. Rylyakov and S. Shekhar, "A Dual-Polarization Silicon-Photonic Coherent Transmitter Supporting 552 Gb/s/wavelength," IEEE Journal of Solid-State Circuits, vol. 55, no. 9, pp. 2597-2608, Sept. 2020.

[2] H. Wakita, M. Nagatani, K. Kurishima, M. Ida and H. Nosaka, "An over-67-GHz-bandwidth 2 Vppd linear differential amplifier with gain control in 0.25-μm InP DHBT technology," in 2016 IEEE MTT-S International Microwave Symposium (IMS), pp. 1-3, 2016.

[3] A. Zandieh, P. Schvan and S. P. Voinigescu, "57.5GHz bandwidth 4.8Vpp swing linear modulator driver for 64GBaud m-PAM systems," in 2017 IEEE MTT-S International Microwave Symposium (IMS), pp. 130-133, 2017.

[4] R. J. A. Baker, J. Hoffman, P. Schvan and S. P. Voinigescu, "SiGe BiCMOS linear modulator drivers with 4.8-Vpp differential output swing for 120-GBaud applications," in 2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp. 260-263, Jun. 2017.

[5] T. Jyo, M. Nagatani, J. Ozaki, M. Ishikawa and H. Nosaka, "12.3 A 48GHz BW 225mW/ch Linear Driver IC with Stacked Current-Reuse Architecture in 65nm CMOS for Beyond-400Gb/s Coherent Optical Transmitters," in 2020 IEEE International Solid- State Circuits Conference - (ISSCC), pp. 212-214, Feb. 2020.