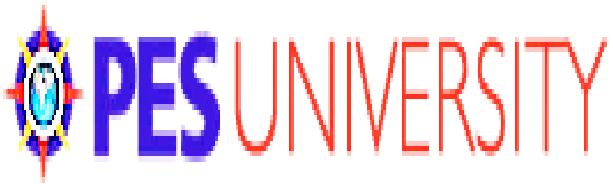

END SEMESTER ASSESSMENT (ESA) B.TECH. (CSE) III SEMESTER

UE20CS206 – DIGITAL DESIGN & COMPUTER ORGANIZATION LABORATORY

PROJECT REPORT

ON

"4 Bit Up /Down Counter"

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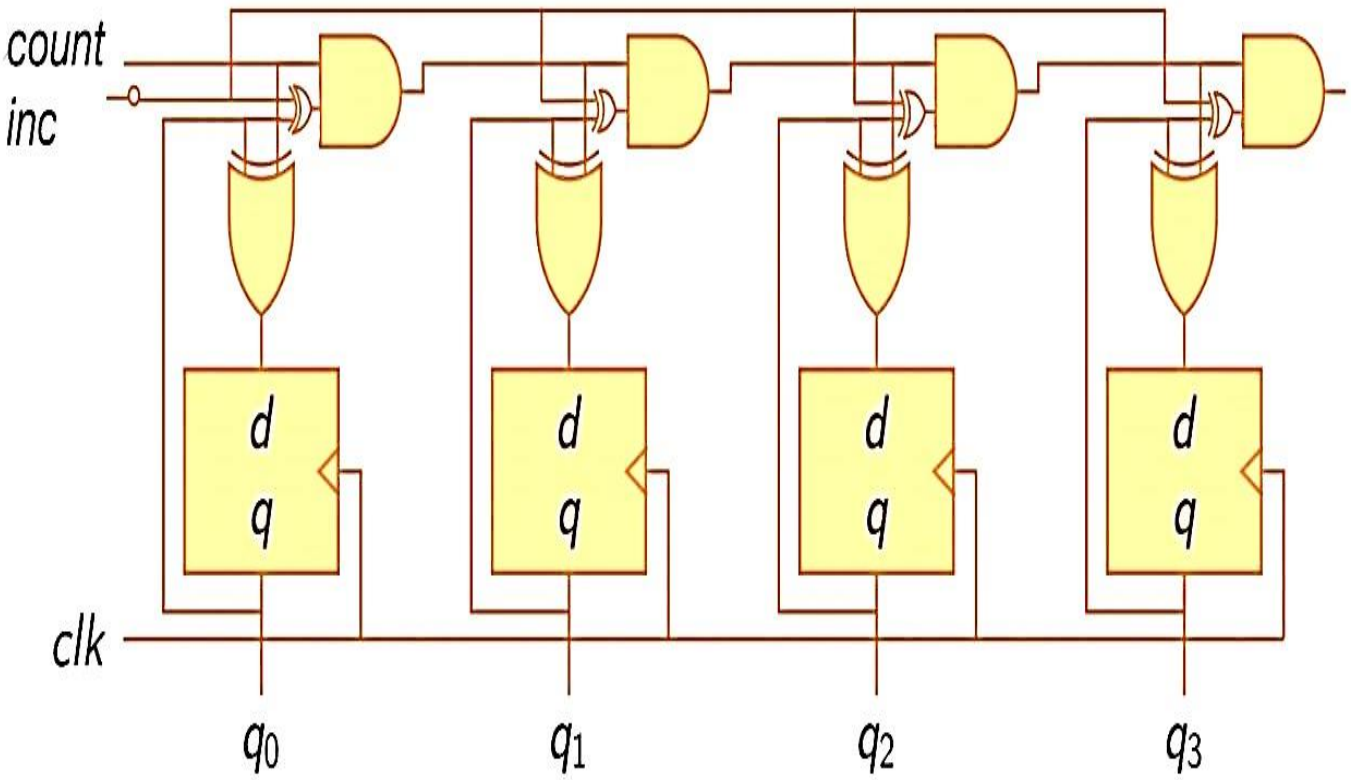
ABSTRACT OF THE PROJECT:

A simple 4-bit up-down counter project made using Icarus Verilog as a part of the Digital Design and Computer Organization Laboratory at PES University.
We have designed an Iverilog program constructing a 4 Bit Up/Down counter which portrays the importance of counters in the calculation process of ALU.

Counters are used in many different applications. Some count up from zero and provide a change in state of output upon reaching a predetermined value (Up counter); others count down from a pre-set value to zero to provide an output state change (Down counter).

However, some counters can operate in both up and down count mode, depending on the state of an up/down count mode input pin. They can be reversed at any point within their count sequence.

CIRCUIT DIAGRAM:



4 Bit Up/Down Counters circuit Diagram using Flip flops.

MAIN VERILOG CODE:

```
module up_counter(input clock, reset, output[3:0] counter);
   reg [3:0] counter_up;                          // Initialise register
//counter_up to find up counter states
   always @(posedge clock or posedge reset)          // Postive edge
//triggered circuit
   begin
if(reset)
begin
            counter_up = 4'd0;                 // If reset==1, set
//counter to 0000
         end
else
begin
            counter_up = counter_up + 4'd1;     // Else, add 0001
//to counter
         end
end
   assign counter = counter_up;                   // Return new value
//of counter
endmodule
module down_counter(input clock, reset, output [3:0] counter);
   reg [3:0] counter_down;                          // Initialise register
//counter_down to find down counter states     always
@(posedge clock or posedge reset)          // Postive edge
//triggered circuit
   begin
if(reset)
begin
            counter_down = 4'hf;            // If reset==1, set counter
//to 1111
         end
else
begin
            counter_down = counter_down - 4'd1; // Else, subtract
//0001 from counter
         end
end
```

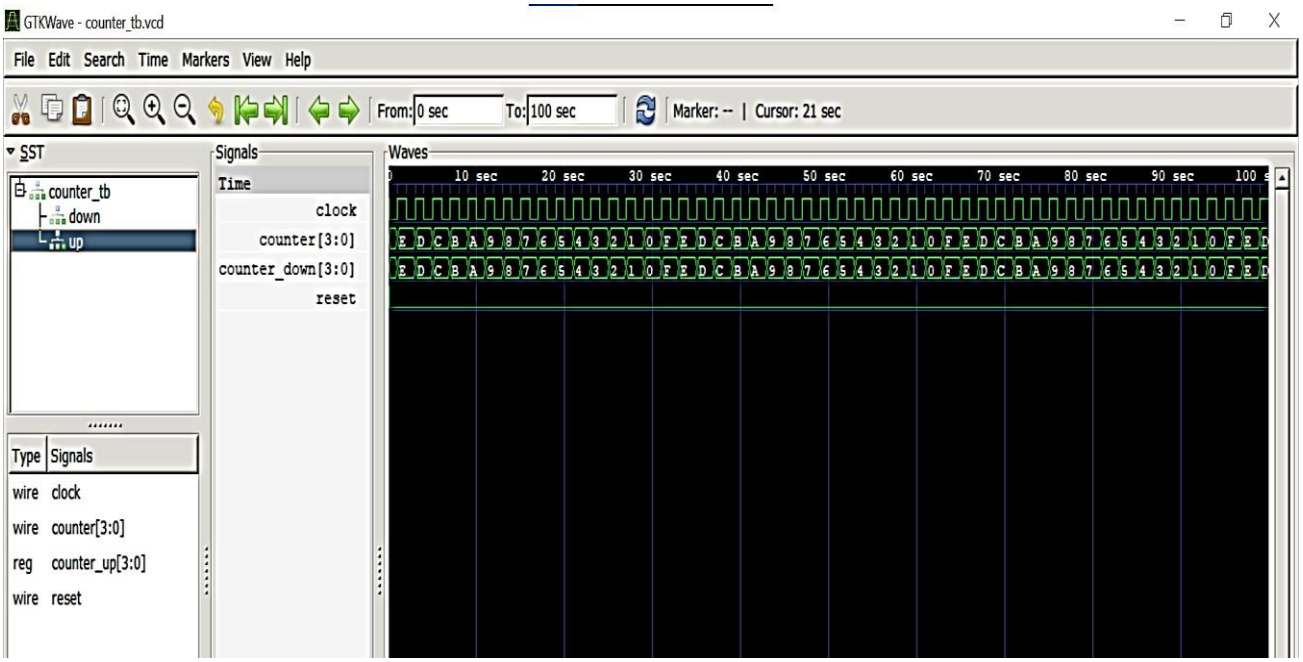
```
    assign counter = counter_down;
// Return new value of counter
endmodule
```

TEST BENCH FILE:

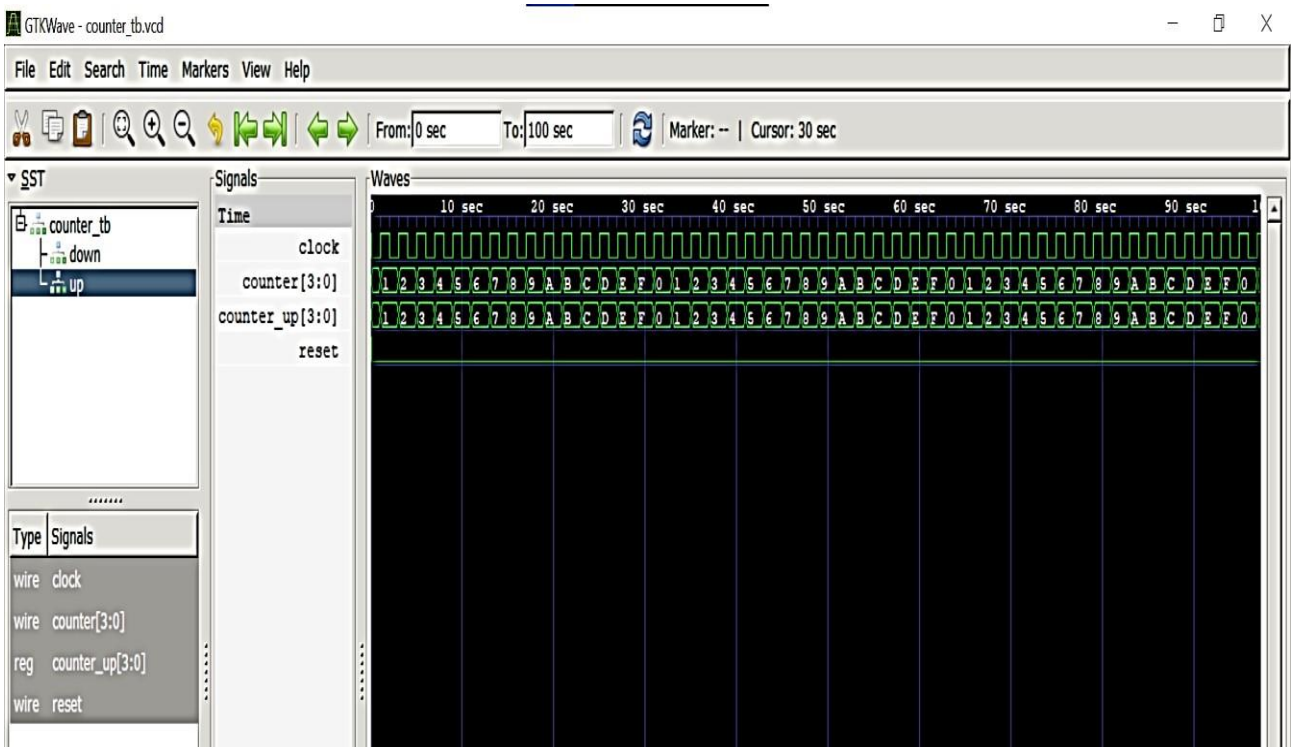
```
module counter_tb();
reg clock, reset;
    wire [3:0] counter_1,counter_2;

    up_counter up(clock, reset, counter_1);
    down_counter down(clock, reset, counter_2);


        initial
begin

        reset = 1;
                #0
                reset = 0;
    end

        initial
begin
        $monitor($time,"clock=%dreset=%d
counter_1[0]=%h",clock,reset,counter_1);
        end

        initial
begin
        clock=0;
repeat(100)             #1
clock=~clock;

    end
initial
        begin
        $dumpfile("counter_tb.vcd");
$dumpvars(0,counter_tb);
    end
endmodule
```

SCREEN SHOT OF THE OUTPUT:

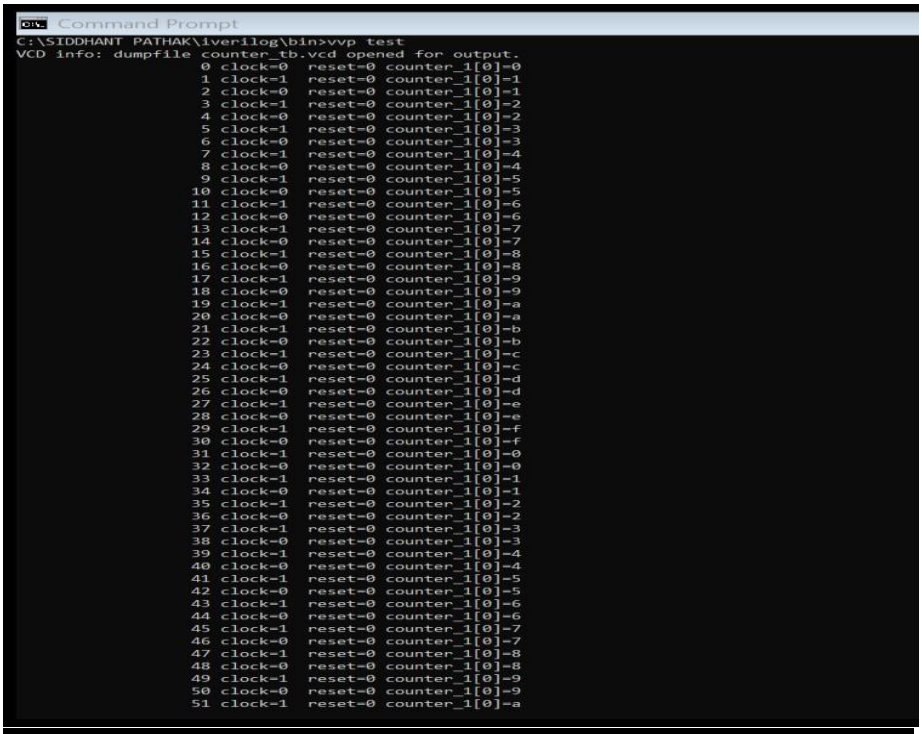
Down counter gtkwave

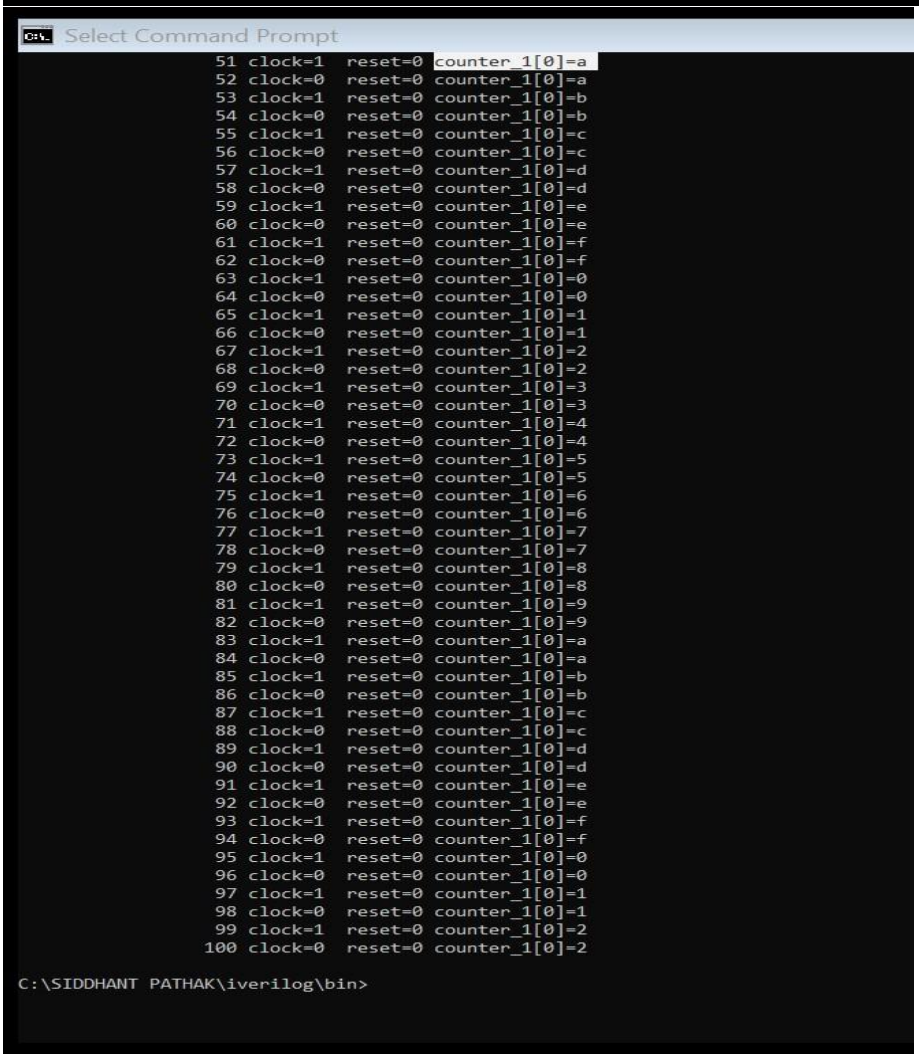


Up counter gtkwave



VVP output:


Command Prompt
C:\SIDDHANT PATHAK\iverilog\bin>vvp test
VCD info: dumpfile counter_tb.vcd opened for output.
0 clock=0 reset=0 counter_1[0]=0
1 clock=1 reset=0 counter_1[0]=1
2 clock=0 reset=0 counter_1[0]=1
3 clock=1 reset=0 counter_1[0]=2
4 clock=0 reset=0 counter_1[0]=2
5 clock=1 reset=0 counter_1[0]=3
6 clock=0 reset=0 counter_1[0]=3
7 clock=1 reset=0 counter_1[0]=4
8 clock=0 reset=0 counter_1[0]=4
9 clock=1 reset=0 counter_1[0]=5
10 clock=0 reset=0 counter_1[0]=5
11 clock=1 reset=0 counter_1[0]=6
12 clock=0 reset=0 counter_1[0]=6
13 clock=1 reset=0 counter_1[0]=7
14 clock=0 reset=0 counter_1[0]=7
15 clock=1 reset=0 counter_1[0]=8
16 clock=0 reset=0 counter_1[0]=8
17 clock=1 reset=0 counter_1[0]=9
18 clock=0 reset=0 counter_1[0]=9
19 clock=1 reset=0 counter_1[0]=a
20 clock=0 reset=0 counter_1[0]=a
21 clock=1 reset=0 counter_1[0]=b
22 clock=0 reset=0 counter_1[0]=b
23 clock=1 reset=0 counter_1[0]=c
24 clock=0 reset=0 counter_1[0]=c
25 clock=1 reset=0 counter_1[0]=d
26 clock=0 reset=0 counter_1[0]=d
27 clock=1 reset=0 counter_1[0]=e
28 clock=0 reset=0 counter_1[0]=e
29 clock=1 reset=0 counter_1[0]=f
30 clock=0 reset=0 counter_1[0]=f
31 clock=1 reset=0 counter_1[0]=0
32 clock=0 reset=0 counter_1[0]=0
33 clock=1 reset=0 counter_1[0]=1
34 clock=0 reset=0 counter_1[0]=1
35 clock=1 reset=0 counter_1[0]=2
36 clock=0 reset=0 counter_1[0]=2
37 clock=1 reset=0 counter_1[0]=3
38 clock=0 reset=0 counter_1[0]=3
39 clock=1 reset=0 counter_1[0]=4
40 clock=0 reset=0 counter_1[0]=4
41 clock=1 reset=0 counter_1[0]=5
42 clock=0 reset=0 counter_1[0]=5
43 clock=1 reset=0 counter_1[0]=6
44 clock=0 reset=0 counter_1[0]=6
45 clock=1 reset=0 counter_1[0]=7
46 clock=0 reset=0 counter_1[0]=7
47 clock=1 reset=0 counter_1[0]=8
48 clock=0 reset=0 counter_1[0]=8
49 clock=1 reset=0 counter_1[0]=9
50 clock=0 reset=0 counter_1[0]=9
51 clock=1 reset=0 counter_1[0]=a


Select Command Prompt
51 clock=1 reset=0 counter_1[0]=a
52 clock=0 reset=0 counter_1[0]=a
53 clock=1 reset=0 counter_1[0]=b
54 clock=0 reset=0 counter_1[0]=b
55 clock=1 reset=0 counter_1[0]=c
56 clock=0 reset=0 counter_1[0]=c
57 clock=1 reset=0 counter_1[0]=d
58 clock=0 reset=0 counter_1[0]=d
59 clock=1 reset=0 counter_1[0]=e
60 clock=0 reset=0 counter_1[0]=e
61 clock=1 reset=0 counter_1[0]=f
62 clock=0 reset=0 counter_1[0]=f
63 clock=1 reset=0 counter_1[0]=0
64 clock=0 reset=0 counter_1[0]=0
65 clock=1 reset=0 counter_1[0]=1
66 clock=0 reset=0 counter_1[0]=1
67 clock=1 reset=0 counter_1[0]=2
68 clock=0 reset=0 counter_1[0]=2
69 clock=1 reset=0 counter_1[0]=3
70 clock=0 reset=0 counter_1[0]=3
71 clock=1 reset=0 counter_1[0]=4
72 clock=0 reset=0 counter_1[0]=4
73 clock=1 reset=0 counter_1[0]=5
74 clock=0 reset=0 counter_1[0]=5
75 clock=1 reset=0 counter_1[0]=6
76 clock=0 reset=0 counter_1[0]=6
77 clock=1 reset=0 counter_1[0]=7
78 clock=0 reset=0 counter_1[0]=7
79 clock=1 reset=0 counter_1[0]=8
80 clock=0 reset=0 counter_1[0]=8
81 clock=1 reset=0 counter_1[0]=9
82 clock=0 reset=0 counter_1[0]=9
83 clock=1 reset=0 counter_1[0]=a
84 clock=0 reset=0 counter_1[0]=a
85 clock=1 reset=0 counter_1[0]=b
86 clock=0 reset=0 counter_1[0]=b
87 clock=1 reset=0 counter_1[0]=c
88 clock=0 reset=0 counter_1[0]=c
89 clock=1 reset=0 counter_1[0]=d
90 clock=0 reset=0 counter_1[0]=d
91 clock=1 reset=0 counter_1[0]=e
92 clock=0 reset=0 counter_1[0]=e
93 clock=1 reset=0 counter_1[0]=f
94 clock=0 reset=0 counter_1[0]=f
95 clock=1 reset=0 counter_1[0]=0
96 clock=0 reset=0 counter_1[0]=0
97 clock=1 reset=0 counter_1[0]=1
98 clock=0 reset=0 counter_1[0]=1
99 clock=1 reset=0 counter_1[0]=2
100 clock=0 reset=0 counter_1[0]=2
C:\SIDDHANT PATHAK\iverilog\bin>