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Shuvro Chowdhury

Postdoctoral Scholar
Department of Electrical & Computer Engineering (ECE)
University of California Santa Barbara
Santa Barbara, CA 93106, USA

Curriculum Vitae

Objective

Highly passionate researcher in the field of nanoelectronics and nanotechnology with
- specialty in probabilistic computing / machine learning (ML), quantum computing and modeling and simulation of nanoelectronic devices,
- proficiency in various programming languages specially in C/C++, Python and MATLAB

and looking for research positions in academia.

Academic Qualification

2016–2022 **Doctor of Philosophy in Electrical & Electronics Engineering**, *Purdue University*, IN-47907, USA, *Current CGPA – **4.00** in scale of **4.00**.*

2011–2014 **Master of Science in Electrical & Electronic Engineering**, *Bangladesh University of Engineering & Technology*, Dhaka-1000, Bangladesh, *CGPA – **3.92** in scale of **4.00**.*

2006–2011 **Bachelor of Science in Electrical & Electronic Engineering**, *Bangladesh University of Engineering & Technology*, Dhaka-1000, Bangladesh, *CGPA – **3.96428** in scale of **4.00**.*
Rank– **6**$^{\text{th}}$ among 134 Students of the department.

2003–2005 **Higher Secondary Certificate**, *Notre Dame College*, Dhaka, Bangladesh, *GPA – **5.00** in scale of **5.00**.*

2001–2003 **Secondary School Certificate**, *Rangpur Cadet College*, Rangpur, Bangladesh, *GPA – **5.00** in scale of **5.00**.*

Fields of Research Interest

- Probabilistic and neuromorphic computing
- Quantum computing
- Machine learning
- Nanoscale device modeling and simulation
- Hardware acceleration

Professional Experience

2022–present **Postdoctoral Scholar**, *Supervisor: Prof. Kerem Y. Camsari*, ECE, University of California Santa Barbara.

2016–present **Graduate Research Assistant**, *Supervisor: Prof. Supriyo Datta*, ECE, Purdue University.

2020–present **Graduate Teaching Assistant** – *Fundamentals of Current Flow, Introduction to Quantum transport, Boltzmann Law: Physics to Computing* – ECE, Purdue University.

2015–2016 **Assistant Professor**, *Department of Electrical and Electronic Engineering (EEE)*, Bangladesh University of Engineering and Technology (BUET), Dhaka-1000, Bangladesh.

2011–2015 **Lecturer**, *Department of EEE*, BUET, Dhaka-1000, Bangladesh.

Courses Taught **Theory** – *Solid State Devices, Electrical Properties of Materials, Microprocessor and Interfacing, Electrical Circuits I, Electrical and Electronic Technology* – 60 undergraduate students per class.

Laboratory – *Control System Laboratory, Microprocessor and Interfacing Laboratory, Electrical Circuit Simulation Laboratory, Electronic Circuit Simulation Laboratory, Communication Laboratory, Measurement and Instrumentation Laboratory* – 30 undergraduate students per class.

Research Experience

- ***Probabilistic computing***
  - Developing methods and algorithms to emulate quantum interference with generalized Ising machines.
  - Proposed stochastic nanomagnet based probabilistic hardware to emulate sign-problem free quantum Hamiltonians.
- ***Nanoscale Semiconductor Devices***
  - Developed a surface potential based analytical model for long-channel double-gate junctionless field effect transistor (Masters thesis).
  - Developed a one-dimensional Schrödinger-Poisson solver for ultra-thin SOI MOSFET and a two-dimensional NEGF based device simulator for double-gate MOSFET with high-κ gate oxide (undergraduate thesis).
  - Analyzed temperature and wave function penetration effects in nanoscale double-gate MOSFETs (undergraduate thesis).
- ***Multi-Valued Logic and Quantum Computation***
  - Developed a method of synthesizing Ternary Galois Field (GF(3)) based reversible/quantum logic circuits without any ancillary trits/qutrits
  - Proposed a realization of multi-input ternary Toffoli gate and square functions of GF(3) variables in the absence of ancillary qutrits.
  - Developed a realization of square operation for quantum ternary logic using basic quantum ternary gates and a square-multiplier unit.

Programming and Software Skills

Advanced	C/C++, MATLAB, Assembly Language, ADOBE Illustrator, Octave, Proteus, Circuit Maker, Microsoft Office Visio, OriginPro, Microsoft Office, Libre Office, LaTeX and CAD tools like ORCAD PSPICE & Capture, HSPICE, Quartus II.
Intermediate	Python, C#, Java, Microwind & Dsch, CYMBASE, CYMFLOW, Vivado, Fedora, Ubuntu.
Basic	Macromedia Flash, Simulink, COMSOL, AutoCAD

Technical Shortcourses Instructed

- **Training on Computer Interfacing and Embedded System**, organized by – IEEE GOLD Bangladesh Section & ITRRC of Jagannath University, Dhaka, Bangladesh in 2013.
- **Workshop on LaTeX and Scientific Writing**, organized by – IEEE GOLD Bangladesh Section in 2013.
- **Short Course on FPGA Digital Logic Design**, organized by – IEEE ED/SSCS Bangladesh Chapter in 2013.
- Along with two other colleagues, jointly designed **'ATMEGA32 Development Kit'** - an ATMEGA32 microcontroller based trainer board.

Selected Peer-reviewed Publications

Journal Papers:

1. **Shuvro Chowdhury**, Kerem Y. Camsari, and Supriyo Datta, Accelerated quantum Monte Carlo with probabilistic computers in *Communications Physics*, 6, 85 (2023). https://doi.org/10.1038/s42005-023-01202-3
2. **S. Chowdhury** *et al.*, A full-stack view of probabilistic computing with p-bits: devices, architectures and algorithms in *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, doi: 10.1109/JXCDC.2023.3256981.
3. **Shuvro Chowdhury**, Kerem Y. Camsari, and Supriyo Datta, Emulating Qunatum interference with Generalised Ising Machines (https://arxiv.org/abs/2007.07379).

4. Kerem Y. Camsari, **Shuvro Chowdhury**, and Supriyo Datta, Scalable Emulation of Sign-Problem–Free Hamiltonians with Room-Temperature ***p***-bits, Phys. Rev. Applied 12, 034061 – Published 30 September 2019.
5. **S. Chowdhury**, E. Farzana, R. Ahmed, A. T. M. G. Sarwar, and M. Z. R. Khan,"C-V Characterization and Analysis of Temperature and Channel Thickness Effects on Threshold Voltage of Ultra-thin SOI MOSFET by Self-Consistent Model," *World Academy of Science, Engineering and Technology,* vol. 45, no. 60, pp. 332-337, September 2010. [Online]. Available: http://www.waset.org/journals/waset/v45/v45- 60.pdf
6. E. Farzana, **S. Chowdhury**, R. Ahmed, and M. Z. Rahman Khan, "Performance Analysis of Nanoscale Double Gate MOSFETs with High-κ Gate Stack," *Applied Mechanics and Materials,* vol. 110-116, pp. 1892-1899, October 2011. [Online]. Available: http://www.scientific.net/AMM.110-116.1892
7. E. Farzana, **S. Chowdhury**, R. Ahmed, and M. Khan, "Analysis of temperature and wave function penetration effects in nanoscale double-gate mosfets," *Applied Nanoscience*, pp. 1-9, 2012, 10.1007/s13204-012-0090-z. [Online]. Available: http://dx.doi.org/10.1007/s13204-012-0090-z

Conference Papers:

1. **S. Chowdhury**, S. Datta and K. Y. Camsari, "A Probabilistic Approach to Quantum Inspired Algorithms," 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2019, pp. 37.5.1-37.5.4.
2. **Chowdhury, S.**; Khan, M.Z.R., "Surface potential modeling of Junctionless Double Gate MOSFETs using gradual depletion approximation," in Electrical and Computer Engineering (ICECE), 2014 International Conference on , vol., no., pp.108-111, 20-22 Dec. 2014
3. A. Grimaldi *et al.*, Experimental evaluation of simulated quantum annealing with MTJ-augmented p-bits *2022 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2022, pp. 22.4.1-22.4.4, doi: 10.1109/IEDM45625.2022.10019530.
4. M. M. M. Khan, A. K. Biswas, **S. Chowdhury**, M. Hasan, and A. I. Khan, "Synthesis of GF(3) Based Reversible/Quantum Logic Circuits without Garbage Output," *Multiple-Valued Logic, IEEE International Symposium on,* vol. 0, pp. 98-102, 2009.
5. A. Biswas, **S. Chowdhury**, M. Khan, M. Hasan, and A. Khan, "Some basic ternary operations using toffoli gates along with the cost of implementation." in *Multiple-Valued Logic (ISMVL), 2011 41st IEEE International Symposium on*, may 2011, pp. 142-146.
6. M. Khan, A. Biswas, **S. Chowdhury**, M. Tanzid, K. Mohsin, M. Hasan, and A. Khan,"Quantum realization of some quaternary circuits," in *TENCON 2008 - 2008 IEEE Region 10 Conference,* nov. 2008, pp. 1.

Book Chapters:

1. Kerem Y. Camsari, **Shuvro Chowdhury**, and Supriyo Datta, *The Non-Equilibrium Green Function (NEGF) Method*, accepted in *Springer Handbook of Semiconductor Devices*, January 2021.

Relevant Coursework

Masters Laser Theory, MOS Devices, Compound Semiconductor Devices, VLSI Technology and device modeling

Undergrduate Semiconductor Device Theory, Solid State Devices, Compound Semiconductor and Hetero-junction Devices, Analog Integrated Circuits, VLSI II, Processing and Fabrication Technology

Professional Affiliations

Member **Institute of Electrical and Electronics Engineers (IEEE)**.

Member **IEEE Electron Devices and Solid-State Circuits Society (ED/SSCS)**, *Bangladesh chapter.*

Member **Board of Undergraduate Studies**, *Dept. of EEE*, Bangladesh University of Engineering and Technology.

Member **Bureau of Research, Testing and Consultation**, *Dept. of EEE*, Bangladesh University of Engineering and Technology.

Synergistic Activities

2014 **Member**, *Technical Committee*, 8th International Conference on Electrical and Computer Engineering (ICECE).

2013 **Vice Chair**, *GOLD Affinity Group*, IEEE Bangladesh Section.

2013 **Secretary**, *IEEE Electron Devices and Solid-State Circuits Society*, Bangladesh Chapter.

2012 **Secretary and Treasurer**, *IEEE Electron Devices and Solid-State Circuits Society (ED/SSCS)*, Bangladesh Chapter.

2012 **Treasurer**, *GOLD Affinity Group*, IEEE Bangladesh Section.

2012 **Member**, *Technical Committee*, 7th International Conference on Electrical and Computer Engineering (ICECE).

Accolades

- **3rd Prize** in Electronics group for undergraduate research work, EEE Ungraduate Project Workshop (EUProW) 2011, organized by Dept. of EEE, Bangladesh University of Engineering and Technology.
- **University Merit Scholarship** for good results in term examinations.
- **University Dean's List Award** for 3.75+ CGPA in all levels.
- **Dhaka Board Scholarship** for obtaining GPA 5.00 in H.S.C.

References

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