4000	MOVC R0, #0	
4004	MOVC R1, #1	
4008	MOVC R2, #2	
4012	MOVC R4, #4	
4016	MOVC R5, #5	
4020	MOVC R6, #1000	
4024	MOVC R7, #4028	
4028	BZ #28	/* goes to HALT when loop ends */
4032	MUL R3, R2, R2	
4036	STR R3, R6, R0	
4040	ADD R6, R6, R4	
4044	ADD R2, R2, R1	
4044	SUB R5, R5, R1	/*sets Z flag if result is zero */
4048	JUMP R7, #0	
4052	HALT	

SOLUTION

STATE OF ARCHITECTURAL REGISTER AND DATA MEMORY:

MOVC R0, #0		R0	0	D[1000]	4	
MOVC R1, #1		R1	1	D[1004]	9	
MOVC R2, #2		R2	7	D[1008]	16	
MOVC R4, #4		R3	36	D[1012]	25	
MOVC R5, #5		R4	4	D[1016]	36	
MOVC R6, #1000		R5	0			
MOVC R7, #4028		R6	1020			
BZ #28		R7	4028			
MUL R3, R2, R2		R8	0			
STR R3, R6, R0		R9	0			
ADD R6, R6, R4		R10	0			
ADD R2, R2, R1		R11	0			
SUB R5, R5, R1		R12	0			
JUMP R7, #0		R13	0			
HALT		R14	0			
		R15	0			
		R16	0			