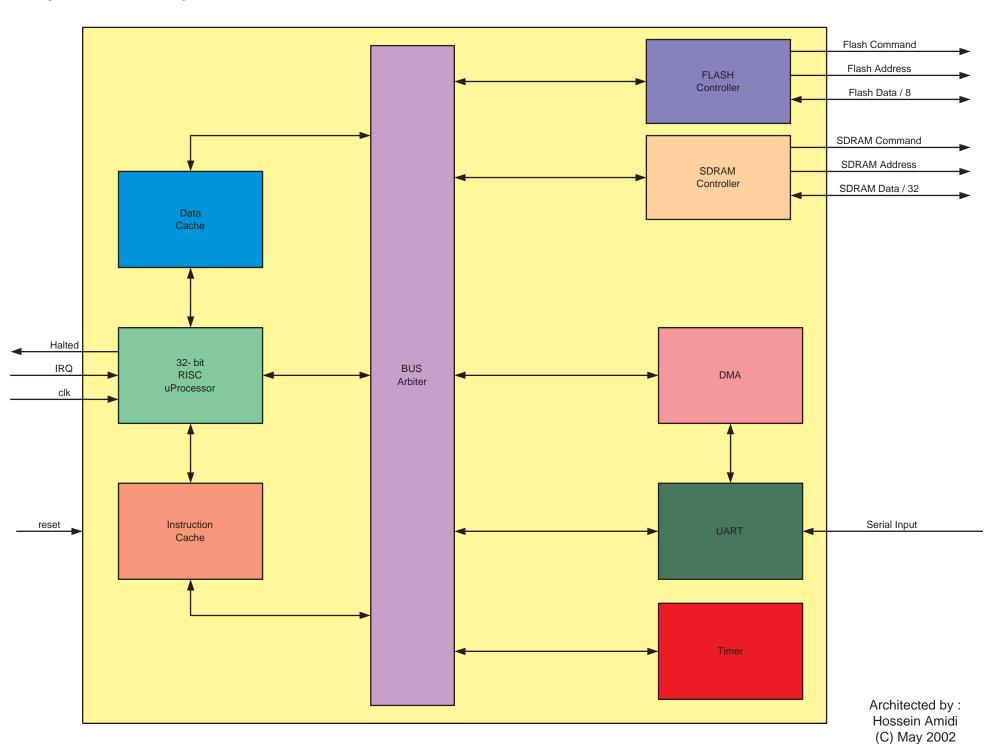
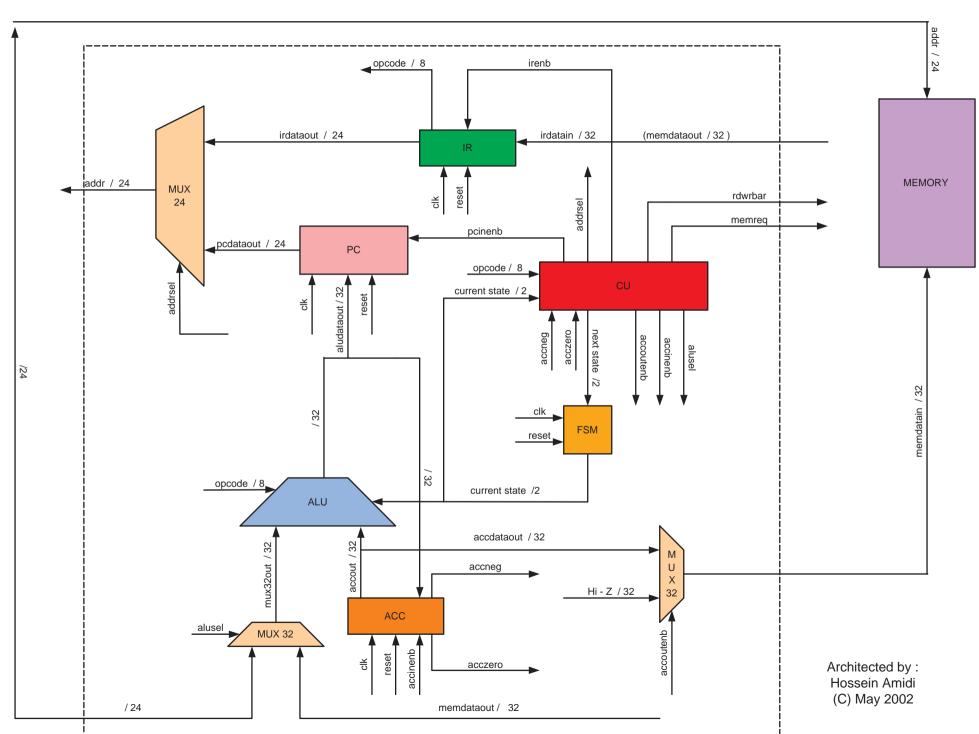
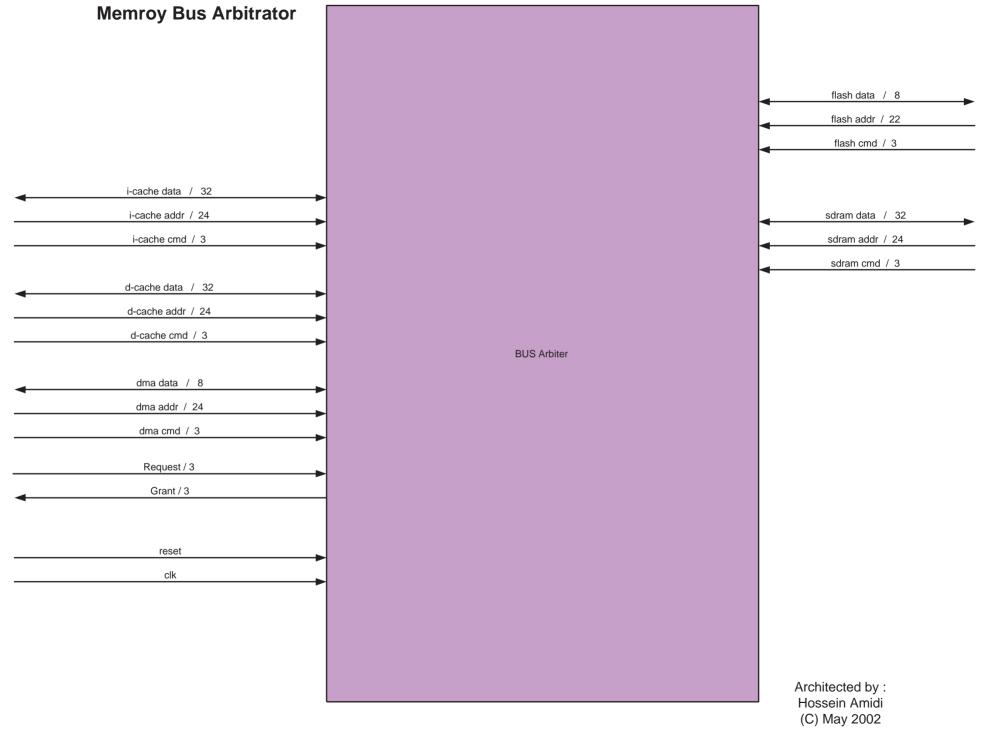
System On a Chip

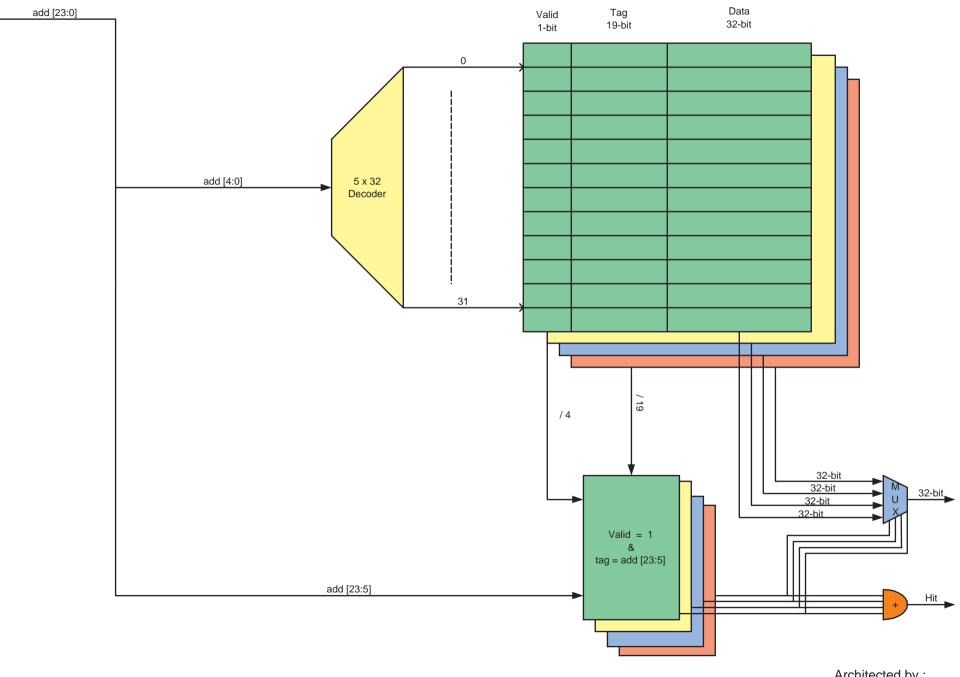


32-bit uRISC Processor

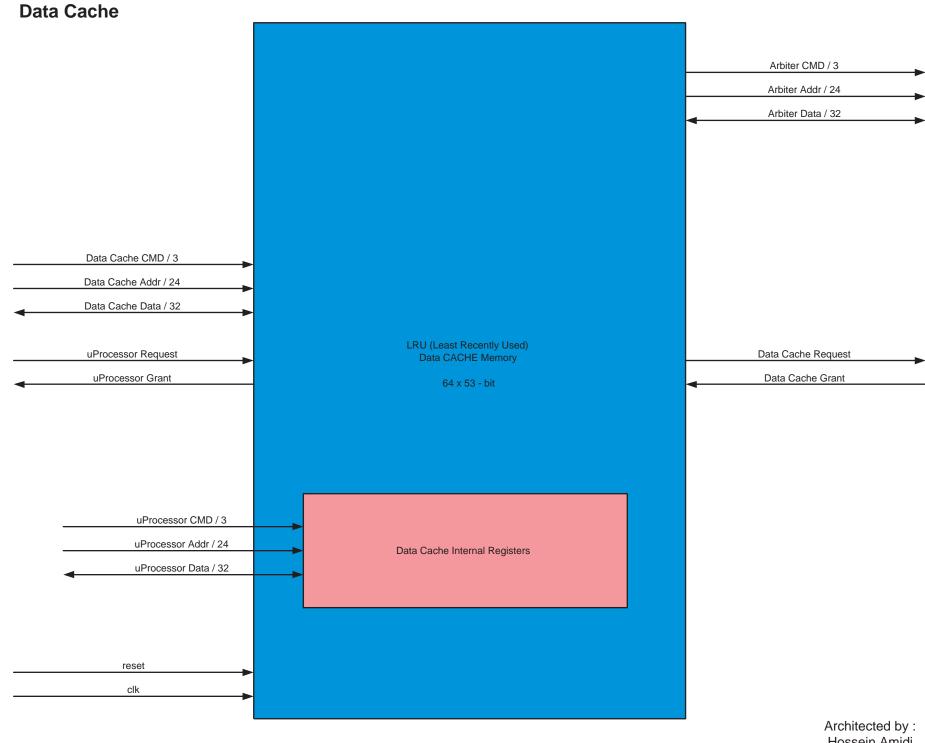


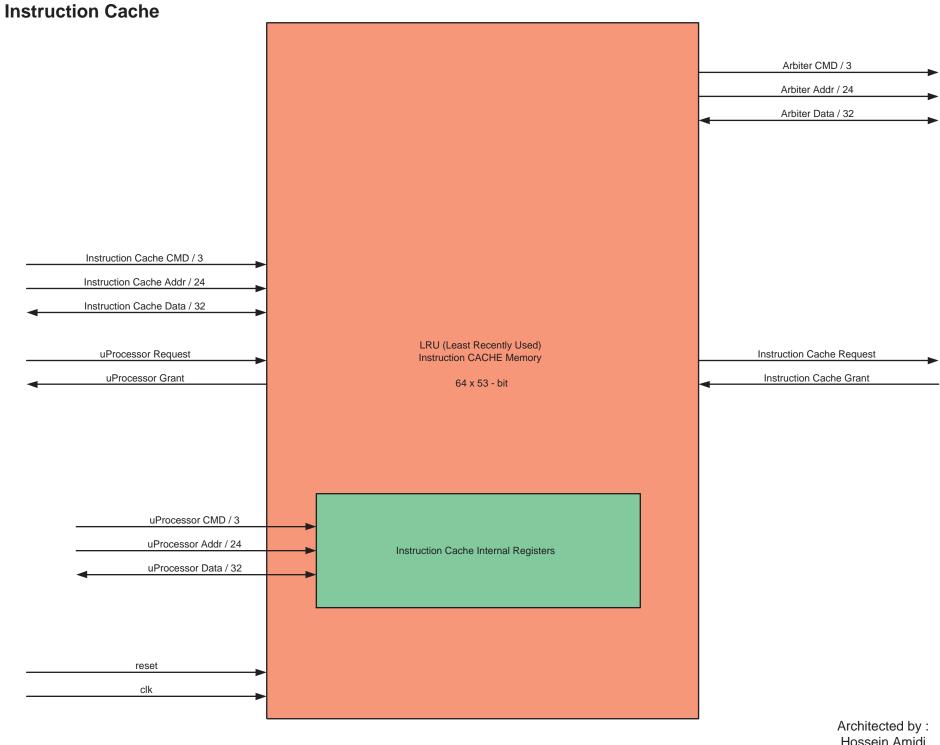


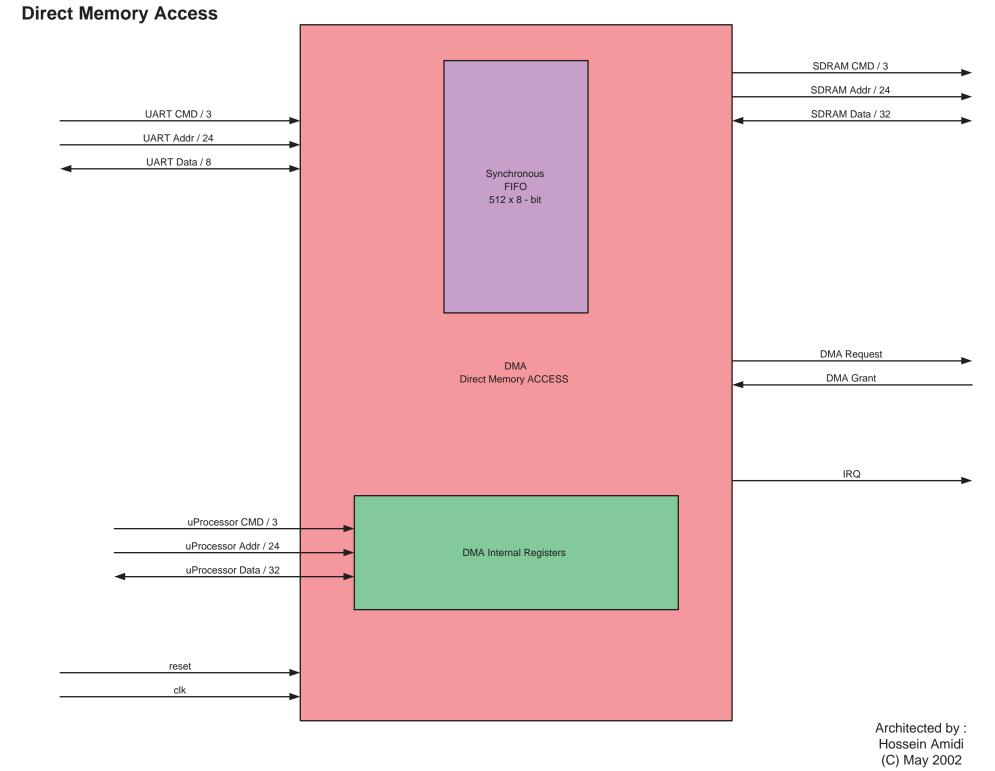
4-Way LRU Cache

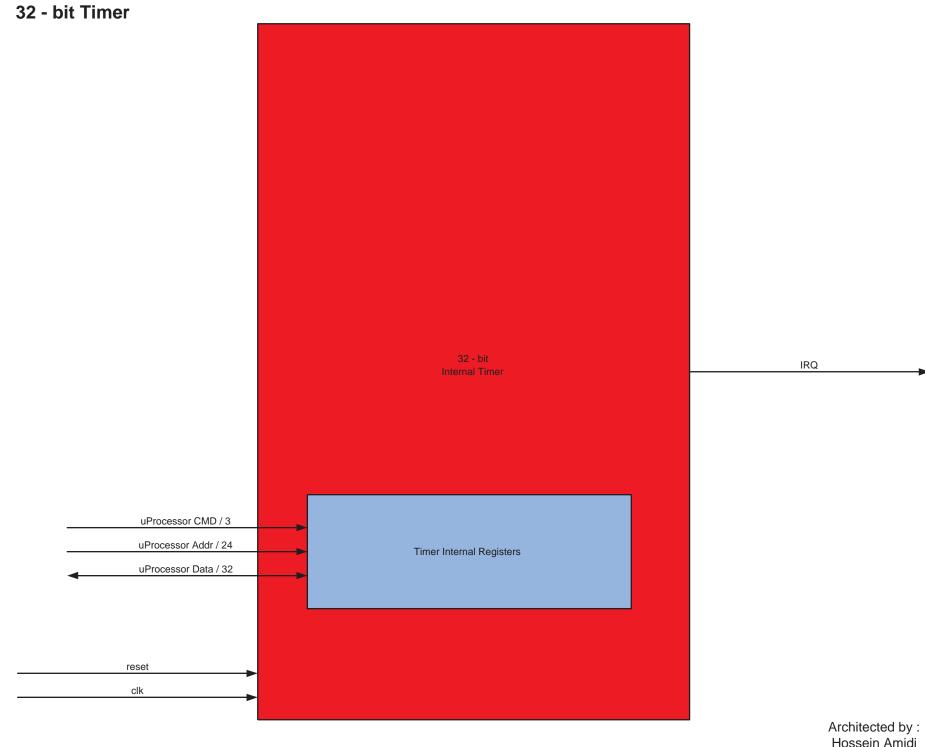


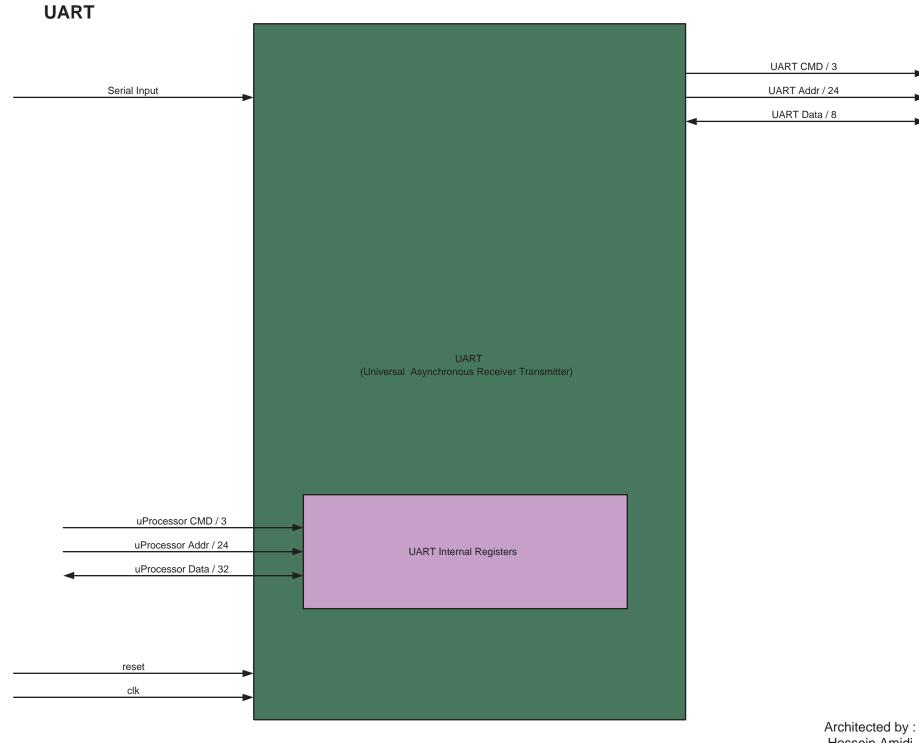
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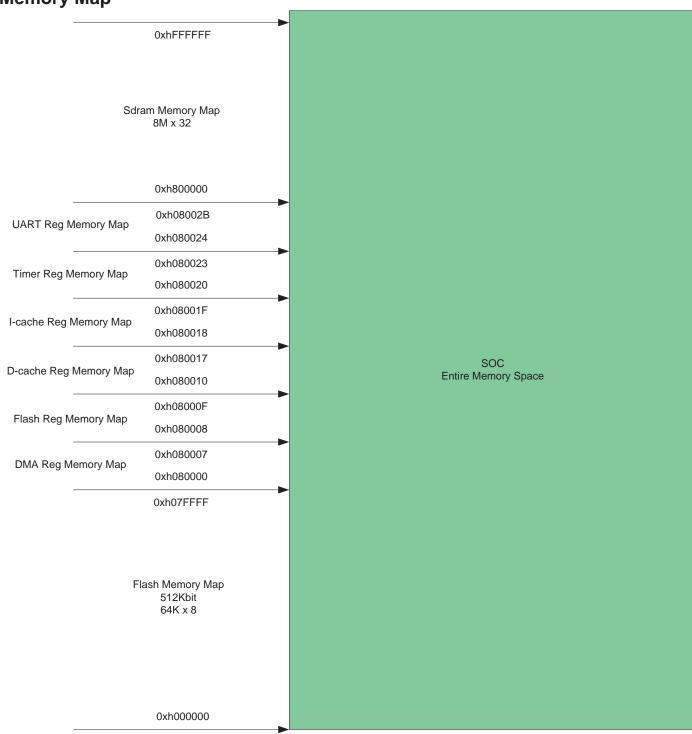
SDRAM Controller SDRAM CMD / 3 add [12 : 0] SDRAM Addr / 24 ba [1:0] SDRAM Data / 32 cs[1:0] clk cke ras cas we dm [2:0] SDRAM Controller IRQ uProcessor CMD / 3 uProcessor Addr / 24 SDRAM Internal Registers uProcessor Data / 32 reset clk Architected by: Hossein Amidi

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Flash Controller FLASH CMD / 3 data [7 : 0] FLASH Addr / 22 cle FLASH Data / 8 ale се re we wp rb FLASH Controller IRQ uProcessor CMD / 3 uProcessor Addr / 24 **FLASH Internal Registers** uProcessor Data / 32 reset clk Architected by: Hossein Amidi

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Memory Map



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