```
## This file is a general
.xdc for the Arty A7-100
Rev. D and Rev. E

## To use it in a project:

## - uncomment the lines corresponding to used pins

## - rename the used ports (in each line, after
get_ports) according to the top level signal names in
the project


## Clock signal

#set_property -dict { PACKAGE_PIN E3    IOSTANDARD
LVCMOS33 } [get_ports { CLK100MHZ }];
#IO_L12P_T1_MRCC_35 Sch=gclk[100]
#create_clock -add -name sys_clk_pin -period 10.00
-waveform {0 5} [get_ports { CLK100MHZ }];


## Switches

#set_property -dict { PACKAGE_PIN A8    IOSTANDARD
LVCMOS33 } [get_ports { sw[0] }]; #IO_L12N_T1_MRCC_16
Sch=sw[0]
#set_property -dict { PACKAGE_PIN C11   IOSTANDARD
LVCMOS33 } [get_ports { sw[1] }]; #IO_L13P_T2_MRCC_16
Sch=sw[1]
#set_property -dict { PACKAGE_PIN C10   IOSTANDARD
LVCMOS33 } [get_ports { sw[2] }]; #IO_L13N_T2_MRCC_16
Sch=sw[2]
#set_property -dict { PACKAGE_PIN A10   IOSTANDARD
LVCMOS33 } [get_ports { sw[3] }]; #IO_L14P_T2_SRCC_16
Sch=sw[3]


## RGB LEDs

#set_property -dict { PACKAGE_PIN E1    IOSTANDARD
LVCMOS33 } [get_ports { led0_b }]; #IO_L18N_T2_35
Sch=led0_b
#set_property -dict { PACKAGE_PIN F6    IOSTANDARD
LVCMOS33 } [get_ports { led0_g }]; #IO_L19N_T3_VREF_35
Sch=led0_g
```

```
#set_property -dict { PACKAGE_PIN G6    IOSTANDARD
LVCMOS33 } [get_ports { led0_r }]; #IO_L19P_T3_35
Sch=led0_r
#set_property -dict { PACKAGE_PIN G4    IOSTANDARD
LVCMOS33 } [get_ports { led1_b }]; #IO_L20P_T3_35
Sch=led1_b
#set_property -dict { PACKAGE_PIN J4    IOSTANDARD
LVCMOS33 } [get_ports { led1_g }]; #IO_L21P_T3_DQS_35
Sch=led1_g
#set_property -dict { PACKAGE_PIN G3    IOSTANDARD
LVCMOS33 } [get_ports { led1_r }]; #IO_L20N_T3_35
Sch=led1_r
#set_property -dict { PACKAGE_PIN H4    IOSTANDARD
LVCMOS33 } [get_ports { led2_b }]; #IO_L21N_T3_DQS_35
Sch=led2_b
#set_property -dict { PACKAGE_PIN J2    IOSTANDARD
LVCMOS33 } [get_ports { led2_g }]; #IO_L22N_T3_35
Sch=led2_g
#set_property -dict { PACKAGE_PIN J3    IOSTANDARD
LVCMOS33 } [get_ports { led2_r }]; #IO_L22P_T3_35
Sch=led2_r
#set_property -dict { PACKAGE_PIN K2    IOSTANDARD
LVCMOS33 } [get_ports { led3_b }]; #IO_L23P_T3_35
Sch=led3_b
#set_property -dict { PACKAGE_PIN H6    IOSTANDARD
LVCMOS33 } [get_ports { led3_g }]; #IO_L24P_T3_35
Sch=led3_g
#set_property -dict { PACKAGE_PIN K1    IOSTANDARD
LVCMOS33 } [get_ports { led3_r }]; #IO_L23N_T3_35
Sch=led3_r


## LEDs

#set_property -dict { PACKAGE_PIN H5    IOSTANDARD
LVCMOS33 } [get_ports { led[0] }]; #IO_L24N_T3_35
Sch=led[4]
#set_property -dict { PACKAGE_PIN J5    IOSTANDARD
LVCMOS33 } [get_ports { led[1] }]; #IO_25_35 Sch=led[5]
#set_property -dict { PACKAGE_PIN T9    IOSTANDARD
LVCMOS33 } [get_ports { led[2] }];
#IO_L24P_T3_A01_D17_14 Sch=led[6]
#set_property -dict { PACKAGE_PIN T10   IOSTANDARD
LVCMOS33 } [get_ports { led[3] }];
#IO_L24N_T3_A00_D16_14 Sch=led[7]
```

```
## Buttons

#set_property -dict { PACKAGE_PIN D9    IOSTANDARD
LVCMOS33 } [get_ports { btn[0] }]; #IO_L6N_T0_VREF_16
Sch=btn[0]
#set_property -dict { PACKAGE_PIN C9    IOSTANDARD
LVCMOS33 } [get_ports { btn[1] }]; #IO_L11P_T1_SRCC_16
Sch=btn[1]
#set_property -dict { PACKAGE_PIN B9    IOSTANDARD
LVCMOS33 } [get_ports { btn[2] }]; #IO_L11N_T1_SRCC_16
Sch=btn[2]
#set_property -dict { PACKAGE_PIN B8    IOSTANDARD
LVCMOS33 } [get_ports { btn[3] }]; #IO_L12P_T1_MRCC_16
Sch=btn[3]


## Pmod Header JA

#set_property -dict { PACKAGE_PIN G13   IOSTANDARD
LVCMOS33 } [get_ports { ja[0] }]; #IO_0_15 Sch=ja[1]
#set_property -dict { PACKAGE_PIN B11   IOSTANDARD
LVCMOS33 } [get_ports { ja[1] }]; #IO_L4P_T0_15
Sch=ja[2]
#set_property -dict { PACKAGE_PIN A11   IOSTANDARD
LVCMOS33 } [get_ports { ja[2] }]; #IO_L4N_T0_15
Sch=ja[3]
#set_property -dict { PACKAGE_PIN D12   IOSTANDARD
LVCMOS33 } [get_ports { ja[3] }]; #IO_L6P_T0_15
Sch=ja[4]
#set_property -dict { PACKAGE_PIN D13   IOSTANDARD
LVCMOS33 } [get_ports { ja[4] }]; #IO_L6N_T0_VREF_15
Sch=ja[7]
#set_property -dict { PACKAGE_PIN B18   IOSTANDARD
LVCMOS33 } [get_ports { ja[5] }]; #IO_L10P_T1_AD11P_15
Sch=ja[8]
#set_property -dict { PACKAGE_PIN A18   IOSTANDARD
LVCMOS33 } [get_ports { ja[6] }]; #IO_L10N_T1_AD11N_15
Sch=ja[9]
#set_property -dict { PACKAGE_PIN K16   IOSTANDARD
LVCMOS33 } [get_ports { ja[7] }]; #IO_25_15 Sch=ja[10]


## Pmod Header JB
```

```
#set_property -dict { PACKAGE_PIN E15   IOSTANDARD
LVCMOS33 } [get_ports { jb[0] }]; #IO_L11P_T1_SRCC_15
Sch=jb_p[1]
#set_property -dict { PACKAGE_PIN E16   IOSTANDARD
LVCMOS33 } [get_ports { jb[1] }]; #IO_L11N_T1_SRCC_15
Sch=jb_n[1]
#set_property -dict { PACKAGE_PIN D15   IOSTANDARD
LVCMOS33 } [get_ports { jb[2] }]; #IO_L12P_T1_MRCC_15
Sch=jb_p[2]
#set_property -dict { PACKAGE_PIN C15   IOSTANDARD
LVCMOS33 } [get_ports { jb[3] }]; #IO_L12N_T1_MRCC_15
Sch=jb_n[2]
#set_property -dict { PACKAGE_PIN J17   IOSTANDARD
LVCMOS33 } [get_ports { jb[4] }]; #IO_L23P_T3_FOE_B_15
Sch=jb_p[3]
#set_property -dict { PACKAGE_PIN J18   IOSTANDARD
LVCMOS33 } [get_ports { jb[5] }]; #IO_L23N_T3_FWE_B_15
Sch=jb_n[3]
#set_property -dict { PACKAGE_PIN K15   IOSTANDARD
LVCMOS33 } [get_ports { jb[6] }]; #IO_L24P_T3_RS1_15
Sch=jb_p[4]
#set_property -dict { PACKAGE_PIN J15   IOSTANDARD
LVCMOS33 } [get_ports { jb[7] }]; #IO_L24N_T3_RS0_15
Sch=jb_n[4]


## Pmod Header JC

#set_property -dict { PACKAGE_PIN U12   IOSTANDARD
LVCMOS33 } [get_ports { jc[0] }];
#IO_L20P_T3_A08_D24_14 Sch=jc_p[1]
#set_property -dict { PACKAGE_PIN V12   IOSTANDARD
LVCMOS33 } [get_ports { jc[1] }];
#IO_L20N_T3_A07_D23_14 Sch=jc_n[1]
#set_property -dict { PACKAGE_PIN V10   IOSTANDARD
LVCMOS33 } [get_ports { jc[2] }]; #IO_L21P_T3_DQS_14
Sch=jc_p[2]
#set_property -dict { PACKAGE_PIN V11   IOSTANDARD
LVCMOS33 } [get_ports { jc[3] }];
#IO_L21N_T3_DQS_A06_D22_14 Sch=jc_n[2]
#set_property -dict { PACKAGE_PIN U14   IOSTANDARD
LVCMOS33 } [get_ports { jc[4] }];
#IO_L22P_T3_A05_D21_14 Sch=jc_p[3]
```

```
#set_property -dict { PACKAGE_PIN V14   IOSTANDARD
LVCMOS33 } [get_ports { jc[5] }];
#IO_L22N_T3_A04_D20_14 Sch=jc_n[3]
#set_property -dict { PACKAGE_PIN T13   IOSTANDARD
LVCMOS33 } [get_ports { jc[6] }];
#IO_L23P_T3_A03_D19_14 Sch=jc_p[4]
#set_property -dict { PACKAGE_PIN U13   IOSTANDARD
LVCMOS33 } [get_ports { jc[7] }];
#IO_L23N_T3_A02_D18_14 Sch=jc_n[4]


## Pmod Header JD

#set_property -dict { PACKAGE_PIN D4    IOSTANDARD
LVCMOS33 } [get_ports { jd[0] }]; #IO_L11N_T1_SRCC_35
Sch=jd[1]
#set_property -dict { PACKAGE_PIN D3    IOSTANDARD
LVCMOS33 } [get_ports { jd[1] }]; #IO_L12N_T1_MRCC_35
Sch=jd[2]
#set_property -dict { PACKAGE_PIN F4    IOSTANDARD
LVCMOS33 } [get_ports { jd[2] }]; #IO_L13P_T2_MRCC_35
Sch=jd[3]
#set_property -dict { PACKAGE_PIN F3    IOSTANDARD
LVCMOS33 } [get_ports { jd[3] }]; #IO_L13N_T2_MRCC_35
Sch=jd[4]
#set_property -dict { PACKAGE_PIN E2    IOSTANDARD
LVCMOS33 } [get_ports { jd[4] }]; #IO_L14P_T2_SRCC_35
Sch=jd[7]
#set_property -dict { PACKAGE_PIN D2    IOSTANDARD
LVCMOS33 } [get_ports { jd[5] }]; #IO_L14N_T2_SRCC_35
Sch=jd[8]
#set_property -dict { PACKAGE_PIN H2    IOSTANDARD
LVCMOS33 } [get_ports { jd[6] }]; #IO_L15P_T2_DQS_35
Sch=jd[9]
#set_property -dict { PACKAGE_PIN G2    IOSTANDARD
LVCMOS33 } [get_ports { jd[7] }]; #IO_L15N_T2_DQS_35
Sch=jd[10]


## USB-UART Interface

#set_property -dict { PACKAGE_PIN D10   IOSTANDARD
LVCMOS33 } [get_ports { uart_rxd_out }];
#IO_L19N_T3_VREF_16 Sch=uart_rxd_out
```

```
#set_property -dict { PACKAGE_PIN A9    IOSTANDARD
LVCMOS33 } [get_ports { uart_txd_in }];
#IO_L14N_T2_SRCC_16 Sch=uart_txd_in


## ChipKit Outer Digital Header

#set_property -dict { PACKAGE_PIN V15   IOSTANDARD
LVCMOS33 } [get_ports { ck_io0  }];
#IO_L16P_T2_CSI_B_14 Sch=ck_io[0]
#set_property -dict { PACKAGE_PIN U16   IOSTANDARD
LVCMOS33 } [get_ports { ck_io1  }];
#IO_L18P_T2_A12_D28_14 Sch=ck_io[1]
#set_property -dict { PACKAGE_PIN P14   IOSTANDARD
LVCMOS33 } [get_ports { ck_io2  }]; #IO_L8N_T1_D12_14
Sch=ck_io[2]
#set_property -dict { PACKAGE_PIN T11   IOSTANDARD
LVCMOS33 } [get_ports { ck_io3  }];
#IO_L19P_T3_A10_D26_14 Sch=ck_io[3]
#set_property -dict { PACKAGE_PIN R12   IOSTANDARD
LVCMOS33 } [get_ports { ck_io4  }]; #IO_L5P_T0_D06_14
Sch=ck_io[4]
#set_property -dict { PACKAGE_PIN T14   IOSTANDARD
LVCMOS33 } [get_ports { ck_io5  }]; #IO_L14P_T2_SRCC_14
Sch=ck_io[5]
#set_property -dict { PACKAGE_PIN T15   IOSTANDARD
LVCMOS33 } [get_ports { ck_io6  }]; #IO_L14N_T2_SRCC_14
Sch=ck_io[6]
#set_property -dict { PACKAGE_PIN T16   IOSTANDARD
LVCMOS33 } [get_ports { ck_io7  }];
#IO_L15N_T2_DQS_DOUT_CSO_B_14 Sch=ck_io[7]
#set_property -dict { PACKAGE_PIN N15   IOSTANDARD
LVCMOS33 } [get_ports { ck_io8  }]; #IO_L11P_T1_SRCC_14
Sch=ck_io[8]
#set_property -dict { PACKAGE_PIN M16   IOSTANDARD
LVCMOS33 } [get_ports { ck_io9  }]; #IO_L10P_T1_D14_14
Sch=ck_io[9]
#set_property -dict { PACKAGE_PIN V17   IOSTANDARD
LVCMOS33 } [get_ports { ck_io10 }];
#IO_L18N_T2_A11_D27_14 Sch=ck_io[10]
#set_property -dict { PACKAGE_PIN U18   IOSTANDARD
LVCMOS33 } [get_ports { ck_io11 }];
#IO_L17N_T2_A13_D29_14 Sch=ck_io[11]
```

```
#set_property -dict { PACKAGE_PIN R17   IOSTANDARD
LVCMOS33 } [get_ports { ck_io12 }]; #IO_L12N_T1_MRCC_14
Sch=ck_io[12]
#set_property -dict { PACKAGE_PIN P17   IOSTANDARD
LVCMOS33 } [get_ports { ck_io13 }]; #IO_L12P_T1_MRCC_14
Sch=ck_io[13]


## ChipKit Inner Digital Header

#set_property -dict { PACKAGE_PIN U11   IOSTANDARD
LVCMOS33 } [get_ports { ck_io26 }];
#IO_L19N_T3_A09_D25_VREF_14 Sch=ck_io[26]
#set_property -dict { PACKAGE_PIN V16   IOSTANDARD
LVCMOS33 } [get_ports { ck_io27 }];
#IO_L16N_T2_A15_D31_14 Sch=ck_io[27]
#set_property -dict { PACKAGE_PIN M13   IOSTANDARD
LVCMOS33 } [get_ports { ck_io28 }];
#IO_L6N_T0_D08_VREF_14 Sch=ck_io[28]
#set_property -dict { PACKAGE_PIN R10   IOSTANDARD
LVCMOS33 } [get_ports { ck_io29 }]; #IO_25_14
Sch=ck_io[29]
#set_property -dict { PACKAGE_PIN R11   IOSTANDARD
LVCMOS33 } [get_ports { ck_io30 }]; #IO_0_14
Sch=ck_io[30]
#set_property -dict { PACKAGE_PIN R13   IOSTANDARD
LVCMOS33 } [get_ports { ck_io31 }]; #IO_L5N_T0_D07_14
Sch=ck_io[31]
#set_property -dict { PACKAGE_PIN R15   IOSTANDARD
LVCMOS33 } [get_ports { ck_io32 }]; #IO_L13N_T2_MRCC_14
Sch=ck_io[32]
#set_property -dict { PACKAGE_PIN P15   IOSTANDARD
LVCMOS33 } [get_ports { ck_io33 }]; #IO_L13P_T2_MRCC_14
Sch=ck_io[33]
#set_property -dict { PACKAGE_PIN R16   IOSTANDARD
LVCMOS33 } [get_ports { ck_io34 }];
#IO_L15P_T2_DQS_RDWR_B_14 Sch=ck_io[34]
#set_property -dict { PACKAGE_PIN N16   IOSTANDARD
LVCMOS33 } [get_ports { ck_io35 }]; #IO_L11N_T1_SRCC_14
Sch=ck_io[35]
#set_property -dict { PACKAGE_PIN N14   IOSTANDARD
LVCMOS33 } [get_ports { ck_io36 }]; #IO_L8P_T1_D11_14
Sch=ck_io[36]
```

```
#set_property -dict { PACKAGE_PIN U17   IOSTANDARD
LVCMOS33 } [get_ports { ck_io37 }];
#IO_L17P_T2_A14_D30_14 Sch=ck_io[37]
#set_property -dict { PACKAGE_PIN T18   IOSTANDARD
LVCMOS33 } [get_ports { ck_io38 }]; #IO_L7N_T1_D10_14
Sch=ck_io[38]
#set_property -dict { PACKAGE_PIN R18   IOSTANDARD
LVCMOS33 } [get_ports { ck_io39 }]; #IO_L7P_T1_D09_14
Sch=ck_io[39]
#set_property -dict { PACKAGE_PIN P18   IOSTANDARD
LVCMOS33 } [get_ports { ck_io40 }];
#IO_L9N_T1_DQS_D13_14 Sch=ck_io[40]
#set_property -dict { PACKAGE_PIN N17   IOSTANDARD
LVCMOS33 } [get_ports { ck_io41 }]; #IO_L9P_T1_DQS_14
Sch=ck_io[41]


## ChipKit Outer Analog Header - as Single-Ended Analog
Inputs
## NOTE: These ports can be used as single-ended analog
inputs with voltages from 0-3.3V (ChipKit analog pins
A0-A5) or as digital I/O.
## WARNING: Do not use both sets of constraints at the
same time!
## NOTE: The following constraints should be used with
the XADC IP core when using these ports as analog
inputs.
#set_property -dict { PACKAGE_PIN C5    IOSTANDARD
LVCMOS33 } [get_ports { vaux4_n  }]; #IO_L1N_T0_AD4N_35
          Sch=ck_an_n[0] ChipKit pin=A0
#set_property -dict { PACKAGE_PIN C6    IOSTANDARD
LVCMOS33 } [get_ports { vaux4_p  }]; #IO_L1P_T0_AD4P_35
          Sch=ck_an_p[0] ChipKit pin=A0
#set_property -dict { PACKAGE_PIN A5    IOSTANDARD
LVCMOS33 } [get_ports { vaux5_n  }];
#IO_L3N_T0_DQS_AD5N_35 Sch=ck_an_n[1] ChipKit pin=A1
#set_property -dict { PACKAGE_PIN A6    IOSTANDARD
LVCMOS33 } [get_ports { vaux5_p  }];
#IO_L3P_T0_DQS_AD5P_35 Sch=ck_an_p[1] ChipKit pin=A1
#set_property -dict { PACKAGE_PIN B4    IOSTANDARD
LVCMOS33 } [get_ports { vaux6_n  }]; #IO_L7N_T1_AD6N_35
          Sch=ck_an_n[2] ChipKit pin=A2
```

```
#set_property -dict { PACKAGE_PIN C4    IOSTANDARD
LVCMOS33 } [get_ports { vaux6_p  }]; #IO_L7P_T1_AD6P_35
          Sch=ck_an_p[2] ChipKit pin=A2
#set_property -dict { PACKAGE_PIN A1    IOSTANDARD
LVCMOS33 } [get_ports { vaux7_n  }];
#IO_L9N_T1_DQS_AD7N_35 Sch=ck_an_n[3] ChipKit pin=A3
#set_property -dict { PACKAGE_PIN B1    IOSTANDARD
LVCMOS33 } [get_ports { vaux7_p  }];
#IO_L9P_T1_DQS_AD7P_35 Sch=ck_an_p[3] ChipKit pin=A3
#set_property -dict { PACKAGE_PIN B2    IOSTANDARD
LVCMOS33 } [get_ports { vaux15_n }];
#IO_L10N_T1_AD15N_35   Sch=ck_an_n[4] ChipKit pin=A4
#set_property -dict { PACKAGE_PIN B3    IOSTANDARD
LVCMOS33 } [get_ports { vaux15_p }];
#IO_L10P_T1_AD15P_35   Sch=ck_an_p[4] ChipKit pin=A4
#set_property -dict { PACKAGE_PIN C14   IOSTANDARD
LVCMOS33 } [get_ports { vaux0_n  }]; #IO_L1N_T0_AD0N_15
          Sch=ck_an_n[5] ChipKit pin=A5
#set_property -dict { PACKAGE_PIN D14   IOSTANDARD
LVCMOS33 } [get_ports { vaux0_p  }]; #IO_L1P_T0_AD0P_15
          Sch=ck_an_p[5] ChipKit pin=A5
## ChipKit Outer Analog Header - as Digital I/O

## NOTE: The following constraints should be used when
using these ports as digital I/O.
#set_property -dict { PACKAGE_PIN F5    IOSTANDARD
LVCMOS33 } [get_ports { ck_a0 }]; #IO_0_35 Sch=ck_a[0]
#set_property -dict { PACKAGE_PIN D8    IOSTANDARD
LVCMOS33 } [get_ports { ck_a1 }]; #IO_L4P_T0_35
Sch=ck_a[1]
#set_property -dict { PACKAGE_PIN C7    IOSTANDARD
LVCMOS33 } [get_ports { ck_a2 }]; #IO_L4N_T0_35
Sch=ck_a[2]
#set_property -dict { PACKAGE_PIN E7    IOSTANDARD
LVCMOS33 } [get_ports { ck_a3 }]; #IO_L6P_T0_35
Sch=ck_a[3]
#set_property -dict { PACKAGE_PIN D7    IOSTANDARD
LVCMOS33 } [get_ports { ck_a4 }]; #IO_L6N_T0_VREF_35
Sch=ck_a[4]
#set_property -dict { PACKAGE_PIN D5    IOSTANDARD
LVCMOS33 } [get_ports { ck_a5 }]; #IO_L11P_T1_SRCC_35
Sch=ck_a[5]
```

```
## ChipKit Inner Analog Header - as Differential Analog Inputs
## NOTE: These ports can be used as differential analog inputs with voltages from 0-1.0V (ChipKit analog pins A6-A11) or as digital I/O.
## WARNING: Do not use both sets of constraints at the same time!
## NOTE: The following constraints should be used with the XADC core when using these ports as analog inputs.
#set_property -dict { PACKAGE_PIN B7    IOSTANDARD LVCMOS33 } [get_ports { vaux12_p }];
#IO_L2P_T0_AD12P_35 Sch=ad_p[12] ChipKit pin=A6
#set_property -dict { PACKAGE_PIN B6    IOSTANDARD LVCMOS33 } [get_ports { vaux12_n }];
#IO_L2N_T0_AD12N_35 Sch=ad_n[12] ChipKit pin=A7
#set_property -dict { PACKAGE_PIN E6    IOSTANDARD LVCMOS33 } [get_ports { vaux13_p }];
#IO_L5P_T0_AD13P_35 Sch=ad_p[13] ChipKit pin=A8
#set_property -dict { PACKAGE_PIN E5    IOSTANDARD LVCMOS33 } [get_ports { vaux13_n }];
#IO_L5N_T0_AD13N_35 Sch=ad_n[13] ChipKit pin=A9
#set_property -dict { PACKAGE_PIN A4    IOSTANDARD LVCMOS33 } [get_ports { vaux14_p }];
#IO_L8P_T1_AD14P_35 Sch=ad_p[14] ChipKit pin=A10
#set_property -dict { PACKAGE_PIN A3    IOSTANDARD LVCMOS33 } [get_ports { vaux14_n }];
#IO_L8N_T1_AD14N_35 Sch=ad_n[14] ChipKit pin=A11
## ChipKit Inner Analog Header - as Digital I/O

## NOTE: The following constraints should be used when using the inner analog header ports as digital I/O.
#set_property -dict { PACKAGE_PIN B7    IOSTANDARD LVCMOS33 } [get_ports { ck_a6  }]; #IO_L2P_T0_AD12P_35 Sch=ad_p[12]
#set_property -dict { PACKAGE_PIN B6    IOSTANDARD LVCMOS33 } [get_ports { ck_a7  }]; #IO_L2N_T0_AD12N_35 Sch=ad_n[12]
#set_property -dict { PACKAGE_PIN E6    IOSTANDARD LVCMOS33 } [get_ports { ck_a8  }]; #IO_L5P_T0_AD13P_35 Sch=ad_p[13]
#set_property -dict { PACKAGE_PIN E5    IOSTANDARD LVCMOS33 } [get_ports { ck_a9  }]; #IO_L5N_T0_AD13N_35 Sch=ad_n[13]
```

```
#set_property -dict { PACKAGE_PIN A4    IOSTANDARD
LVCMOS33 } [get_ports { ck_a10 }]; #IO_L8P_T1_AD14P_35
Sch=ad_p[14]
#set_property -dict { PACKAGE_PIN A3    IOSTANDARD
LVCMOS33 } [get_ports { ck_a11 }]; #IO_L8N_T1_AD14N_35
Sch=ad_n[14]


## ChipKit SPI

#set_property -dict { PACKAGE_PIN G1    IOSTANDARD
LVCMOS33 } [get_ports { ck_miso }]; #IO_L17N_T2_35
Sch=ck_miso
#set_property -dict { PACKAGE_PIN H1    IOSTANDARD
LVCMOS33 } [get_ports { ck_mosi }]; #IO_L17P_T2_35
Sch=ck_mosi
#set_property -dict { PACKAGE_PIN F1    IOSTANDARD
LVCMOS33 } [get_ports { ck_sck }]; #IO_L18P_T2_35
Sch=ck_sck
#set_property -dict { PACKAGE_PIN C1    IOSTANDARD
LVCMOS33 } [get_ports { ck_ss }]; #IO_L16N_T2_35
Sch=ck_ss


## ChipKit I2C

#set_property -dict { PACKAGE_PIN L18   IOSTANDARD
LVCMOS33 } [get_ports { ck_scl }]; #IO_L4P_T0_D04_14
Sch=ck_scl
#set_property -dict { PACKAGE_PIN M18   IOSTANDARD
LVCMOS33 } [get_ports { ck_sda }]; #IO_L4N_T0_D05_14
Sch=ck_sda
#set_property -dict { PACKAGE_PIN A14   IOSTANDARD
LVCMOS33 } [get_ports { scl_pup }];
#IO_L9N_T1_DQS_AD3N_15 Sch=scl_pup
#set_property -dict { PACKAGE_PIN A13   IOSTANDARD
LVCMOS33 } [get_ports { sda_pup }];
#IO_L9P_T1_DQS_AD3P_15 Sch=sda_pup


## Misc. ChipKit Ports

#set_property -dict { PACKAGE_PIN M17   IOSTANDARD
LVCMOS33 } [get_ports { ck_ioa }]; #IO_L10N_T1_D15_14
Sch=ck_ioa
```

```
#set_property -dict { PACKAGE_PIN C2    IOSTANDARD
LVCMOS33 } [get_ports { ck_rst }]; #IO_L16P_T2_35
Sch=ck_rst


## SMSC Ethernet PHY

#set_property -dict { PACKAGE_PIN D17   IOSTANDARD
LVCMOS33 } [get_ports { eth_col }]; #IO_L16N_T2_A27_15
Sch=eth_col
#set_property -dict { PACKAGE_PIN G14   IOSTANDARD
LVCMOS33 } [get_ports { eth_crs }];
#IO_L15N_T2_DQS_ADV_B_15 Sch=eth_crs
#set_property -dict { PACKAGE_PIN F16   IOSTANDARD
LVCMOS33 } [get_ports { eth_mdc }]; #IO_L14N_T2_SRCC_15
Sch=eth_mdc
#set_property -dict { PACKAGE_PIN K13   IOSTANDARD
LVCMOS33 } [get_ports { eth_mdio }]; #IO_L17P_T2_A26_15
Sch=eth_mdio
#set_property -dict { PACKAGE_PIN G18   IOSTANDARD
LVCMOS33 } [get_ports { eth_ref_clk }];
#IO_L22P_T3_A17_15 Sch=eth_ref_clk
#set_property -dict { PACKAGE_PIN C16   IOSTANDARD
LVCMOS33 } [get_ports { eth_rstn }]; #IO_L20P_T3_A20_15
Sch=eth_rstn
#set_property -dict { PACKAGE_PIN F15   IOSTANDARD
LVCMOS33 } [get_ports { eth_rx_clk }];
#IO_L14P_T2_SRCC_15 Sch=eth_rx_clk
#set_property -dict { PACKAGE_PIN G16   IOSTANDARD
LVCMOS33 } [get_ports { eth_rx_dv }];
#IO_L13N_T2_MRCC_15 Sch=eth_rx_dv
#set_property -dict { PACKAGE_PIN D18   IOSTANDARD
LVCMOS33 } [get_ports { eth_rxd[0] }];
#IO_L21N_T3_DQS_A18_15 Sch=eth_rxd[0]
#set_property -dict { PACKAGE_PIN E17   IOSTANDARD
LVCMOS33 } [get_ports { eth_rxd[1] }];
#IO_L16P_T2_A28_15 Sch=eth_rxd[1]
#set_property -dict { PACKAGE_PIN E18   IOSTANDARD
LVCMOS33 } [get_ports { eth_rxd[2] }];
#IO_L21P_T3_DQS_15 Sch=eth_rxd[2]
#set_property -dict { PACKAGE_PIN G17   IOSTANDARD
LVCMOS33 } [get_ports { eth_rxd[3] }];
#IO_L18N_T2_A23_15 Sch=eth_rxd[3]
```

```
#set_property -dict { PACKAGE_PIN C17   IOSTANDARD
LVCMOS33 } [get_ports { eth_rxerr }];
#IO_L20N_T3_A19_15 Sch=eth_rxerr
#set_property -dict { PACKAGE_PIN H16   IOSTANDARD
LVCMOS33 } [get_ports { eth_tx_clk }];
#IO_L13P_T2_MRCC_15 Sch=eth_tx_clk
#set_property -dict { PACKAGE_PIN H15   IOSTANDARD
LVCMOS33 } [get_ports { eth_tx_en }];
#IO_L19N_T3_A21_VREF_15 Sch=eth_tx_en
#set_property -dict { PACKAGE_PIN H14   IOSTANDARD
LVCMOS33 } [get_ports { eth_txd[0] }];
#IO_L15P_T2_DQS_15 Sch=eth_txd[0]
#set_property -dict { PACKAGE_PIN J14   IOSTANDARD
LVCMOS33 } [get_ports { eth_txd[1] }];
#IO_L19P_T3_A22_15 Sch=eth_txd[1]
#set_property -dict { PACKAGE_PIN J13   IOSTANDARD
LVCMOS33 } [get_ports { eth_txd[2] }];
#IO_L17N_T2_A25_15 Sch=eth_txd[2]
#set_property -dict { PACKAGE_PIN H17   IOSTANDARD
LVCMOS33 } [get_ports { eth_txd[3] }];
#IO_L18P_T2_A24_15 Sch=eth_txd[3]


## Quad SPI Flash

#set_property -dict { PACKAGE_PIN L13   IOSTANDARD
LVCMOS33 } [get_ports { qspi_cs }]; #IO_L6P_T0_FCS_B_14
Sch=qspi_cs
#set_property -dict { PACKAGE_PIN K17   IOSTANDARD
LVCMOS33 } [get_ports { qspi_dq[0] }];
#IO_L1P_T0_D00_MOSI_14 Sch=qspi_dq[0]
#set_property -dict { PACKAGE_PIN K18   IOSTANDARD
LVCMOS33 } [get_ports { qspi_dq[1] }];
#IO_L1N_T0_D01_DIN_14 Sch=qspi_dq[1]
#set_property -dict { PACKAGE_PIN L14   IOSTANDARD
LVCMOS33 } [get_ports { qspi_dq[2] }];
#IO_L2P_T0_D02_14 Sch=qspi_dq[2]
#set_property -dict { PACKAGE_PIN M14   IOSTANDARD
LVCMOS33 } [get_ports { qspi_dq[3] }];
#IO_L2N_T0_D03_14 Sch=qspi_dq[3]


## Power Measurements
```

```
#set_property -dict { PACKAGE_PIN B17   IOSTANDARD
LVCMOS33     } [get_ports { vsnsvu_n }];
#IO_L7N_T1_AD2N_15 Sch=ad_n[2]
#set_property -dict { PACKAGE_PIN B16   IOSTANDARD
LVCMOS33     } [get_ports { vsnsvu_p }];
#IO_L7P_T1_AD2P_15 Sch=ad_p[2]
#set_property -dict { PACKAGE_PIN B12   IOSTANDARD
LVCMOS33     } [get_ports { vsns5v0_n }];
#IO_L3N_T0_DQS_AD1N_15 Sch=ad_n[1]
#set_property -dict { PACKAGE_PIN C12   IOSTANDARD
LVCMOS33     } [get_ports { vsns5v0_p }];
#IO_L3P_T0_DQS_AD1P_15 Sch=ad_p[1]
#set_property -dict { PACKAGE_PIN F14   IOSTANDARD
LVCMOS33     } [get_ports { isns5v0_n }];
#IO_L5N_T0_AD9N_15 Sch=ad_n[9]
#set_property -dict { PACKAGE_PIN F13   IOSTANDARD
LVCMOS33     } [get_ports { isns5v0_p }];
#IO_L5P_T0_AD9P_15 Sch=ad_p[9]
#set_property -dict { PACKAGE_PIN A16   IOSTANDARD
LVCMOS33     } [get_ports { isns0v95_n }];
#IO_L8N_T1_AD10N_15 Sch=ad_n[10]
#set_property -dict { PACKAGE_PIN A15   IOSTANDARD
LVCMOS33     } [get_ports { isns0v95_p }];
#IO_L8P_T1_AD10P_15 Sch=ad_p[10]
```

Give feedback

7 Series FPGAs Data Sheet: Overview
https://docs.xilinx.com/v/u/en-US/ds180_7Series_Overview

Arty A7 E2 Schematic:
https://digilent.com/reference/_media/programmable-logic/arty-a7/arty-a7-e2-sch.pdf

Programming Guide:
https://digilent.com/reference/learn/programmable-logic/tutorials/arty-programming-guide/start

.XDC for Shakti
This file is a general .xdc for the Arty A7-100 Rev. D
To use it in a project:
- uncomment the lines corresponding to used pins
- rename the used ports (in each line, after get_ports) according to the top level signal names in the project

```
set_property CLOCK_DEDICATED_ROUTE BACKBONE [get_nets sys_clk_IBUF]

## Pmod Header JB
set_property -dict { PACKAGE_PIN E15   IOSTANDARD LVCMOS33 } [get_ports { i2c0_sda }];
#IO_L11P_T1_SRCC_15 Sch=jb_p[1]
set_property -dict { PACKAGE_PIN E16   IOSTANDARD LVCMOS33 } [get_ports { i2c0_scl }];
#IO_L11N_T1_SRCC_15 Sch=jb_n[1]
set_property -dict { PACKAGE_PIN D15   IOSTANDARD LVCMOS33 } [get_ports { gpio_14 }];
#IO_L12P_T1_MRCC_15 Sch=jb_p[2]
set_property PULLDOWN true [get_ports { gpio_14 }];
set_property -dict { PACKAGE_PIN C15   IOSTANDARD LVCMOS33 } [get_ports { gpio_15 }];
#IO_L12N_T1_MRCC_15 Sch=jb_n[2]
set_property PULLDOWN true [get_ports { gpio_15 }];

## Pmod Header JC
#set_property -dict { PACKAGE_PIN U12   IOSTANDARD LVCMOS33 } [get_ports { spi1_nss }];
#IO_L20P_T3_A08_D24_14 Sch=jc_p[1]
#set_property -dict { PACKAGE_PIN V12   IOSTANDARD LVCMOS33 } [get_ports { spi1_mosi
}]; #IO_L20N_T3_A07_D23_14 Sch=jc_n[1]
#set_property -dict { PACKAGE_PIN V10   IOSTANDARD LVCMOS33 } [get_ports { spi1_miso
}]; #IO_L21P_T3_DQS_14 Sch=jc_p[2]
#set_property -dict { PACKAGE_PIN U14   IOSTANDARD LVCMOS33 } [get_ports { spi1_sclk ]
}]; #IO_L22P_T3_A05_D21_14 Sch=jc_p[3]

## USB-UART Interface
set_property -dict { PACKAGE_PIN D10   IOSTANDARD LVCMOS33 } [get_ports { uart0_SOUT
}]; #IO_L19N_T3_VREF_16 Sch=uart_rxd_out
set_property -dict { PACKAGE_PIN A9    IOSTANDARD LVCMOS33 } [get_ports { uart0_SIN }];
#IO_L14N_T2_SRCC_16 Sch=uart_txd_in

## ChipKit Outer Digital Header
set_property -dict { PACKAGE_PIN V15   IOSTANDARD LVCMOS33 } [get_ports { io7_cell  }];
#IO_L16P_T2_CSI_B_14 Sch=ck_io[0]
set_property PULLDOWN true [get_ports { io7_cell }];
set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports { io8_cell  }];
#IO_L18P_T2_A12_D28_14 Sch=ck_io[1]
set_property PULLDOWN true [get_ports { io8_cell }];
set_property -dict { PACKAGE_PIN P14   IOSTANDARD LVCMOS33 } [get_ports { io9_cell  }];
#IO_L8N_T1_D12_14 Sch=ck_io[2]
set_property PULLDOWN true [get_ports { io9_cell }];
set_property -dict { PACKAGE_PIN T11   IOSTANDARD LVCMOS33 } [get_ports { io10_cell  }];
#IO_L19P_T3_A10_D26_14 Sch=ck_io[3]
set_property PULLDOWN true [get_ports { io10_cell }];
```

```
set_property -dict { PACKAGE_PIN R12   IOSTANDARD LVCMOS33 } [get_ports { gpio_4  }];
#IO_L5P_T0_D06_14 Sch=ck_io[4]
set_property PULLDOWN true [get_ports { gpio_4 }];
set_property -dict { PACKAGE_PIN T14   IOSTANDARD LVCMOS33 } [get_ports { io12_cell  }];
#IO_L14P_T2_SRCC_14 Sch=ck_io[5]
set_property PULLDOWN true [get_ports { io12_cell }];
set_property -dict { PACKAGE_PIN T15   IOSTANDARD LVCMOS33 } [get_ports { io13_cell  }];
#IO_L14N_T2_SRCC_14 Sch=ck_io[6]
set_property PULLDOWN true [get_ports { io13_cell }];
set_property -dict { PACKAGE_PIN T16   IOSTANDARD LVCMOS33 } [get_ports { gpio_7 }];
#IO_L15N_T2_DQS_DOUT_CSO_B_14 Sch=ck_io[7]
set_property PULLDOWN true [get_ports { gpio_7 }];
set_property -dict { PACKAGE_PIN N15   IOSTANDARD LVCMOS33 } [get_ports { gpio_8  }];
#IO_L11P_T1_SRCC_14 Sch=ck_io[8]
set_property PULLDOWN true [get_ports { gpio_8 }];
set_property -dict { PACKAGE_PIN M16   IOSTANDARD LVCMOS33 } [get_ports { io16_cell  }];
#IO_L10P_T1_D14_14 Sch=ck_io[9]
set_property PULLDOWN true [get_ports { io16_cell }];
set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports { io17_cell }];
#IO_L18N_T2_A11_D27_14 Sch=ck_io[10]
set_property PULLDOWN true [get_ports { io17_cell }];
set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports { io18_cell }];
#IO_L17N_T2_A13_D29_14 Sch=ck_io[11]
set_property PULLDOWN true [get_ports { io18_cell }];
set_property -dict { PACKAGE_PIN R17   IOSTANDARD LVCMOS33 } [get_ports { io19_cell }];
#IO_L12N_T1_MRCC_14 Sch=ck_io[12]
set_property PULLDOWN true [get_ports { io19_cell }];
set_property -dict { PACKAGE_PIN P17   IOSTANDARD LVCMOS33 } [get_ports { io20_cell }];
#IO_L12P_T1_MRCC_14 Sch=ck_io[13]
set_property PULLDOWN true [get_ports { io20_cell }];

## LEDs
set_property -dict { PACKAGE_PIN H5    IOSTANDARD LVCMOS33 } [get_ports { gpio_16 }];
#IO_L24N_T3_35 Sch=led[4]
set_property -dict { PACKAGE_PIN J5    IOSTANDARD LVCMOS33 } [get_ports { gpio_17 }];
#IO_25_35 Sch=led[5]
set_property -dict { PACKAGE_PIN T9    IOSTANDARD LVCMOS33 } [get_ports { gpio_18 }];
#IO_L24P_T3_A01_D17_14 Sch=led[6]
set_property -dict { PACKAGE_PIN T10   IOSTANDARD LVCMOS33 } [get_ports { gpio_19 }];
#IO_L24N_T3_A00_D16_14 Sch=led[7]

## Buttons
set_property -dict { PACKAGE_PIN D9    IOSTANDARD LVCMOS33 } [get_ports { gpio_20 }];
#IO_L6N_T0_VREF_16 Sch=btn[0]
```

```
set_property -dict { PACKAGE_PIN C9    IOSTANDARD LVCMOS33 } [get_ports { gpio_21 }];
#IO_L11P_T1_SRCC_16 Sch=btn[1]
set_property -dict { PACKAGE_PIN B9    IOSTANDARD LVCMOS33 } [get_ports { gpio_22 }];
#IO_L11N_T1_SRCC_16 Sch=btn[2]
set_property -dict { PACKAGE_PIN B8    IOSTANDARD LVCMOS33 } [get_ports { gpio_23 }];
#IO_L12P_T1_MRCC_16 Sch=btn[3]

## Pmod Header JD
set_property -dict { PACKAGE_PIN D4    IOSTANDARD LVCMOS33 } [get_ports { gpio_24 }];
#IO_L11N_T1_SRCC_35 Sch=jd[1]
set_property PULLDOWN true [get_ports { gpio_24 }];
set_property -dict { PACKAGE_PIN D3    IOSTANDARD LVCMOS33 } [get_ports { gpio_25 }];
#IO_L12N_T1_MRCC_35 Sch=jd[2]
set_property PULLDOWN true [get_ports { gpio_25 }];
set_property -dict { PACKAGE_PIN F4    IOSTANDARD LVCMOS33 } [get_ports { gpio_26 }];
#IO_L13P_T2_MRCC_35 Sch=jd[3]
set_property PULLDOWN true [get_ports { gpio_26 }];
set_property -dict { PACKAGE_PIN F3    IOSTANDARD LVCMOS33 } [get_ports { gpio_27 }];
#IO_L13N_T2_MRCC_35 Sch=jd[4]
set_property PULLDOWN true [get_ports { gpio_27 }];
set_property -dict { PACKAGE_PIN E2    IOSTANDARD LVCMOS33 } [get_ports { gpio_28 }];
#IO_L14P_T2_SRCC_35 Sch=jd[7]
set_property PULLDOWN true [get_ports { gpio_28 }];
set_property -dict { PACKAGE_PIN D2    IOSTANDARD LVCMOS33 } [get_ports { gpio_29 }];
#IO_L14N_T2_SRCC_35 Sch=jd[8]
set_property PULLDOWN true [get_ports { gpio_29 }];
set_property -dict { PACKAGE_PIN H2    IOSTANDARD LVCMOS33 } [get_ports { gpio_30 }];
#IO_L15P_T2_DQS_35 Sch=jd[9]
set_property PULLDOWN true [get_ports { gpio_30 }];
set_property -dict { PACKAGE_PIN G2    IOSTANDARD LVCMOS33 } [get_ports { gpio_31 }];
#IO_L15N_T2_DQS_35 Sch=jd[10]
set_property PULLDOWN true [get_ports { gpio_31 }];

# ChipKit Outer Analog Header - as Single-Ended Analog Inputs
# NOTE: These ports can be used as single-ended analog inputs with voltages from 0-3.3V
(ChipKit analog pins A0-A5) or as digital I/O.
set_property -dict { PACKAGE_PIN C5    IOSTANDARD LVCMOS33 } [get_ports { vauxn4  }];
#IO_L1N_T0_AD4N_35              Sch=ck_an_n[0]        ChipKit pin=A0
set_property -dict { PACKAGE_PIN C6    IOSTANDARD LVCMOS33 } [get_ports { vauxp4  }];
#IO_L1P_T0_AD4P_35              Sch=ck_an_p[0]        ChipKit pin=A0
set_property -dict { PACKAGE_PIN A5    IOSTANDARD LVCMOS33 } [get_ports { vauxn5  }];
#IO_L3N_T0_DQS_AD5N_35          Sch=ck_an_n[1]        ChipKit pin=A1
set_property -dict { PACKAGE_PIN A6    IOSTANDARD LVCMOS33 } [get_ports { vauxp5  }];
#IO_L3P_T0_DQS_AD5P_35          Sch=ck_an_p[1]        ChipKit pin=A1
```

```
set_property -dict { PACKAGE_PIN B4    IOSTANDARD LVCMOS33 } [get_ports { vauxn6  }];
#IO_L7N_T1_AD6N_35                Sch=ck_an_n[2]        ChipKit pin=A2
set_property -dict { PACKAGE_PIN C4    IOSTANDARD LVCMOS33 } [get_ports { vauxp6  }];
#IO_L7P_T1_AD6P_35                Sch=ck_an_p[2]        ChipKit pin=A2
set_property -dict { PACKAGE_PIN A1    IOSTANDARD LVCMOS33 } [get_ports { vauxn7  }];
#IO_L9N_T1_DQS_AD7N_35         Sch=ck_an_n[3]        ChipKit pin=A3
set_property -dict { PACKAGE_PIN B1    IOSTANDARD LVCMOS33 } [get_ports { vauxp7  }];
#IO_L9P_T1_DQS_AD7P_35         Sch=ck_an_p[3]        ChipKit pin=A3
set_property -dict { PACKAGE_PIN B2    IOSTANDARD LVCMOS33 } [get_ports { vauxn15 }];
#IO_L10N_T1_AD15N_35     Sch=ck_an_n[4]        ChipKit pin=A4
set_property -dict { PACKAGE_PIN B3    IOSTANDARD LVCMOS33 } [get_ports { vauxp15 }];
#IO_L10P_T1_AD15P_35     Sch=ck_an_p[4]        ChipKit pin=A4
set_property -dict { PACKAGE_PIN C14   IOSTANDARD LVCMOS33 } [get_ports { vauxn0  }];
#IO_L1N_T0_AD0N_15                Sch=ck_an_n[5]        ChipKit pin=A5
set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 } [get_ports { vauxp0  }];
#IO_L1P_T0_AD0P_15                Sch=ck_an_p[5]        ChipKit pin=A5

# ChipKit Inner Analog Header - as Differential Analog Inputs
# NOTE: These ports can be used as differential analog inputs with voltages from 0-1.0V
(ChipKit Analog pins A6-A11) or as digital I/O.
set_property -dict { PACKAGE_PIN B7    IOSTANDARD LVCMOS33 } [get_ports { vauxp12 }];
#IO_L2P_T0_AD12P_35       Sch=ad_p[12] ChipKit pin=A6
set_property -dict { PACKAGE_PIN B6    IOSTANDARD LVCMOS33 } [get_ports { vauxn12 }];
#IO_L2N_T0_AD12N_35       Sch=ad_n[12] ChipKit pin=A7
set_property -dict { PACKAGE_PIN E6    IOSTANDARD LVCMOS33 } [get_ports { vauxp13 }];
#IO_L5P_T0_AD13P_35       Sch=ad_p[13] ChipKit pin=A8
set_property -dict { PACKAGE_PIN E5    IOSTANDARD LVCMOS33 } [get_ports { vauxn13 }];
#IO_L5N_T0_AD13N_35       Sch=ad_n[13] ChipKit pin=A9
set_property -dict { PACKAGE_PIN A4    IOSTANDARD LVCMOS33 } [get_ports { vauxp14 }];
#IO_L8P_T1_AD14P_35       Sch=ad_p[14] ChipKit pin=A10
set_property -dict { PACKAGE_PIN A3    IOSTANDARD LVCMOS33 } [get_ports { vauxn14 }];
#IO_L8N_T1_AD14N_35       Sch=ad_n[14] ChipKit pin=A11

## Quad SPI Flash
set_property -dict { PACKAGE_PIN L13   IOSTANDARD LVCMOS33 } [get_ports { spi0_nss }];
#IO_L6P_T0_FCS_B_14 Sch=qspi_cs
set_property -dict { PACKAGE_PIN K17   IOSTANDARD LVCMOS33 } [get_ports { spi0_mosi }];
#IO_L1P_T0_D00_MOSI_14 Sch=qspi_dq[0]
set_property -dict { PACKAGE_PIN K18   IOSTANDARD LVCMOS33 } [get_ports { spi0_miso }];
#IO_L1N_T0_D01_DIN_14 Sch=qspi_dq[1]
#set_property -dict { PACKAGE_PIN L14   IOSTANDARD LVCMOS33 } [get_ports { qspi_dq[2]
}]; #IO_L2P_T0_D02_14 Sch=qspi_dq[2]
#set_property -dict { PACKAGE_PIN M14   IOSTANDARD LVCMOS33 } [get_ports { qspi_dq[3]
}]; #IO_L2N_T0_D03_14 Sch=qspi_dq[3]
```

```
## ChipKit I2C
set_property -dict { PACKAGE_PIN L18   IOSTANDARD LVCMOS33 } [get_ports { i2c1_scl }];
#IO_L4P_T0_D04_14 Sch=ck_scl
set_property -dict { PACKAGE_PIN M18   IOSTANDARD LVCMOS33 } [get_ports { i2c1_sda }];
#IO_L4N_T0_D05_14 Sch=ck_sda

set_property -dict { PACKAGE_PIN C2    IOSTANDARD LVCMOS33 } [get_ports { sys_rst }];
#IO_L16P_T2_35 Sch=ck_rst

# SMSC Ethernet PHY
set_property -dict { PACKAGE_PIN D17   IOSTANDARD LVCMOS33 } [get_ports { phy_col }];
#IO_L16N_T2_A27_15 Sch=eth_col
set_property -dict { PACKAGE_PIN G14   IOSTANDARD LVCMOS33 } [get_ports { phy_crs }];
#IO_L15N_T2_DQS_ADV_B_15 Sch=eth_crs
set_property -dict { PACKAGE_PIN F16   IOSTANDARD LVCMOS33 } [get_ports { phy_mdc }];
#IO_L14N_T2_SRCC_15 Sch=eth_mdc
set_property -dict { PACKAGE_PIN K13   IOSTANDARD LVCMOS33 } [get_ports { phy_mdio }];
#IO_L17P_T2_A26_15 Sch=eth_mdio
set_property -dict { PACKAGE_PIN G18   IOSTANDARD LVCMOS33 } [get_ports { phy_ref_clk
}]; #IO_L22P_T3_A17_15 Sch=eth_ref_clk
set_property -dict { PACKAGE_PIN C16   IOSTANDARD LVCMOS33 } [get_ports { phy_rst_n }];
#IO_L20P_T3_A20_15 Sch=eth_rstn
set_property -dict { PACKAGE_PIN F15   IOSTANDARD LVCMOS33 } [get_ports { phy_rx_clk
}]; #IO_L14P_T2_SRCC_15 Sch=eth_rx_clk
set_property -dict { PACKAGE_PIN G16   IOSTANDARD LVCMOS33 } [get_ports { phy_dv }];
#IO_L13N_T2_MRCC_15 Sch=eth_rx_dv
set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports {
phy_rx_data[0] }]; #IO_L21N_T3_DQS_A18_15 Sch=eth_rxd[0]
set_property -dict { PACKAGE_PIN E17   IOSTANDARD LVCMOS33 } [get_ports {
phy_rx_data[1] }]; #IO_L16P_T2_A28_15 Sch=eth_rxd[1]
set_property -dict { PACKAGE_PIN E18   IOSTANDARD LVCMOS33 } [get_ports {
phy_rx_data[2] }]; #IO_L21P_T3_DQS_15 Sch=eth_rxd[2]
set_property -dict { PACKAGE_PIN G17   IOSTANDARD LVCMOS33 } [get_ports {
phy_rx_data[3] }]; #IO_L18N_T2_A23_15 Sch=eth_rxd[3]
set_property -dict { PACKAGE_PIN C17   IOSTANDARD LVCMOS33 } [get_ports { phy_rx_er }];
#IO_L20N_T3_A19_15 Sch=eth_rxerr
set_property -dict { PACKAGE_PIN H16   IOSTANDARD LVCMOS33 } [get_ports { phy_tx_clk
}]; #IO_L13P_T2_MRCC_15 Sch=eth_tx_clk
set_property -dict { PACKAGE_PIN H15   IOSTANDARD LVCMOS33 } [get_ports { phy_tx_en }];
#IO_L19N_T3_A21_VREF_15 Sch=eth_tx_en
set_property -dict { PACKAGE_PIN H14   IOSTANDARD LVCMOS33 } [get_ports {
phy_tx_data[0] }]; #IO_L15P_T2_DQS_15 Sch=eth_txd[0]
```

```
set_property -dict { PACKAGE_PIN J14   IOSTANDARD LVCMOS33 } [get_ports {
phy_tx_data[1] }]; #IO_L19P_T3_A22_15 Sch=eth_txd[1]
set_property -dict { PACKAGE_PIN J13   IOSTANDARD LVCMOS33 } [get_ports {
phy_tx_data[2] }]; #IO_L17N_T2_A25_15 Sch=eth_txd[2]
set_property -dict { PACKAGE_PIN H17   IOSTANDARD LVCMOS33 } [get_ports {
phy_tx_data[3] }]; #IO_L18P_T2_A24_15 Sch=eth_txd[3]
```