DIGITAL SAFE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SUBMITTED TO:

Sumam David
DEPARTMENT OF ECE
NITK SURATHKAL

SUBMITTED BY:

Pranjal Mishra : 232CN023
Saurabh Gupta : 232CN028
Shwetank : 232VL033

1. Introduction

Our project begins with the development of a comprehensive system architecture that outlines the key components of the digital safe. This includes the creation of a secure entry system with password protection and user authentication mechanisms. Verilog will be employed to design and implement these security features on the Altera DE10 board.

The hardware components of the project will be realized using the capabilities of Intel Quartus, a powerful FPGA design software. The Altera DE10 development board, equipped with Intel Cyclone V FPGA, serves as the hardware platform for the implementation of the digital safe. The utilization of FPGA technology allows for parallel processing, enabling efficient execution of cryptographic algorithms and enhancing the overall security of the system.

The project aims to provide a hands-on learning experience in digital system design, FPGA programming, and hardware security. The outcomes of the project will be evaluated through rigorous testing, including functionality testing, security analysis, and performance assessments.

In conclusion, this mini project seeks to showcase the potential of Intel Quartus, Altera DE10 board, and Verilog in the development of a secure digital safe. The project not only serves as a practical application of FPGA technology but also contributes to the exploration of hardware-based security solutions in the digital era.

2. Features

The features of this project include

- Keyboard integration : Includes a digilent keypad that allows for manual password input.
- User Profiles : Allows for different users to have different passwords and different levels of access depending on authority.
- GPS : Includes proximity warning using digilent pmod GPS and 3DFIX pin.

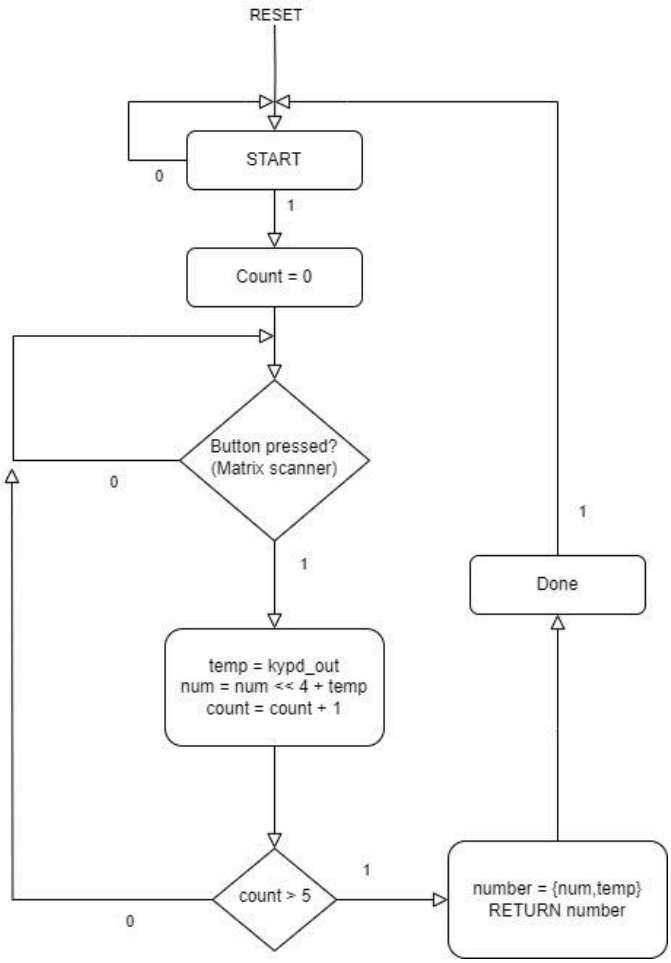
3. Keypad

The Digilent Pmod Keypad is an input device designed to provide a convenient way to accept user inputs in the form of key presses. This module typically interfaces with microcontroller or FPGA development boards using the Pmod standard, which is a set of guidelines for designing peripherals that can be easily connected to compatible host devices.

The Pmod Keypad consists of a set of buttons arranged in a matrix format. The number of buttons and the specific arrangement may vary depending on the model. The buttons are arranged in rows and columns, forming a matrix. Each button is at the intersection of a specific row and column. The Pmod Keypad typically uses a method called "switching matrix" to scan the state of the buttons. This involves sequentially activating each row and checking the state of the buttons in that row.The scanning is done in a rapid sequence, and the microcontroller or FPGA can determine which button is pressed based on the activated row and column. The Pmod Keypad module is designed to connect to the host device using GPIO pins. These pins usually include power, ground, and signal pins.

When the scanning clock for column and pressed row intersect the keyboard gives output signal for that number.

- Keypad ASM chart:



4. PMOD GPS

Digilent Pmod GPS is designed to interface with microcontroller or FPGA development boards using the Pmod standard. The module incorporate a GPS receiver to receive signals from satellites and determine its own position (latitude, longitude, and altitude), as well as other information such as time and velocity. It has a communication interface i.e UART through which the GPS module communicates with the host device.The module also handles the parsing and processing of NMEA (National Marine Electronics Association) sentences, which are standard sentences output by GPS receivers containing position and timing information.
The Pmod GPS module is designed to be compatible with Vivado and Xilinx FPGA board that support the Pmod standard. Depending on the module, there are supporting drivers or libraries that facilitate the integration of the GPS functionality into the host device's firmware or software.

In our project we used the functionality of 3DFIX pin that allows us to use the gps module as GPIO. The term "3D Fix" typically refers to the quality of the GPS signal and the ability of the GPS receiver to determine three-dimensional position information (latitude, longitude, and altitude). A "3D Fix" indicates that the GPS receiver has acquired signals from satellites in three dimensions, allowing it to calculate a more accurate and complete position. In pmod GPS module, the signal strength changes with every 3 to 5 meter thus allowing us to treat it as a low power and low precision position fix, when the module goes 3 to 5 meter out of range from the position it was fixed with the 3DFIX pin gets activated and our board provides a warning thus making it anti-Theft.

Connector J1		
Pin	**Signal**	**Description**
1	3DF	3D-Fix Indicator
2	RX	Receive
3	TX	Transmit
4	1PPS	1 Pulse Per Second
5	GND	Power Supply Ground
6	VCC	Power Supply (3.3v)
Connector J2		
Pin	**Signal**	**Description**
1	~RST	Reset (active low)
2	RTCM	DGPS data pin (contact GlobalTop for use)

Fig 4.1 : Pin schematic for PMOD GPS with Gms-u1LP antenna

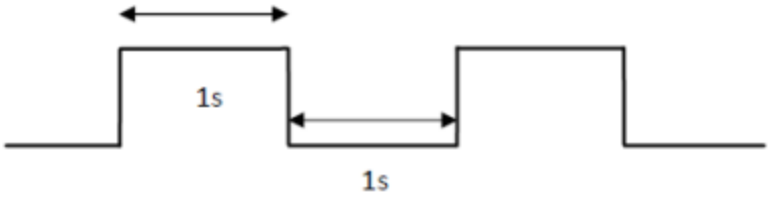
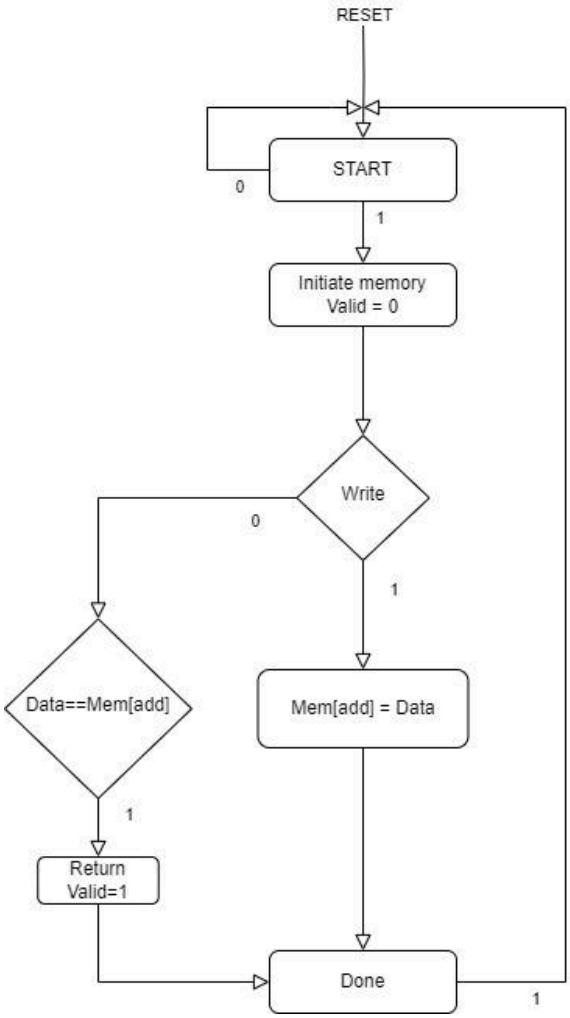


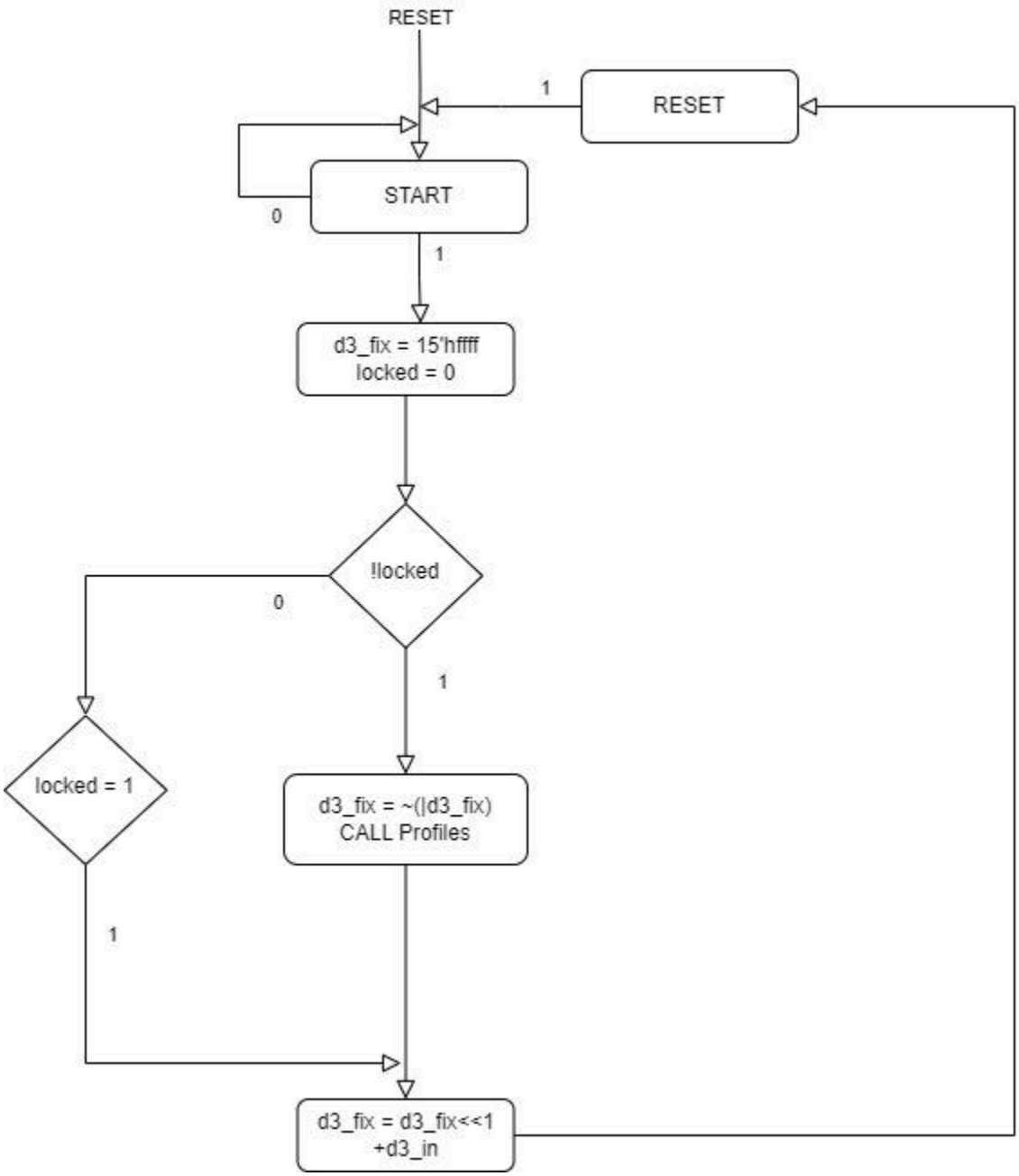
Fig 4.2 : Waveform for 3DFIX without a fix

5. Profiles

We used a memory module to save the profiles we enter. When the save password pin is on, the module takes inputs of profile number and password entered and saves both data in a matrix with 16 bit word length and 4 bit stack height. 16 bit word length allows for a 4 digit hex password to be saved and 4 bit stack length allows for 16 profiles.



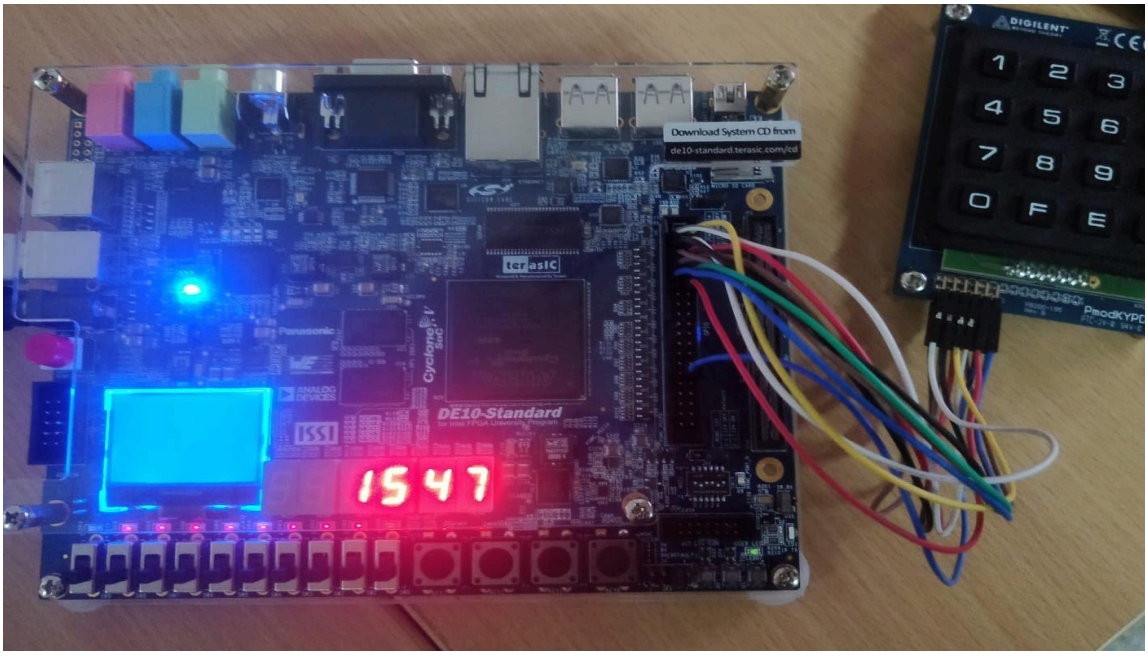
6. Warning from 3DFIX



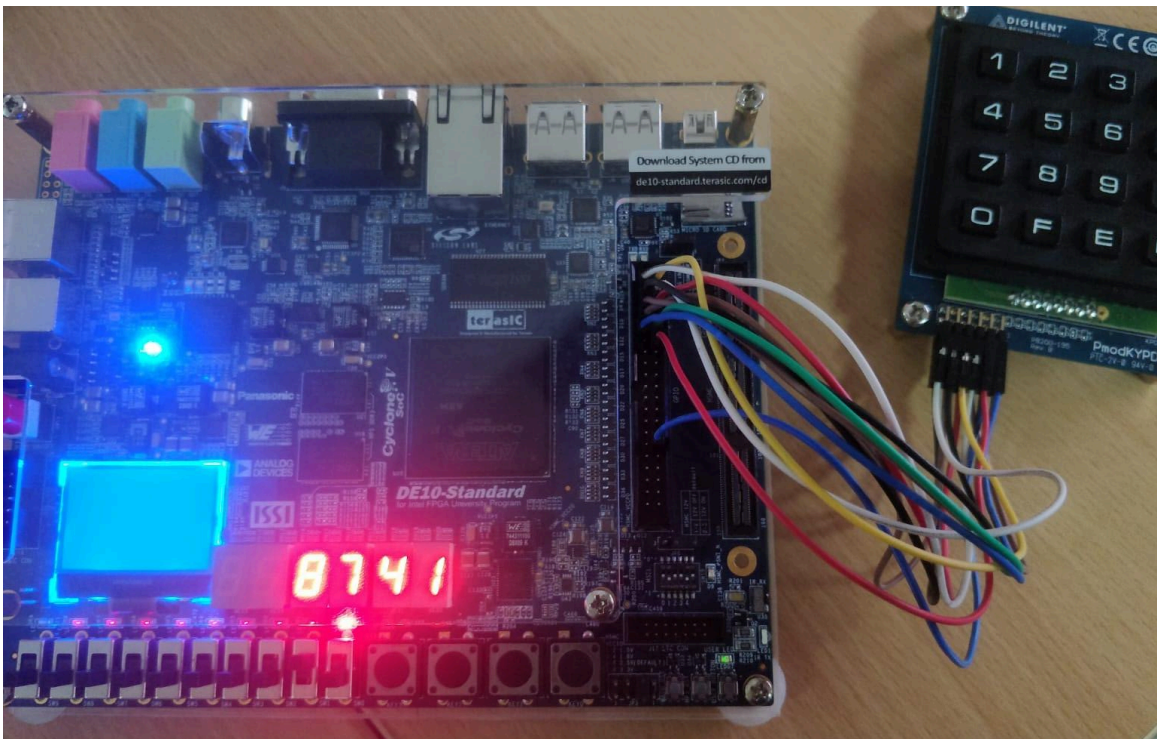
7. Pin Planner

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair
add_profile	Input	PIN_AC29	5B	B5B_N0	2.5 V (default)		12mA (default)		
clk	Input	PIN_AF14	3B	B3B_N0	2.5 V (default)		12mA (default)		
col[3]	Output	PIN_AK3	3B	B3B_N0	2.5 V (default)		12mA (default)	1 (default)	
col[2]	Output	PIN_Y16	3B	B3B_N0	2.5 V (default)		12mA (default)	1 (default)	
col[1]	Output	PIN_AK2	3B	B3B_N0	2.5 V (default)		12mA (default)	1 (default)	
col[0]	Output	PIN_W15	3B	B3B_N0	2.5 V (default)		12mA (default)	1 (default)	
d3_in	Input	PIN_AJ4	3B	B3B_N0	2.5 V (default)		12mA (default)		
dis_code0[6]	Output	PIN_AH18	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code0[5]	Output	PIN_AG18	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code0[4]	Output	PIN_AH17	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code0[3]	Output	PIN_AG16	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code0[2]	Output	PIN_AG17	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code0[1]	Output	PIN_V18	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code0[0]	Output	PIN_W17	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code1[6]	Output	PIN_V17	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code1[5]	Output	PIN_AE17	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code1[4]	Output	PIN_AE18	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code1[3]	Output	PIN_AD17	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code1[2]	Output	PIN_AE16	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code1[1]	Output	PIN_V16	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code1[0]	Output	PIN_AF16	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code2[6]	Output	PIN_W16	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code2[5]	Output	PIN_AF18	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code2[4]	Output	PIN_Y18	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code2[3]	Output	PIN_Y17	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code2[2]	Output	PIN_AA18	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code2[1]	Output	PIN_AB17	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code2[0]	Output	PIN_AA21	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code3[6]	Output	PIN_AD20	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code3[5]	Output	PIN_AA19	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code3[4]	Output	PIN_AC20	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code3[3]	Output	PIN_AA20	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code3[2]	Output	PIN_AD19	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code3[1]	Output	PIN_W19	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
dis_code3[0]	Output	PIN_Y19	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
high[1]	Output	PIN_AH4	3A	B3A_N0	2.5 V (default)		12mA (default)	1 (default)	
high[0]	Output	PIN_AH5	3A	B3A_N0	2.5 V (default)		12mA (default)	1 (default)	
locked	Output	PIN_AC22	4A	B4A_N0	2.5 V (default)		12mA (default)	1 (default)	
low[1]	Output	PIN_AG2	3A	B3A_N0	2.5 V (default)		12mA (default)	1 (default)	
low[0]	Output	PIN_AD10	3A	B3A_N0	2.5 V (default)		12mA (default)	1 (default)	
profile_selected[3]	Input	PIN_AC30	5B	B5B_N0	2.5 V (default)		12mA (default)		
profile_selected[2]	Input	PIN_AB28	5B	B5B_N0	2.5 V (default)		12mA (default)		
profile_selected[1]	Input	PIN_Y27	5B	B5B_N0	2.5 V (default)		12mA (default)		
profile_selected[0]	Input	PIN_AB30	5B	B5B_N0	2.5 V (default)		12mA (default)		
row[3]	Input	PIN_AH3	3A	B3A_N0	2.5 V (default)		12mA (default)		
row[2]	Input	PIN_AH2	3A	B3A_N0	2.5 V (default)		12mA (default)		
row[1]	Input	PIN_AJ2	3A	B3A_N0	2.5 V (default)		12mA (default)		
row[0]	Input	PIN_AJ1	3A	B3A_N0	2.5 V (default)		12mA (default)		
rst	Input	PIN_AA30	5B	B5B_N0	2.5 V (default)		12mA (default)		
valid	Output	PIN_AA24	5A	B5A_N0	2.5 V (default)		12mA (default)	1 (default)	
<<new node>>									

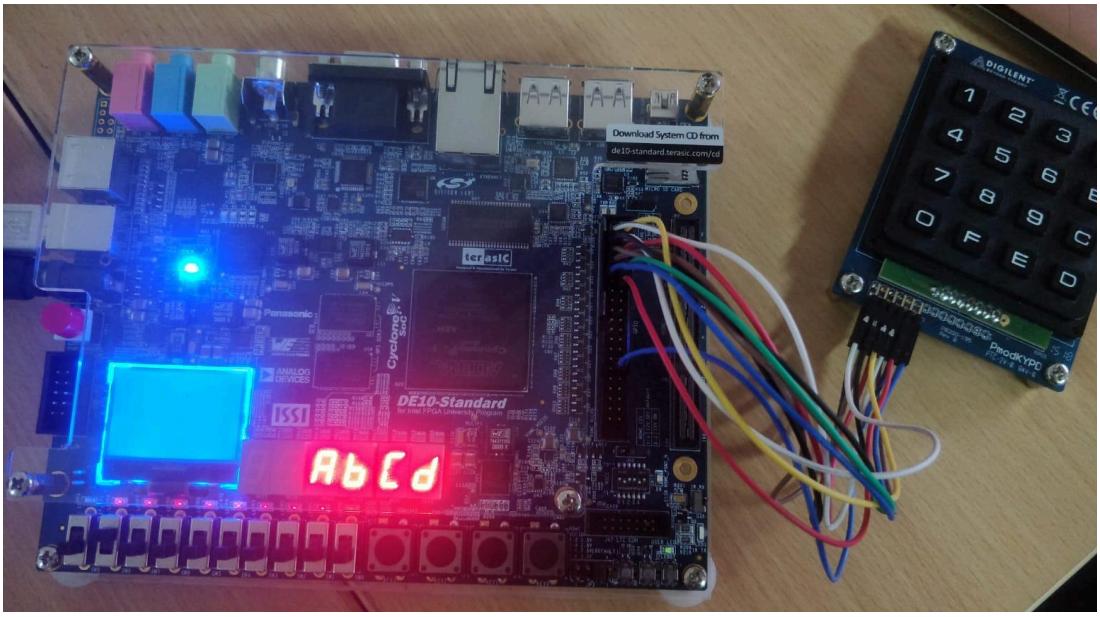
8. Practical output



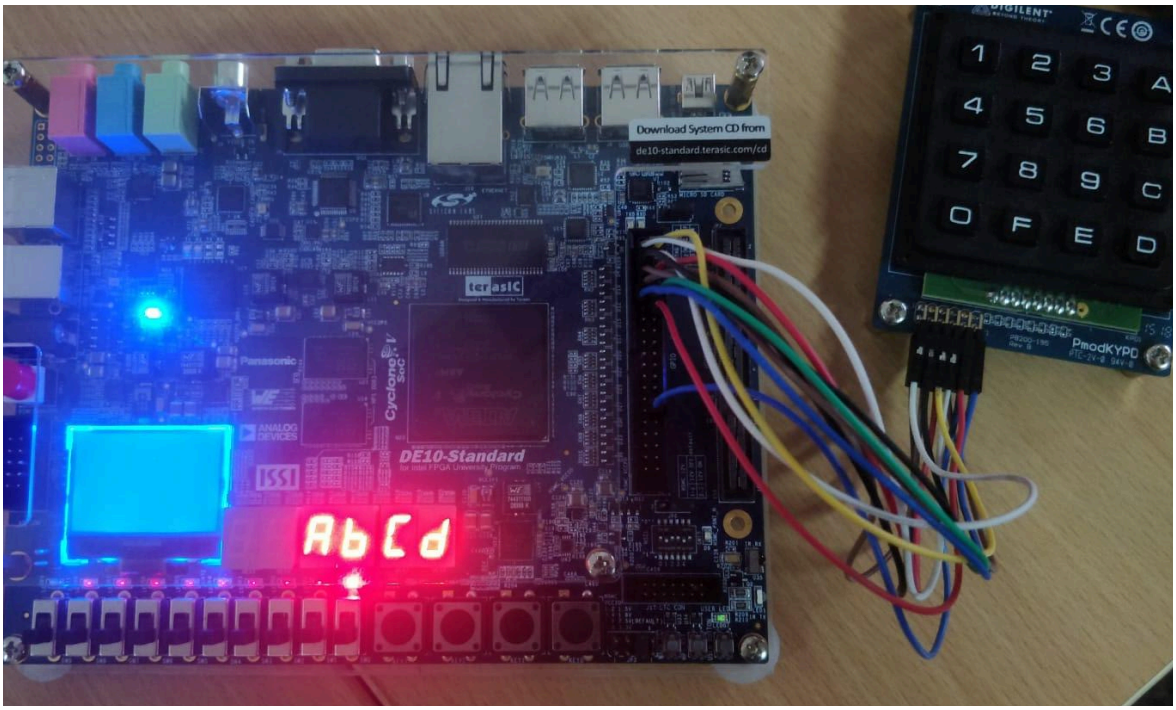
Output : For wrong password input, no LED output



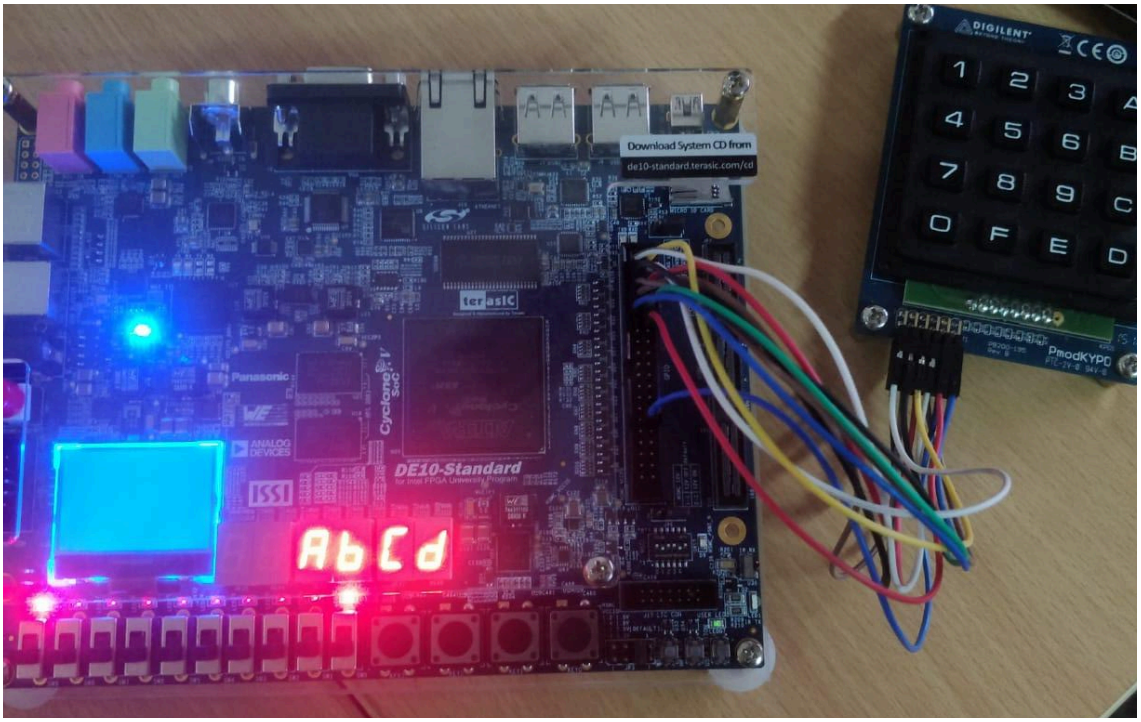
Output : For right password input, LED glows



Output : Setting Profile 0 and saving password ABCD



Output : Checking output for ABCD input, LED glows



Output : Warning LED glows for activated 3DFIX