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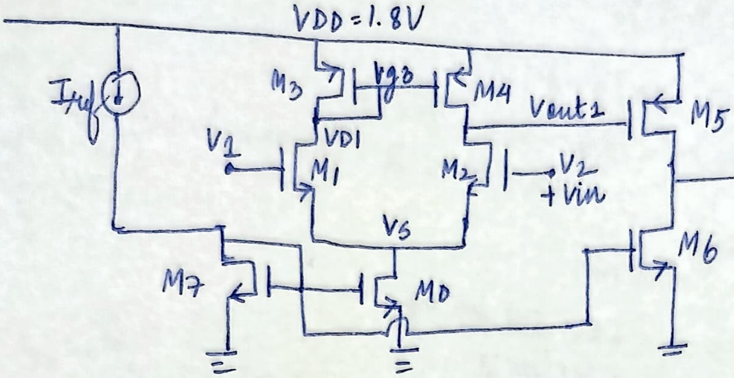
EE 206
ANALOG CIRCUITS
OTA DESIGN ASSIGNMENT

I) OPEN LOOP ANALYSIS

(i) Circuit diagram :



* Assumptions for initial CMOS (M7)

→ $I_{ref} : 4.25\,\mu A$

$V_{ov_7} = V_{gs7} - V_{th7}$

→ $V_{ov_7} = 0.09V$

(ii) Calculations :

* Based on the initial assumptions as stated above,

$$\left(\frac{W}{L}\right)_7 = \frac{2 I_{ref}}{\mu_n C_{ox} (V_{ov7})^2} = \frac{2 \times 4.25}{230 \times 81} \times 10^4 \simeq 4.5 \quad \left(\begin{array}{l} L = 900\,nm \\ W = 3600\,nm \end{array}\right)$$

∵ The tail current of the OTA is designed to be 10 times of the reference I_{ref},

$$\left(\frac{W}{L}\right)_0 = 10\left(\frac{W}{L}\right)_7 = 45 \quad \left(\begin{array}{l} L = 900\,nm \\ W = \cancel{40}\,500\,nm \end{array}\right)$$

* For M0 to be in saturation : $V_S > (V_{gs} - V_{th})_0 \Rightarrow V_S > 0.09V$

* For the current to split equally at node S, $\left(\frac{W}{L}\right)_{M1} = \left(\frac{W}{L}\right)_{M2} = \frac{1}{2}\left(\frac{W}{L}\right)_0 \simeq 22.5$

Thus, $W_1 = W_2 = \cancel{18}\ 20\,250\,nm$; $L_1 = L_2 = 900\,nm$

* $V_{gs_1} - V_{th\,1} = 0.09V$

$\Rightarrow 0.9 - V_S - 0.37 = 0.09 \Rightarrow V_S = 0.44V > 0.09V$

(∴ M0 is in saturation)

NOTE
$VDD = 1.8V$
$V_1 = 0.9V$
$V_2 = 0.9V + \cancel{\ }\,2\times10^{-4}\sin(2000\pi t)$

* For M_1 to be saturation, $V_{D1} > V_{gs1} - V_{th1} > 0.09V$

* For M_3 and M_4, $I_3 = I_4 = 21.25\,\mu A$

$$I_3 = \frac{\mu_p C_{ox}}{2} \times \left(\frac{W}{L}\right)_3 \times (V_{sg} - |V_{tp}|)_3^2$$

* Assume $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \cancel{4}3.5 \Rightarrow (V_{sg} - |V_{tp}|)_3 = 0.372\,V$ (for the sake of simplicity in calculations)

Thus, $W_3 = W_4 = 3150\,nm \simeq 3200\,nm$

$L_3 = L_4 = 900\,nm$

For M_3 to be on, $V_{sg3} > |V_{tp}|_3 \Rightarrow 1.8 - |V_{tp}| > V_{g3}$ $(|V_{tp}| = 0.39V)$

∴ $V_{g3} = V_{D1} < 1.41V$

$(V_{sg} - |V_{tp}|)_3 = 0.372 \Rightarrow \cancel{1.8 - 0.372 - 0.39 = V_{D1}}$ $1.8 - 0.39 - V_{D1} = 0.372$

$\Rightarrow V_{D1} = 1.038\,V < 1.41V.$

$\Rightarrow$ M_3 and M_4 are in sat^n.

Thus, even the above theoretical calculations require modifications due to presence of non-idealities such as channel length modulation and body effect.

$$\left(\frac{W}{L}\right)_7 = \frac{3400\,nm}{900\,nm} \simeq 3.77$$

The first stage gain may be calculated using the values from the log file attached.

$|A_{v1}| = \left|\frac{V_{out1}}{V_{in}}\right| = g_{m2}\,(r_{on2} \,||\, r_{op4})$

$|A_{v1}| = 4.03\times10^{-4}\,(343{,}642 \,||\, 952{,}380)$

$|A_{v1}| = 101.76$

As per simulation, $|A_{v1}| = 101.23$

$\therefore$ error is nearly 0.5%

* For M6 :

Assume / choose $I_6 = 25.5\,\mu A$

Then, since, $(V_{gs}-V_{th})_6 = (V_{gs}-V_{th})_0 = 0.09V$,

$\left(\frac{W}{L}\right)_6 = \frac{2 I_6}{\mu_n C_{ox}\,(V_{gs}-V_{th})_6^2} = 22.04 \approx 20$ (approximated due to practical considerations pertaining to non-idealities)

$\therefore W = 20000\,nm$, $L = 900\,nm$

Practical observation of $I_6 = 24.48\,\mu A$

Also $V_{out} > (V_{gs}-V_{th})_6 \Rightarrow V_{out} > 0.09V$

* For M5 :

$(V_{sg}-|V_{tp}|)_5 = \cancel{V_S - V_{out1} - |V_{tp}|}\ (V_S - V_{out1}) - |V_{tp}|$

where $V_{out1} = 906.98\,mV \approx 0.9V$, but theoretical $= 1.038V$ (as calculated earlier)

$\therefore V_{sg}-|V_{tp}|_5 = \cancel{1.8 - 0.9 - 0.39} = 1.8 - 1.038 - 0.39$

$= 0.372V$

$I_5 = I_6 = 25.5\,\mu A$

$\therefore 25.5\times10^{-6} = \frac{100\times10^{-6}}{2}\times\left(\frac{W}{L}\right)_5\times(0.372)^2$

$\left(\frac{W}{L}\right)_5 = 3.71$

Using $V_{sd} > V_{sg}-|V_{tp}|_5 \Rightarrow V_{out} = 0.9V$

Thus, M5 and M6 both are in saturation

* Second stage gain

$|A_{v2}| = g_{m5}\times(r_{op5} \,||\, r_{on6})$

$= 9.4\times10^{-5}\times(840336.13 \,||\, 381{,}679.38)$

$= 24.67$

$\therefore$ Overall voltage gain for open loop OTA $|A_v| = |A_{v1}|\,|A_{v2}|$

$|A_v| = 101.76\times24.67$

$\boxed{|A_v| = 2510.61}$

Practically,

$|A_{v1}| = 101.23$

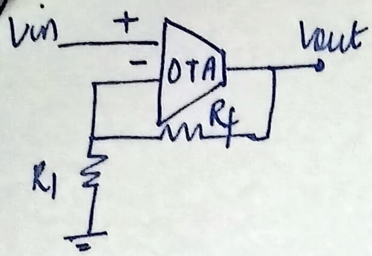
$|A_{v2}| = 26.71$

$\therefore |A_v| = |A_{v1}|\,|A_{v2}|$

$= 2703.3$

$\therefore$ % error $= 7.4\%$

II) CLOSED LOOP CONFIGURATION



$V_{out} = A(V_+ - V_-)$

Consider ∞ gain, $V_+ = V_-$,

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_1}$$

For gain = 2, $R_f = R_1 = 20k\Omega$

However, the OTA I designed has $A \neq \infty$ ($A = 2550$)

$\therefore V_{out} - AV_{in} = -AV_-$

$\Rightarrow V_- = \dfrac{AV_{in} - V_{out}}{A}$

KCL at V^- yields:

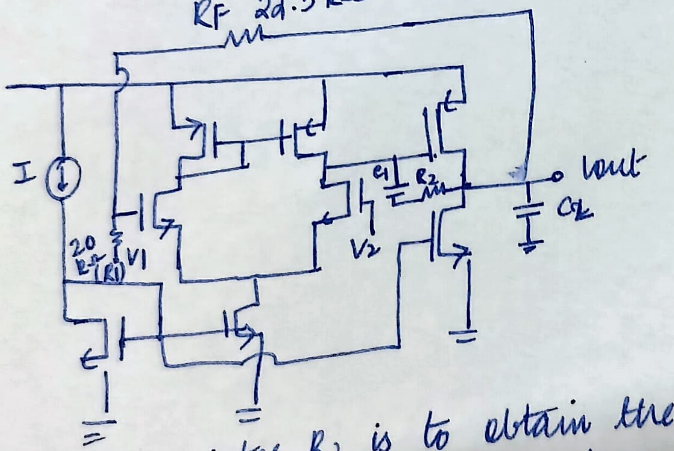
$$\frac{\frac{AV_{in} - V_{out}}{A} - V_{out}}{R_F} = \frac{V_{out} - AV_{in}}{AR_1}$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{A(R_1 + R_F)}{(A+1)R_1 + R_F}$$

Choose $R_F = 22.5k\Omega$ and $R_1 = 20k\Omega \Rightarrow \dfrac{V_{out}}{V_{in}} = 2.124$

Practically, $\dfrac{V_{out}}{V_{in}} = 2.18$

Circuit diagram:



$V_1 = 0.9V$
$V_2 = 0.9V + 0.0001\sin(2000\pi t)$
$C_1 = 3pF$, $C_2 = 10pF$

The purpose of the resistor R_2 is to obtain the required phase margin ($60°$-$70°$) ~~∴~~ choosing a suitable R_2 is important so as to fix the P.M at $60°$

$\therefore R_2 = 9.6k\Omega$

3 dB bandwidth = 12.974 MHz

Location of dominant pole $= \dfrac{1}{A_{V2} \times C_1 \times (r_{op5} \parallel r_{on6})} = \dfrac{1}{24.61 \times 3\times10^{-12} \times (840336 \parallel 381679)}$

$= 52{,}995.86\ s^{-1}$

Power dissipation $= V_{DD} \times (I_{D7} + I_{D5} + I_{D3} + I_{D4})$

$= 1.8 \times (9.25 + 42.5 + 24.48) \times 10^{-6}$

$= 128.86\ \mu W$

Theoretical:

(i) $\left(\frac{W}{L}\right)_7 = 4.5$

(ii) $\left(\frac{W}{L}\right)_0 = 45$

(iii) $\left(\frac{W}{L}\right)_1 = 22.5$

(iv) $\left(\frac{W}{L}\right)_2 = 22.5$

(v) $\left(\frac{W}{L}\right)_3 = 3.5$

(vi) $\left(\frac{W}{L}\right)_4 = 3.5$

(vii) $\left(\frac{W}{L}\right)_5 = \cancel{23}\ 3.7$

(viii) $\left(\frac{W}{L}\right)_6 = 22$

(ix) Stage-1 gain = 101.76

(x) ~~Stage~~ g_{m2} = 4.03×10^{-4}

(xi) Stage-2 gain = 24.67

(xii) g_{m5} = 9.4×10^{-5}

(xiii) overall gain = 2510.61

(xiv) Closed loop gain = 2.124

Practical:

(i) $\left(\frac{W}{L}\right)_7 = 3.77$

(ii) $\left(\frac{W}{L}\right)_0 = 38.88$

(iii) $(W/L)_1 = 30$

(iv) $(W/L)_2 = 30$

(v) $(W/L)_3 = 3.55$

(vi) $(W/L)_4 = 3.55$

(vii) $(W/L)_5 = 4$

(viii) $(W/L)_6 = 21.11$

(ix) Stage-1 gain = 101.2 } open loop

(x) Stage-2 gain = 26.71 } open loop

(xi) overall gain = 2703.3 } open loop

(xii) Phase margin = 62^0

(xiii) Dominant pole = $521295\ s^{-1}$

(xiv) Power dissipation = 128.86 pW

(xv) Closed loop gain (overall) = 2.18