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A high-speed and scalable XOR-XNOR-based hybrid full adder design☆

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ABSTRACT

This work presents the design of a scalable and full-swing Full Adder (FA) based on the XOR-XNOR module. The performance of the design has been compared with eleven existing state-of-the-art FAs. The proposed FA obtains 19.35% improvement in Silicon area, 33.59% improvement in Average Power, 36.15% improvement in Propagation Delay, 56.22% improvement in Area Delay Product (ADP), and 57.59% improvement in Power Delay Product compared to the conventional Mirror CMOS FA. Moreover, performance parameters have been examined in wide adder structures by extending the FAs to 32-bits without adding level restoring buffers in the intermediate stages. The obtained simulation data suggest that the proposed FA and 5 out of the 11 existing FAs can be practically scaled up to 32-bits. The proposed FA showed superior performance in the 32-bit operation. Because of the improved features, the proposed hybrid FA can be a reliable and superior alternative to existing FAs.

1. Introduction

Modern electronic devices demand faster operation and longer battery life with minimum layout footprint [1]. However, silicon area and power dissipation are inversely proportional to the computing speed. Therefore, circuit designers need to make trade-offs to meet the system demand.

Arithmetic blocks perform an important role in digital microprocessors and consume a significant amount of power [2]. The arithmetic circuits are often responsible for generating hot spots in microprocessors, which need to be accounted for during circuit design. Several digital arithmetic applications rely highly on the effective design of arithmetic circuits. The addition of binary bits is of vital significance among the arithmetic operations since addition is essential in magnitude comparison, multiplication, division, and subtraction [3-4]. Moreover, the addition of digital bits is highly utilized in video processing, image processing, Fast Fourier Transform (FFT), digital signal processing, etc. Due to the widespread utilization of adder in various arithmetic operations and digital system designs, effective adder design methodology will bring about a comprehensive change in the system performance.

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In digital arithmetic circuits, the Full Adder (1-bit adder) is a core component, which is required to build wide word-length adders [5]. The Full Adder (FA) is usually part of the worst-case delay paths in most arithmetic circuits because of its repeated use in arithmetic operations [6]. As a result, the speed of digital arithmetic blocks in modern microprocessors is highly dependent on the propagation delay of the FAs.

This paper presents a high-speed and scalable hybrid FA based on the XOR-XNOR approach with a CCMOS structure in the last stage of the carry path for achieving the required drive power and speed in the cascaded FA stages. At first, an XOR-XNOR module has been proposed. Later, the carry-generation and sum generation circuits are implemented using the output signals of the XOR-XNOR module. The FA utilizes the hybrid logic design method. The performance evaluation of the proposed FA has been extensively carried out by comparing it with 12 existing FAs. The scalability of FAs has been tested by extending them to 32-bits. The proposed XOR-XNOR-based FA and its extended 32-bit version showed excellent performance according to the simulation conducted using Cadence tools at the 45nm technology node.

The paper is organized as follows. After the introduction in section 1, a literature review of the recent FA designs has been provided in section 2. Section 3 describes the proposed adder circuit and its operation principle. The simulation setup is explained in section 4. Simulation results, both for the proposed FA and its wide word length extension, are given in section 5. Section 6 outlines the major findings with the relevant discussions. Section 7 concludes the paper.

2. Existing Full Adder Designs

To cope up with the stringent energy and speed requirements of new electronic devices and applications, several FAs using different logic methods have been designed. As per logic technique, FAs are classified into two major groups: designs developed using a single logic method are called single logic FAs, while FAs that employ more than one logic method are known as hybrid FAs [7].

In the single logic domain, the FA design which utilizes Complimentary Pass Logic (CPL) is considered one of the oldest CMOS-based FA cells [8]. This FA cell can be built using 32 transistors. The critical issue associated with CPL FA is the reduction of voltage level due to the use of n-channel CMOS (NMOS) transistors. As NMOS passes weak logic 1, voltage restoring buffers are required in CPL logic, which further increases its Transistor Count (TC). Moreover, a large silicon area is required for implementing CPL FAs due to high TC. The Conventional CMOS (CCMOS) logic employing pull-down and pull-up networks was able to solve the issue of voltage reduction in CPL logic. FAs based on the CCMOS technique in [9] use 28 transistors to provide a full swing output voltage. Although the issue of voltage degradation was resolved through the use of the NMOS pull-down network and PMOS pull-up network, high TC remains a major issue, costing more layout area.

The hybrid logic-based adder design has gained much interest in recent times due to its several advantages over the single logic FA [10]. The hybrid design enables full swing logic circuits with significant performance improvement compared to the single logic-based circuits. Implementation using XOR-XNOR circuits is one of the widely utilized methods in hybrid FA design. FAs designed by Tirumalasetty *et al.* [11], Bhattacharyya *et al.* [12], Kandpal *et al.* [13] and Parameshwara *et al.* [14] are state-of-the-art XOR-XNOR-based designs. XOR-XNOR-based FAs in [11, 12, 14] required only 16 transistors to provide full swing output, whereas FA demonstrated by Kandpal [13] required 20 transistors.

In addition to the XOR XNOR-based designs, several hybrid FAs [15-18] have been reported. Hassoune *et al.* [15] provided a hybrid FA design using a combination of branched transistor (BT) network and pass transistors (PT). In addition to BT and PT, the utilization of CCMOS logic in the carry-out terminal provided ample drive power and scalability. The same condition applies to the carry-generation circuit of FA developed by Mirzaee *et al.* [17].

In recent years, Gate Diffusion Input (GDI) method-based VLSI circuit design has received high attraction due to its simplicity and ability to implement logic functions using fewer transistors [19-20]. However, GDI circuits lack drive power due to voltage degradation [21-22]. For the same reason, scalability is a major challenge. GDI-based FA designed by Sanapala *et al.* [23] used only 14 transistors. To deal with voltage degradation, Shoba *et al.* [24] proposed modified GDI method-based AND-OR and XOR-XNOR circuits, which can produce full swing outputs. Based on the modified GDI cells, the design of full swing GDI FA has been provided [24].

Although CCMOS FA is one of the oldest FA topologies, it is still widely used due to its robustness and versatility. Hybrid designs are becoming popular due to the ability to implement logic circuits with fewer transistors and improved performance. The GDI-based design method offers the ability to design circuits with low power consumption and smaller layout area. However, the threshold voltage drop issue limits its widespread application.

Table 1
Truth table of FA.

Input Pattern			Outputs	
C_{in}	A	B	C_{out}	Sum
0	0	0	0	0
	0	1	0	1
	1	0	0	1
	1	1	1	0
1	0	0	0	1
	0	1	1	0
	1	0	1	0
	1	1	1	1

3. Proposed XOR-XNOR-Based Hybrid Full Adder Design

The Truth Table of FA operation is presented in Table 1. Here, *A, B*, and$C_{in}$are the input bits whereas C_{out} and *Sum* are the output bits. Fig. 1 shows the block diagram of the proposed XOR-XNOR-based FA. It comprises an XOR-XNOR module followed by a TG-based module to generate the Sum output whereas a separate carry generation module takes the inputs from the XOR-XNOR module to generate the output C_{out}. These three different modules will be described in the following sub-sections.

3.1. XOR-XNOR Circuit Design

Table 2 depicts the operation of the proposed XOR-XNOR module and the corresponding circuit diagram is shown in Fig. 2. For different input-output patterns, the operation of the proposed XOR circuit can be understood as follows:

Input Pattern $AB = 00$: *XOR*output $= B = 0$ (since $B = 0$); for this input combination, p_3 transistor is ON, n_1 and n_2 transistors are OFF. Through p_3, strong logic 1 is passed on to the intermediate node *IND*. As a result, $IND = 1$ switches ON n_3 which causes XOR output to go down to strong logic 0 because of input $B = 0$. In addition to this, p_1 and p_2 transistors are ON through which weak zero is passed towards XOR output. However, in the case of hybrid design, if there exists at least one transistor path which provides strong logic 0, then, the output of the circuit will be strong logic 0 [11-18]. Since n_3 is providing strong logic 0 for input pattern $AB = 00$, the XOR output will be strong logic 0 for this case.

Input Pattern $AB = 01$: *XOR*output $= B = 1$ (since $B = 1$); for this input combination, p_2 transistor is ON (since input $A = 0$), and XOR output is pulled up to strong logic 1 because $B = 1$. Moreover, p_3 is ON for this input pattern by which strong logic 1 is passed on to the intermediate node *IND*. As a result, n_3 is switched ON and passes weak logic 1 to the XOR output. Furthermore, $B = 1$ switches ON n_1 through which weak logic 1 is passed on to the XOR output. However, there exists at least one transistor path (p_2 transistor) which provides full swing output without any voltage drop. Therefore, the output of the XOR for input pattern $AB = 01$ will be strong logic 1.

Input Pattern $AB = 10$: *XOR*output $= A = 1$ (since $A = 1$); for this input combination, p_1 transistor is ON (input $B = 0$) and XOR output is pulled up to strong logic 1 because $A = 1$.

Input Pattern $AB = 11$: *XOR*output $= 0$; for this input combination, n_1 and n_2 transistors are ON (since inputs $A = B = 1$) and XOR output is pulled down to strong logic 0.

Similarly, the operation of an XNOR circuit can be understood as follows:

Input Pattern $AB = 00$: *XNOR*output $= 1$; for this input combination, p_3 and $p_4$transistors are ON (inputs $A = B = 0$). Through p_3 and p_4, XNOR output is pulled up to strong logic 1.

Input Pattern $AB = 01$: *XNOR*output $= A = 0$ (since $A = 0$); for this input combination,n_5 transistor is ON (input$B = 1$) and XNOR output is pulled down to strong logic 0 because $A = 0$.

Input Pattern $AB = 10$: *XNOR*output $= B = 0$ (since $B = 0$); for this input combination,n_4 transistor is ON (input $A = 1$) and XNOR output is pulled down to strong logic 0 because $B = 0$. Moreover, $A = 1$ turns ON n_2 and the intermediate node *IND* is pulled down to strong logic 0. This $IND = 0$ turns ON p_5 through which weak logic 0 is passed towards the XNOR output. Furthermore, $B = 0$ turns ON p_4 through which weak logic 0 is passed towards the XNOR output. However, there is at least one transistor path (n_4) that provides strong logic 0 to the XNOR output. Therefore, for the input pattern $AB = 10$, the final XNOR output will be a strong logic 0.

Input Pattern $AB = 11$: *XNOR*output $= 1$ (since $B = 1$); for this input combination, n_2 transistor is ON and p_3 and p_4 transistors are OFF. As a result, strong logic level 0 is passed on to the intermediate node *IND* through n_2. This $IND = 0$ switches ON p_5 which causes XNOR output to be pulled up to strong logic 1 because of input $B = 1$. Moreover, n_4 and n_5 transistors are ON for $AB = 11$ which provides weak logic 0 towards the XNOR output. But, since n_2 provides strong logic 0, the final XNOR output for $AB = 11$ is weak logic 0.

Table 2 provides a complete summary of the full swing and non-full swing transistor paths for all possible input combinations of the XOR-XNOR module. From the Table, it can be seen that for each input pattern, there is at least one transistor path that can provide full-swing output without any threshold voltage drop issue. As a result, the proposed hybrid XOR-XNOR produces full swing output.

3.2. Sum Generation Circuit

With careful observation of the input-output logic levels of *Sum* in Table 1, the following set of conditions are required to implement the *Sum* generation circuit.

Condition no. 1: When $C_{in} = 0$, $Sum = A \oplus B$ (XOR operation between *A* and *B*)

Condition no.2: When $C_{in} = 1$, $Sum = A \overline{\oplus} B$ (XNOR operation between *A* and *B*)

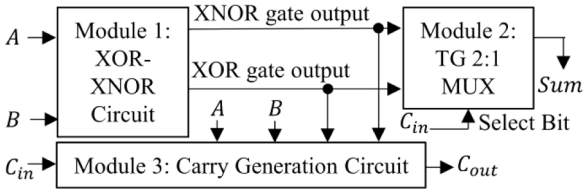

Fig. 1. Block diagram of proposed XOR-XNOR-based FA.

Table 2
Operation table of XOR-XNOR module.

XOR Circuit					
	Input Side		Output Transistor Path		Output Side
Pattern no.	*A*	*B*	Full Swing Transistor Path	Non-Full Swing Transistor Path	Output Signal/logic
1.	0	0	n_3	p_1/ p_2	*B*/0
2.	0	1	p_2	n_1/ n_3	*B*/1
3.	1	0	p_1	None	*A*/1
4.	1	1	n_1 and n_2	None	0
XNOR Circuit					
	Input Side		Output Transistor Path		Output Side
Pattern no.	*A*	*B*	Full Swing Transistor Path	Non-Full Swing Transistor Path	Output Signal/logic
1.	0	0	p_3 and p_4	None	1
2.	0	1	n_5	None	*A*/0
3.	1	0	n_4	p_4/p_5	*B*/0
4.	1	1	p_5	n_4/n_5	*B*/1

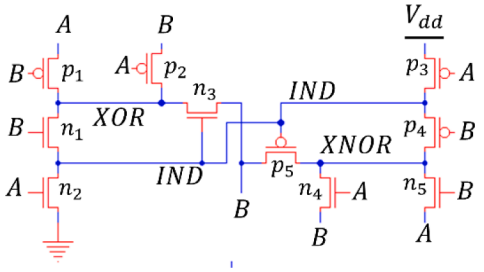

Fig. 2. Proposed XOR-XNOR Circuit.

For implementing the conditions mentioned above, a 2:1 Multiplexer (2:1 MUX) based on Transmission Gate (TG) has been used. In Fig. 3, TG_1 (comprised of n_6 and p_6) and TG_2 (comprised of n_7 and p_7) are used to implement 2:1 MUX for the *Sum* generation circuit. Since TG can pass strong logic 0 and strong logic 1, the *Sum* generation circuit will provide full swing output.

3.3. Carry Generation Circuit

The carry generation module, as shown in Fig. 3, is considered the most important part of FA since the scalability of a FA design depends highly on the signal strength of the carry-out signal (C_{out}). In wide word length adders, the C_{out} of one FA stage is utilized as the C_{in} signal of the next stage. Therefore, the C_{out} signal of FA needs to have ample drive power and the voltage level needs to be

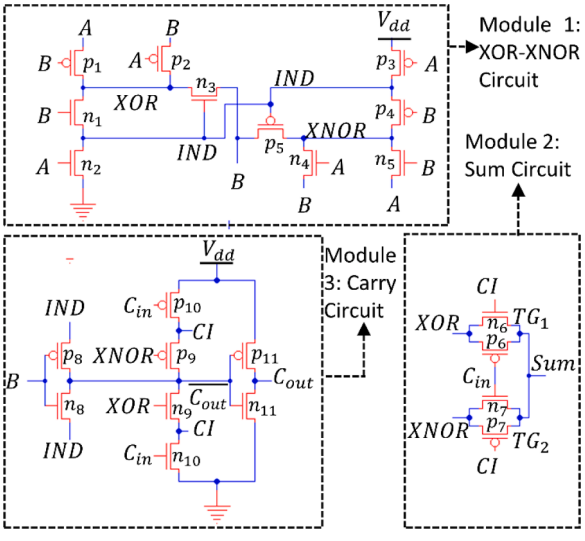

Fig. 3. Proposed FA Circuit.

replenished. For this reason, the proposed C_{out} circuit consists of CCMOS logic-based inverter at the output terminal which consists of a pull-up transistor p_{11} and a pull-down transistor n_{11}. In the case of CCMOS logic, the output terminal is either connected to V_{dd} (pull-up transistor p_{11}) or connected to *Gnd* (pull-down transistor n_{11}) for which the output voltage level of the proposed C_{out} circuit is either V_{dd} or *Gnd*. Therefore, when the circuit is extended to multiple bits, the output voltage of the carry circuit in each stage obtains V_{dd} or *Gnd* level. As a result, the design can be scaled up to wide adder architectures without adding voltage level restoring buffers. In addition, CCMOS logic provides adequate driving power to the circuit. Moreover, the inverter at the output reduces the carry chain delay due to the presence of only one pull-up and pull-down transistors.

As per Table 1, the operation of the C_{out} generation module for different input patterns can be understood as follows:

Input patterns $AB = 00$ or $AB = 11$: $\overline{C_{out}} = IND$, $C_{out} = \overline{IND}$. For $AB = 00$ combination, p_8 and n_{11} transistors are switched ON. PMOS p_8 provides strong logic 1 to the gate of n_{11} since $IND = 1$ for this case. This turns ON n_{11} by which the C_{out} output is pulled down to strong logic 0. On the other hand, for $AB = 11$ combination, n_8 and p_{11} transistors are switched ON. NMOS n_8 provides strong logic 0 to the gate of p_{11} since $IND = 0$ for this case. This turns ON p_{11} by which the C_{out} output is pulled up to strong logic 0. The carry output C_{out} is independent of C_{in} for these patterns ($AB = 00$ or $AB = 11$).

Input patterns $C_{in} = 0$, $AB = 01$or $AB = 10$: $Cin = 0$ and $XNOR = 0$ (for $AB = 01/10$, $XNOR = 0$) will switch ON p_{10} and p_9. Therefore, the $\overline{C_{out}}$ node will be pulled up to '1' through p_{10},p_9. This $\overline{C_{out}} = 1$ will switch ON $n_{11}$by which C_{out} will be pulled down to '0'.

Input patterns $C_{in} = 1$, $AB = 01$or $AB = 10$: $Cin = 1$ and $XOR = 1$ (for $AB = 01/10$, $XOR = 1$) will switch ON n_{10} and n_9. Therefore, the $\overline{C_{out}}$ node will be pulled down to logic '0' through n_{10} and n_9. This $\overline{C_{out}} = 0$ will switch ON p_{11} by which C_{out} will be pulled up to '1'.

The layout of the proposed FA cell is shown in Fig. 4 and the corresponding transistor sizes are given in Table 3.

4. Circuit Simulation Setup and Parameters

FAs have been implemented using Cadence circuit design and simulation tools. The transistor technology used for implementing FA designs is the 45 nm CMOS process. The simulation test bench is presented in Fig. 5 which is similar to the test benches used in [13, 16, 18]. At first, square-shaped signals are generated by In_A, In_B, and In_C_{in}. The signals generated by In_A, In_B, and In_C_{in} are then passed through buffers in order to incorporate distortion in the signals. Outputs of the buffers (A, B, and C_{in}) are considered as inputs to the FA cells. *Sum* and C_{out} are the output terminals of the FA cell. For the load circuit, a fan out of 4 unit-size inverters (FO4) has been added with the output terminals (*Sum* and C_{out}). Some existing papers used buffers in the output terminals as load circuits [21, 22]. If a buffer is used as the load circuit, then, only the 1st inverter of the buffer acts as load whereas the 2nd inverter of the buffer does not have any effect on the circuit. Therefore, using a buffer at the output terminal load circuit is unnecessary. This is the main reason, why this research and some recent papers [13, 16, 18] used FO4 inverter at the output terminal as load. For simulation, the proposed FA is implemented using the transistor sizes provided in Table 3. In the case of existing designs, transistor channel lengths are selected as 45 nm for all cases. Channel widths are selected in an appropriate manner in order to ensure optimal performance.

Average Power Consumption (APC), Propagation Delay (PD) due to the critical path, Area Delay Product (ADP), and Power Delay Product (PDP) are the major parameters that have been used to compare the performance of FAs. For APC, all possible patterns of the input signals are applied to the Circuit Under Test (CUT). Power consumption due to each of the input signal patterns has been calculated. Finally, APC is determined by taking the average of the previously calculated power dissipations. The power consumption occurred due to the output side FO4 inverters and the input side buffers are not taken into consideration while calculating the APC of a FA cell.

In CMOS circuits, different input patterns result in different PDs. However, there exists one delay path for which the maximum PD occurs. This delay path is known as the critical path delay or worst-case delay path. For PD calculation in this research, critical path PD has been considered. The PDP is obtained by multiplying critical path PD by APC. The ADP design metric is computed by multiplying

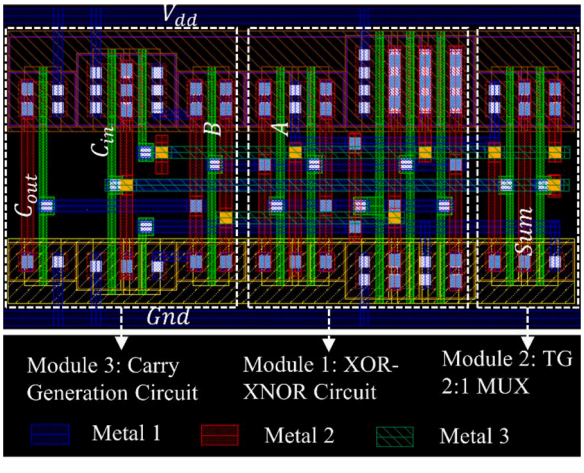

Fig. 4. Layout of the proposed XOR-XNOR-based FA.

Table 3
Transistor sizes used to implement the proposed FA.

Transistor Identification	Type of Transistor	Channel Width (nm)	Channel Length (nm)
n_1,n_2,n_3	N-MOS	240	45
n_9,n_{10}	N-MOS	180	45
n_4,n_5,n_6,n_7,n_8,n_{11}	N-MOS	120	45
p_3,p_4,p_5	P-MOS	480	45
p_9,p_{10}	P-MOS	360	45
p_1,p_2,p_6,p_7,p_8,p_{11}	P-MOS	240	45
	Minimum Allowable Channel Width of PMOS and NMOS: 120 nm		

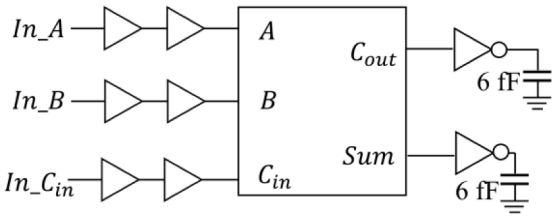

Fig. 5. 1-bit FA Simulation Test bench.

the Area with the PD. The simulation results are obtained after the post-layout simulation.

In the case of VLSI circuit design, simulation, and analysis, a proper simulation testbench is necessary. A common simulation testbench ensuring the same simulation criteria is required to compare several circuits. Therefore, the same simulation testbench has been used for simulating all the FAs.

5. Simulation Result, Discussion, and Comparison

At first, the input versus output graph has been plotted in section 5.1, which verifies the functionality of the proposed FA. Then, the FAs (existing and proposed) are tested as single cells. To investigate scalability, the FAs have been extended to 32-bits. Simulation results and comparative analysis of FA designs are discussed in Sections 5.2 and 5.3.

5.1. Input-Output Logic Verification and Voltage Level Analysis

To analyze and verify the functionality of the proposed FA cell, the input versus output graph has been plotted in Fig. 6 using 1 V as the supply voltage. Fig. 6 contains all possible input patterns for the FA and the corresponding outputs. From Fig. 6, it is visible that the output voltage levels of the XOR-XNOR module, *Sum*, and C_{out} circuits are equal to the input voltage level. Therefore, it can be inferred that the proposed FA design achieves full swing outputs without exhibiting any threshold voltage drop issues.

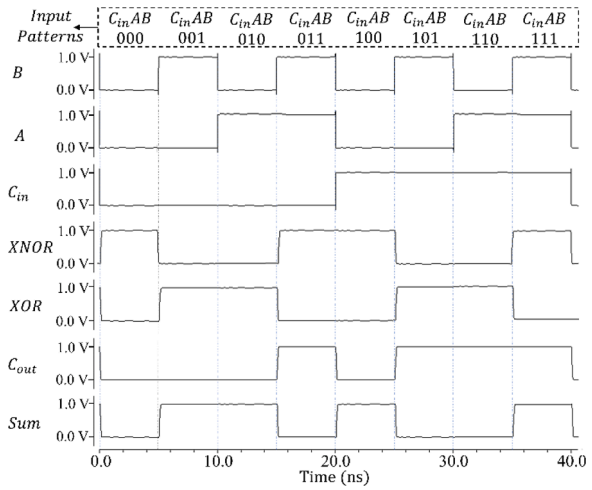

Fig. 6. Input versus output waveform of the proposed FA.

5.2. Full Adder Cell Performance

For 1-bit FA performance analysis, at first, the designs have been analyzed by applying 1 V supply voltage using the simulation testbench in Fig. 5. The APC, PD, PDP, and ADP obtained are given in Table 4. To observe the impact of supply voltage variation of FA performance, 0.6 V-1.2 V supply voltages have been applied to the circuits. The results are shown in Figs. 7-9.

From simulation data presented in Fig. 8 and Table 4, it is obvious that the proposed XOR-XNOR-based FA design achieved foremost performance in speed since its PD is the lowest. The deliberate utilization of the C_{in} signal as the gate control signal of p_{10} and n_{10} transistors is the main reason behind the high-speed performance. The transistor p_{10} falls in the fall-time critical path, whereas, the n_{10} transistor falls in the rise-time critical path. Being one of the input signals, C_{in} appears in the gates of p_{10} or n_{10} before the XOR-XNOR signals are computed. For this reason, C_{in} turns ON p_{10} or n_{10} before the p_9 or n_9 transistors are turned on. As a result, signals appear in the source/drain of p_9 or n_9 through p_{10} or n_{10} before p_9 or n_9 are turned ON. Therefore, the rise-time or fall-time critical path does not experience the delay due to p_{10} or n_{10} and consequently results in high-speed operation.

In the case of APC, the proposed FA obtained better results than 6 of the 11 existing FAs reported in this research. In the case of APC, the performance of Bhattacharyya's [12], Tirumalasetty's [11], Parameshwara's [14], Sanapala's [23], and Valashani's [16] FAs are superior to the proposed FA. However, as presented in Fig. 7, the APC of the proposed FA design is still satisfactory. Due to high speed and satisfactory APC, the FA design in this work achieved the foremost performance in PDP. Moreover, the ADP design metric is also minimum for the proposed design. The transistor count and layout area data presented in Table 4 show that the layout area is not fully dependent on the transistor count, i.e., two designs having the same transistor count may not have the same layout area.

5.3. Full Adder Performance in Wide Word-Length Adders

In the practical microprocessor design process, fundamental digital circuits need to have scalability, so that they can be extended to wide word-length architectures. Therefore, the scalability of the FA circuits needs to be examined. To do so, all FA circuits have been extended to 32-bits using a simple Ripple Carry Adder (RCA) structure, as expressed in Fig. 10 [25]. In the case of the FA circuits in RCA style, no voltage level restoring buffers have been added. Supply voltage has been fixed to 1 V. Obtained simulation results of FAs operating in wide word-length RCA structures have been listed in Table 5. The simulation results presented in Table 5 imply that the proposed XOR-XNOR-based FA is scalable along with 5 out of the 11 existing FA designs. For the remaining 6 existing designs, voltage degradation of the carry signal passing through a series of FA stages was the main reason behind the lack of scalability. As discussed in section 3.3, the proposed carry-generation circuit has CCMOS logic in the outermost part. Therefore, in a wide word-length structure, the output carry signal gets replenished to V_{dd} or *Gnd* level after each stage of FA operation. As a result, the carry signal never gets degraded while propagating through a series of FA stages. The layout of 32-bit RCA implemented using the proposed XOR-XNOR-based FA is presented using Fig. 11.

Table 5 confirms the scalability of the proposed FA design. Moreover, the obtained simulation results demonstrate that the performance of the proposed FA, in terms of APC, PD, and PDP, is superior to the existing FAs when extended to a structure of 32 bits.

6. Discussion

Investigation of the simulation data presented in Tables 4-5 shows that Tirumallasetty's [11], Bhattacharrya's [12], Kandpal's [13], Parameshwara's [14], Valashani's [16], and Sanapala's [23] FAs could not be extended to 32-bits despite having satisfactory and acceptable performance parameters while operating as a 1-bit adder. As discussed in section 5.3, voltage degradation of the same carry signals passing through several stages is the main reason behind its inability to operate in large structures. According to the analysis conducted in [12], voltage level restoring buffers are required after every 4-bit operation to scale up Bhattacharrya's FA [12] to 32-bits. Although adding voltage level restoring buffers seem to be a solution, this will add a large number of inverters in the critical path of the adder for which the circuit will experience speed issues. For example, if buffers are required after every 4-bit operation [12], a 32-bit RCA adder will require a total of 8 buffers (16 inverters). These 8 buffers will be directly added in series with the critical

Table 4
Full Adder performance investigation with 1 V supply voltage.

Full Adder Cell	TC	Performance Parameters					Percentage Improvements with Respect to CCMOS FA				
		Area (μm^2)	AP (μW)	PD (ps)	ADP (μm^2.ps)	PDP (aJ)	Area (%)	AP (%)	PD (%)	ADP (%)	PDP (%)
CCMOS [9]	28	10.13	1.28	60.3	610.84	77.18	0.00	0.00	0.00	0.00	0.00
Tirumalasetty's [11]	16	7.82	0.65	83.34	651.72	54.17	22.80	49.22	-38.21	-6.69	29.81
Bhattacharrya's [12]	16	7.58	***0.62***	98.7	748.15	61.19	25.17	***51.56***	-63.68	-22.48	20.72
Kandpal's [13]	20	9.18	0.92	54.06	496.27	49.74	9.38	28.13	10.35	18.76	35.55
Parameshwara's [14]	16	7.41	0.7	51.2	379.39	35.84	26.85	45.31	15.09	37.89	53.56
Hassoune's [15]	24	10.16	1.48	79.15	804.16	117.14	-0.30	-15.63	-31.26	-31.65	-51.78
Valashani's [16]	18	7.98	0.79	74.8	596.9	59.09	21.22	38.28	-24.05	2.28	23.44
Mirzaee's [17]	22	9.26	1.15	66.0	611.16	75.9	8.59	10.16	-9.45	-0.05	1.66
Kumar's [18]	27	10.05	0.78	82.31	827.22	64.2	0.79	39.06	-36.50	-35.42	16.82
Sanapala's [23]	14	***7.38***	0.75	56.7	415.45	42.53	***27.15***	41.41	5.97	31.99	44.90
Shoba's [24]	22	8.74	1.06	42.8	374.07	45.37	13.72	17.19	29.02	38.76	41.22
Proposed	22	8.17	0.85	***38.5***	***267.40***	***32.73***	19.35	33.59	***36.15***	***56.22***	***57.59***

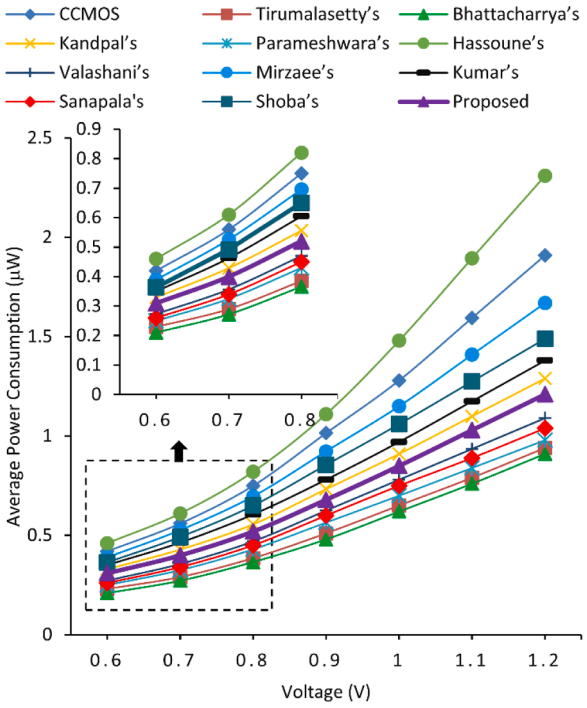

Fig. 7. Average Power analysis of FAs with different supply voltages.

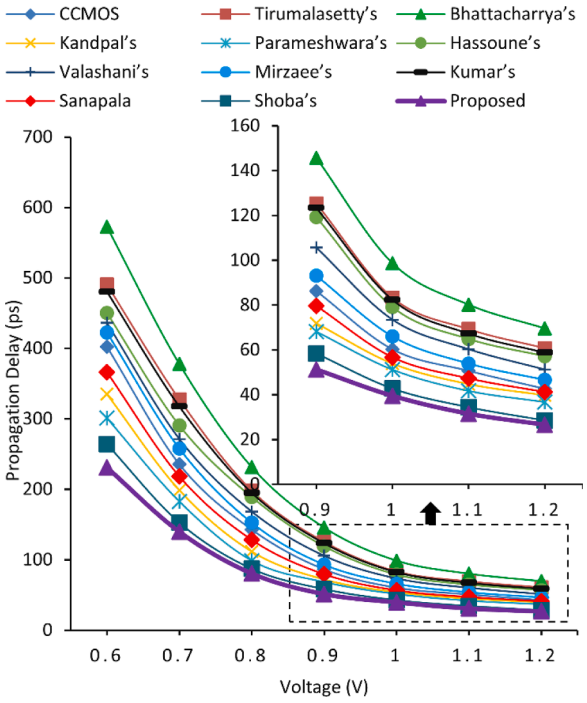

Fig. 8. Propagation Delay (PD) analysis of FAs with different supply voltages.

carry-generation path for which the circuit will experience severe speed issues. Moreover, the addition of these buffers will cost more hardware and silicon area. In addition, the power consumption of the circuit will intensify due to the incorporation of level restoring buffers. Furthermore, industrial IC designers prefer designs that can be simply used in the system without the requirement of extra hardware. For these reasons, the incorporation of extra level restoring buffers is not practically an effective solution. Rather, adder

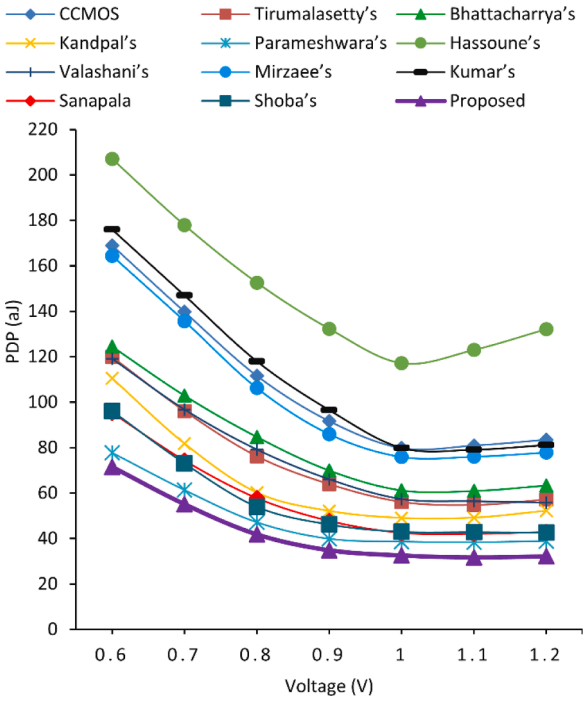

Fig. 9. PDP analysis of FAs with different supply voltages.

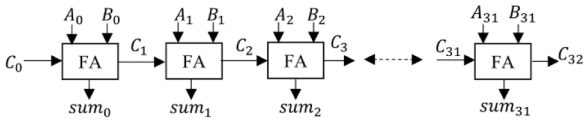

Fig. 10. 32-bit RCA using FA.

circuits are required to be designed in such a way that eliminates the need of incorporating level restoring buffers. Hence, in this research, no level restoring buffers are added in intermediate stages of RCA extension to show a clear distinction between the FAs which are scalable without buffers, and the FAs which are unable to operate without buffers.

As already explained in sections 3.3 and 5.3, the outer terminal of the proposed XOR-XNOR-based FA consists of a CCMOS-based inverter which helps in extending it to multiple bits without the requirement of adding level restoring buffers. Due to the same reason, Hassoune's [15] and Mirzaee's [17] are scalable. In case of Tirumallasetty's [11], Bhattacharrya's [12], Kandpal's [13], Parameshwara's [14], Valashani's [16], and Sanapala's [23] FAs, the C_{in} signal is used in the source/drain of the transistors. When the C_{in} signal is used in the source/ drain, then, the same carry signal is passed from one FA stage to another. While passing through several FA stages, the voltage level deteriorates. This is the main reason behind the inability to operate in a large adder structure for these FAs. For Kumar's [18] and Shoba's [24] FAs, the designs do not incorporate a CCMOS-based circuit in the outermost terminal of the carry-generation circuit. However, the designs could be extended to 32-bits because C_{in} is only used as the gate control of transistors.

After analyzing Table 5, it becomes obvious that in a wide word-length adder structure, CCMOS FA performs better than most of the existing state-of-the-art FAs. This is the main reason for the widespread utilization of CCMOS logic despite being one of the most basic and oldest VLSI circuit design methods. However, CCMOS FA is slower than Shoba's and proposed FA for wide word-length RCA. $\overline{C_{out}}$ signal of CCMOS FA needs to drive more transistors compared to the proposed FA due to which the rise/ fall time of $\overline{C_{out}}$ signal in CCMOS FA is longer. Moreover, CCMOS FA has the highest transistor count (TC) among the FAs reported in this research. Due to this high TC, each input signal faces high input impedance due to which it takes more time for the signals to turn on the transistors. In addition, parasitics associated with interconnects become a major source of concern in lower technology nodes. Circuits with a higher transistor count (CCMOS FA) require a high layout area and interconnects. Therefore, the speed and power degrade in general for higher transistor count circuits at the nanoscale due to the excessive delay and power contribution by the dominating interconnect parasitics. Furthermore, the CCMOS FA has more series-connected transistor paths compared to the existing designs. To reduce resistance in series transistor paths, the transistor width needs to be increased to decrease resistance. However, increasing channel width increases gate capacitance and hence input impedance. These are the main reasons why the CCMOS FA has less speed in RCA compared to Shoba's and proposed FAs. It should be mentioned that as technology scales down, circuits need to operate at very low voltages where IR drop becomes a major issue of concern. Therefore, transistor resistance should be properly dealt with to reduce the

Table 5
FA performance observation in wide word-length adder structures.

Full Adder	Average Power (AP) AP (μW) Bit-Width				Percentage Improvements with Respect to CCMOS FA Bit-Width			
	4	8	16	32	4	8	16	32
CCMOS [9]	4.84	9.41	18.59	36.94	0.00	0.00	0.00	0.00
Tirumalasetty's [11]	2.57	5.18	CNO	CNO	46.90	44.95	CNO	CNO
Bhattacharrya's [12]	***2.62***	***4.77***	CNO	CNO	45.87	49.31	CNO	CNO
Kandpal's [13]	3.79	7.78	CNO	CNO	21.69	17.32	CNO	CNO
Parameshwara's [14]	2.88	5.93	CNO	CNO	40.50	36.98	CNO	CNO
Hassoune's [15]	5.5	10.59	20.61	40.56	-13.64	-12.54	-10.87	-9.80
Valashani's [16]	3.28	7.04	CNO	CNO	32.23	25.19	CNO	CNO
Mirzaee's [17]	4.81	9.73	19.58	40.48	-1.45	-3.40	-5.33	-9.58
Kumar's [18]	3.017	6.01	11.98	24.21	37.67	36.13	35.56	34.46
Sanapala's [23]	3.04	6.11	CNO	CNO	37.19	6.11	CNO	CNO
Shoba's [24]	4.33	8.92	18.64	39.07	10.54	10.52	10.49	10.48
Proposed	3.48	6.69	***13.13***	***28.87***	28.10	28.91	29.05	29.16

Full Adder	Propagation Delay (PD) PD (ns) Bit-Width				Percentage Improvements with Respect to CCMOS FA Bit-Width			
	4	8	16	32	4	8	16	32
CCMOS [9]	0.245	0.501	1.009	2.203	0.00	0.00	0.00	0.00
Tirumalasetty's [11]	0.442	3.051	CNO	CNO	-82.64	-499.41	CNO	CNO
Bhattacharrya's [12]	0.718	3.411	CNO	CNO	-196.69	-570.14	CNO	CNO
Kandpal's [13]	0.228	2.471	CNO	CNO	5.79	-385.46	CNO	CNO
Parameshwara's [14]	0.298	1.58	CNO	CNO	-23.14	-210.41	CNO	CNO
Hassoune's [15]	0.322	0.651	1.349	2.817	-28.93	-27.90	-27.80	-27.87
Valashani's [16]	0.241	1.318	CNO	CNO	0.41	-158.94	CNO	CNO
Mirzaee's [17]	0.269	0.562	1.129	2.264	-11.16	-10.41	-10.19	-10.03
Kumar's [18]	0.331	0.682	1.403	2.957	-34.71	-33.99	-33.73	-33.77
Sanapala's [23]	0.421	3.04	CNO	CNO	-73.97	6.11	CNO	CNO
Shoba's [24]	0.175	0.366	0.768	1.55	27.69	28.09	28.82	29.64
Proposed	***0.163***	***0.342***	***0.713***	***1.438***	32.64	32.81	33.92	34.73

Full Adder	Power Delay Product (PDP) PDP (fJ) Bit-Width				Percentage Improvements with Respect to CCMOS FA Bit-Width			
	4	8	16	32	4	8	16	32
CCMOS [9]	1.185	4.714	18.767	74.951	0.00	0.00	0.00	0.00
Tirumalasetty's [11]	1.316	15.83	CNO	CNO	3.02	-229.96	CNO	CNO
Bhattacharrya's [12]	1.881	16.27	CNO	CNO	-60.61	-239.70	CNO	CNO
Kandpal's [13]	0.864	19.224	CNO	CNO	26.22	-301.37	CNO	CNO
Parameshwara's [14]	0.858	9.369	CNO	CNO	26.73	-95.62	CNO	CNO
Hassoune's [15]	1.771	6.894	27.802	114.25	-46.51	-43.94	-41.69	-40.40
Valashani's [16]	0.79	9.279	CNO	CNO	32.51	-93.72	CNO	CNO
Mirzaee's [17]	1.294	5.468	22.106	91.646	-12.76	-14.17	-16.06	-20.58
Kumar's [18]	0.999	3.919	16.808	71.558	16.03	14.42	13.82	12.33
Sanapala's [23]	1.28	18.57	CNO	CNO	-9.27	6.11	CNO	CNO
Shoba's [24]	0.758	3.265	13.932	62.968	35.31	35.66	36.29	37.01
Proposed	***0.565***	***2.287***	***9.362***	***41.515***	51.57	52.23	53.12	53.76

CNO: Could not Operate

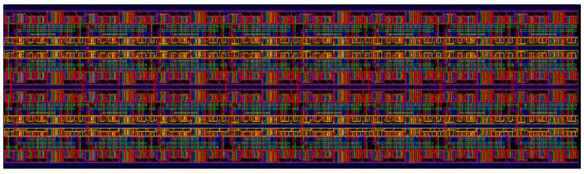

Fig. 11. The layout of 32-bit RCA using the proposed XOR-XNOR-based FA.

possibility of IR drop in lower technology nodes (such as 45 nm or lower).

7. Conclusion

A full-swing hybrid FA implementation using the XOR-XNOR module is presented in this research. The FA design has been

implemented using Cadence design and simulation tools. A comparative analysis of existing and proposed FAs has been presented. Compared to the conventional CCMOS FA, the proposed FA exhibits 19.35% improvement in silicon area, 33.59% improvement in Average Power, and 36.15% improvement in Propagation Delay. The scalability of existing and proposed FA designs in wide word-length architecture has been investigated by extending the designs to 32-bits. When extended to a 32-bit configuration, the percentage of improvements are 29.16% in Average Power, 34.73% in Propagation Delay, and 53.76% in PDP, when compared to the CCMOS FA. The simulation-based analysis conducted in this work proves that the proposed FA design is highly suitable for modern high-performance VLSI arithmetic block designs. As a future scope of this work, the effect of using the proposed FA in other arithmetic blocks such as multiplication, subtraction, magnitude comparison can be analyzed.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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