PI15592 8-Channel Control IC
12-bit ADC/DAC and GPIO with SPI Interface

1 Features

- **8 general purpose I/O.**
  - Each I/O configurable as DAC or ADC or GPIO.
  - Each I/O read by ADC
- **8 Voltage DACs**
  - 12-bit with Vref or 2*Vref full scale
  - 35mA output.
- **8 input ADC**
  - 12-bit, 500ksps
  - 8 external inputs
  - Temperature sensor
- **Internal Voltage Reference**
- **GPIO**
  - Configurable options: pull-down, open drain, High Impedance
- **SPI Slave**
- **Reset**
  - Both hardware pin and software bit are available to reset the PI5592 to its default, power-on state

2 Applications

- **Fiber Optic Modules**
- **Analog and Digital Inputs and Outputs**
- **Mixed Signal Control and Monitoring**

3 Package Options

Operating temperature range: –40°C to +105°C

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PI15592	16 pin WLCSP	2.0 mm × 2.0 mm

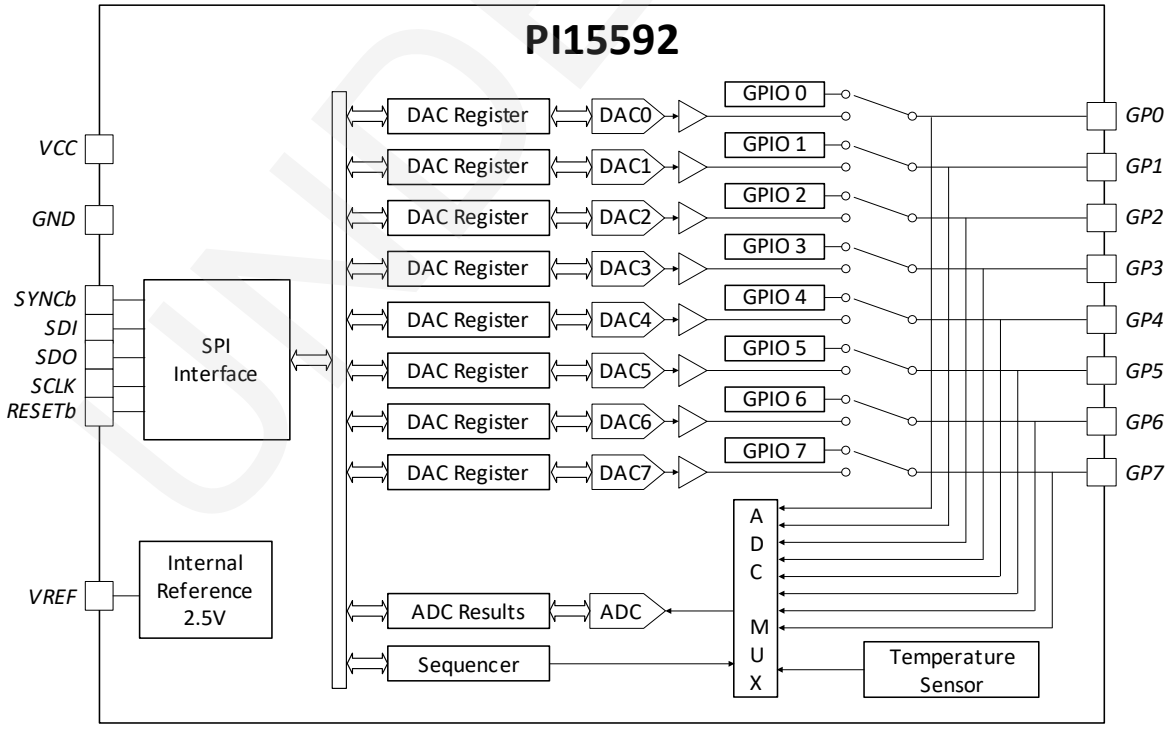

Figure 1: PI15592 Block Diagram

4 Table of Contents

5 Pin Description

PIN	NAME	FUNCTION
B4	VCC	Positive supply. Decouple with 0.1uF capacitor to GND.
B3	GP0	Voltage DAC, GPIO. ADC Input.
C4	GP1	Voltage DAC, GPIO. ADC Input.
C3	GP2	Voltage DAC, GPIO. ADC Input.
C2	GP3	Voltage DAC, GPIO. ADC Input.
D3	VREF	Voltage Reference input or output. Decouple with 4.7uf capacitor to GND.
D2	SDO	Serial Data Out
D1	GP4	Voltage DAC, GPIO. ADC Input.
D4	GP5	Voltage DAC, GPIO. ADC Input.
C1	GP6	Voltage DAC, GPIO. ADC Input.
B2	GP7	Voltage DAC, GPIO. ADC Input.
B1	GND	Ground.
A1	SDI	Serial Data In
A2	SCLK	Serial Clock.
A3	RESETb	Reset Pin. Active low. Pull low to reset registers to initial conditions. Optionally, the GPIO and DAC outputs may be retained during reset.
A4	CSb	Chip Select. Active low

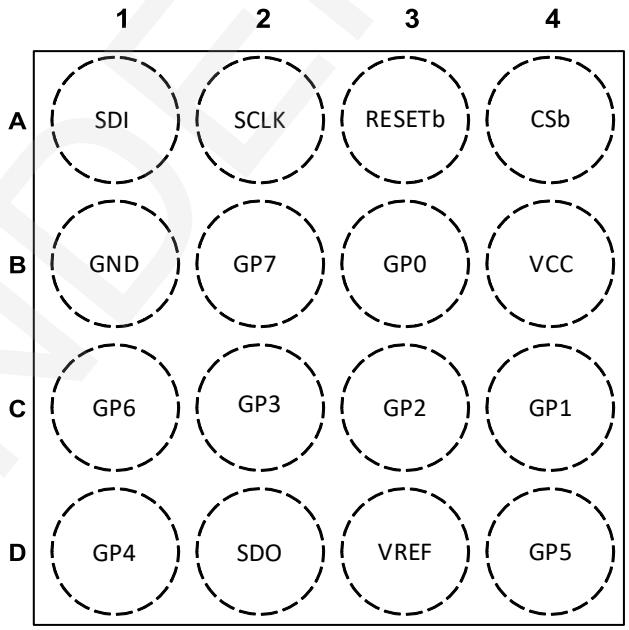

Figure 2. WLCSP-16 pin out.

6 Package Outline Drawing

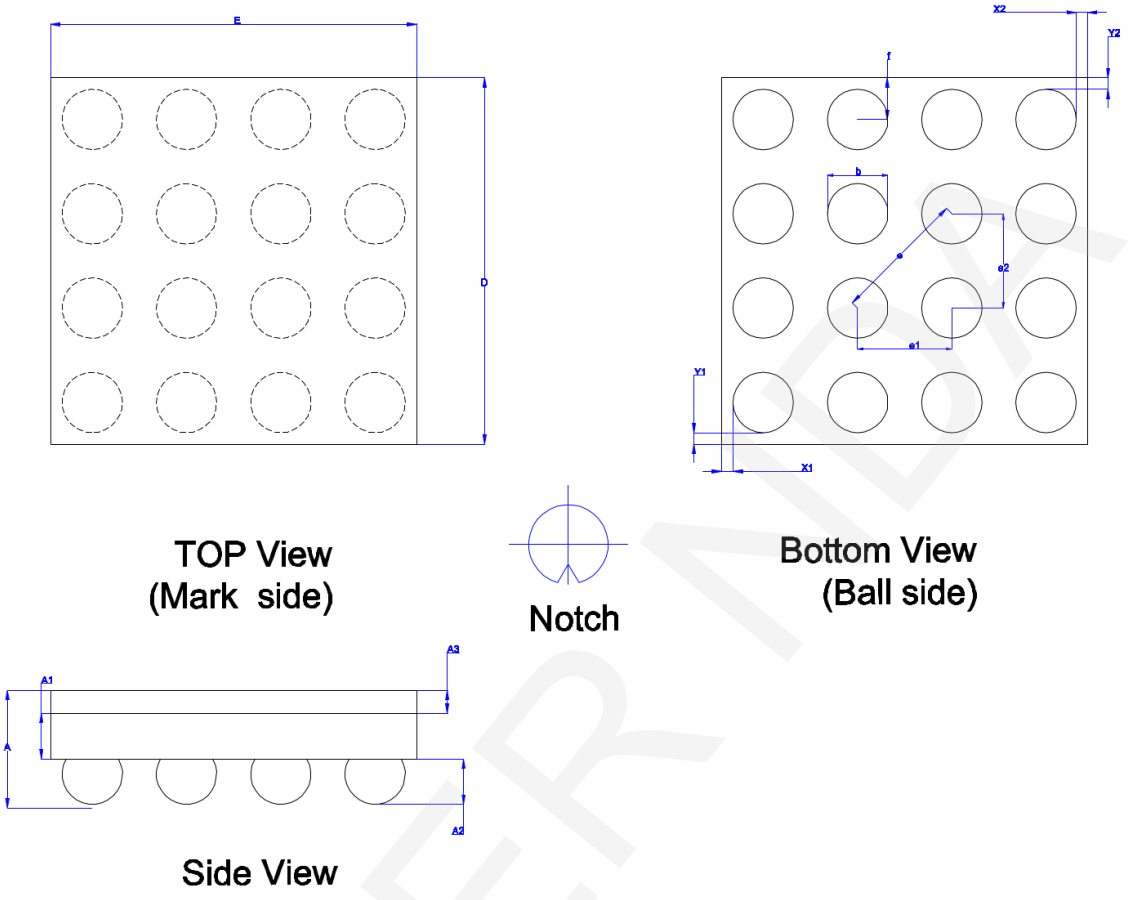

Table1: Package Dimension

Parameter	Symbol	Nominal(um)	Min(um)	Max(um)
Package Height	A	615	580	650
Package Body Thickness	A1	350	325	375
Ball Height	A2	240	215	265
BSC	A3		25	
Package Body Dimension x	E	1940.00	1910.00	1970.00
Package Body Dimension y	D	1940.00	1910.00	1970.00
Ball pitch	e		707.1 REF	
Ball pitch	e1		500	
Ball pitch	e2		500	
Ball Center to Edge Distance	f		220	
Ball Diameter	b	320	290.0	350.0
Ball Count			16 ea	
Edge to Ball Edge Distance along x	X1		60 REF	
Edge to Ball Edge Distance along y	Y1		60 REF	
Edge to Ball Edge Distance along x	X2		60 REF	
Edge to Ball Edge Distance along y	Y2		60 REF	

Figure 3. WLCSP-16 dimensions.

7 Specifications

7.1 Absolute Maximum Ratings

Across recommended operating junction temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply Voltage	V_{CC} to GND	–0.3	7	V
Pin Voltage	SDI, SDO, SCLK, CSb, RESETb to GND	–0.3	7	V
	GP[7:0] to GND	– 0.3	V_{CC} + 0.3	V
	VREF to GND	–0.3	V_{IO} + 0.3	V
Temperature	Operating Junction temperature Range	–40	150	°C
	Storage temperature, T_{stg}	–65	150	°C
	Soldering Lead Temperature Range	JEDEC J-STD-020		

(1) Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. The product may not operate correctly while it is stressed to the values listed in this table.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±500	

(1) Stresses beyond those listed under *ESD Ratings* may cause permanent damage to the device.

7.3 Thermal Information

PACKAGE	Θ_{JA} (1)	UNIT
WLCSP-16	60	°C/W

(1) JEDEC standard 4-layer PCB.

8 Electrical Characteristics

All minimum/maximum specifications at T_A=–40℃ to +105℃, VCC =2.7 V to 5.5V, VREF=2.5V and all outputs unloaded (unless otherwise noted).

All typical specifications at T_A=25℃, VCC=3.3V, VREF=2.5V, and DAC outputs unloaded (unless otherwise noted).

8.1 DAC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		12			Bits
INL	INL			±5		LSB
DNL	DNL		-1		+1	LSB
	Full Scale	Gain of 1			+ VREF	V
		Gain of 2, 4.5 V < VCC			+2* VREF	V
	Load Current	Sourcing: (V_GPx + 0.5 V) < VCC			35	mA
		Sinking: (Ground + 0.5 V) < V_GPx	-35			mA
	Output Impedance at Rails			14		Ω
	Settling Time	0.5% change, settled to 1 LSB		10		µs
		25% FS to 75% FS settled to 1 LSB		12		µs
	Offset Error at T_A=25°C	0V < GPx < VREF, VCC = 3.3V	-2	0	+2	mV
		0V < GPx < 2 * VREF, VCC = 5V	4	7	10	mV
	Offset Error Drift	0V < GPx < VREF, VCC = 3.3V		25		µV/°C
		0V < GPx < 2 * VREF, VCC = 5V		50		µV/°C
	Gain Error at T_A =25°C	0V < GPx < VREF, VCC = 3.3V	-0.4		+0.4	% FSR
		0V < GPx < 2 * VREF, VCC = 5V	-0.9		+0.9	% FSR
	Gain Error Drift	0V < GPx < VREF, VCC = 3.3V		-40		µV/°C
		0V < GPx < 2 * VREF, VCC = 5V		±300		µV/°C
	Zero Code Error	0V < GPx < VREF, VCC = 3.3V		0.65		mV
		0V < GPx < 2 * VREF, VCC = 5V		5		mV
	Total Unadjusted Error	0V < GPx < VREF		±0.15	±0.65	% FSR
		0V < GPx < 2 * VREF, 4.5 V < VCC		±0.30	±1.20	% FSR
	Capacitive Load Stability	High Impedance Load			2	nF
		Load = 1kΩ			10	nF
	DC Crosstalk	One Channel Aggressor, 100% FS change. Gain of 1. High Impedance Load.	-0.5		+0.5	LSB
	DC Output Impedance			0.2		Ω
	DC Power Supply Rejection Ratio	2.7 V < VCC < 3.3 V DAC = 50% FSR		0.04		mV/V
		4.5 V < VCC < 5.5 V. DAC = 50% FSR		0.4		mV/V
	Load Regulation	2.7 V < VCC < 3.3 V or 4.5 V < VCC < 5.5 V. DAC = 50% FSR DAC Sinking 35mA		100		µV/mA
		2.7 V < VCC < 3.3 V or 4.5 V < VCC < 5.5 V. DAC = 50% FSR DAC Sourcing 35mA		250		µV/mA

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Slew Rate	Change from 10% to 90% FS		0.2		V/µs
	Code change glitch impulse	1 LSB change around major carrier		1		nV-s
	Code change glitch amplitude	1 LSB change around major carrier		25		µV
	Channel-to-channel DC crosstalk	Measured DAC output at midscale, all other DAC outputs at full-scale, no output loads		150		µV

8.2 ADC and Temperature Sensor

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Fs	Sample Rate			500		ksps
	Resolution		12			Bits
INL	INL			±2		LSBs
DNL	DNL		-1		1	LSBs
FSR	Full Scale Range	Single Ended, gain of 1	0		+VREF	V
		Single Ended, gain of 2	0		+2*VREF	V
	Temperature Resolution		12			Bits
	Temperature Accuracy	5 sample average. Customer calibrated at room temperature		±3		°C
	Offset Error		-7		+7	mV
	Gain Error		-0.4		+0.4	%FSR
tTRACK	Track Time		500			ns
tCONV	Conversion Time				2	µs
	Signal-to-Noise Ratio	VCC = 2.7 V. 0V < V_GPx < V_{REF}		69		dB
		VCC = 5.5 V. 0V < V_GPx < V_{REF}		67		dB
		VCC = 2.7 V. 0V < V_GPx < V_{REF}		61		dB
	Channel-to-Channel Isolation	f_{IN} = 5 kHz		-95		dB
R_{GP-PD0}	Input Pull-Down Resistor	Resistance to GND on pin. Pull Down Configuration = 0		137.5		kΩ
	Input Capacitance			24		pF
	Full Power Bandwidth	-3 dB		8.2		MHz
		-0.1 dB		1.6		MHz

8.3 Reference Input

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
	Input Voltage		2.5		VCC	V
	Input Resistance	Resistance to GND		155		kΩ

8.4 Reference Output

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
VREF	Output Voltage	T_A = 25°C, VCC=3.3V	2.495	2.5	2.505	V
	Output Voltage Temperature Coefficient			±80		ppm/°C
	Capacitive Load Stability	Capacitance value across temperature, aging, and biased at 2.5V.	1.6	4.7		µF
	Output Impedance	VCC = 2.7 V		2.7		Ω
		VCC = 5 V		3.7		Ω
	Output Voltage Noise	0.1 Hz to 10 Hz		10		µV p-p
	Output Voltage Noise Density	f = 10 kHz, C_L = 10 nF		240		nV/√Hz
	Line Regulation	2.7 V < VCC < 3.3 V		-5.1		mV/V
		2.7 V < VCC < 5.5 V		3.9		mV/V

8.5 Power

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
VCC	Supply Voltage		2.7		5.5	V
	Supply Current	All GP[7:0] configured as GPIO with all inputs = VCC or GND			3.4	mA
	Supply Current	VCC = 5 V. GP[7:0] configured as DACs, internal reference, gain = 2.		1.5		mA
	Supply Current	VCC = 5 V. GP[7:0] configured as DACs, external reference, gain = 2.		1		mA
	Supply Current	VCC = 5 V. GP[7:0] configured as DAC and measured by the ADC, internal reference, gain = 2.		2.3		mA
	Supply Current	VCC = 5 V. GP[7:0] configured as DAC and measured by the ADC, external reference, gain = 2.		1		mA
	Supply Current	VCC = 5 V. GP[7:0] configured as ADCs, internal reference, gain = 2.		1		mA
	Supply Current	VCC = 5 V. GP[7:0] configured as ADCs, external reference, gain = 2.		0.7		mA
	Supply Current	VCC = 5 V. GP[7:0] configured as GPIOs, internal reference, gain = 2.		0.5		mA
	Supply Current	VCC = 5 V. GP[7:0] configured as GPIOs, external reference, gain = 2.		0.5		mA
	Supply Current	VCC = 3 V. GP[7:0] configured as DACs, internal reference, gain = 1.		1		mA
	Supply Current	VCC = 3 V. GP[7:0] configured as DACs, external reference, gain = 1.		1		mA
	Supply Current	VCC = 3 V. GP[7:0] configured as DAC and measured by the ADC, internal reference, gain = 1.		1		mA
	Supply Current	VCC = 3 V. GP[7:0] configured as DAC and measured by the ADC, external reference, gain = 1.		0.75		mA
	Supply Current	VCC = 3 V. GP[7:0] configured as ADCs, internal reference, gain = 1.		0.7		mA
	Supply Current	VCC = 3 V. GP[7:0] configured as ADCs, external reference, gain = 1.		0.5		mA
	Supply Current	VCC = 3 V. GP[7:0] configured as GPIOs, internal reference, gain = 1.		0.4		mA
	Supply Current	VCC = 3 V. GP[7:0] configured as GPIOs, external reference, gain = 1.		0.4		mA

8.6 GPIO

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Voh	Output High Voltage	ISOURCE = 2 mA	VCC-0.4			V
Vol	Output Low Voltage	ISINK = 2 mA			0.4	V
Vih	Input High Voltage		0.7 * VCC		VCC+0.3	V
Vil	Input Low Voltage		-0.3		0.3 * VCC	V
	Hysteresis			0.2		V
R_{GP-PD1}	Pull Down Resistance 1	Pull Down Configuration = 1		35		kΩ
R_{GP-PD0}	Pull Down Resistance 0	Pull Down Configuration = 0		137.5		kΩ
	Input Capacitance				20	pF

8.7 Interface Inputs: SDI, SCL, CSb, RESETb

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
VIL	Input Low Voltage		-0.3		0.3 * VCC	V
VIH	Input High Voltage		0.7 * VCC		VCC	V
	Input Current		-1	±0.01	1	µA
	Input Capacitance				10	pF

8.8 Interface Output: SDO

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
VOL	Output Low Voltage	ISINK= 3mA, 2V < VCC			0.4	V
		ISINK= 2mA, VCC < 2V			0.2*VCC	V
	Output Capacitance				10	pF

8.9 SPI Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI TIMING REQUIREMENTS						
fsclk	SCLK frequency	Write to slave			*10MHz*	MHz
		Read from slave			10	
t_{hi}	SCLK high time		45			ns
t_{low}	SCLK low time		45			ns
t_{sui}	SDI setup time		20			ns
t_{hdi}	SDI hold time		20			ns
t_{sdodz}	SDO driven to tri-state		0		20	ns
t_{sdozd}	SDO tri-state to driven		0		20	ns
t_{od}	SDO output delay		0		20	ns
t_{sucs}	CSB setup time		50			ns
t_{hdcs}	CSB hold time		50			ns
t_{csbhi}	CSB high time		50			ns

9 Description

The PI15592 includes eight multi-function pins: GP[7:0]. Each may be configured as a DAC output, ADC input, or digital I/O. An I/O may be configured as both a DAC and an ADC. All functionality is controlled and monitored using a slave serial interface.

9.1 DACs

Eight 12bit DACs are included. The output range of each DAC is 0V to Vref or 0V to 2 x Vref. DAC output values are set through the slave serial interface. Each DAC includes an output buffer. These buffers are capable of supplying +/-35mA to each respective DAC output load. The DAC outputs may be asynchronously updated by writing to their respective input registers. Alternately, multiple DACs may be synchronously updated using the LDAC register.

A DAC output is set using two parameters: DAC_Gain (Register 0x03, bit D4) and the respective DAC Register .

V_{OUT} = DAC_Gain * V_{REF} * (DAC Register / 4096).

Where:

V_{OUT} is the output voltage from the DAC.

DAC_Gain is either 1 or 2.

DAC Register is the decimal value of the 12 bit DAC Register, ranging from 0 to 4095.

4096 is the maximum possible code for a 12 bit value (2^{12} = 4096).

9.2 ADC

A 12bit ADC is used in conjunction with an input multiplexer to measure the analog input values. The input range of the ADC is 0V to Vref or 0V to 2 x Vref. The analog value of a pin may be read at any time, even if the pin is configured as an output. The ADC may also be used to read the internal temperature of the die. ADC conversions are controlled and read back through the slave serial interface.

An ADC conversion is started based on a serial interface transaction. A conversion starts on the rising edge of ACK following the slave address. The ADC result is determined by both the input signal and the ADC_Gain (Register 0x03, bit D5)

V_{IN} = ADC_Gain * V_{REF} * (ADC Result / 4096).

Where:

V_{IN} is the voltage present on pin the configured GP pin as calculated from the ADC result.

ADC_Gain is either 1 or 2.

ADC Result is the decimal value of the 12 bit ADC result, ranging from 0 to 4095.

4096 is the maximum possible code for a 12 bit value (2^{12} = 4096).

9.2.1 Pull-Down Resistors

A pull-down resistor to ground is present on each GP[7:0] pin. One of two resistance values may be selected by Pull Down Configuration[7:0] as described in the register map. This register allows the choice of either R_{GP-PD0} or R_{GP-PD1} but does not allow for both resistors to be disconnected. When using a GP pin as an ADC input, Pull Down Configuration should be set to 0 to select $R_{GP-PD0.}$ This input structure is shown for GP0 in the figure below.

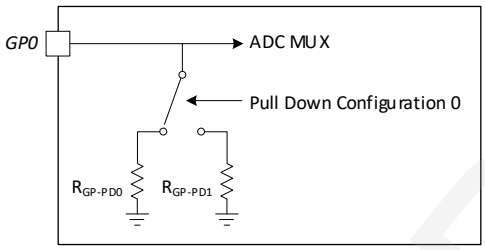

Figure 4 Input Pull Down Resistor as shown for GP0

9.2.2 Die Temperature Sensor

The PI15592 includes a die temperature sensor. The ADC may be configured to readback temperature by setting a bit in the ADC sequencer (Register 0x02, bit D8).

Temperature (°C)= (0.75 / ADC Gain)* (ADC Result) - Offset

Where:

Temperature is the die temperature in °C as calculated from the ADC result.

ADC Gain. Value of 1 or 2.

ADC Result is the decimal value of the 12 bit ADC result, ranging from 0 to 4095.

Offset. Typical value of 273. This value should be calibrated by the customer at room temperature, with all DACs and I/O unloaded.

9.3 Digital I/O

Eight digital I/Os are included. In digital input mode, the input logic level of an I/O pin may be read through the serial interface. When configured as an output, either push-pull or open-drain output mode may be selected. The digital output values are set through the slave serial interface.

9.4 Internal and External Reference

The PI15592 includes a 2.5 V reference. By default, the PI15592 selects an external reference (Register 0x0B, bit D9 = 0). When an external reference is selected, an appropriate external reference must be connected to VREF. Decouple the internal reference to GND using a capacitor per the EC table requirements. The internal reference does not support external loading.

9.5 Reset

The PI15592 includes an asynchronous, active low reset pin RESETb. Connect RESETb to logic high (RESETb > V_{IH}). A falling edge on RESETb causes all registers to be set to their respective default values. This also causes all GP[7:0] pins to be configured with R_{GP-PD1} pull-down resistors to GND. Do not write to the slave serial interface while RESETb is held low.

A software reset function is available. Write 0x0F to the pointer byte followed by 0x0D to the MSByte and 0xAC to the LSByte.

10 Serial Interface

The PI15592 has a serial interface (CSb, SCLK, SDI, and SDO), which is compatible with SPI standards. The SPI access cycle is initiated by asserting the CSb pin low. The serial clock SCLK can be a continuous or gated clock. SDI data are clocked on SCLK rising edges. A regular serial interface access cycle is 16 bits long, thus the CSb pin must stay low for at least 16 SCLK rising edges. The access cycle ends when theCSb pin is de-asserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges, only the last 16 bits are used by the device. When CSb is high, the SCLK and SDI signals are blocked and the SDO pin is in a Hi-Z state.

10.1 Write Mode

Figure 5 shows the write timing for the PI15592. A write sequence begins by bringing the CSb line low. Data on SDI is clocked into the 16-bit shift register on the falling edge of SCLK. After the 16th falling clock edge, the last data bit is clocked in. CSb is brought high, and the programmed function is executed (that is, a change in a DAC input register or a change in a control register). All interface pins must be operated close to the VDD or VLOGIC rails to minimize power consumption in the digital input buffers.

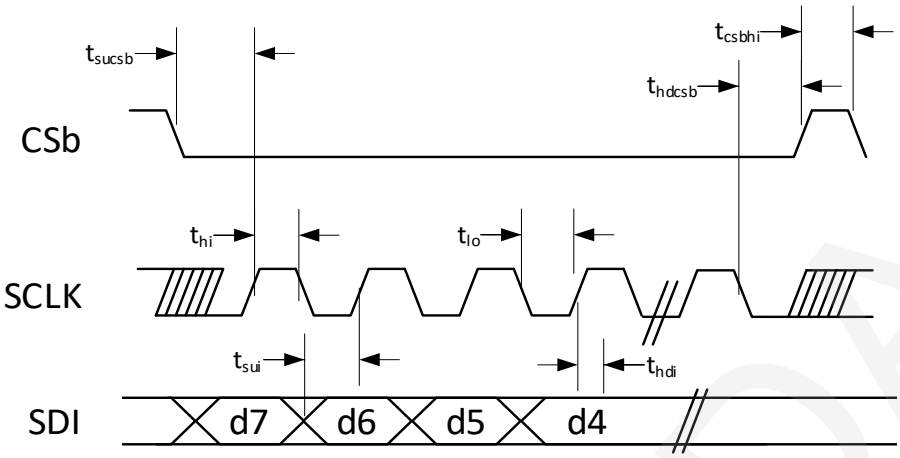

Figure 5 SPI Write Timing

10.2 Read Mode

The PI5592 allows data readback from the ADCs and control registers via the serial interface. ADC conversions are automatically clocked out on the serial interface as part of a sequence or as a single ADC conversion. Reading from a register first requires a write to the readback and LDAC mode register to select the register to read back. The contents of the selected register are clocked out on the next 16 SCLKs following a falling edge of CSb. Note that the maximum speed of the SPI interface during a read operation must not exceed 10MHz. During the ADC conversion cycle, only the ADC conversion result and the temperature reading results can be read back and all other read requests are ignored. Figure 6 SPI Read Timing shows the timing for READ operation.

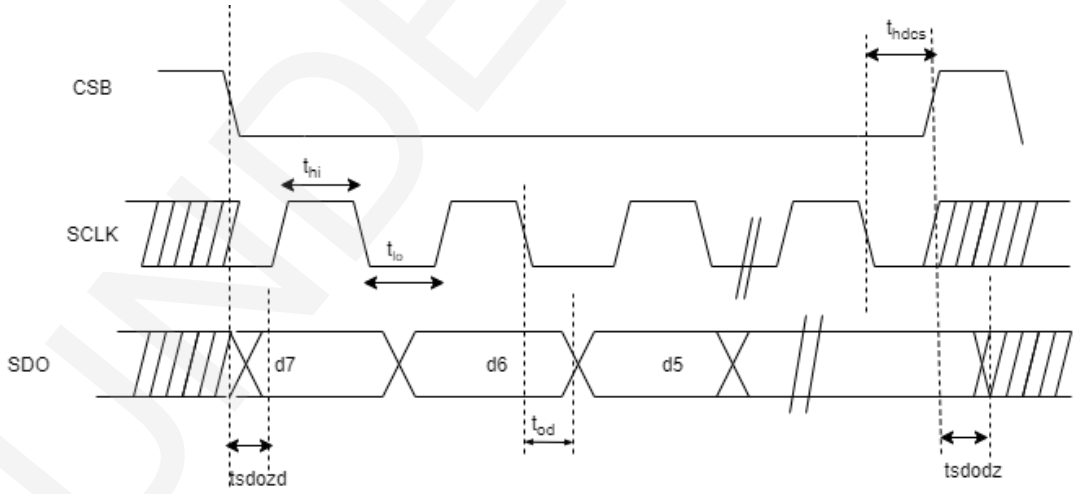

Figure 6 SPI Read Timing

10.3 Input Shift Register Format

Table 1 shows the input shift register format for the SPI write operation. The MSB (Bit 15) determines what type of write function is required. When Bit 15 is 0, a write to the control register is selected. The control register address is selected by Bits[14:11]. Bits[10:9] are reserved and are 0s. Bits[8:0] set the data that is written to the selected control register. When Bit 15 is 1, data is written to a DAC channel (assuming that channel has been set to be a DAC).

Input Shift Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Control Register Address				0	0	Control Register Data								
1	DAC Select				DAC Write Data										

Table 1

10.4 Register Map

Table 2 Shows the register map for PI5592.

MSB (Bit 15)	Address [14:11]	Default Value	Description
0	0000	0x000	NOP
0	0001	0x000	DAC Readback
0	0010	0x000	ADC Sequencer
0	0011	0x000	General Configuration
0	0100	0x000	ADC pin Configuration
0	0101	0x0FF	DAC pin Configuration
0	0110	0x000	Pull Down Configuration
0	0111	0x000	LDAC Configuration
0	1000	0x000	GPIO Write Configuration
0	1001	0x000	GPIO Write Data
0	1010	0x000	GPIO Read Configuration
0	1011	0x000	Reference Control
0	1100	0x000	GP Output Configuration
0	1101	0x000	High Impedance Configuration
0	1110	0x000	Reserved
0	1111	0x000	Software Reset
1	XXX	0x000	Write to DAC register selected by bits [14:12]

Table 2

10.5 DAC Write Operation

To set a pin as a DAC, set the appropriate bit in the DAC pin configuration register to 1 as in Table 3 and Table 4. Data can be written to a DAC by setting the MSB of the serial write to 1. Bits [14:12] determine which DAC is addressed, and bits [11:0] contain the data to be written to the DAC, as shown in Table 5 and Table 6. Data is written to the selected DAC input register. Data written to the input register can be automatically copied to the DAC register using the LDAC settings if required. See Readback and LDAC Mode Register for further details.

DAC Pin Configuration Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register Address				0	0	0	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

Table 3

Bits	Name	Description
15		Set to 0
[14:11]	Register Address	Set to 0b0101
[10:8]	Reserved	Reserved. Set to 0b000
[7:0]	DAC[7:0]	Set IO pins as DAC outputs 1: DAC Output 0: Function determined by pin configuration registers (default)

Table 4

DAC Write Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	DAC Address			DAC Data											

Table 5

Bits	Name	Description
15		Set to 1
[14:12]	DAC Address	Set to 0b0101
[11:0]	DAC Data	12-bit DAC data

Table 6

10.6 DAC Read Operation

The DAC input registers can be read back to confirm that the data was received correctly. Data can only be read back from a DAC when there is no ADC conversion taking place.

To read back a DAC input register, it is first necessary to enable the read function and select the DAC channel. This is done by writing to the DAC read register as in Table 7 and Table 8. The DAC data is clocked out on the next SPI operation. An NOP write can be used. Bits [14:12] contain the address of the DAC being read.

DAC Readback Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register Address				0	0	0	0	0	0	Read Enable		DAC channel		

Table 7

Bits	Name	Description
15		Set to 0
[14:11]	Register Address	Set to 0b0001
[10:5]	Reserved	Reserved. Set to 0b000
[4:3]	Read Enable	11: Read Enabled 00: Read Disabled (default)
[2:0]	DAC Channel	Select DAC Channel 000: DAC0 001: DAC1 010: DAC2 011: DAC3 100: DAC4 101: DAC5 110: DAC6 111: DAC7

Table 8

10.7 ADC Operation

A GP pin can be set as an ADC input using the ADC pin configuration register as in Table 9 and Table 10. For example, setting Bit 0 to 1 enables GP0 as an ADC input. The ADC channels operate as a traditional multichannel ADC, where each serial transfer selects the next channel for conversion. The ADC sequence register (see Table 11 and Table 12) selects which ADC channels are included in the sequence. The REP bit determines if the sequence is repeated.

The CSb signal is part of the write sequence on the SDI pin as described in Write Mode. The data that appears on the SDO pin during the first write to the ADC sequence register is not valid. Once the sequence register is written, the ADC begins to track the first channel in the sequence. Tracking takes 500 ns. Do not start a conversion during this time. The next CSb falling edge starts a conversion on the selected channel. The next CSb falling edge starts clocking out the ADC result and initiates the next conversion. The ADC operates with one cycle delay. The result for each conversion is available one read cycle after the cycle in which the conversion was initiated.

If more than one channel is selected in the ADC sequence register, the ADC converts all selected channels sequentially in ascending order on successive CSb falling edges. Once all the selected channels in the control register are converted, the ADC repeats the sequence if the REP bit is set. If the REP bit is clear, the ADC pins go to three-state.

GP7 can be configured as a BUSYb output pin to indicate when a conversion result is available. BUSYb goes low while a conversion takes place and goes high when the conversion result is available.

ADC Pin Configuration Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register Address				0	0	0	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

Table 9

Bits	Name	Description
15		Set to 0
[14:11]	Register Address	Set to 0b0100
[10:8]	Reserved	Reserved. Set to 0b000
[7:0]	ADC[7:0]	Set IO pins as ADC inputs 1: ADC input 0: Function determined by pin configuration registers (default)

Table 10

ADC Sequence Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register Address				0	REP	TEMP	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

Table 11

Bits	Name	Description
15		Set to 0
[14:11]	Register Address	Set to 0b0010
10	Reserved	Set to 0
9	REP	ADC sequence repeat 1: Repeat 0: Single shot (default)
8	TEMP	Include temperature indicator 1: Include temperature indicator 0: Do not include temperature indicator
[7:0]	ADC[7:0]	Include ADC channels in sequence 1: ADC channel included 0: ADC channel not included

Table 12

ADC Results															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	ADC Address			ADC Data											

Table 13

To change the channels included in an ADC sequence, the existing conversion sequence must be stopped. The sequence is stopped by clearing the REP, TEMP, and ADC7 to ADC0 bits in the ADC sequence register.

If an ADC conversion is in progress then it must be allowed finish before a new sequence can be written to the ADC sequence register. Allow a minimum of 2μs between starting the write to end the current sequence and starting the write to select a new sequence. After selecting the new sequence, allow an ADC track time of 500 ns before initiating the next conversion.

10.8 GPIO Operation

Each of the GP pins can operate as a digital input or output pin.

10.8.1 Setting Pins as Outputs

To set a pin as a digital output, set the appropriate bit in the GPIO write configuration register to 1 (see Table 14 and Table 15). For example, setting Bit 0 to Bit 1 enables GP0 as a general-purpose output. The state of the output pin is controlled by setting or clearing the bits in the GPIO write data register (see Table 18). A data bit is ignored if it is written to a location that is not configured as an output.

GPIO Write Configuration Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register Address				0	0	Enable BUSYb	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Table 14

Bits	Name	Description
15		Set to 0
[14:11]	Register Address	Set to 0b1000
[10:9]	Reserved	Set to 0
8	Enable BUSYb	Enable GP7 as BUSYb 1: Enabled. GPIO7 (bit 7) must also be enabled. 0: Not enabled
[7:0]	GPIO[7:0]	Select GP pins as GPIO 1: Pin is GPIO 0: Pin function as per pin configuration register (default)

Table 15

The outputs can be independently configured as push/pull or open-drain outputs by setting the appropriate bit in the GPIO open-drain configuration register as described in Table 16 and Table 17.

GPIO Open-Drain Configuration Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register Address				0	0	0	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0

Table 16

Bits	Name	Description
15		Set to 0
[14:11]	Register Address	Set to 0b1100
[10:8]	Reserved	Set to 0
[7:0]	OD[7:0]	Set as Open-Drain (Must also be set as GPIO) 1: Open-Drain 0: Push-Pull (default)

Table 17

A write to the GPIO write data register is used to change the state of the GP pins.

GPIO Write Data Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register Address				0	0	0	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Table 18

Bits	Name	Description
15		Set to 0
[14:11]	Register Address	Set to 0b1001
[10:8]	Reserved	Set to 0
[7:0]	GPIO[7:0]	Set GP pin state 1: GP set to logic 1 0: GP set to logic 0

Table 19

10.8.2 Setting Pins as Inputs

To set a GP pin as a digital input, set the appropriate bit in the GPIO read configuration register to 1 as described in Table 20 and Table 21. To read the state of the general-purpose inputs, write to the GPIO read and configuration register to set Bit D10 to 1 and also any of Bits [7:0] that correspond to a general-purpose input pin. The next SPI operation clocks out the state of any pins set as digital inputs.

GPIO Read Configuration Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register Address				Enable Read	0	0	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Table 20

Bits	Name	Description
15		Set to 0
[14:11]	Register Address	Set to 0b1010
10	Enable Read	Enable GPIO Read 1: Next SPI operation returns state of GPIO 0: Select which GP pins are set as GPIO input
[9:8]	Reserved	Set to 0
[7:0]	GPIO[7:0]	Set GP pins as GPIO input 1: Pin is GPIO input 0: Pin function as per pin configuration register (default)

Table 21

10.8.3 Three-State Pins

The GP pins can be set to three-state by writing to the three-state configuration register, as shown in Table 22 and Table 23.

Three-State Configuration Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register Address				0	0	0	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0

Table 22

Bits	Name	Description
15		Set to 0
[14:11]	Register Address	Set to 0b1101
[10:8]	Reserved	Set to 0
[7:0]	TS[7:0]	Set GP pin as Tri-state 1: GP is Tri-state 0: Pin function as per pin configuration register (default)

Table 23

10.8.4 Pull-Down Resistor Pins

The GP pins can be connected to GND via a pull-down resistor (85 kΩ) by setting the appropriate bits in the pull-down configuration register, as shown in Table 24 and Table 25.

Pull-Down Configuration Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register Address				0	0	0	PULL7	PULL6	PULL5	PULL4	PULL3	PULL2	PULL1	PULL0

Table 24

Bits	Name	Description
15		Set to 0
[14:11]	Register Address	Set to 0b0110
[10:8]	Reserved	Set to 0
[7:0]	PULL[7:0]	Set GP pin as outputs with pull-down. 1: GP has weak pull-down 0: Pin function as per pin configuration register (default)

Table 25

10.9 Power-Down Mode

The power-down register allows any channels set as DACs to be individually placed in a power-down state. When in a power-down state, the DAC outputs are three-state. When a DAC channel is put back into normal mode, the DAC output returns to its previous value. The internal reference and its buffer are powered down by default and are enabled by setting the EN_REF bit in the power-down register. The internal reference voltage then appears at the VREF pin. Ensure the reference is powered-down when applying an external reference.

There is no dedicated power-down function for the ADC, but the ADC is automatically powered down if none of the GP pins are selected as ADCs. The PD_ALL bit powers down all the DACs, the reference and its buffer, and the ADC simultaneously. Table 26 and Table 27 show the power-down register.

Pull-Down Configuration Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register Address				PD_ALL	EN_REF	0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Table 26

Bits	Name	Description
15		Set to 0
[14:11]	Register Address	Set to 0b1011
10	PD_ALL	Power-down DACs and Reference 1: Reference, DACs and ADC are powered down 0: Power-down state determined by bits 9 and [7:0] (default)
9	EN_REF	Enable internal reference 1: Reference is powered-up 0: Reference is powered-down (default)
8	Reserved	Set to 0
[7:0]	PD[7:0]	Power-down DACs 1: DAC is powered down 0: Normal operating mode (default)

Table 27

10.10 Reset

The PI15592 can be reset to its default settings by writing a fixed code to the reset register as shown in Table 28. The reset function takes 250 µs. Do not write new data to the part during this time. The RESETb pin that performs the same function. For normal operation, RESETb is tied high. A falling edge on RESETb triggers the reset function.

Reset Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	0	1	1	0	1	0	1	1	0	0

Table 28

10.11 Readback and LDAC Mode Register

The values contained in the configuration registers can be read back to ensure that they are correctly set up. The register readback is initiated by writing to the readback and LDAC mode register with Bit 6 set to 1. Bits [5:2] select which register is to be read back. The register data is clocked out on the next SPI transaction.

Bits [1:0] of the readback and LDAC mode register select the LDAC mode. The LDAC mode determines if the data that is written to a DAC input register is also transferred to the DAC register.

Readback and LDAC Mode Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register Address				0	0	0	0	EN	REG_READBACK				LDAC mode	

Table 29

Bits	Name	Description
15		Set to 0
[14:11]	Register Address	Set to 0b0111
[10:7]	Reserved	Set to 0
6	EN	Enable readback 1: Bits [5:2] select which register is read back. Bit 6 clears when read is complete 0: no readback initialized
[5:2]	REG_READBACK	Select register to be read 0000: NOP 0001: DAC Readback 0010: ADC Sequencer 0011: General Configuration 0100: ADC pin Configuration 0101: DAC pin Configuration 0110: Pull Down Configuration 0111: LDAC Configuration 1000: GPIO Write Configuration 1001: GPIO Write Data 1010: GPIO Read Configuration 1011: Power Down and Reference Control 1100: GP Output Configuration 1101: Three-State Configuration 1110: Reserved 1111: Software Reset
[1:0]	LDAC mode	Set LDAC mode. 00: Data written to an input register is immediately transferred to DAC register (default) 01: Data is written to an input register only 10: Data in the input register is copied to the DAC register 11: Reserved

Table 30

10.12 Power-Up Time

When power is applied to the PI15592, the power-on reset block begins to configure the device and to load the registers with their default values. The configuration process takes 250 µs; do not write to any of the registers during this time.

11 Order Information

Ship device	Packaging	Shipment Type
PI15592-W1R	WLCSP	Tape and reel

12 Revision History

Date	Revision	Notes
Nov 20th 2023	0.1	Preliminary Release