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Comparative Analysis of 4-bit CMOS Vedic Multiplier and GDI Vedic Multiplier using 18nm FinFET Technology

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***Abstract*— Today's modern market needs application computational blocks to execute complex operations with an ease to satisfy low power requirements, wherein relentless efforts are being made by the researchers to optimize these computational blocks in terms of speed, power, and area requirements. The core key component in these computational blocks is Multipliers. Since, these multiplier circuits directly effects the performance of overall computation block or overall system, where there is a need to optimize the multiplier circuit. Since, it is already known that the multiplication requires several steps and is a lengthy process, the algorithm of Vedic multiplication is used to speed-up the multiplication process. Moreover, by implementing the Vedic multiplier circuit with the GDI technique, there will be a further reduction in number of transistors and propagation delay. So, here in this paper the Vedic multiplier circuit is implemented by using GDI technique and also 18nm FinFET is deployed for analyzing simulation results. Here, the primary objective is to optimize the proposed multiplier circuitry, where an experimental analysis is conducted by comprising the parameters such as propagation Delay, Power, Area and Power-Delay-Product (PDP). All experimental analysis is done using Cadence Virtuoso.**

Keywords: Short channel effects (SCE), GDI(Gate Diffusion Input), PDP(Power Delay Product), N-FinFET, P-FinFET, Vedic Mathematics, NPS,ASIC,FPGA

I. INTRODUCTION

From past four decades, MOSFETs are used as basic building component to derive very large circuitries such as CPUs-Cores, GPU-Cores, ALU Blocks and many more, but in order to obey Moore's law that is "the number of transistors double every year for a particular area under consideration". But MOSFETs were lagging in their respective scaled derivatives year by year. for example the basic operation of a MOSFET is to behave like a switch that is "it should pass the current when Turn-on and should shut off the current while Turn-off" but on contrary this characteristic was diminishing as it moves into deeper submicron regions, the reason behind that are various shorts channel effects came into the picture and hindered the overall performance of the MOSFET. So various IC fabrication Industries such as TSMC, Global foundries, Samsung semiconductors and other big giants collaborated in order to obtain a new device which was obeying the principle of the basic transistor, the device released was FinFET , got this name from the fact that there was actually Fin-shaped channel introduced between the Source and the Drain terminal which was completely or partially wrapped by the gate terminal as in Fig.1 .which further gave the FinFETs greater driving capability and less Sub-Micron leakage currents. with the FinFETs in the market the transistor density were increasing for a specific chip or an ASIC /FPGA .also, main focus of interest for various IC Designers and industries was that FinFETs were not prone to short-channel effects that were hampering the performance of traditional MOSFETs . Such as Scattering, Subthreshold slope, Drain Induced barrier lowering and many more. Moreover, it is not required to increase the doping density as it did the same in MOSFETs, where it reduced the short channel abnormalities but bring increased resistance as a trade-off. By incorporating FinFETs not even succeeded in increasing the transistor density but it has also succeeded in minimising the number of devices/transistors as the FinFETs possessed non-singular gate terminal and now it can provide more than one logic for a specific input-gate-terminal which further reduced the demand for more number of gates in a specific Boolean logic circuit for example the NAND Gate circuitry requires four transistors while using MOSFET but it uses the three transistors while using Double Gate FinFET. As the merits were getting piled up for this specific device the efforts are now being made by IC industry to standardise FinFET implemented circuits such as computational blocks, workstations, neural processing units etc. Currently, the 7nm benchmark is reached with FinFETs without any substantial degradation in circuit performance which wouldn't be possible if the same has been implemented using MOSFET.

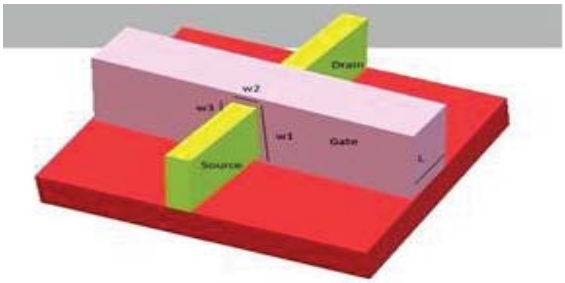


Fig.1: FinFET Structure (Reproduced from [2])

II. VEDIC MULTIPLICATION

Vedic Multiplication has proven itself to be one of the efficient and simplified way of multiplying technique, it is an ancient technique and follows a unique set of steps to give required product.it is a robust technique and gives accurate arithmetic results. Fig.2 (a) shows the steps involved in Vedic Multiplication Method for two decimal numbers.

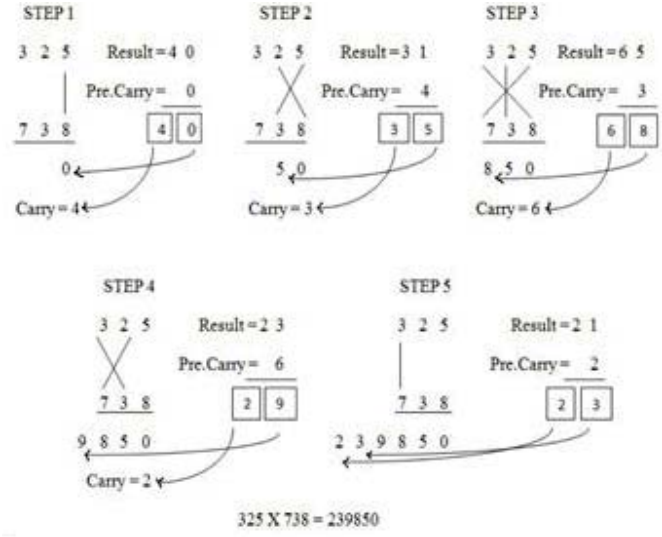


Fig. 2(a) Vedic Multiplication of two decimal numbers

As shown in Fig 2(a), the multiplication of two numbers (decimal numbers) 325 and 738 is depicted using Vedic algorithm. Here, a straight or criss-cross multiplication is performed to generate result and carry (which is propagated in next step).similarly Fig.2 (b) shows the multiplication of 4-bit binary no. using Vedic multiplication method. Here dots are represented by either '0' or '1'.

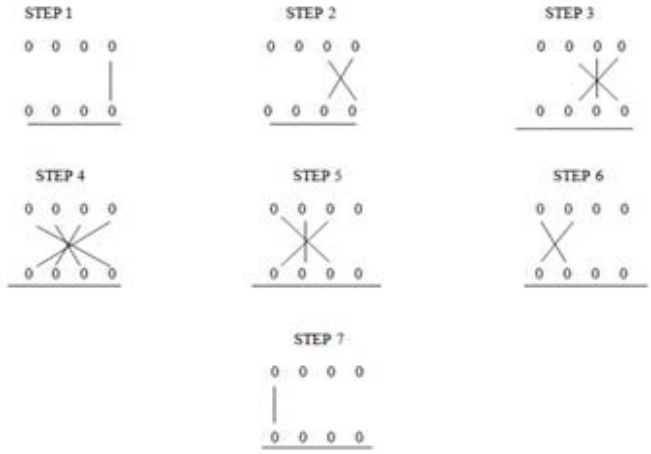


Fig.2 (b) Vedic Multiplication of two 4-bit binary no.s

III. GATE DIFFUSION INPUT (GDI)

Maintaining lower design complexity for Digital circuits is the goal for modern digital circuit designers in order to achieve this deliverable GDI technique [1] is one of the suitable candidate. In this technique, it has been entitled to realise various logics as observed in Table-I. All these logics can be realised by using two transistors. The main building cell to assist logic-realisation is the GDI cell, as shown in Fig.3 the first glimpse the GDI cell might look familiar with traditional CMOS inverter but it differs in logic farther than expected.

1) given GDI cell has 3 particular input terminal that is G,N and P, where G acts as an input terminal for PMOS and NMOS respectively and P and N are logic that are fed to the GD cell.

2) Both P and N terminals of the GDA cell are tied to the substrate of NMOS and PMOS respectively in order to mitigate conflicting logical errors.

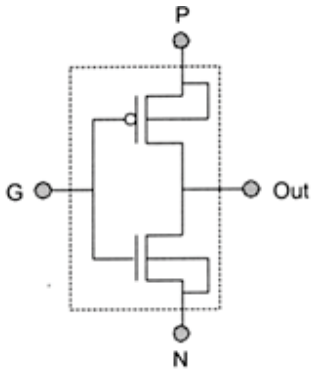


Fig.3 Basic GDI cell

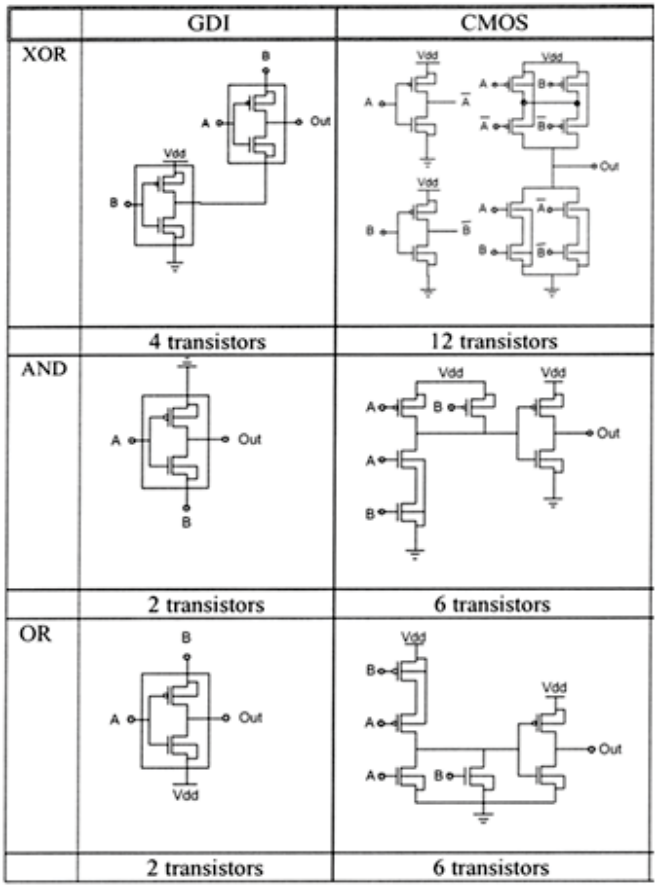
As shown in table-I, just by changing the configuration of different input terminals (i.e. G,N and P) of GDI cell, where it can realise numerous Boolean functions. The functions realised can differ in their complexity but the catch here is that all these Complex logic functions shown in Table-I can be realised by just using two transistors, which offers minimalistic overhead in terms of transistor density as compared to both Pass Transistor Logic and CMOS logic. It is realised that GDI is a simple yet efficient technique for small order systems. Although on realising circuits using GDI cell, it is observed that there was a substantial decrease in voltage level as GDI faces an issue of logic level degradation, this is the basic trade-off one can incur by using GDI technique although it can drastically reduce the transistor count (TC) and power dissipation in further complex circuits such as Multipliers or signal processors

Table I - Implementation of Boolean-functions using GDI

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

As discussed in the beginning of Section-II that the GDI technique is employed where it is required to reduce the transistor count(TC),and in this paper we'll be implementing GDI vedic multiplier which would comprise of certain core cells such as XOR,AND gates, so we'll be using GDI technique for their implementation. As it is shown in Table II, that basic XOR, AND, OR gates can be realized using GDI technique and it can construct bigger modules out of them, where it indeed possess less transistor count and lesser delay.

Table II Implementation of various gates using GDI Technique



IV. GDI VEDIC MULTIPLIER

In order to optimize the conventional CMOS variant, here in this section we'll be realising 4-bit GDI Vedic Multiplier using FinFETs, the operating principle or algorithm of multiplier is discussed in section-II and we'll be implementing same using the GDI technique. For this we'll first need to implement the fundamental block of any multiplier that is, adder. For the CMOS Vedic Multiplier we'll be using conventional 28T CMOS full adder and for GDI one we'll be utilising 10T GDI Full Adder (shown in Fig.4 (b)). From here the actual optimisation takes place. Since the GDI Multiplier would tend to exhibit less transistor count, less propagation delay and less power as compared to CMOS counterpart. Here in Fig.4 (a) it is observed that the two 4-bit inputs are applied to the Multiplier circuit and 8-bit product is generated. Here, the internal inputs 0.0, 0.1, 0.2... Etc. depicts the ANDing operation of bit A_0B_0, A_0B_1, A_0B_2 respectively. Also, the full adder is realised using GDI technique. The main advantage observed is that there was a drastic decrease in transistor count which will be depicted in the simulation and results section. But there is always a direct trade off in power, delay and Area in VLSI industry. This model exhibits certain level of distortions in its product waveform which can be taken care of by adding buffers of suitable sizes in the critical path.

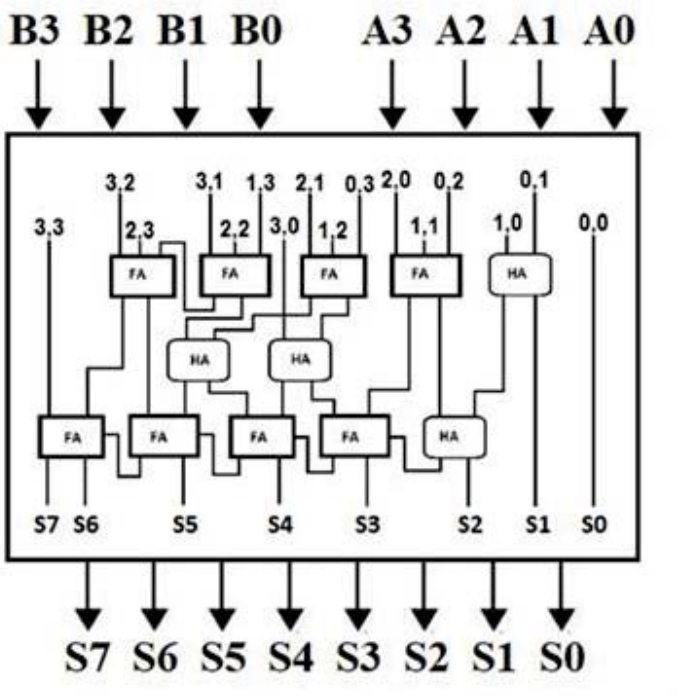


Fig. 4(a) realisation of 4-bit Vedic Multiplier circuit [6]

Furthermore, the GDI logic Adder depicted in Fig. 4(b) is realized using GDI cell (Fig.3) as a building block. The circuit has just 10 transistors to realize the logic equivalent to a full adder and if it is required to realize the same logic with traditional CMOS strategy then it will take around 28 transistors so here an IC designer has the ability to suppress the area overhead for the given logical block and when these tiny modifications are taken into the picture for a bigger block generates significant impact. As observed in Vedic multiplier, it effects holistically. For the GDI adder, it doesn't require to apply different delay balancing techniques as sum and carry are obtained at the same time interval.

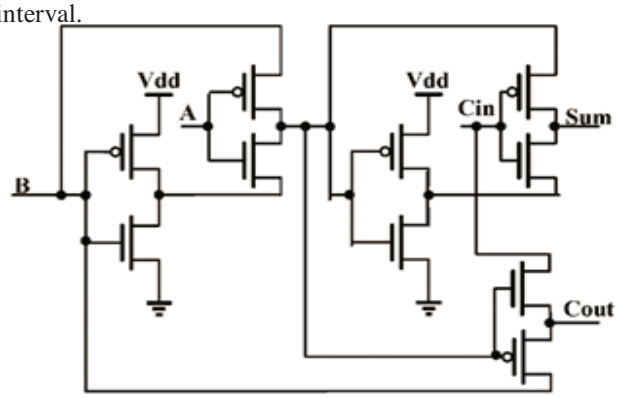


Fig 4(b). 10T GDI Full Adder

V. Simulation and Results

The literature presented has holistic comparison between 4-bit CMOS Vedic multiplier and 4-bit GDI Vedic multiplier. Various attributes such as power, power-delay-product, area and propagation delay are considered for detailed analysis. And it is observed that Vedic multiplier is realized using GDI technique displayed overwhelming results and it can be viewed as an appropriate candidate for upcoming design in multipliers circuit.

a) Power - As compared to conventional CMOS the Vedic multiplier realized using GDI technique displayed less power consumption.

b) Delay– in GDI Vedic Multiplier , the delay for generation of 8-bit output is less as compared to CMOS variant.

c) PDP – GDI Multiplier performs superior.

d) Transistor count-GDI has lesser number of transistors

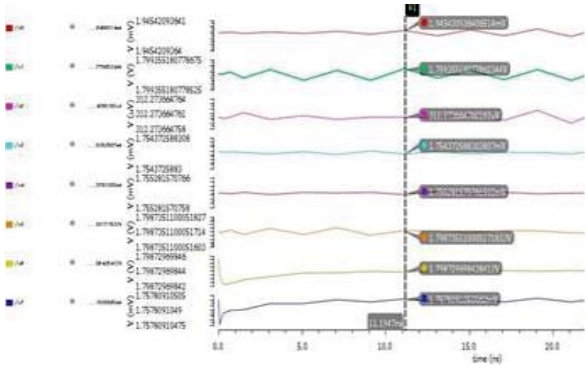


Fig.5(a) Product Plot of CMOS vedic Multiplier

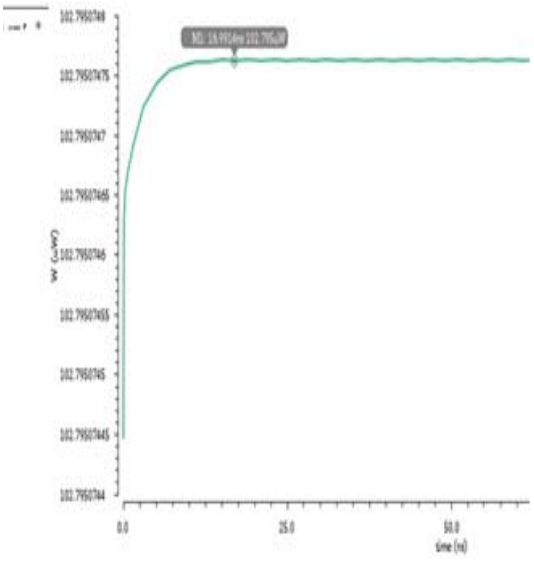


Fig.5(b) Power Plot of CMOS vedic Multiplier

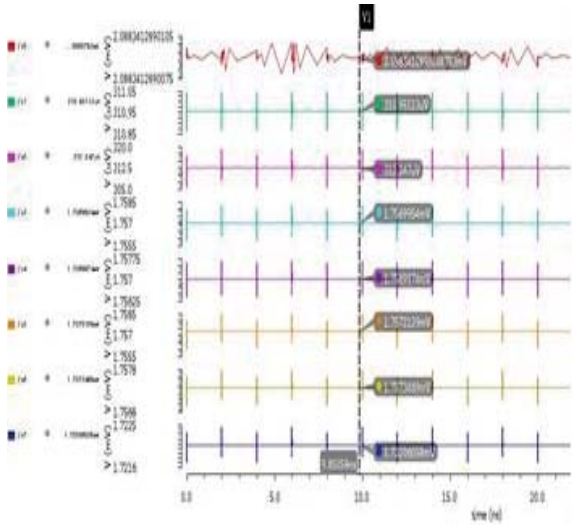


Fig.5(c) Product Plot of GDI vedic Multiplier

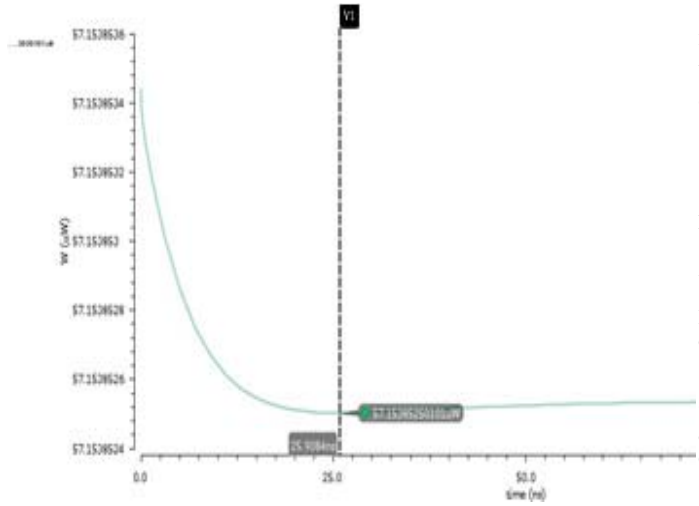


Fig.5(d) Power Plot of GDI vedic Multiplier

Table III Performance assessment of 4-bit CMOS and GDI Vedic Multiplier

CIRCUIT (LOGIC)	TRANSISTOR COUNT	DELAY (NS)	POWER (μW)	POWER DELAY PRODUCT (J)
GDI MULTIPLIER	152	38.146	57.15	2.18×10^{-12}
CMOS MULTIPLIER	432	119.78	102.8	12.31×10^{-12}

VI. CONCLUSION

This research work has deployed Vedic Algorithms to carry out multiplication process, as it is well known that Vedic algorithms are quite robust and reliable as they keep circuit complexity minimum. Moreover, Multiplier circuits can be used to realize more complex circuitry such as signal-processors such as convolutes so it can also appoint GDI technique to further optimize those complex circuits as well. Here, a detailed comparison between GDI Multiplier and CMOS Multiplier has been conducted by using FinFETs (18nm) for distinct attributes such as Propagation-delay, Power, Power-delay-product and transistor count (as shown in Table III). It is observed that the GDI multiplier has displayed superior performance than conventional one as it has 31% lesser propagation delay, 55.6 % reduction in power and 35.18% less transistor count ; moreover, it has gone deep into optimization curve by implementing former circuit using FinFETs, as it obtained sharp performance characteristics. Since it is a known fact that, multiplier is the basic yet crucial module for modern day ALU's, it can be optimized further by using GDI technique to improve its performance in distinct dimensions.

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