# Silicon Photonics Design and Fabrication of a Fabry-Perot Resonator using Bragg Gratings and Waveguides to Achieve Lowest Free Spectral Range

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***Abstract*—*need to write still***

***Index Terms*—Free Spectral Range, Resonator, Silicon Photonics, Bragg Grating, Effective Index, Group Index, EBeam Lithography, Fabry-Perot.**

## I. INTRODUCTION

The concept of this experiment is to design and fabricate a device that will measure a small portion of an input LASER that will require very specific fine-tuning in order for the output light to get detected. Using a splitter tree the light from the LASER will be split up into 64 individual sources that will enter Fabry-Perot resonators made using bragg gratings and waveguides.

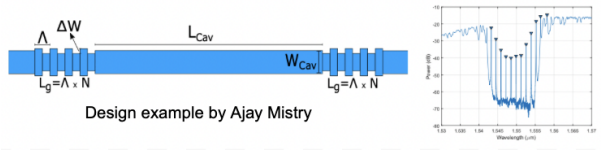


Fig 1. - Bragg grating resonator and output signal example [1].

As shown in Figure 1, the output signal requires a small free spectral range (<0.2) of the reflective output of the resonator in order to be detected. This Fabry-Perot resonator will be modeled and designed using silicon photonic bragg gratings and waveguides.
*need to add more still and a better/clearer image*

## II. MODELLING

A waveguide consists of a core and a cladding, the core is made of a material with a high index of refraction and the cladding of a low index of refraction. The light is then guided down the core by Total Internal Refraction (TIR). The core for this design is made up of silicon and the cladding is made up of an Oxide layer, more specifically, Silicon Dioxide. TE polarization will be the mode of the waveguide, TE mode is dependent on the transverse electric waves, relying on the electric field vector being perpendicular to the direction of propagation. Comparatively, TM waves are dependent on the magnetic field perpendicular to the waveguide propagation. The TE waveguides were designed with a Silicon strip with slab thickness of 220 nm thickness, making them single mode devices. The 220 nm thickness is a set parameter based on the chip that will be used.

To decide on a waveguide width at 220 nm thickness can be done by comparing the effective index. The group index is especially important to consider in photonics, more specifically the group velocity. However, increasing the width of the waveguide will increase the effective index, but decrease the group index. This is the tradeoff between the designs that were considered.

Additionally, the modeling was done using Lumerical MODE to design the waveguide and its properties. This software allows you to simulate and predict the behavior using different sizes, index of reflection of materials, and pathlength, to name a few. These design choices will alter the results of group index and free spectral range (FSR).

Another consideration when modeling and designing the device, fabrication bias needs to be considered. These values can be estimated based on similar processes done by Sheri at UBC. Most importantly there is a “shrink” factor of 35 nm. To counter this factor the design choice of using 315 nm for simulations was used, in order to theoretically produce a fabricated device with a width of 350 nm.

| mode # | effective index | wavelength (μm) | loss (dB/cm) | group index |
|---|---|---|---|---|
| 1 | 2.305157+1.678546e-09i | 1.31 | 0.00069929 | 4.597812+4.720473e-09i |
| 2 | 1.956194+1.423532e-09i | 1.31 | 0.00059305 | 4.500709+7.010733e-09i |
| 3 | 1.437701+3.324504e-10i | 1.31 | 0.00013850 | 1.885643+9.564892e-10 |
| 4 | 1.370584+2.305745e-10i | 1.31 | 9.6058e-05 | 1.756121+1.323717e-09i |

Fig. 2 - Table of calculated effective and group index, as well as losses at 1310nm wavelength, using 315 nm width.

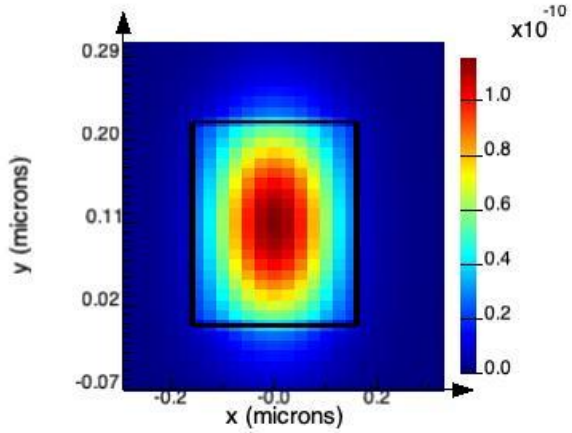


Fig. 3 - Energy density of a Si waveguide with 315 nm width and 220 nm height.

In Figure 3 you can see that most of the light is traveling inside the waveguide, which is desired.

## III. DESIGN

This chip is designed and fabricated based on the SiEPIC EBeam ZEP package, ZEP refers to the positive/negative photoresist that is required for the polarity of the EBeam lithography that the SOI wafer undergoes, see fabrication section for more details. The designs are made using python scripts (see appendix), the parameters are individually determined to design the measurement with an FSR smaller than the tuning range of the LASER (>0.2). All of the individual designs will be integrated onto one layout as shown in Figure 3. After fabrication a small laser will be attached as shown as the blue beam on the left of Figure 4. This LASER is used to input the light into the entire device, so that the individual measurements can be taken from the grating couplers on the left of Figure 5. using fibre-array detectors.

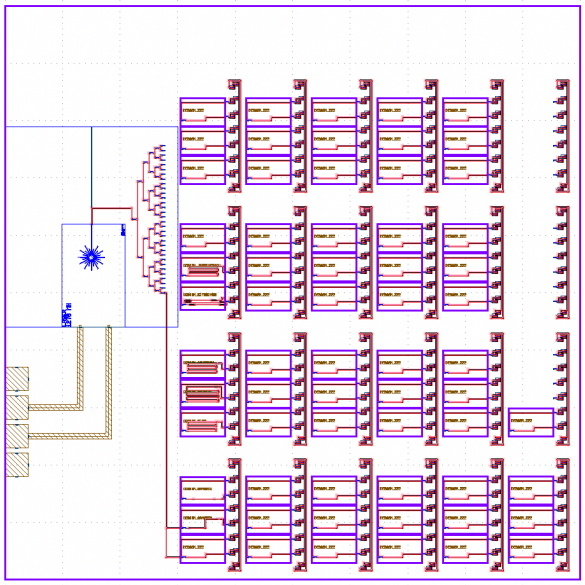

Fig. 4 - All of the designs integrated onto one device (note there are missing waveguides for easier and faster running and merging the scripts).

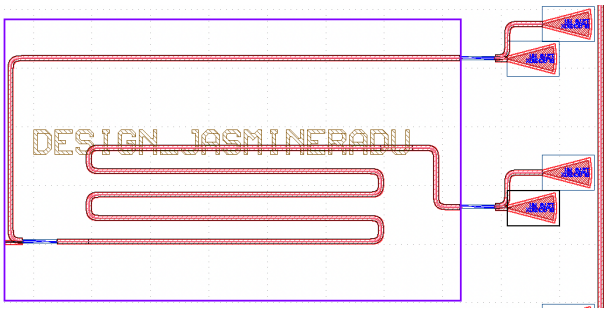


Fig. 5 - Design of device that was created with a python script using the SiEPIC EBeam ZEP package in KLayout.

```
cell_bragg = ly.create_cell('Bragg_grating', library, {
    'number_of_periods':100,
    'grating_period': 0.270,
    'corrugation_width': 0.05,
    'wg_width': 0.35,
    'sinusoidal': True})
```

Fig. 6 - Parameters used in the design macros for the layout.

## IV. FABRICATION

Fabrication of the chip will take place by Sheri Jahan Chowdhury at the Brimacombe Building at the University of British Columbia where Advanced Materials and Process Engineering Laboratory (AMPEL) and Stewart Blusson Quantum Matter

Institute (Blusson QMI) operate. The research teams operate with cleanrooms that range from class 100-10000 to minimize errors in nanofabrication.


Fig. 7 - Cross section of SOI Wafer (Prefabrication) with a Si layer with a thickness of approx. 220 nm, Buried Silicon Dioxide layer (BOX) and a Si Substrate layer.

The first step is a thorough clean, hot plate bake and plasma etch of the SOI wafer before a spin of photoresist compatible with the layout and the EBeam lithography system (JEOL JBX-8100FX 100kV Electron Beam Lithography System). The photoresist, as mentioned before was ZEP, which acts as a positive to negative resist after EBeam exposure, typically spun with a thickness of approx 560 nm. See Figure 8.


Fig. 8 - Cross Section of the chip after a layer of ZEP Photoresist has been spun on it.

The chip would now undergo the exposure to the 100kV Electron Beam Lithography System shown in Figure 9.

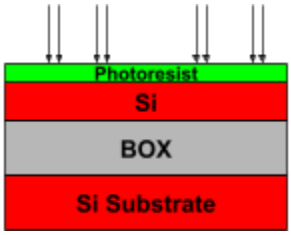


Fig. 9 - Cross section of Chip1 during exposure (arrows are exposure beams).

This is an overnight process as the detail and minimum feature size is carefully planned and executed by the Beamer system.

After the exposure, development is to begin in the cleanroom. This process typically starts with a 1 min soak in the ZED-N50 (developer) at 20°C to work with the ZEP-520A (resist), followed by 1 min at 20°C in IPA and dried with $N_2$. After calibrating the PlasmaPro 100 cobra to 5 mins at 15°C, 10mT, 25 sccm $SF_6$, 35 sccm $CF_4$, DC bias 220V HF power 30W and ICP power 800W for 5 mins. Place the chip on the carrier wafer using vacuum grease to hold the chip in the center of the wafer. Insert, start, remove, then clean the chip of the grease. See Fig. 10 for the result after the ICP etcher.


Fig. 10 - Cross section of the chip after development.

To remove the remaining resist, start by exposing the chip to UV light for 30 mins to break the bonds. Follow with a 10 minute soak in resist remover,, then a room temp soak for 5 mins. Finally, a 30 minute soak in a highly corrosive material, EKC 265 at 80°C. With an isopropanol rinse in between each soak and as a final rinse.

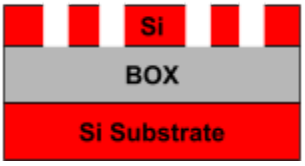


Fig. 11 - Cross section of the chip after stripping the photoresist.

Next will be the integration of the LASER onto the chip. This process is depicted in Figure 11 below.

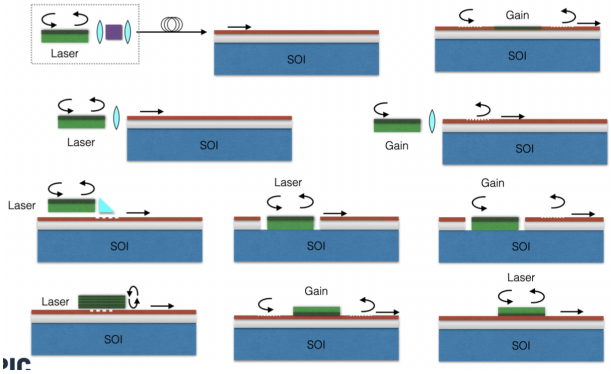


Fig. 11 - Integration process of the LASER onto the chip.

The final expected device is shown in Figure 12.

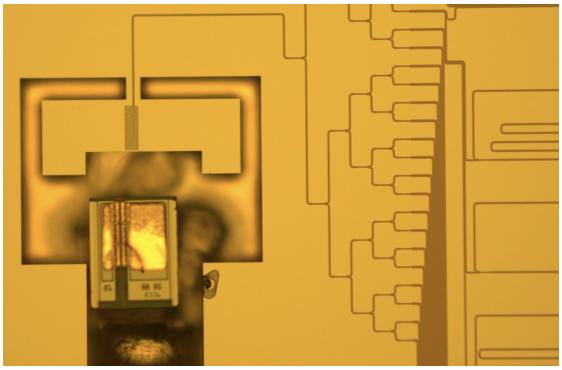

Fig. 12 - The LASER (left) that will be attached to the printed chip with all the students designs [1].

## V. EXPERIMENTS

*NEED MEASUREMENTS AFTER FABRICATION*

## VI. ANALYSIS

*NEED MEASUREMENTS AFTER FABRICATION*

## VII. DISCUSSION

*NEED MEASUREMENTS AFTER FABRICATION*

## VIII. CONCLUSION

*WILL WRITE LATER*

## ACKNOWLEDGEMENT

I acknowledge the ELEC 413 professor, Lucas Chrostowski and his teaching assistant, Kithmin Randula. I acknowledge the edX UBCx Silicon Photonics Design, Fabrication and Data Analysis course, which is supported by the Natural Sciences and Engineering Research Council of Canada (NSERC) Silicon Electronic-Photonic Integrated Circuits (SiEPIC) Program. The devices were fabricated by Sheri Jahan Chowdhury at the UBC nanofabrication facility. I acknowledge Lumerical Solutions, Inc., Mathworks, Mentor Graphics, Python, and KLayout for the design software.

## REFERENCES

[1] ELEC413-2023 Tunable Laser Diode Spectroscopy (TLDS) of a silicon photonic Bragg grating resonator, SiEPICfab Slides provided by Lucas Chrostowski.

## APPENDIX

Python code used in Klayout.

```
from pya import *
def design_jasmineradu(cell, cell_y, inst_wg1, inst_wg2, inst_wg3, waveguide_type):
  # load functions
  from SiEPIC.scripts import connect_pins_with_waveguide, connect_cell
  ly = cell.layout()
  library = ly.technology().name
##### designer circuit:
  # Create a physical text label so we can see under the microscope
  # How do we find out the PCell parameter variables?
  '''
  c = ly.create_cell('TEXT','Basic')
  [p.name for p in c.pcell_declaration().get_parameters() if c.is_pcell_variant]
  c.delete()
  '''
  # returns: ['text', 'font_name', 'layer', 'mag', 'inverse', 'bias', 'cspacing', 'lspacing', 'eff_cw', 'eff_ch', 'eff_lw', 'eff_dr', 'font']
  from SiEPIC.utils import get_technology_by_name
  TECHNOLOGY = get_technology_by_name(library)
  cell_text = ly.create_cell('TEXT', "Basic", {
     'text':cell.name,
     'layer': TECHNOLOGY['M1'],
     'mag': 30,
      })
  if not cell_text:
     raise Exception ('Cannot load text label cell; please check the script carefully.')
  cell.insert(CellInstArray(cell_text.cell_index(), Trans(Trans.R0, 25000,125000)))

  # load the cells from the PDK
  # choose appropriate parameters
```

```
  cell_bragg = ly.create_cell('Bragg_grating',
library, {
      'number_of_periods':100,
      'grating_period': 0.270,
      'corrugation_width': 0.05,
      'wg_width': 0.35,
      'sinusoidal': True})
  if not cell_bragg:
      raise Exception ('Cannot load Bragg grating
cell; please check the script carefully.')

  # instantiate y-branch (attached to input
waveguide)
  inst_y1 = connect_cell(inst_wg1, 'opt2', cell_y,
'opt2')

  # instantiate Bragg grating (attached to y branch)
  inst_bragg1 = connect_cell(inst_y1, 'opt1',
cell_bragg, 'opt1')

  # instantiate Bragg grating (attached to the first
Bragg grating)
  inst_bragg2 = connect_cell(inst_bragg1, 'opt2',
cell_bragg, 'opt2')

  # move the Bragg grating to the right, and up
  inst_bragg2.transform(Trans(250000,80000))

  #####
  # Waveguides for the two outputs:
  connect_pins_with_waveguide(inst_y1, 'opt3',
inst_wg3, 'opt1',
waveguide_type=waveguide_type)
  connect_pins_with_waveguide(inst_bragg2,
'opt1', inst_wg2, 'opt1',
waveguide_type=waveguide_type)

  '''
  make a long waveguide, back and forth,
  target 0.2 nm FSR assuming ng = 4
  > wavelength=1270e-9; ng=4; fsr=0.2e-9;
  > L = wavelength**2/2/ng/fsr
  > L * 1e6
  > 1000 [microns]
  using "turtle" routing

https://github.com/SiEPIC/SiEPIC-Tools/wiki/Scri
pted-Layout#adding-a-waveguide-between-compo
nents
  '''
  connect_pins_with_waveguide(inst_bragg1,
'opt2', inst_bragg2, 'opt2',
waveguide_type=waveguide_type,
      turtle_A =
[250,90,20,90,250,-90,20,-90,250,90,20,90,250,-90
,20,-90] )

  return inst_wg1, inst_wg2, inst_wg3
```