GPAC
GENERAL PURPOSE ANALOG CARD

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Introduction

The General-Purpose-Analog-Card (GPAC) is an adapter card for the Multi-IO FPGA board. It extends the digital IO capabilities of the Multi-IO card by analog blocks (power supplies, voltage and current sources, fast ADC etc.) , programmable level LV-CMOS, and LVDS digital IOs.

Figure 1: Overview of the connectivity between Multi-IO card, General Purpose Analog Card, and a PCB with a Device-Under-Test.

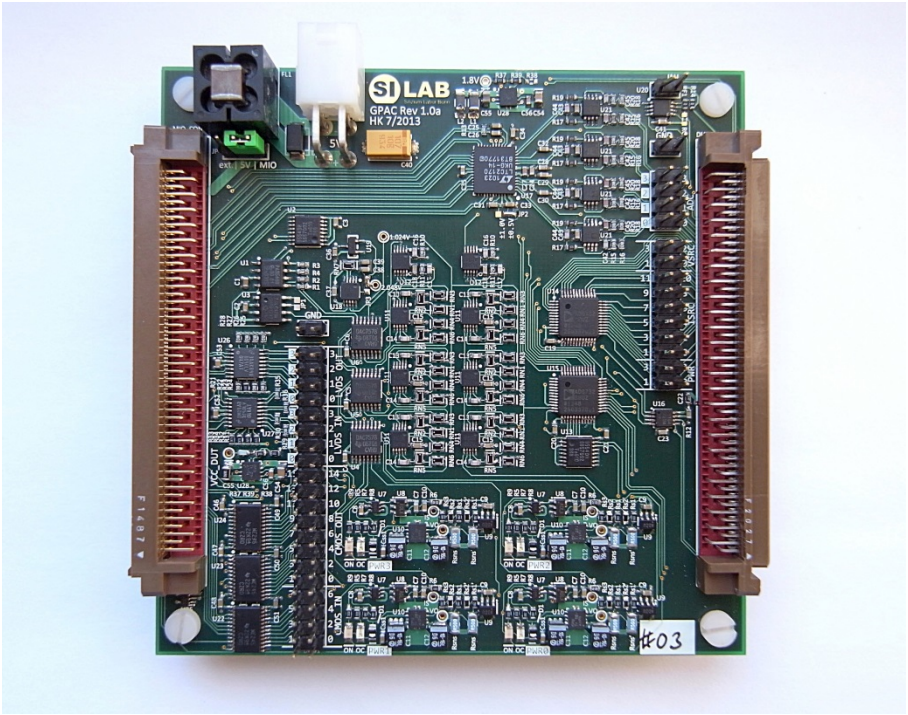


Figure 2: Picture of the GPA-Card. On the left the 100 pin KEL receptacle connects to the MultIO Board, on the upper edge the external lab power supply is connected and the KEL receptacle to the right connects to the DUT.

General-Purpose-Analog Card Overview

The Burn-In Card has numerous analog support functions and digital level shifting capabilities:

- 4 Power Supply Channels PWR[3..0]
  - Individual programmable output voltage: 0.8V – 2.8V (voltage range can be set by adjusting resistors values)
  - Maximum output current: 1.0 A (per channel, limited by LDO specs.)
  - Programmable current limit: 0..250 mA (common for all channels, can be changed by adjusting resistors values)
  - Current and voltage monitoring
- 12 Current Source Channels ISRC[11..0]
  - Output current: ±1mA
  - Programmable in 0.5µA steps (12-bit DAC)
  - Current and voltage monitoring
- 4 Voltage Sources Channels VSRC[3..0]
  - Output voltage: 0V – 2.048V
  - Programmable in 0.5mV steps (12-bit DAC)
  - Current and voltage monitoring
- Low voltage CMOS IO (level shifter)
  - 8 inputs
  - 16 outputs
  - CMOS levels controlled by setting of PWR[0]
- LVDS IO
  - 4 inputs
  - 4 outputs
- Fast ADC
  - Four channels
  - 14-Bit, 25 Msps
  - Differential inputs with fully differential drivers
- Injection Pulse Generator
  - Programmable voltage levels (high and low)
- Miscellaneous
  - Storage of calibration constants with on-board EEPROM
  - All outputs (analog and digital) can be simultaneously enabled and disabled
  - Clamping of all analog output levels to potential defined by PWR[0]
  - Four auxiliary slow ADC inputs for monitoring purposes

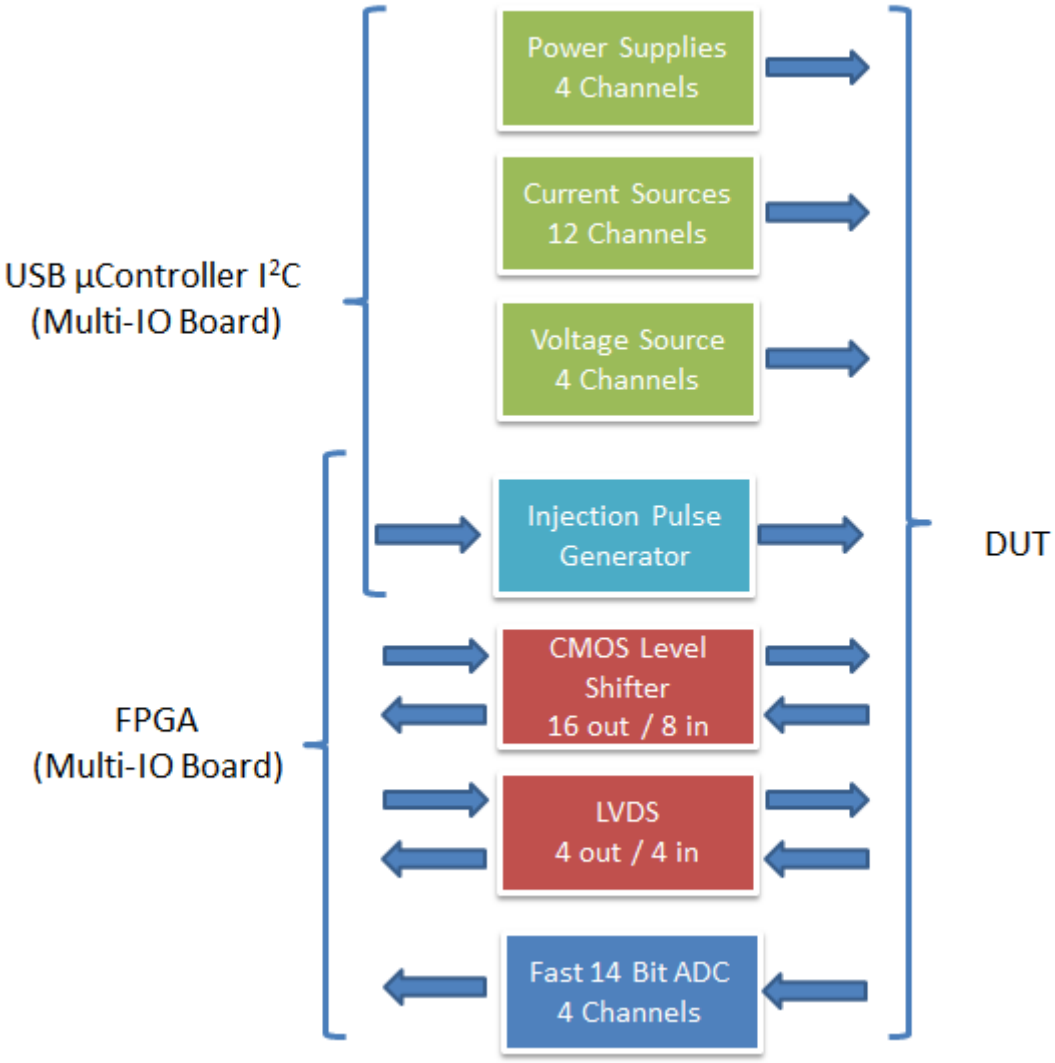


Figure 3: Function block diagram of the General-Purpose-Analog Card

Theory of Operation

Analog Channels

All analog settings and voltage and current readback are controlled via the I2C interface of the Multi-IO board. 23 DAC channels with 12 bits resolution control the output of 4 power channels PWR[3:0], 4 voltage outputs VSRC[3:0], 12 current outputs ISRC[11:0], two injection levels and a current limit for the power channels. The outputs of all current and voltage sources are enabled with the enable signal of the power supply PWR[0]. For additional safety of the DUT the analog outputs are clamped to (a replica) potential of PWR[0].

The power supplies can be enabled individually which is signaled by green LEDs. The current limit for the power supplies is common to all four channels and sets a trip threshold: an over-current event switches the affected supply off (i.e. it is not going into constant output current mode). In case of an over-current event the given power channel will switch off immediately and a red LED will be turned on. After removing the over-current condition the affected power supply has to be switched off and on again to reset the current limit latch.

Digital Channels

The digital IO consists of 4 LVDS outputs, 4 LVDS inputs, 16 low voltage CMOS outputs and 8 low voltage CMOS inputs. After appropriate level-shifting / translation these IOs connect to FPGA pins to the MIO board. The outputs (both LVDS and LVCMOS) to the DUT are – as the analog outputs – enabled with the enable signal for the power supply PWR[0]. In addition the voltage level for the LVCMOS IOs (inputs and outputs) track the output voltage of PWR[0]. For generating this voltage rail for the level shifters an individual voltage regulator which tracks PWR[0] is used. Therefore the current consumed by the level shifters is not seen in PWR[0].

Injection Pulse Generator

To generate a voltage step for calibration purposes an analog multiplexer, controlled by an FPGA signal can switch its output between two programmable output levels INJ[0] and INJ[1]. For optimal operation the lower level should be set at least to 200mV above ground.

Fast ADC

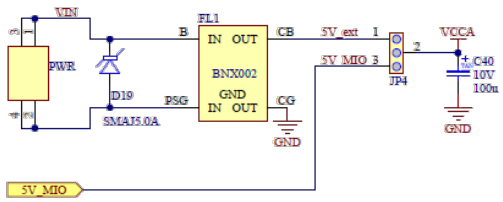
For the read-out of analog output DUTs a four channel 14-bit, 25 Msps ADC with differential inputs is available which is controlled by the FPGA on the MIO board.

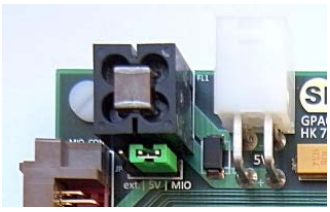
Configuration

The GPA card provides some HW-selectable configuration options for its main supply, the input range of the fast ADC and the gain of the injection pulse generator.

GPAC input voltage

The supply voltage for the GPA card (VCCA = 5V) can be either taken from an external power supply via the MOLEX connector or the MultIO board can be used. Note that if power from the MIO board is used it is strongly recommended that the MIO board itself is powered from an external 5V supply and **not from the USB bus.**

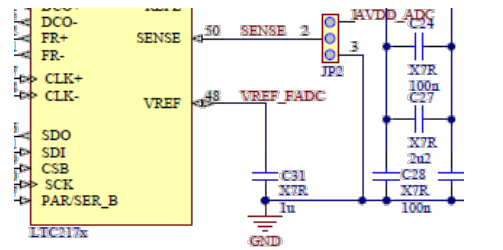


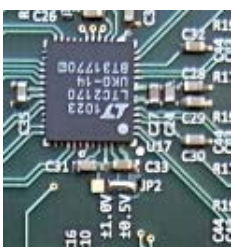


JP4 (5V) setting	Power supply
Ext.	External 5V
MIO	MultiIO board

Fast ADC input range

The input range of the quad channel fast ADC can be set to ±1.0V or ±0.5V. Please note that the silk screen print on the Rev. 1.0a of the PCB are swapped (i.e. closing JP2 labeled “±0.5V” will set the range to ±1.0V and vice versa.

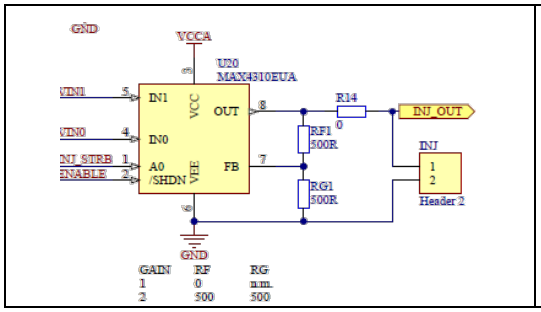




JP2 setting	Input range
GND	±0.5V
MIO	±1.0V

Injection pulse generator

The injection pulse generator uses a buffered analog multiplexer with adjustable output gain. When *RF1* is 0Ω and *RG1* not mounted the gain is one (default configuration). For a gain of two *RF1* and *RG1*should both be set to 500Ω. In this configuration *R14* can be set to match an existing termination resistor at the DUT input without reducing the pulse amplitude.



RF1 / RG1	Gain
0 Ω / open	1 (default)
500 Ω / 500Ω	2

Known Issues

Revision 1.1

- none so far

Revision 1.0a

- Silk screen prints of R12 and C22 are swapped
- Silk screen print of JP2 for ADC range setting ±1.0V / ±0.5V is swapped

Revision History

PCB Revision	*Comment*
1.0	Initial design
1.0a	Small bug fixes (manually fixed on existing Rev 1.0 cards)
1.1	Fixed silk screen prints in two places

Document Revision	*Comment*	*Author/Date*
1.0	Initial	HK / Dec 2013
1.0a	• Added configuration description • Few corrections	HK / 8.5.14
1.1	• Changes current limit range	HK / 26.3.2015