

VDD
GND

INP

INN

CLK

I1

INP

INN

CLK

Double_tail

OUTP

OUTN

GND
VDD
GND
VDD

COMP_P

COMP_N

I0

COMP_P

COMP_N

SR_Latch

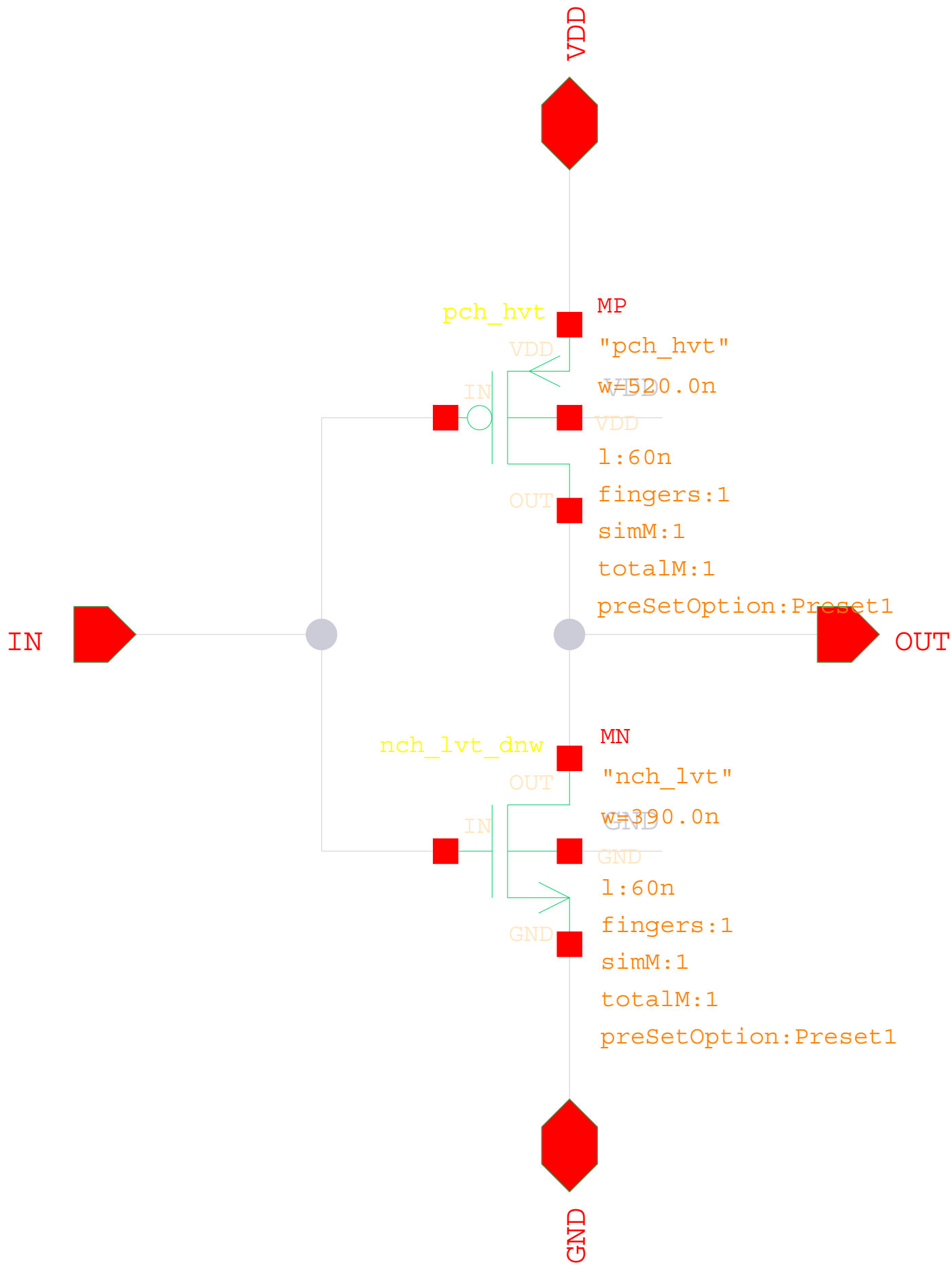
LATCH_P

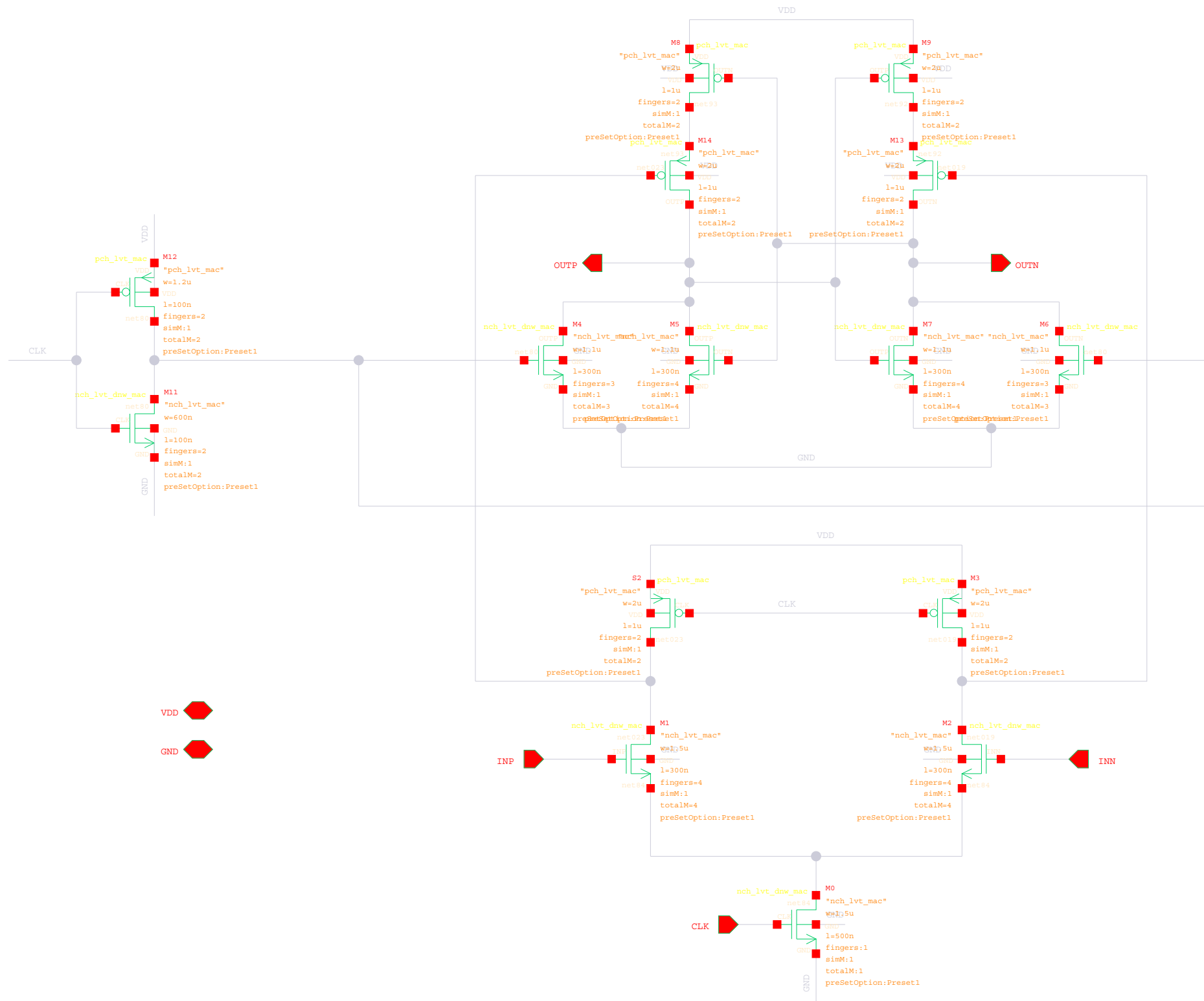
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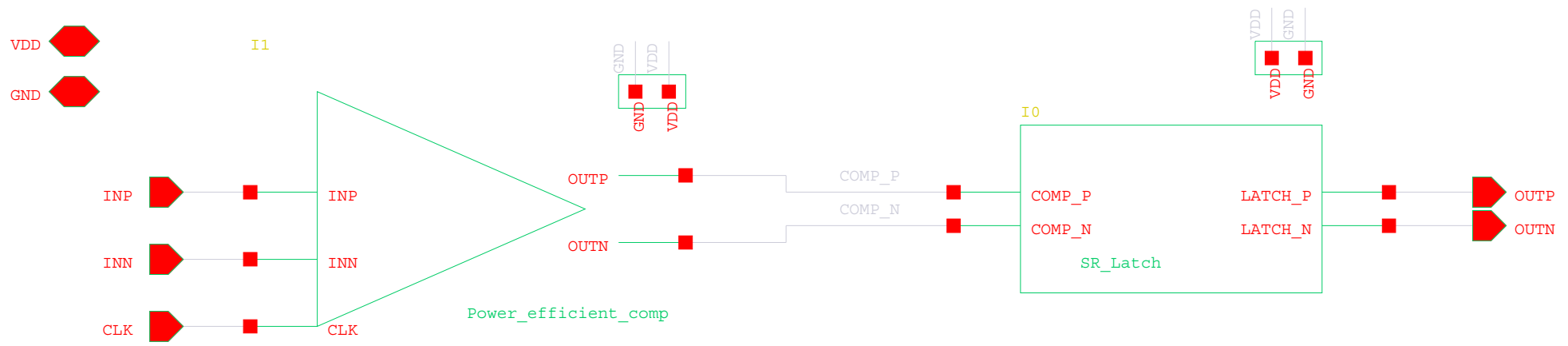
VDD
GND
VDD
GND

OUTP

OUTN



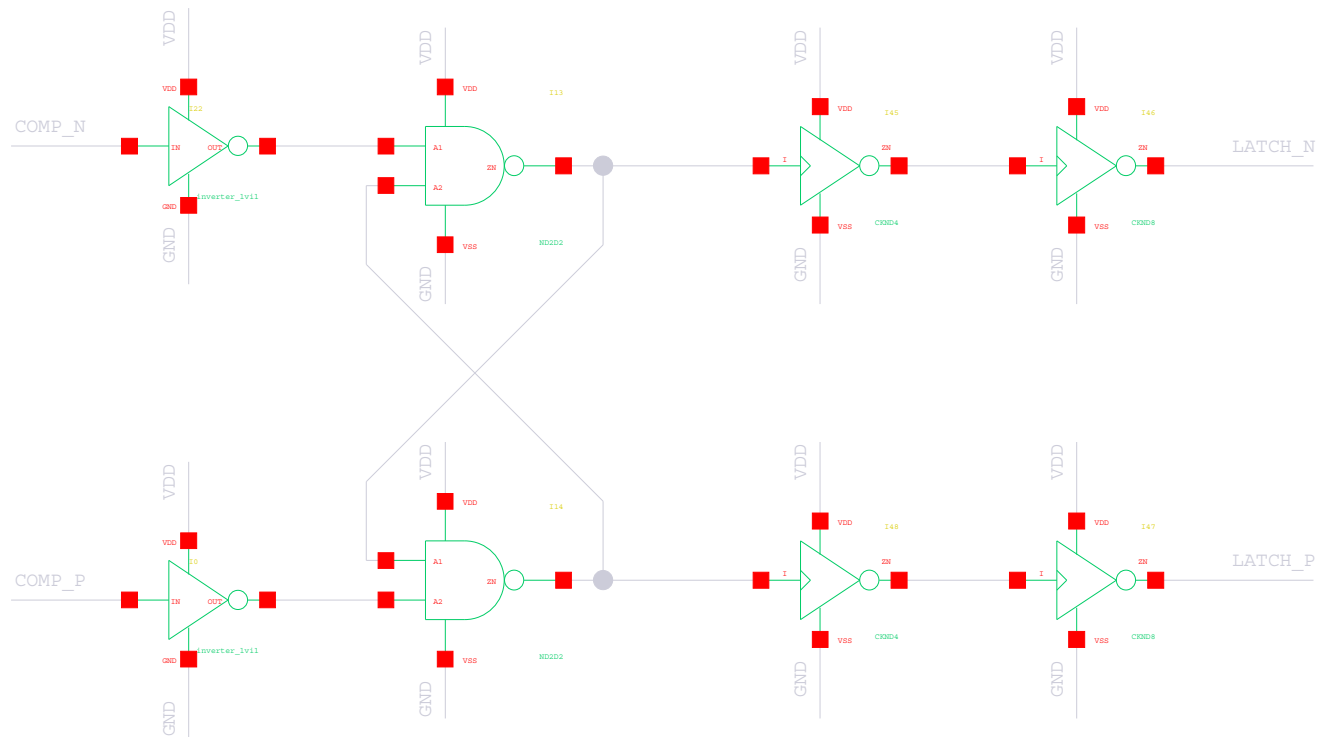




VDD
GND

COMP_N

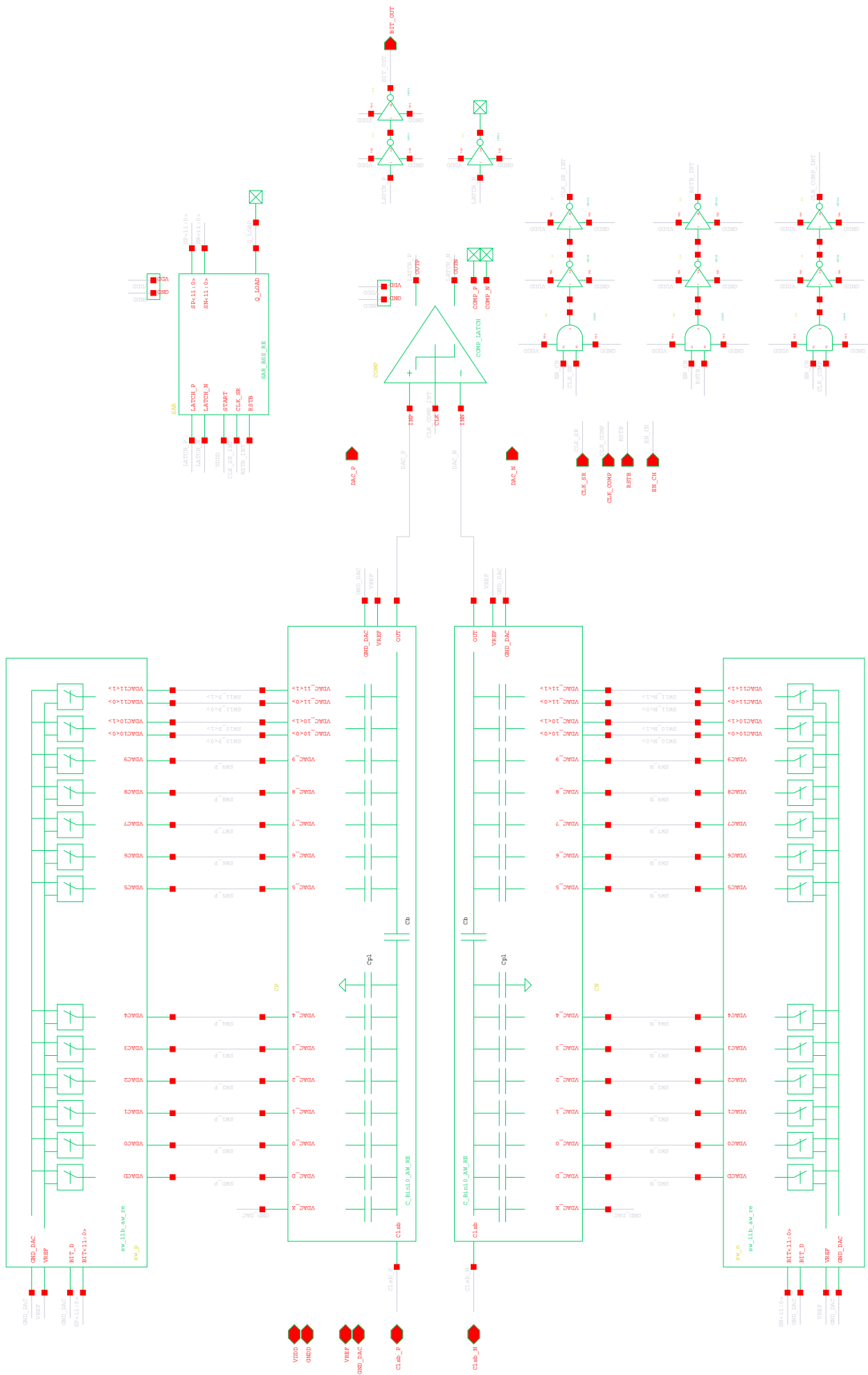
COMP_P

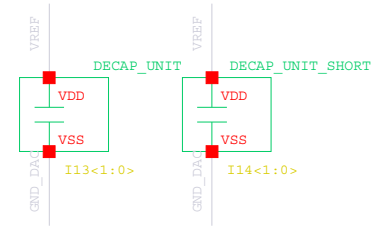
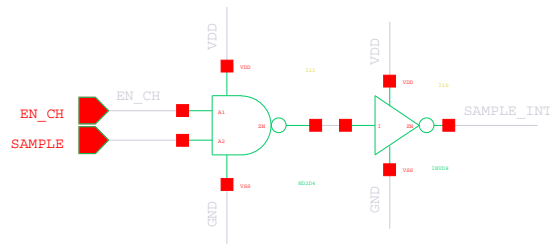
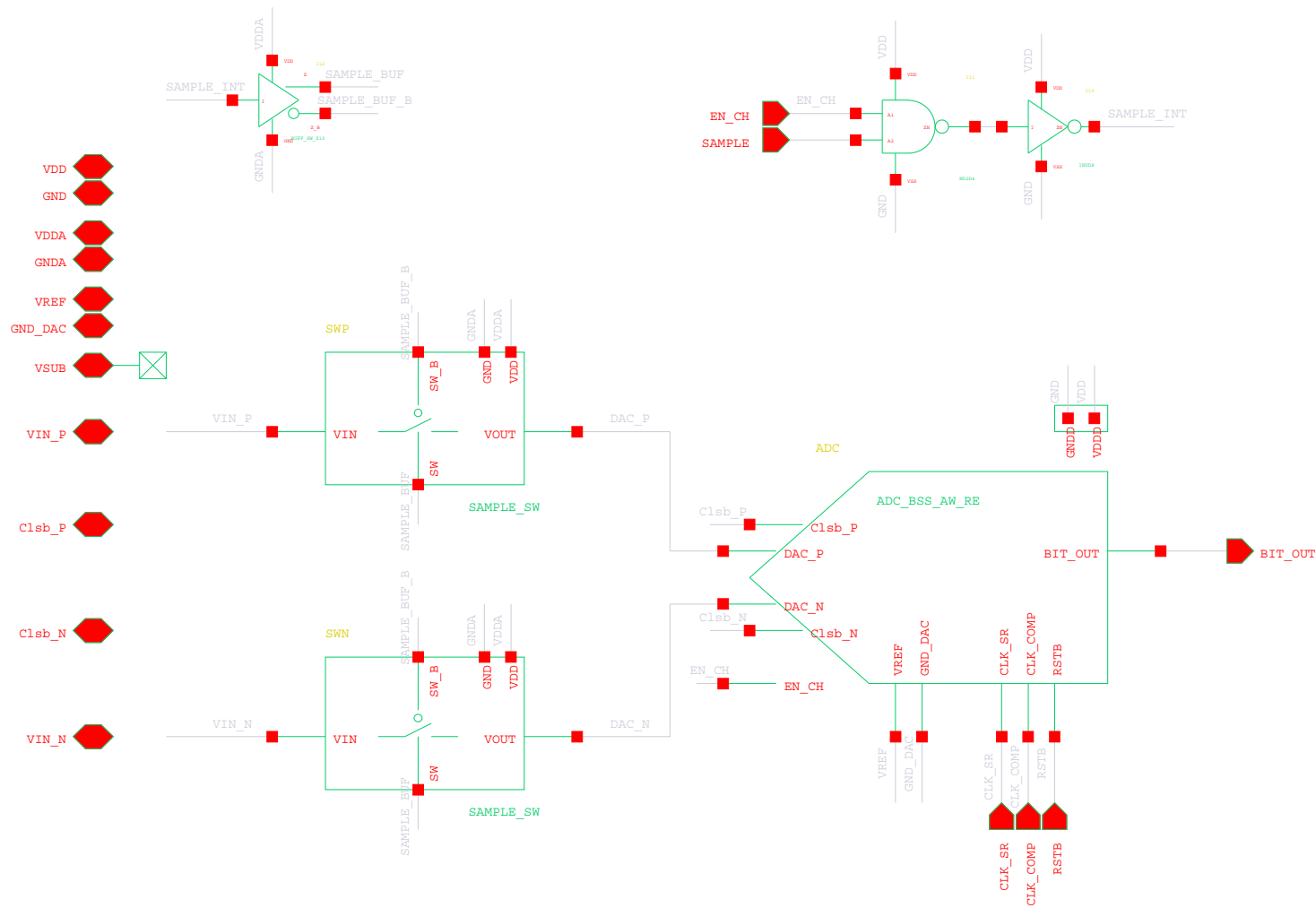


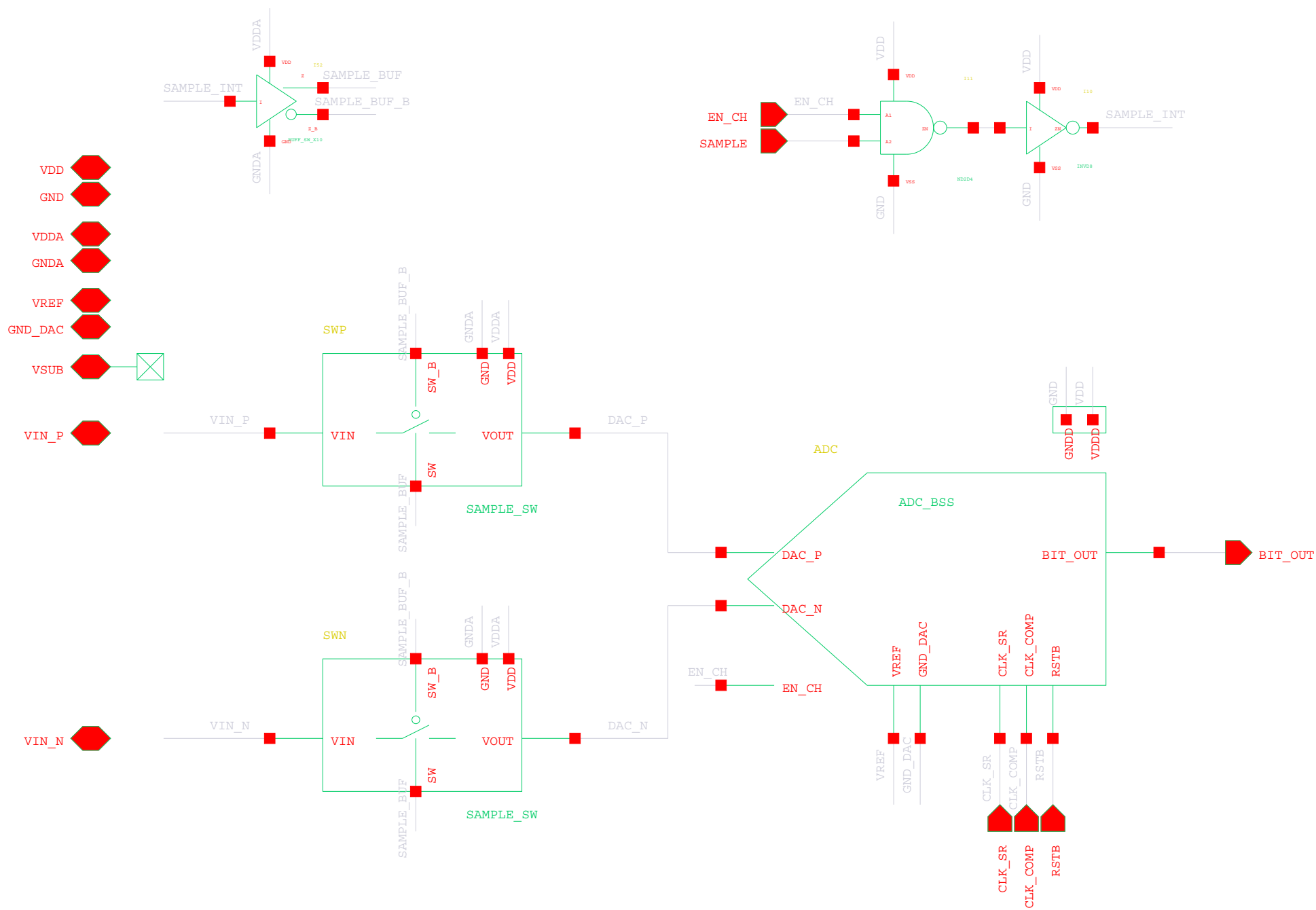
LATCH_N

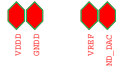
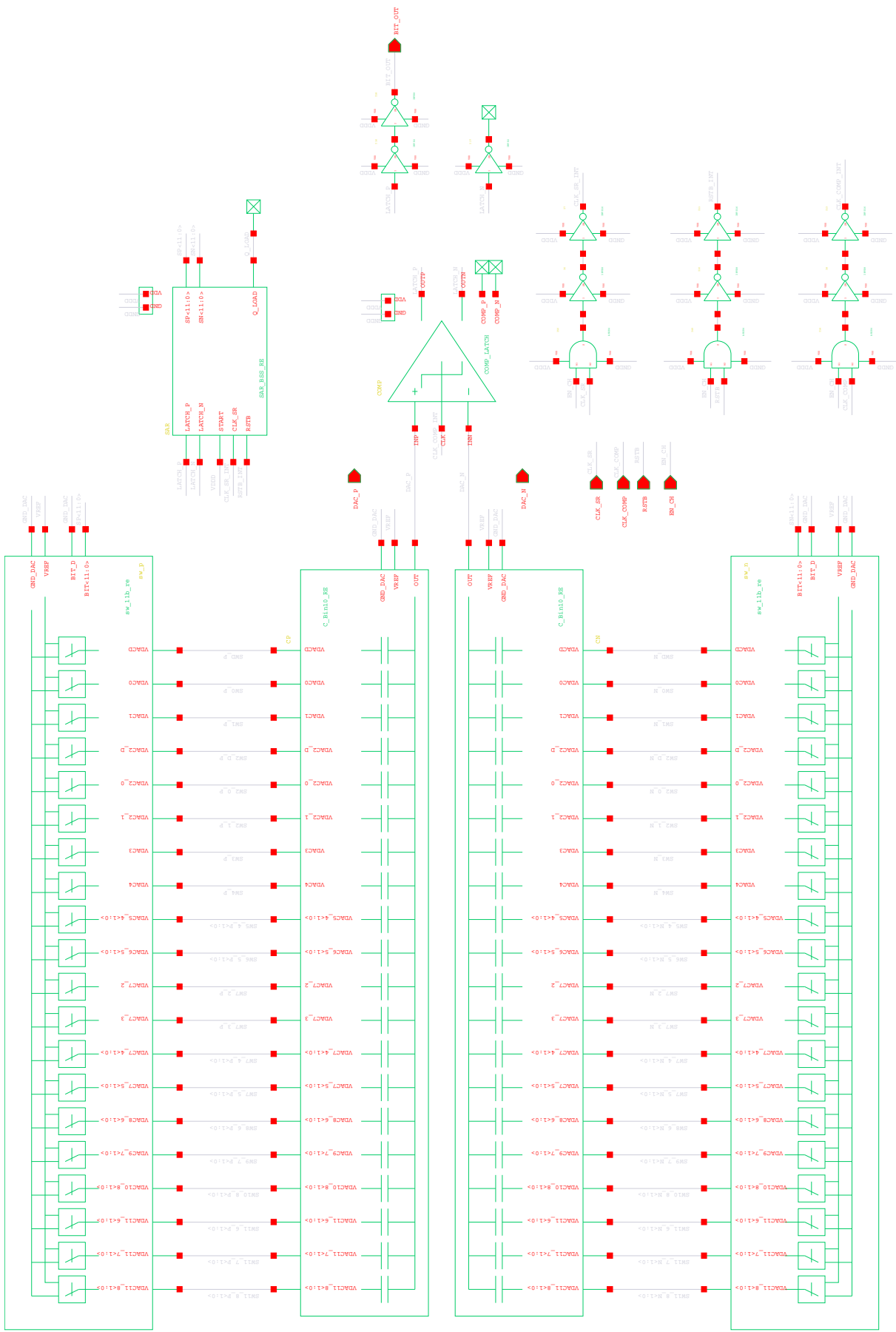
LATCH_P

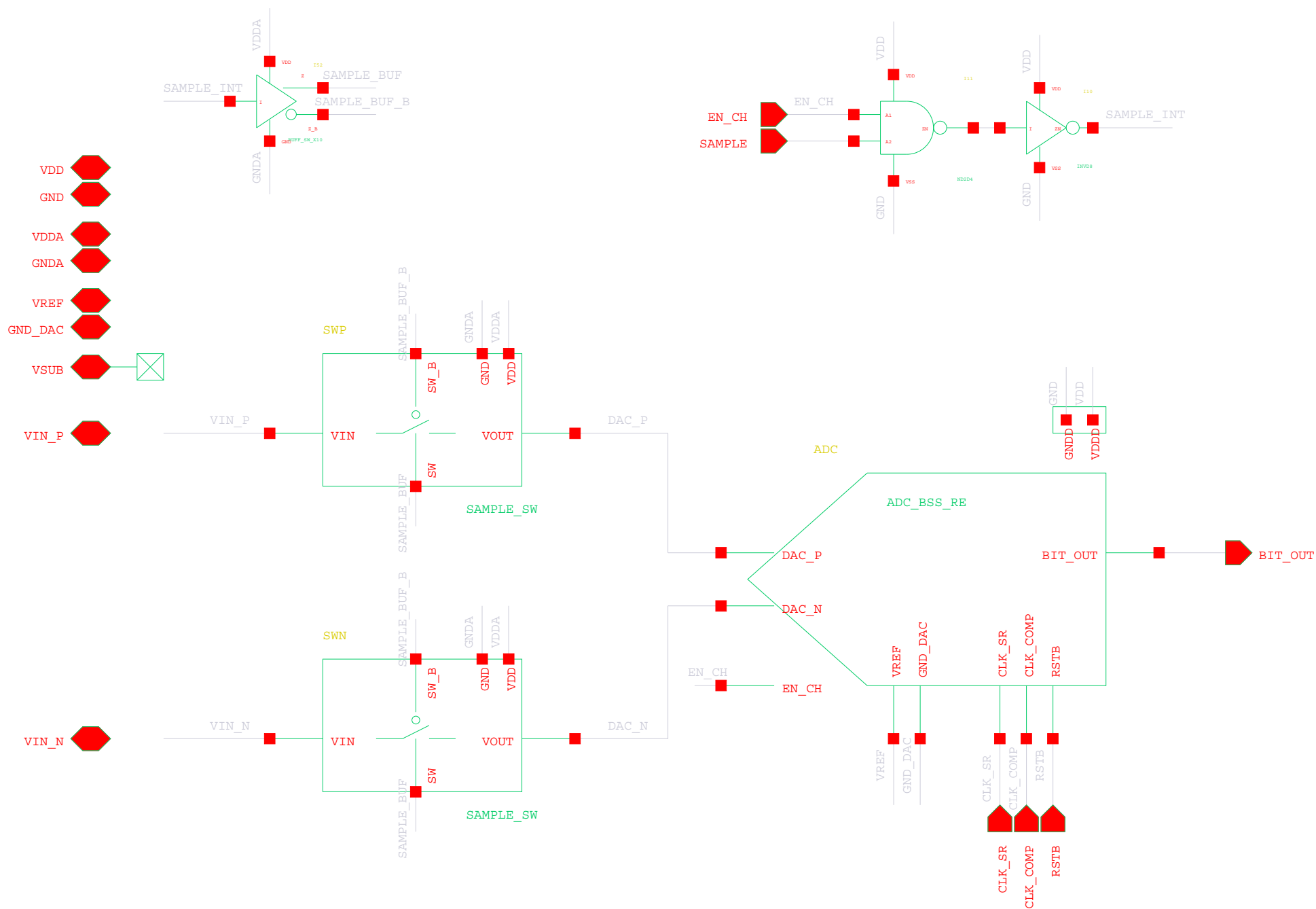


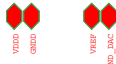


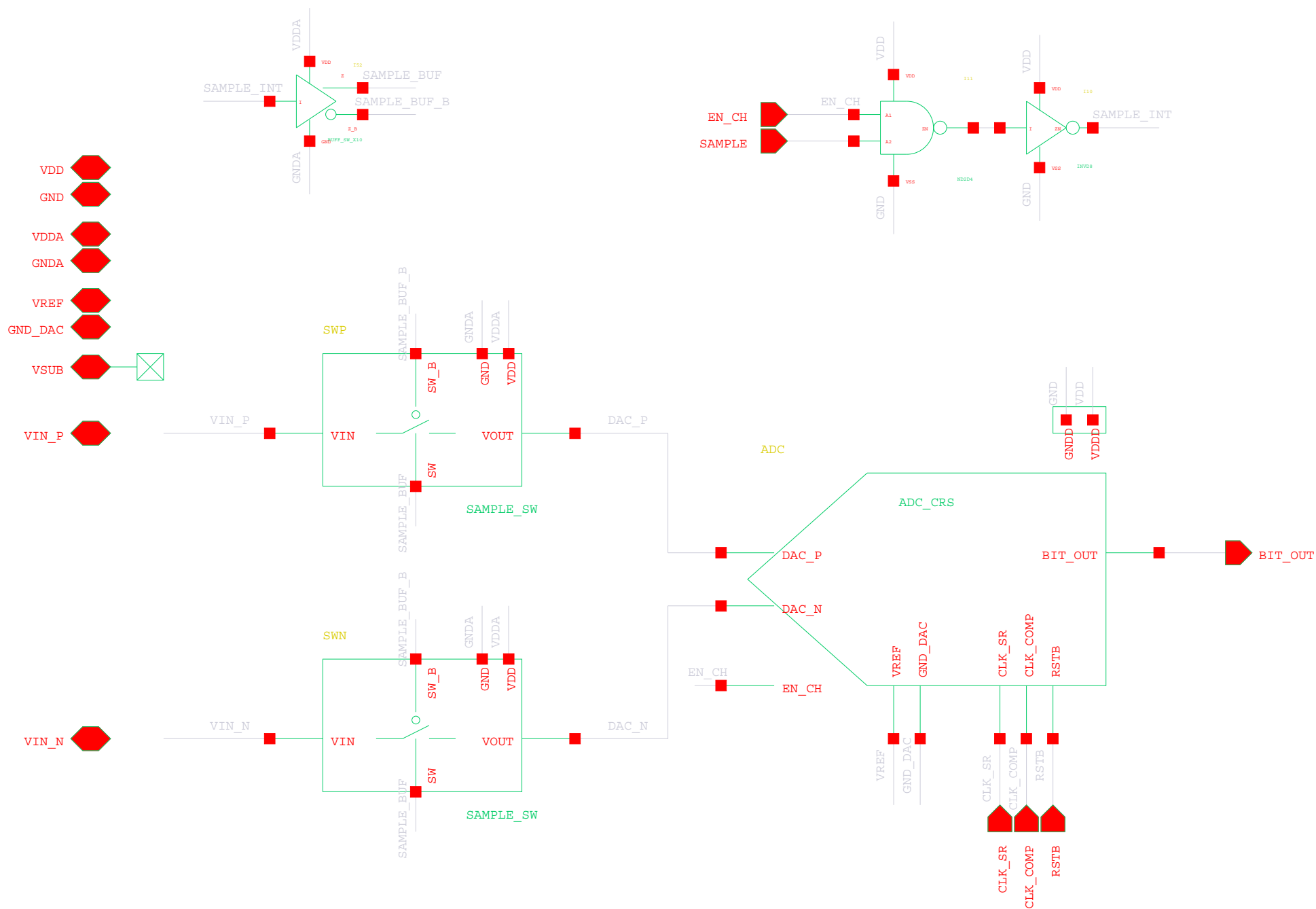


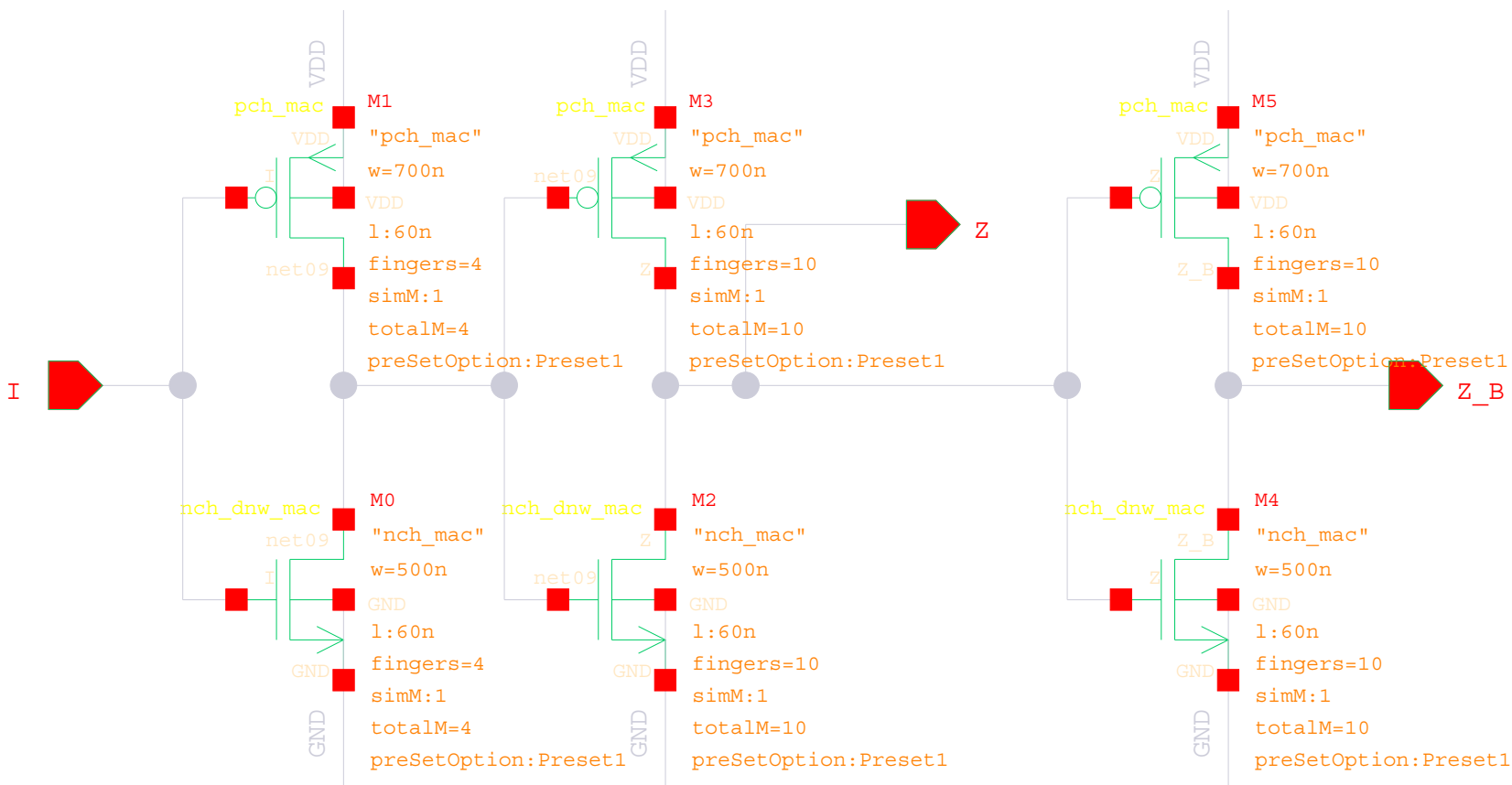




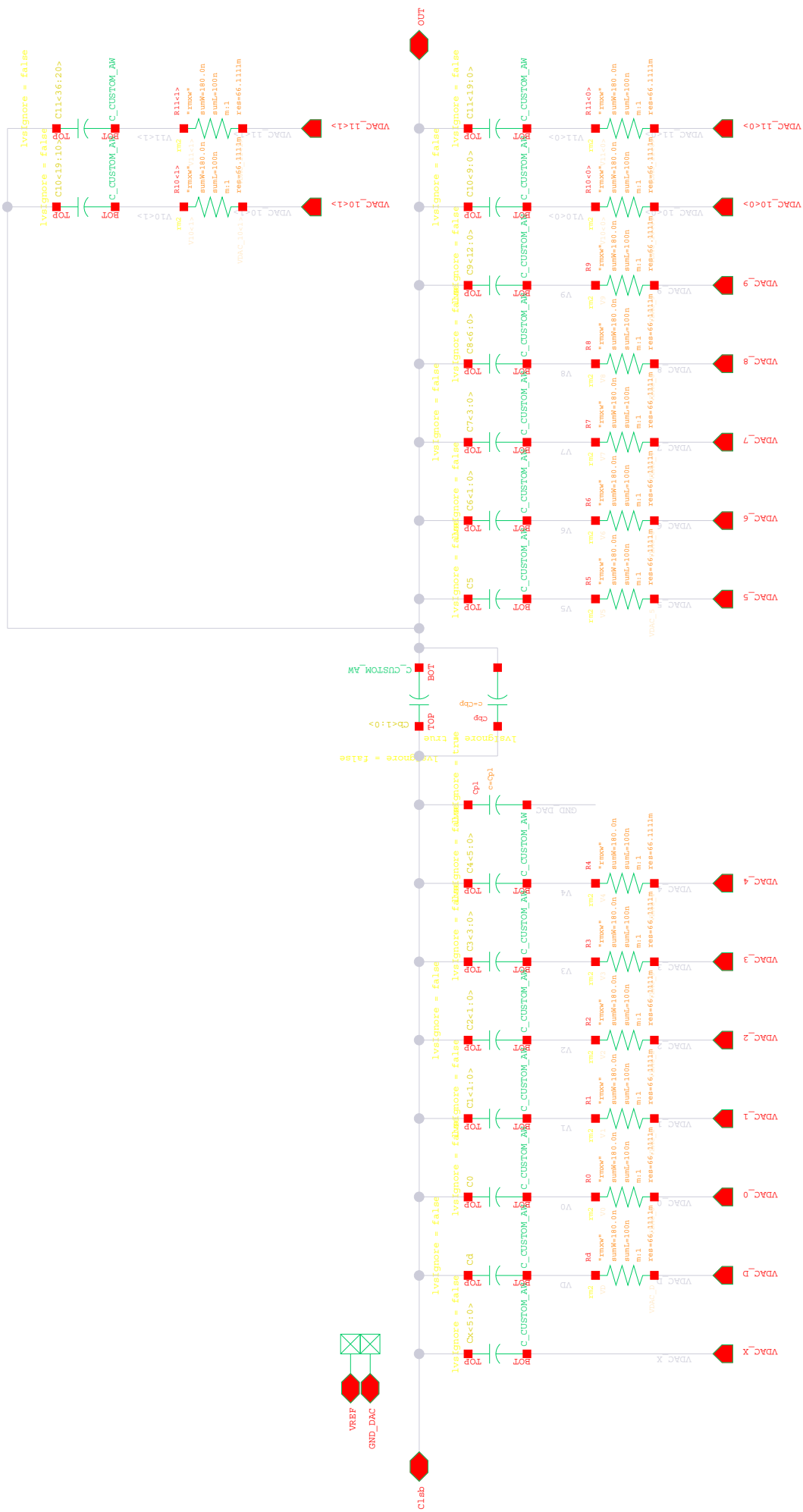


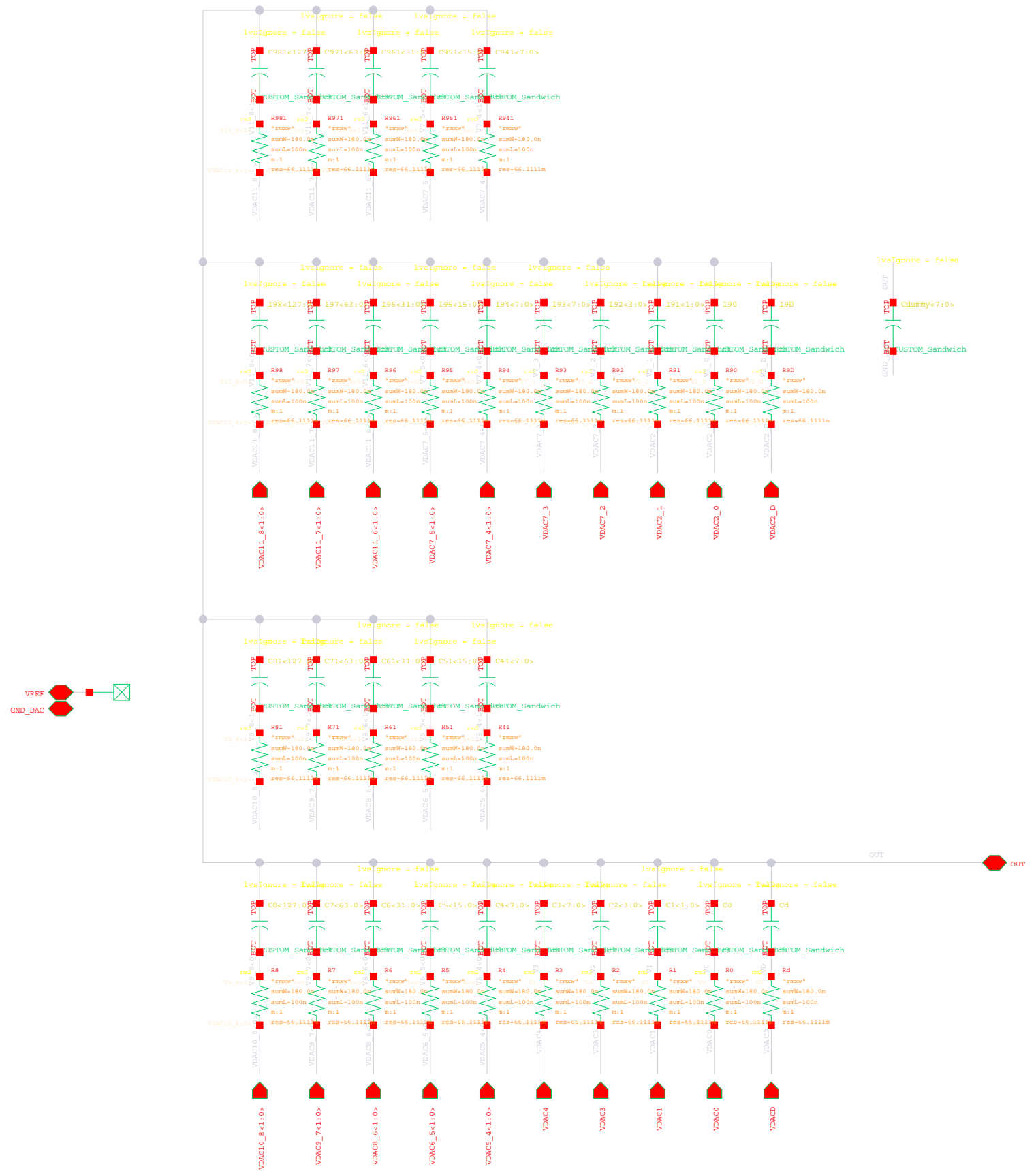


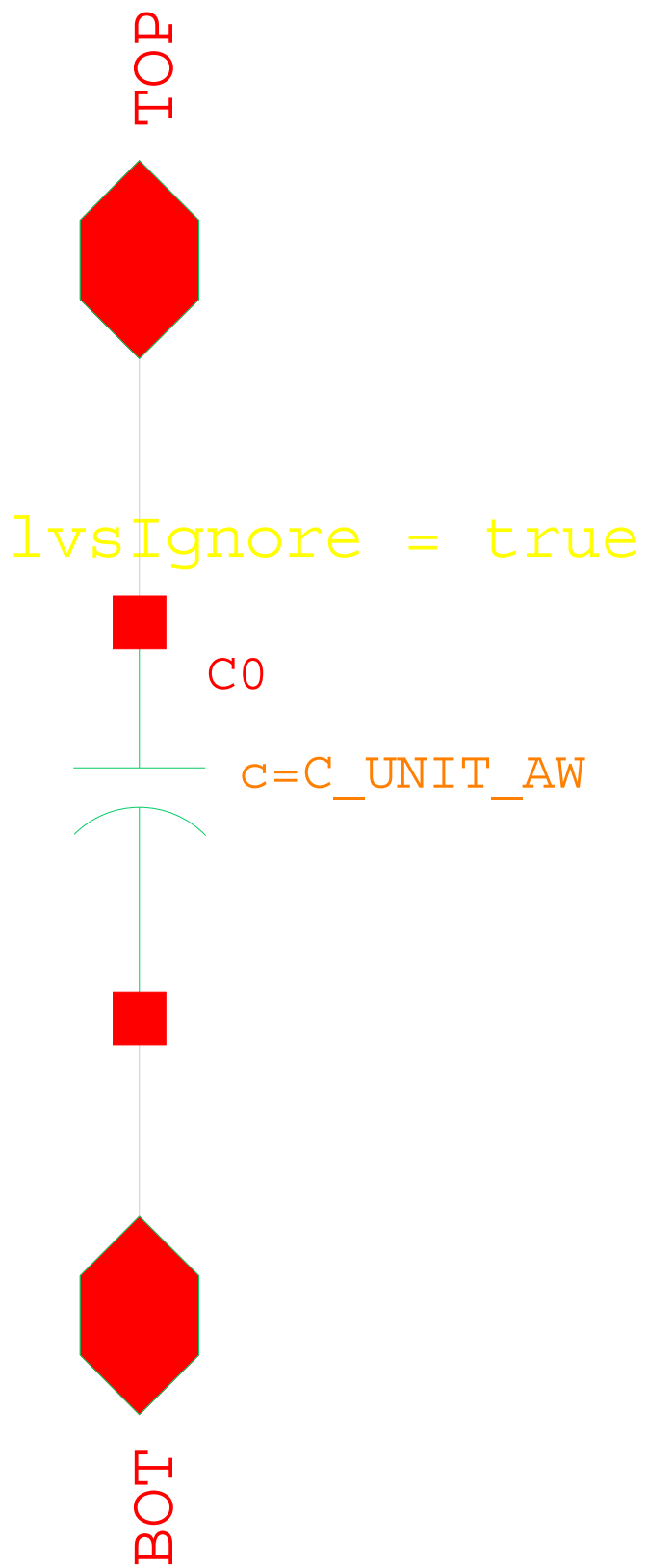


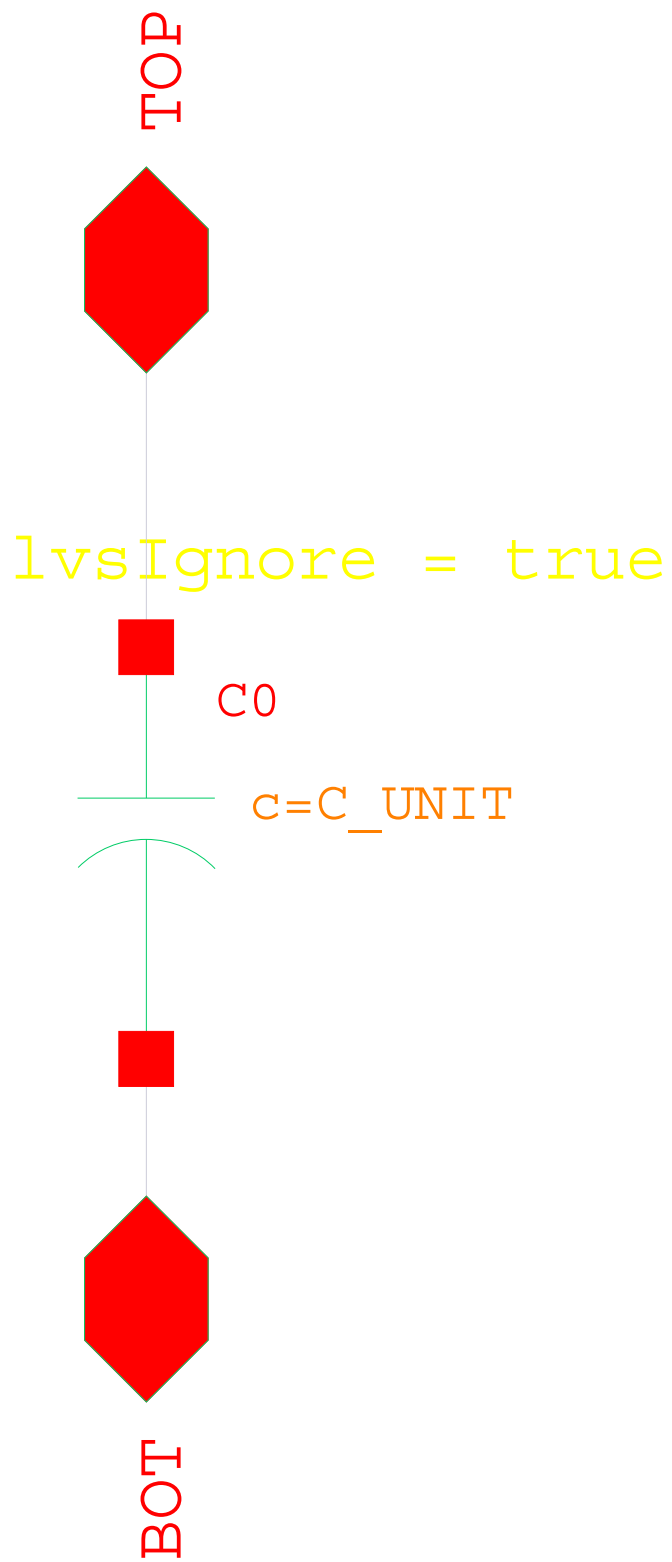


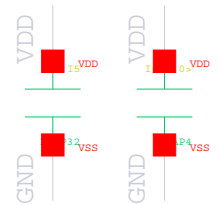
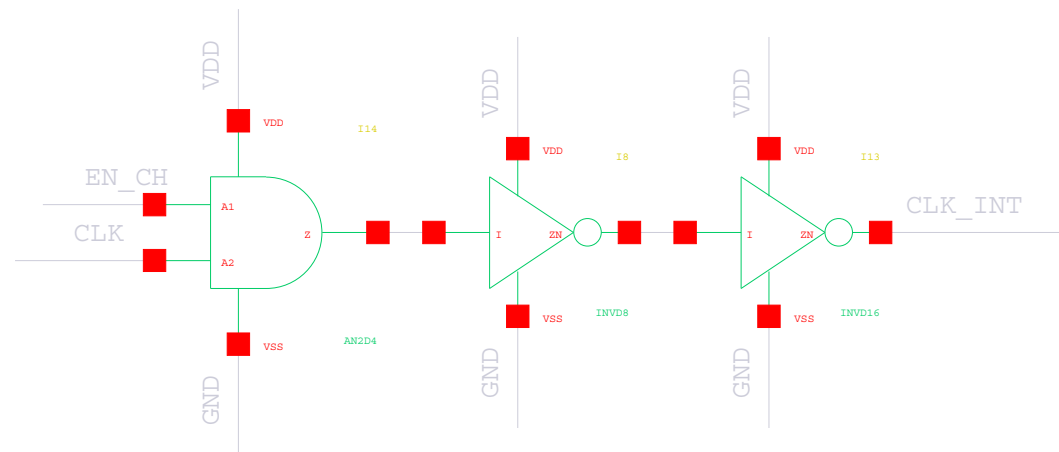
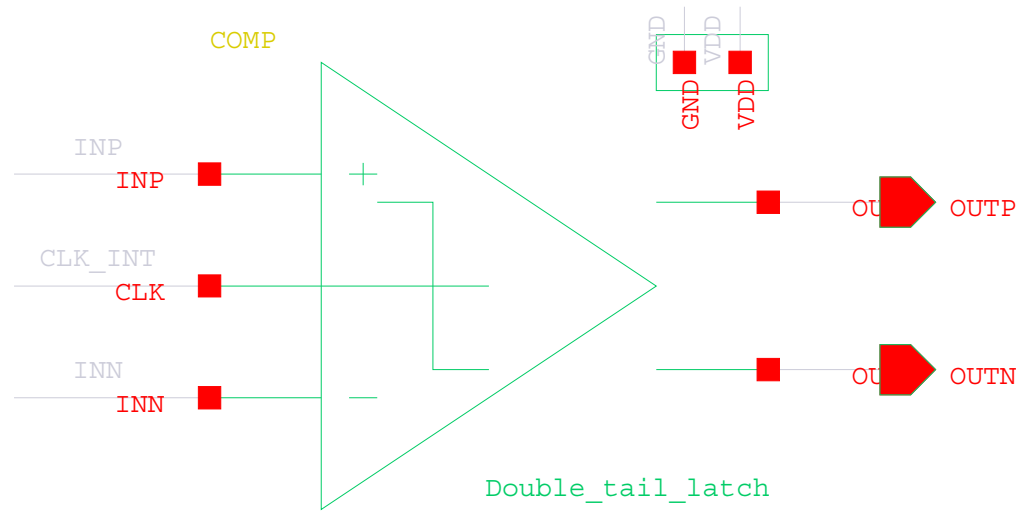
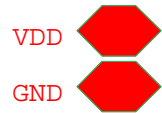


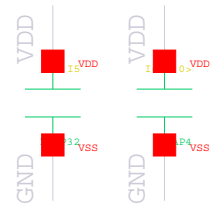
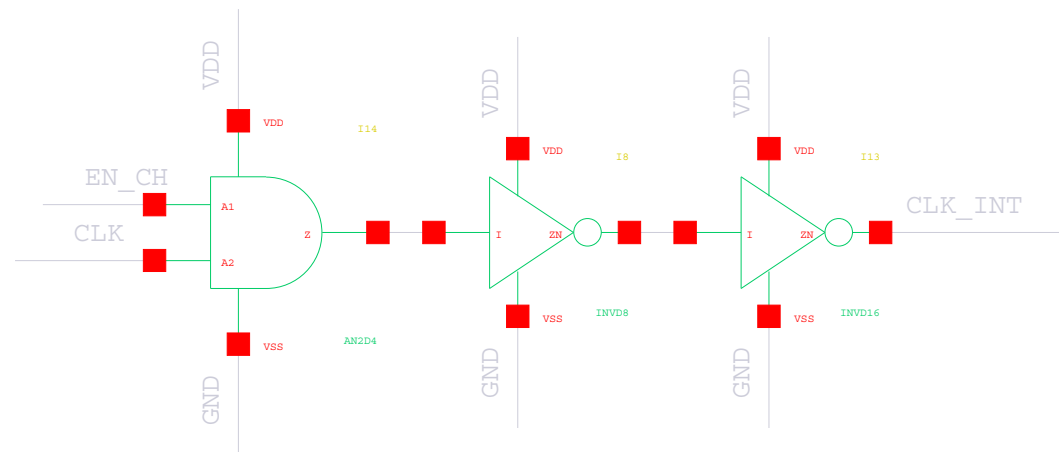
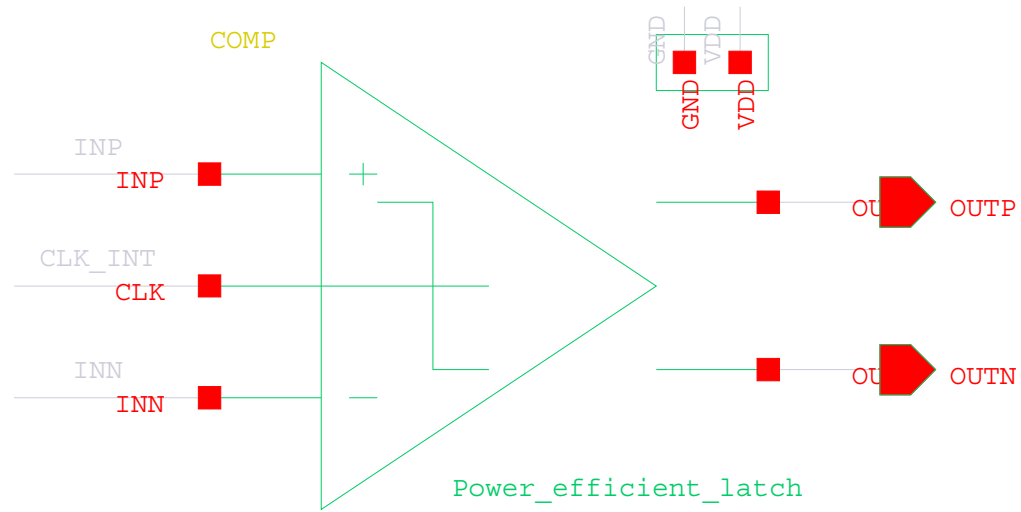
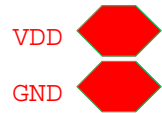












VDD

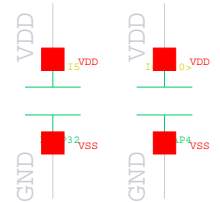
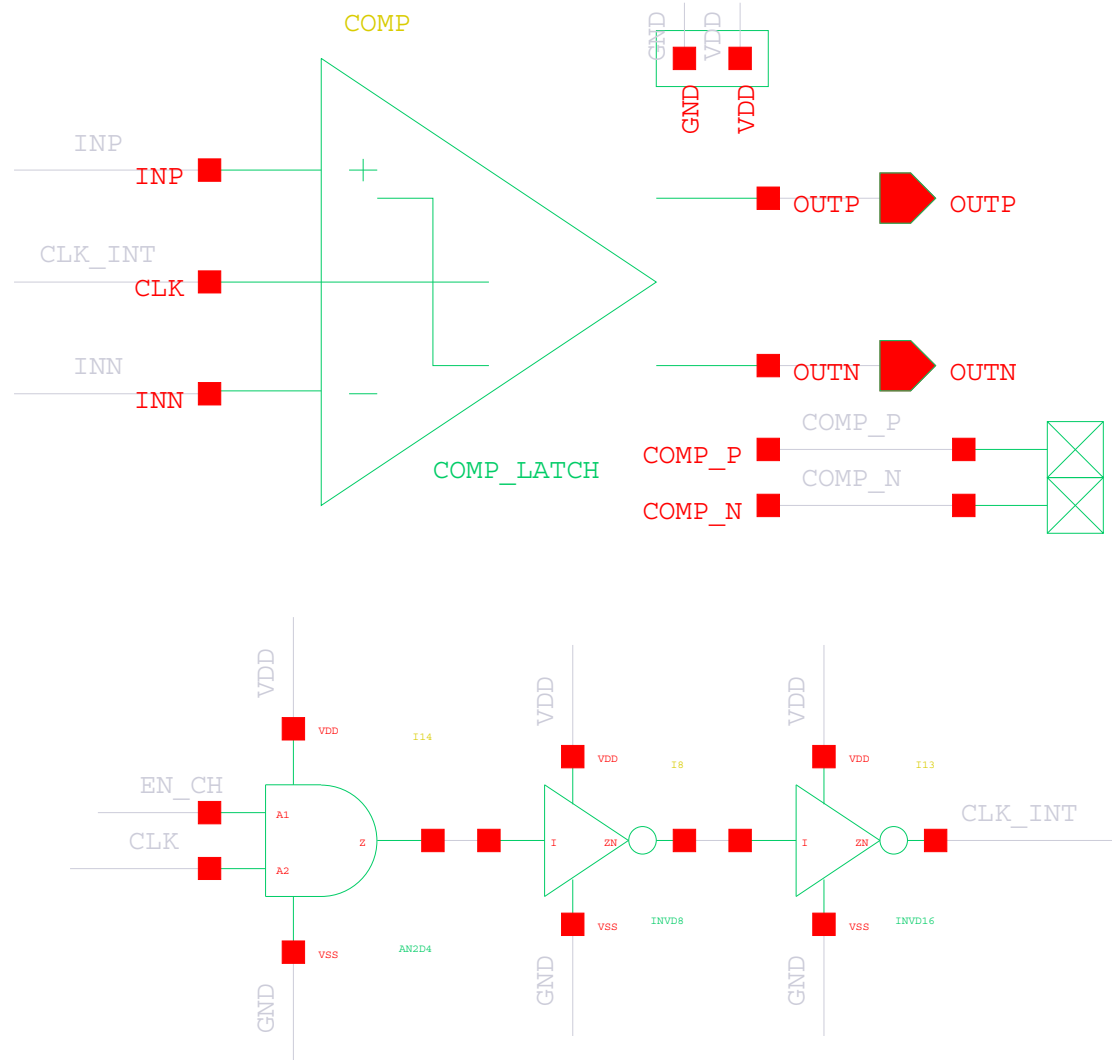
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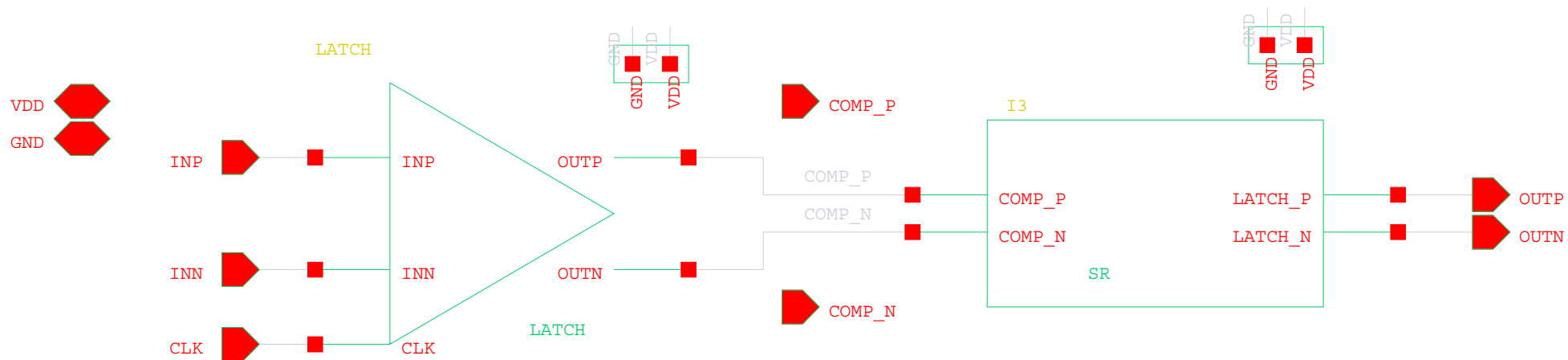
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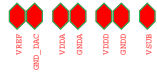
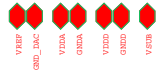
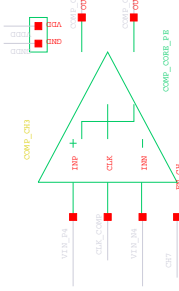
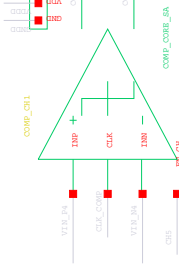
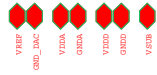
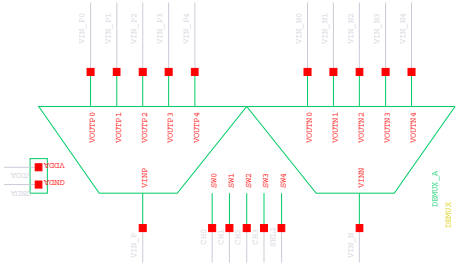
INN

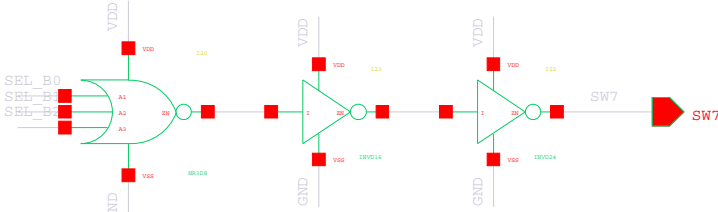
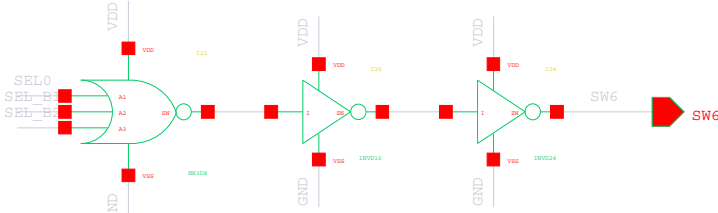
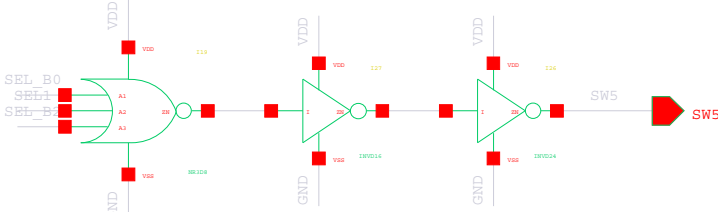
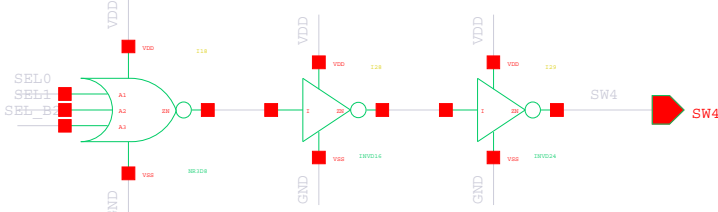
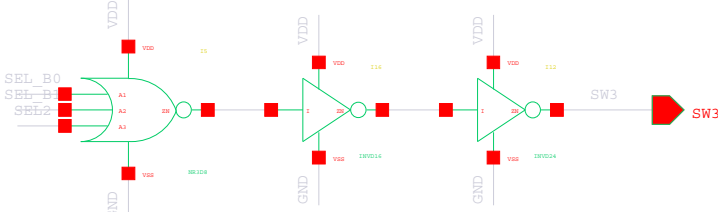
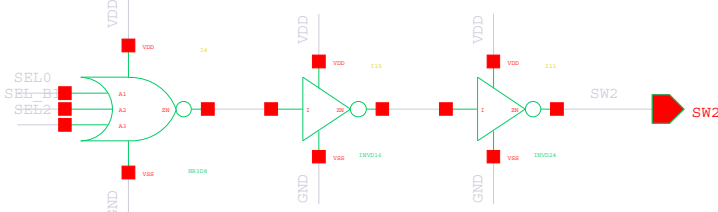
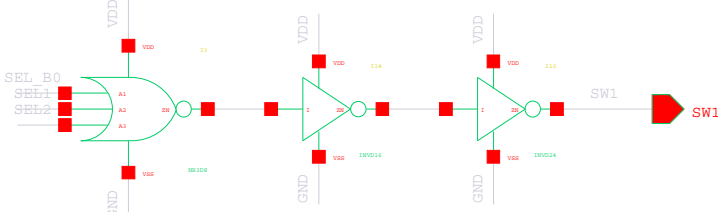
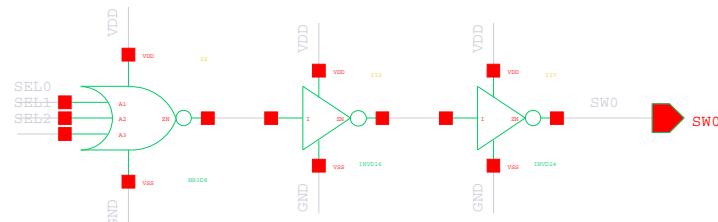
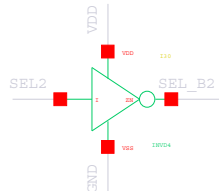
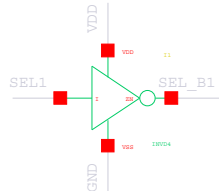
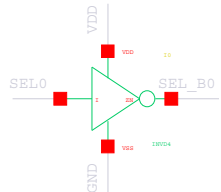
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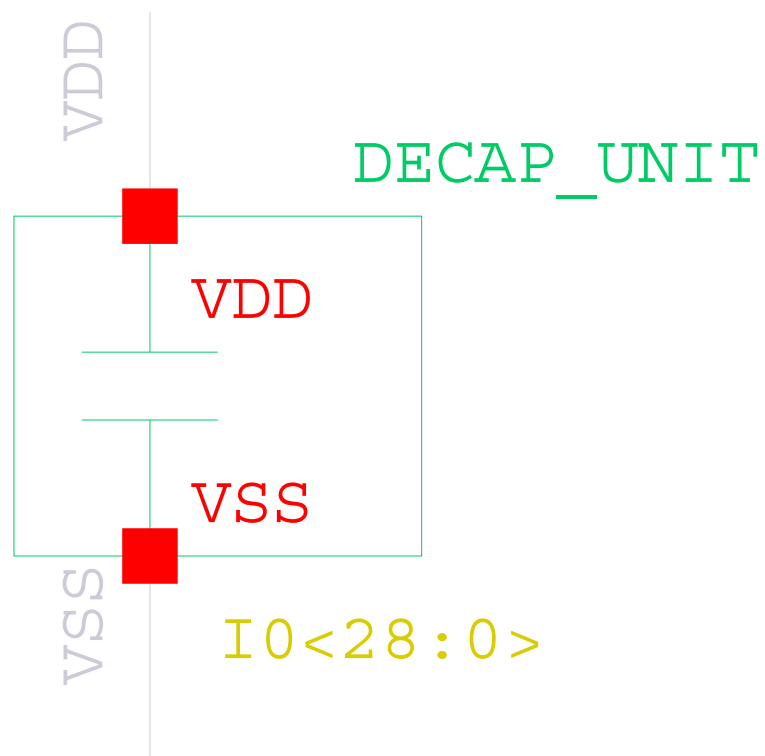
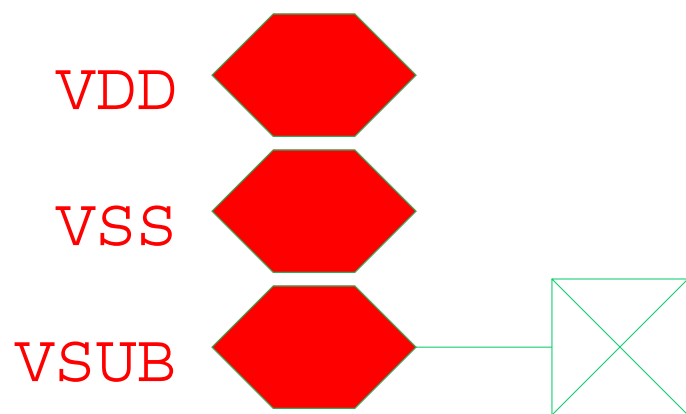
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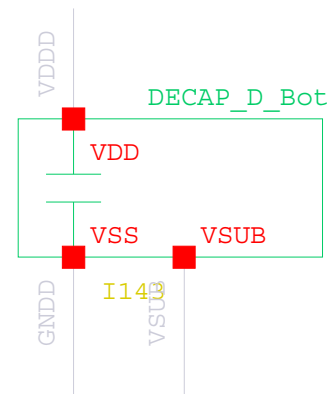
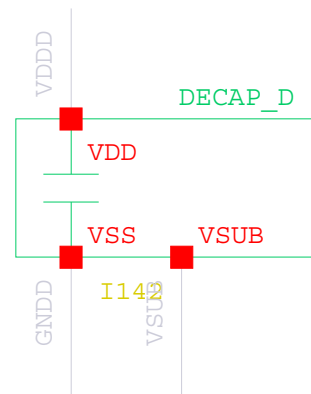
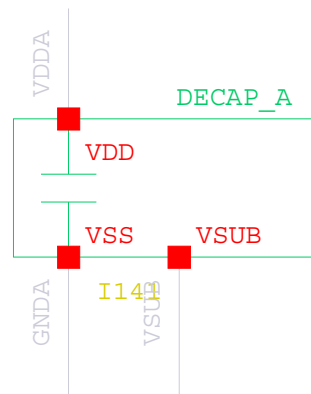
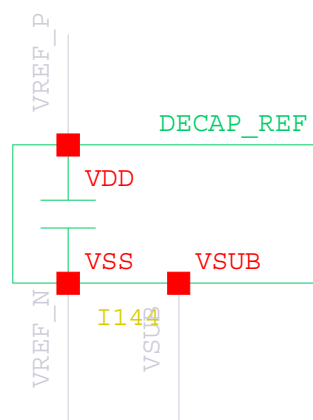
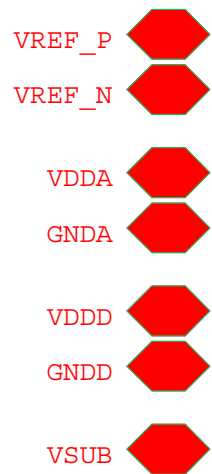


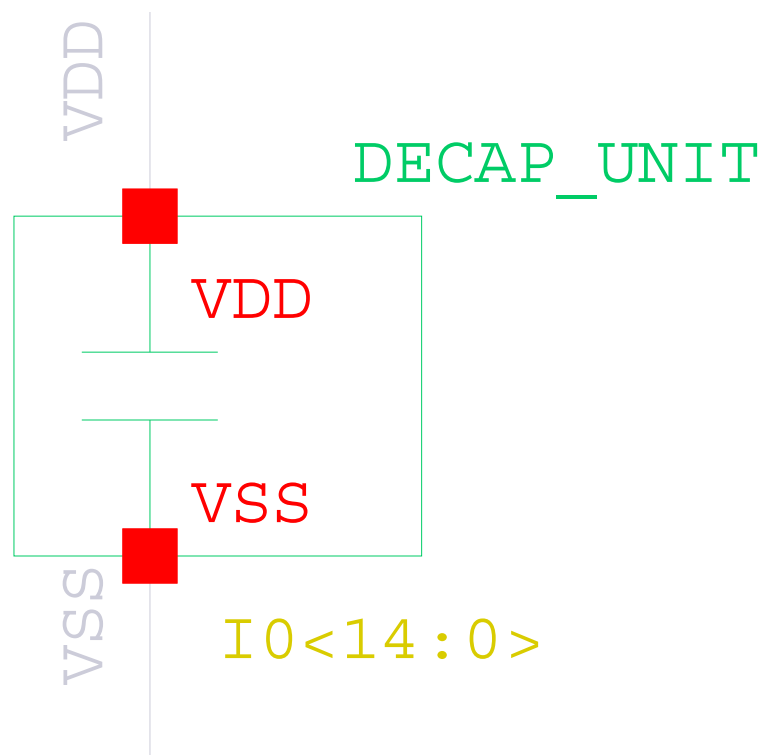
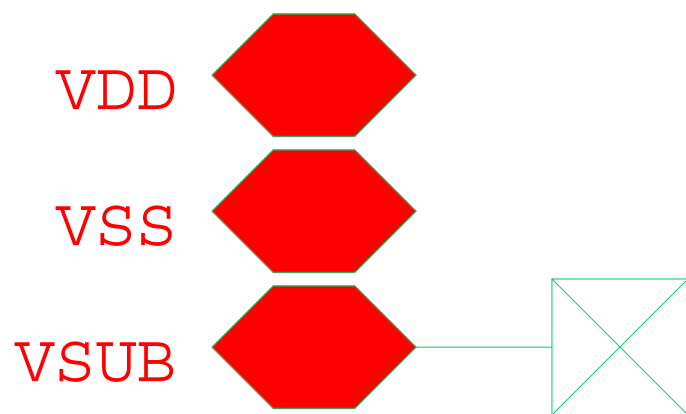


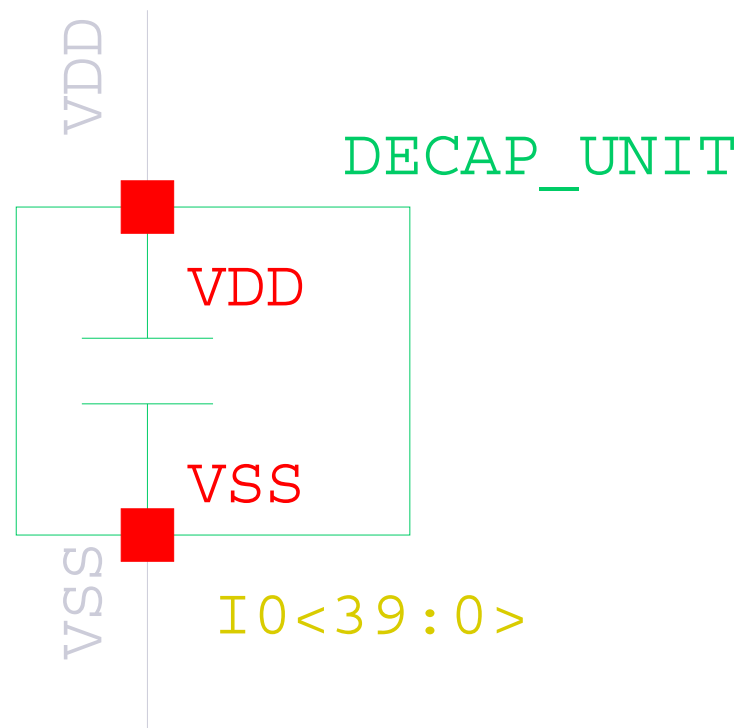
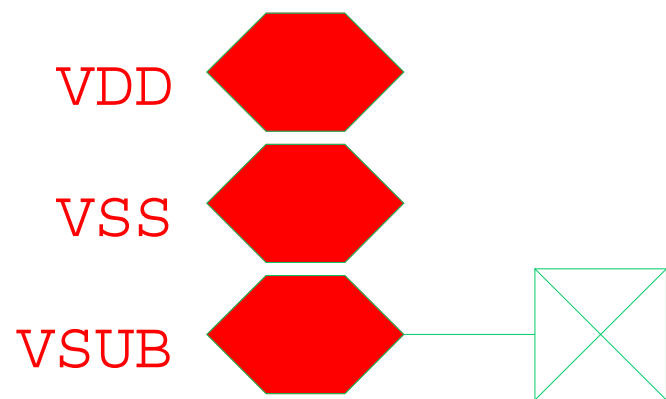


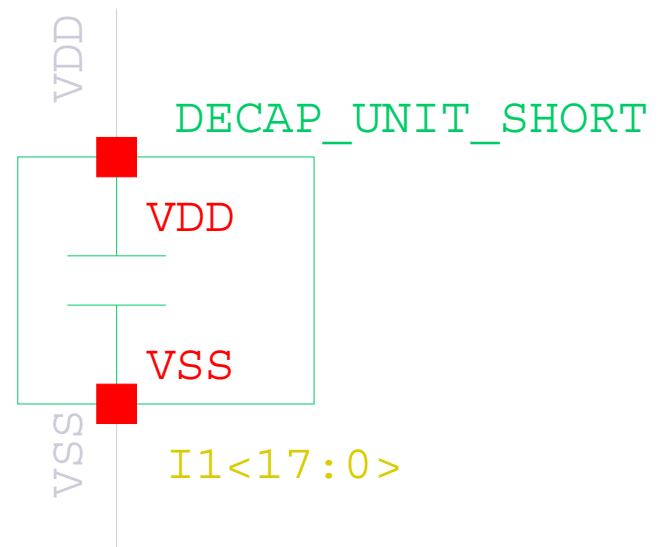
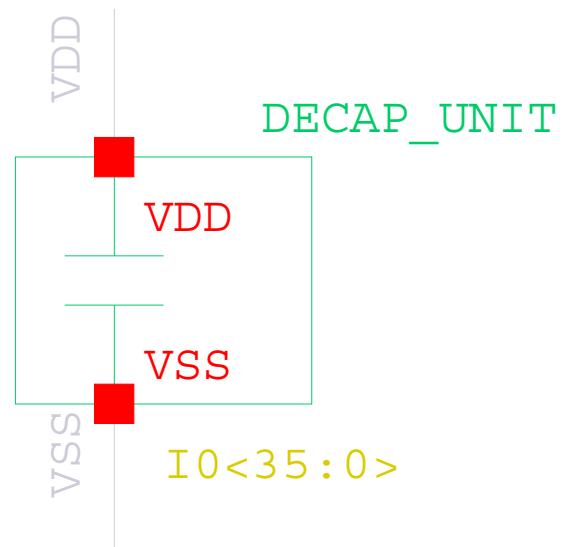
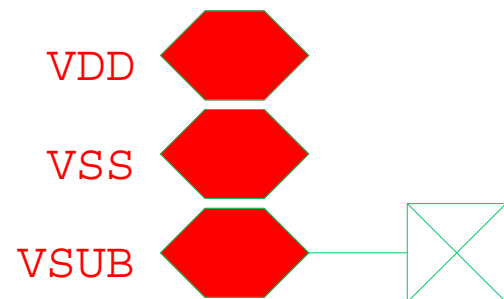




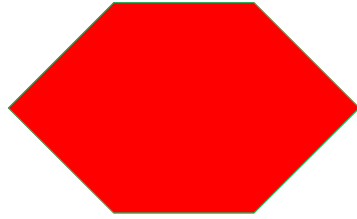




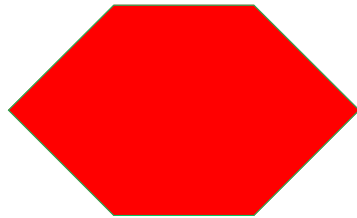




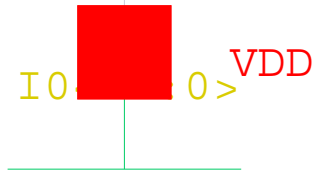
VDD



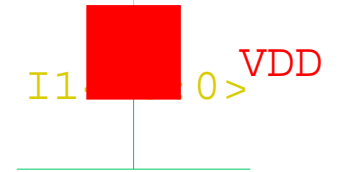
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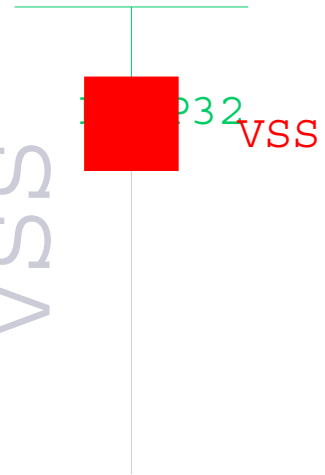
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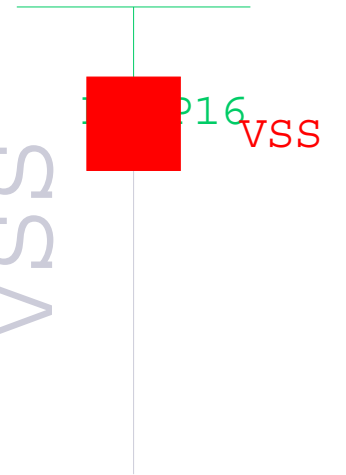
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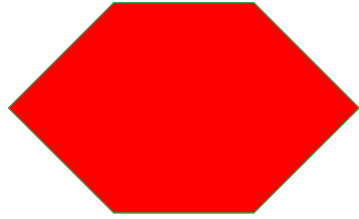
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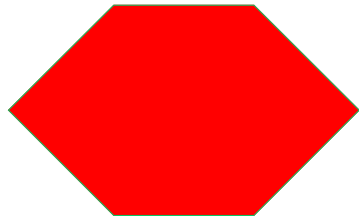
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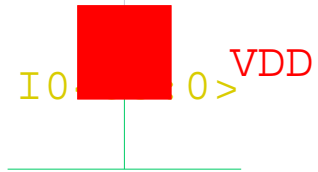
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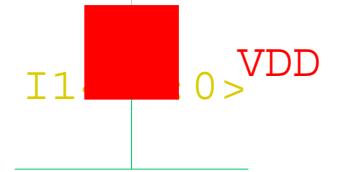
VSS



VDD



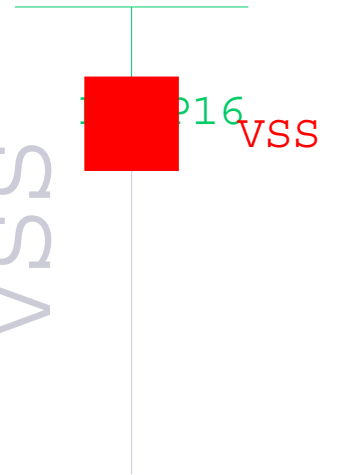
VDD

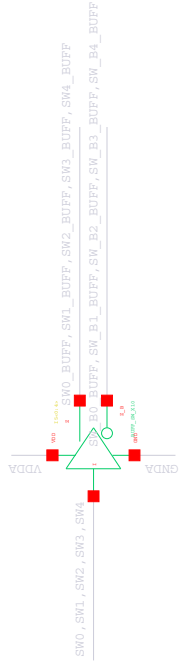


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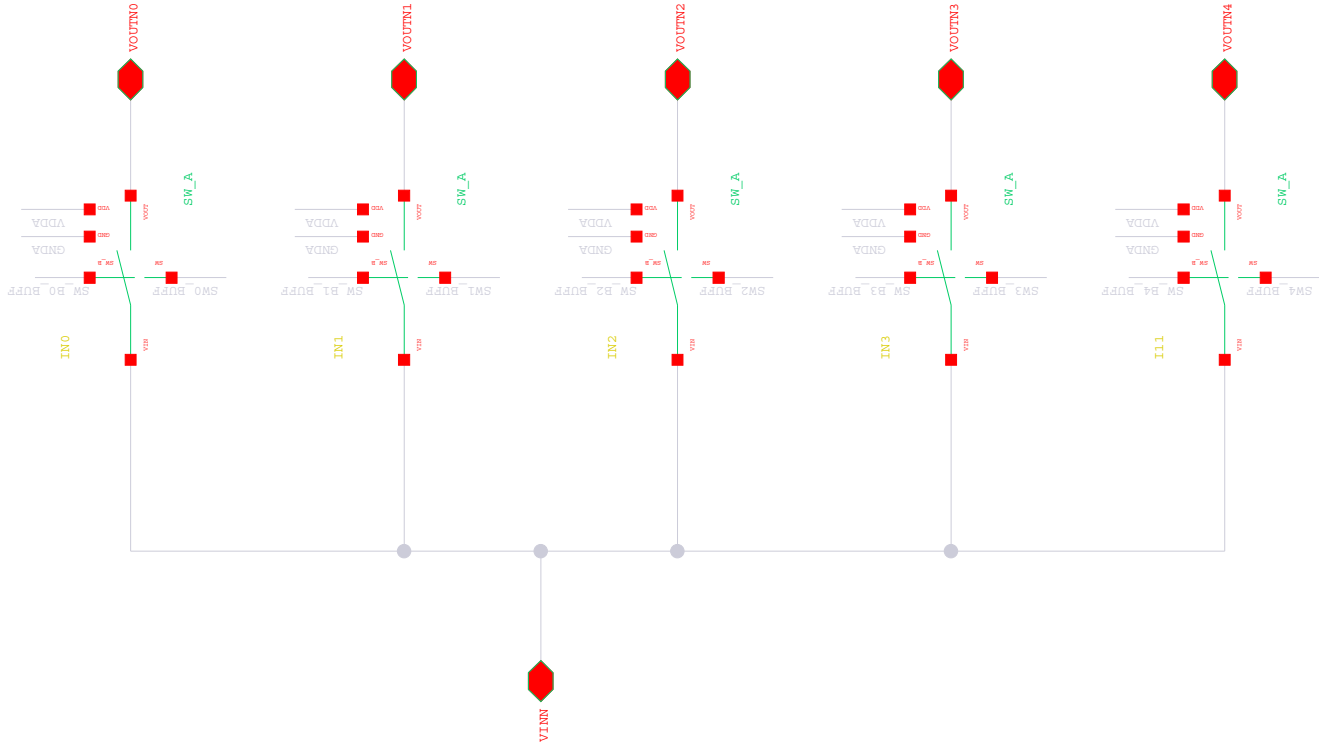
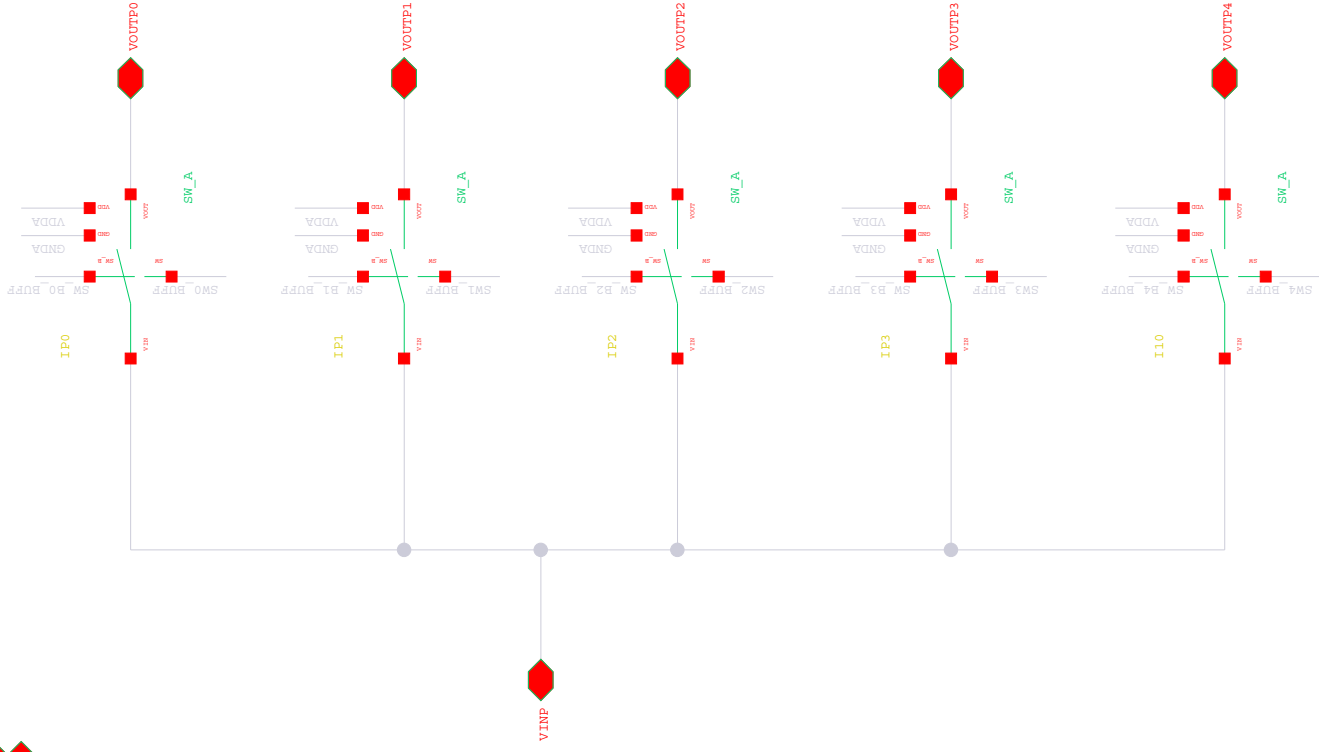
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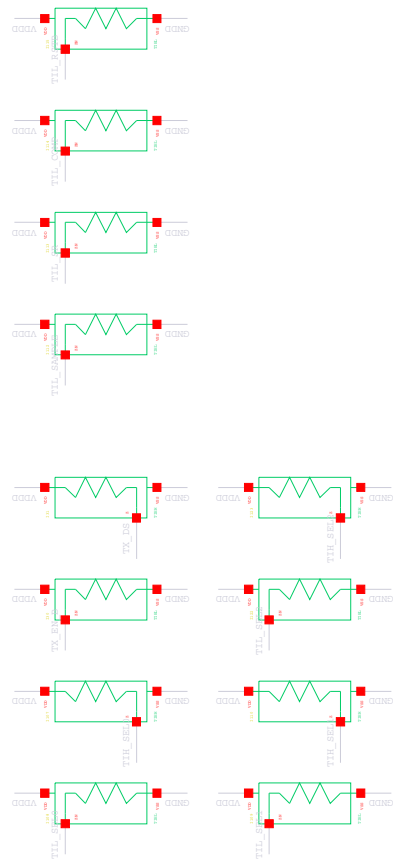
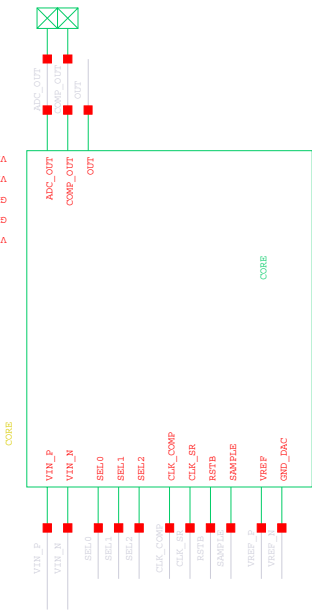
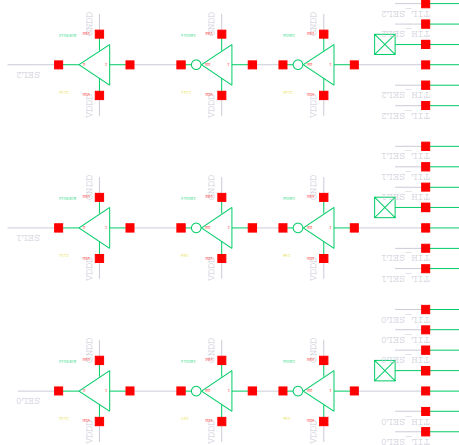
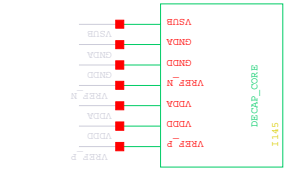
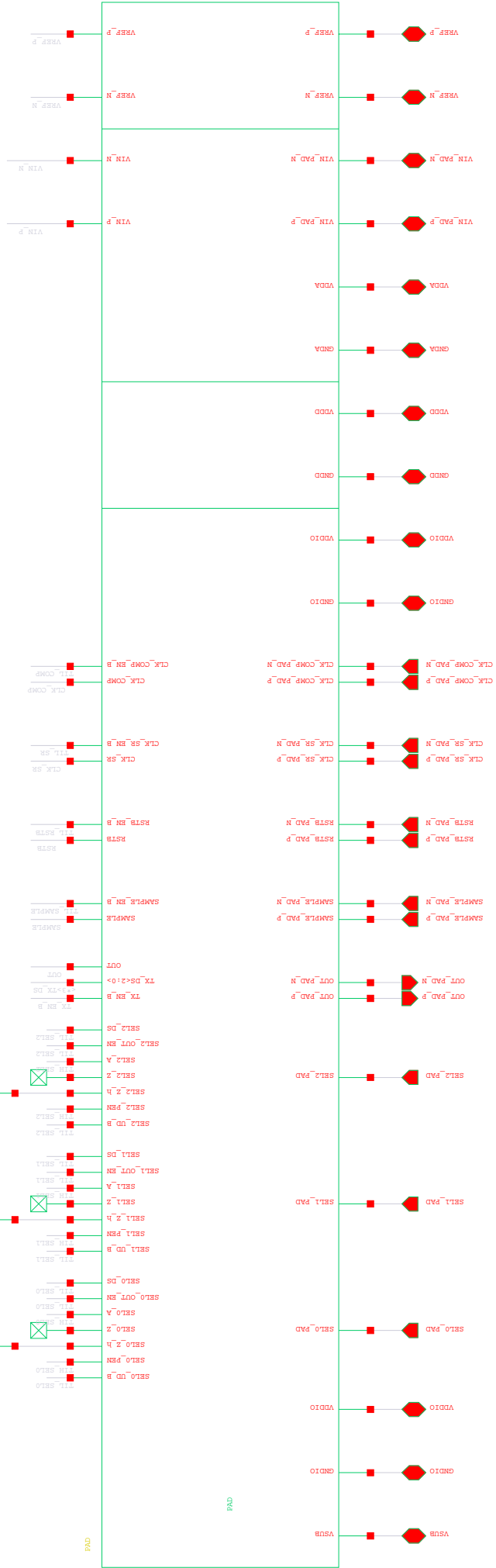


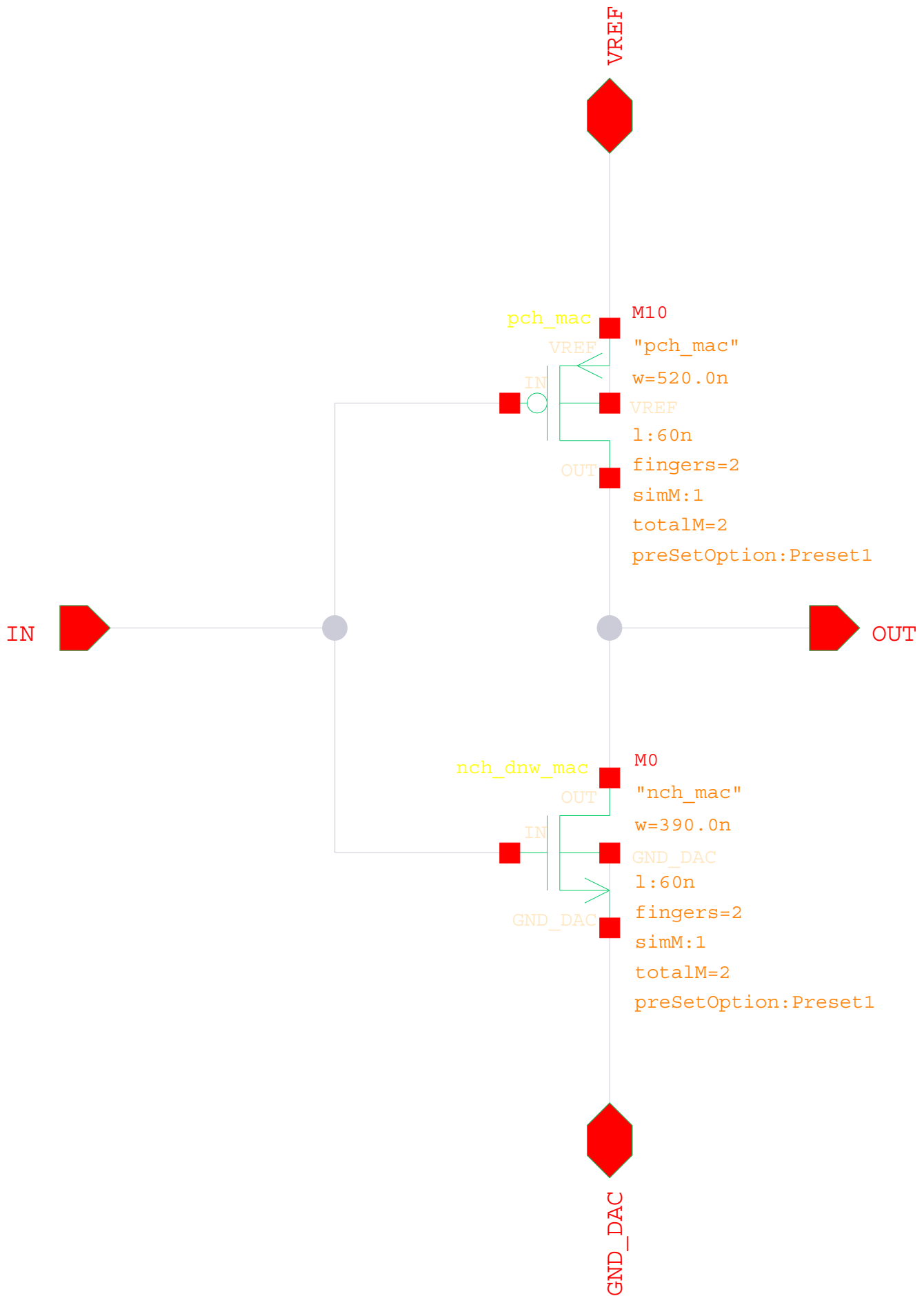


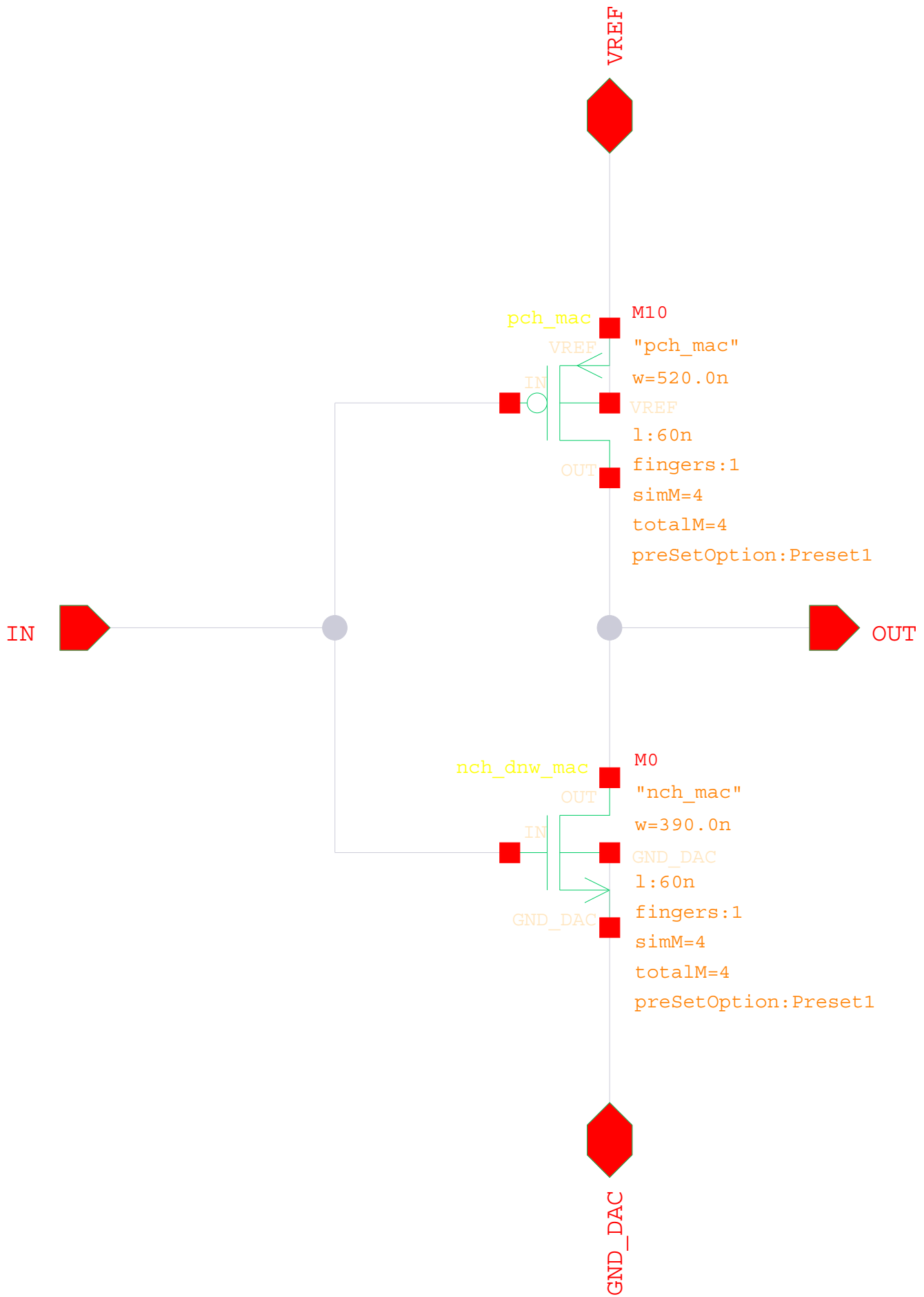
VDDA
GND

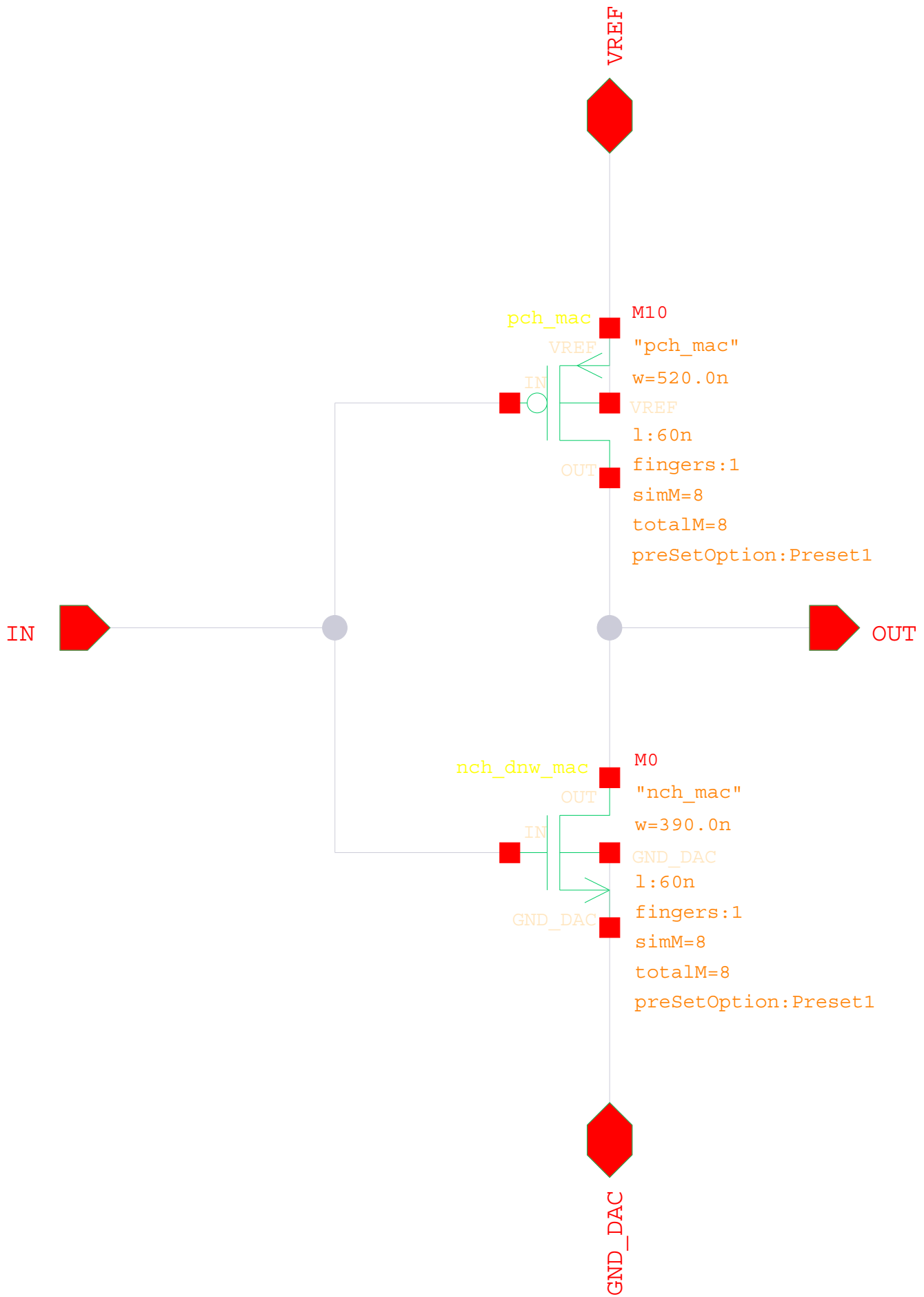
SW0
SW1
SW2
SW3
SW4

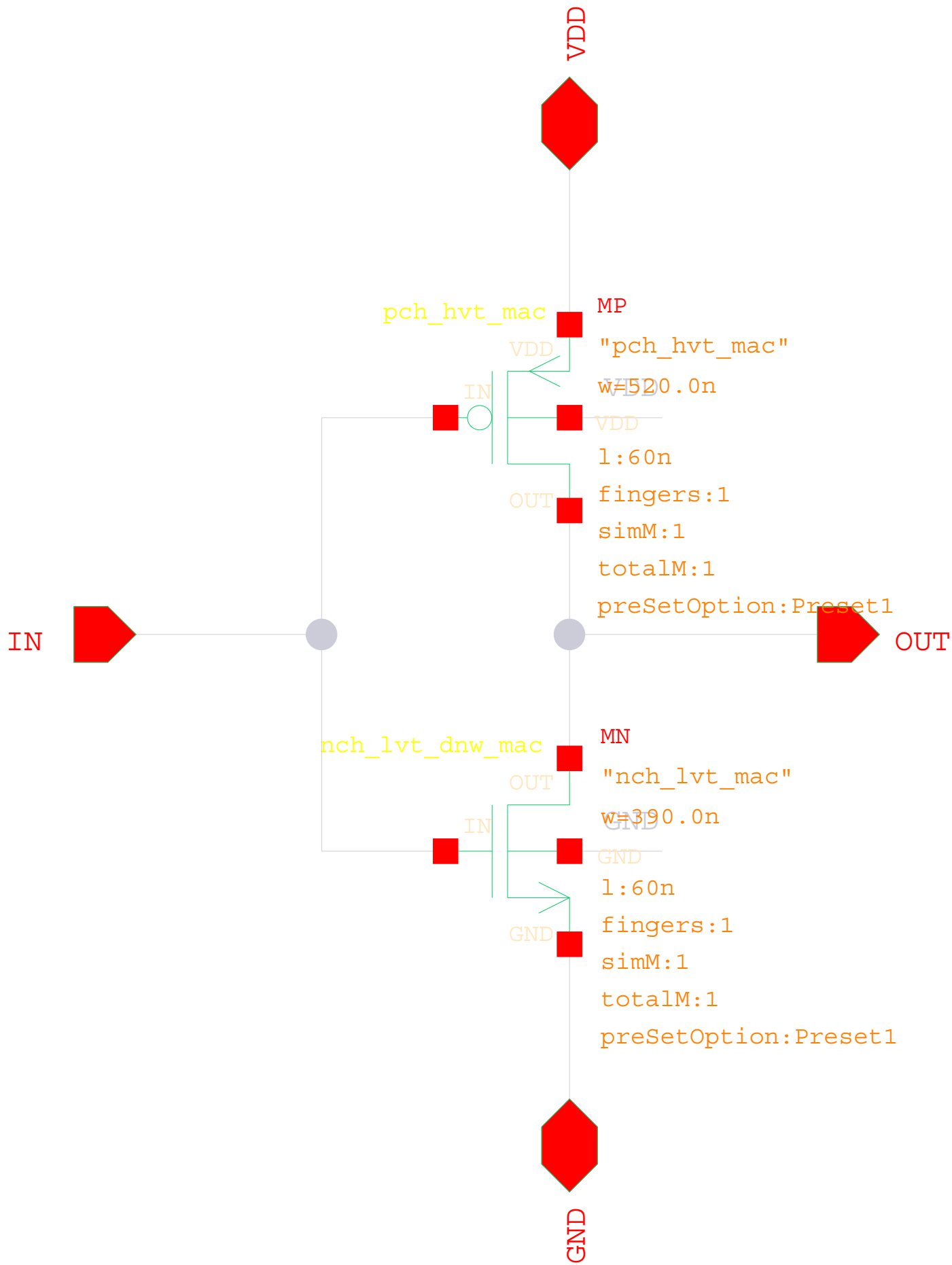


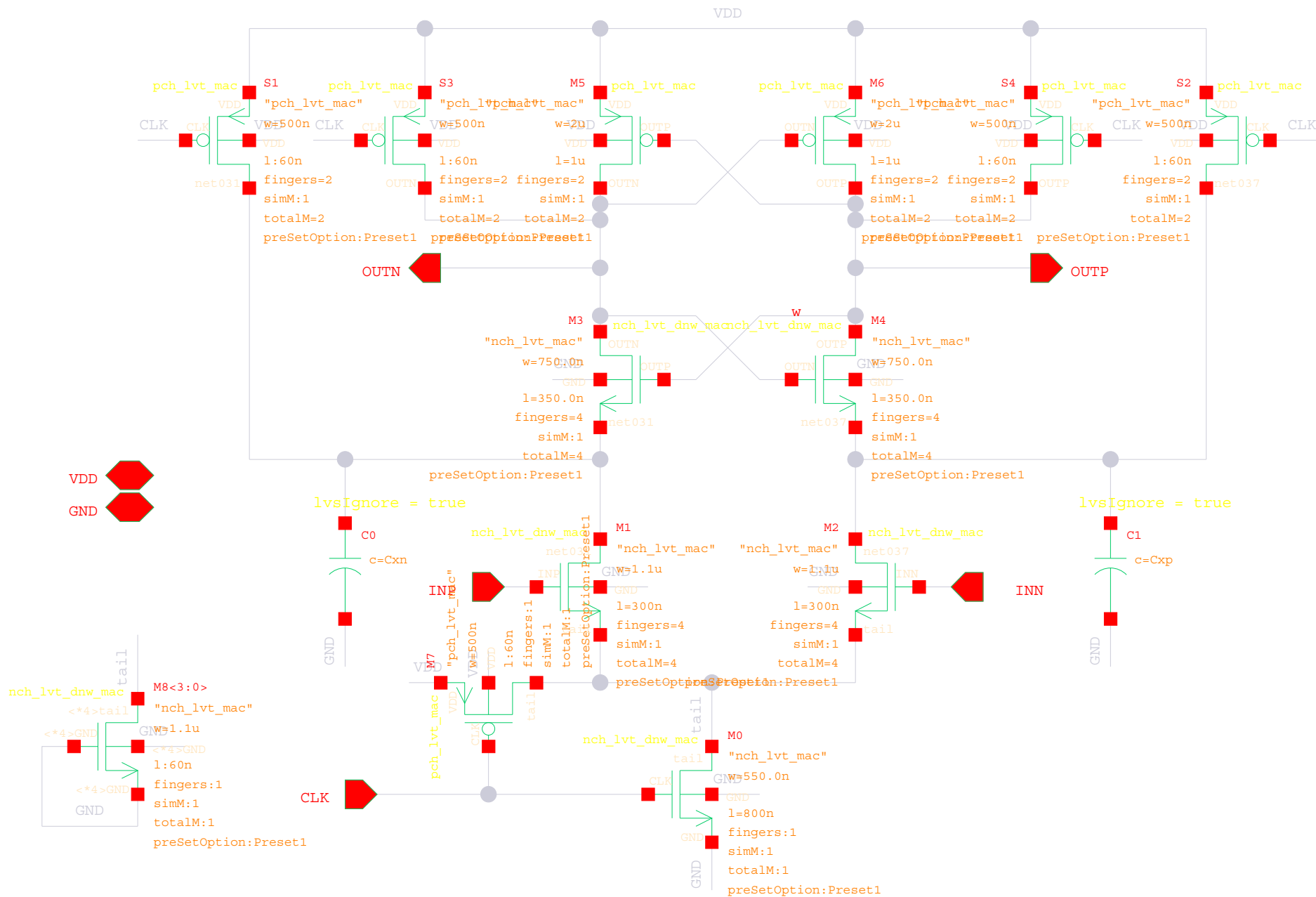


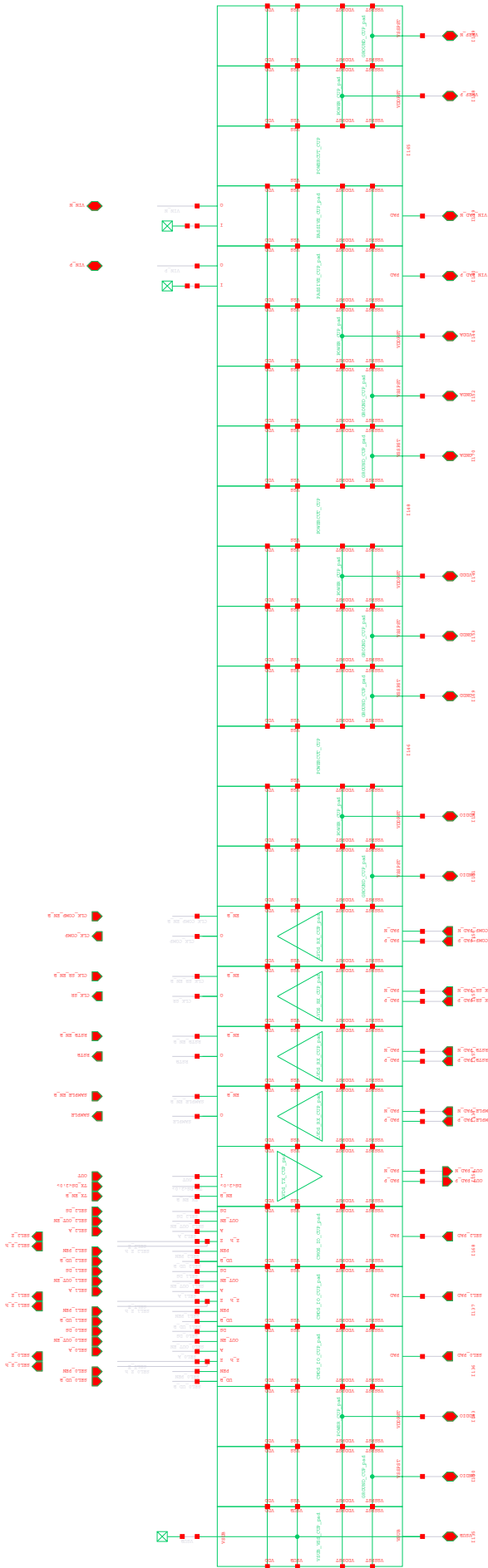












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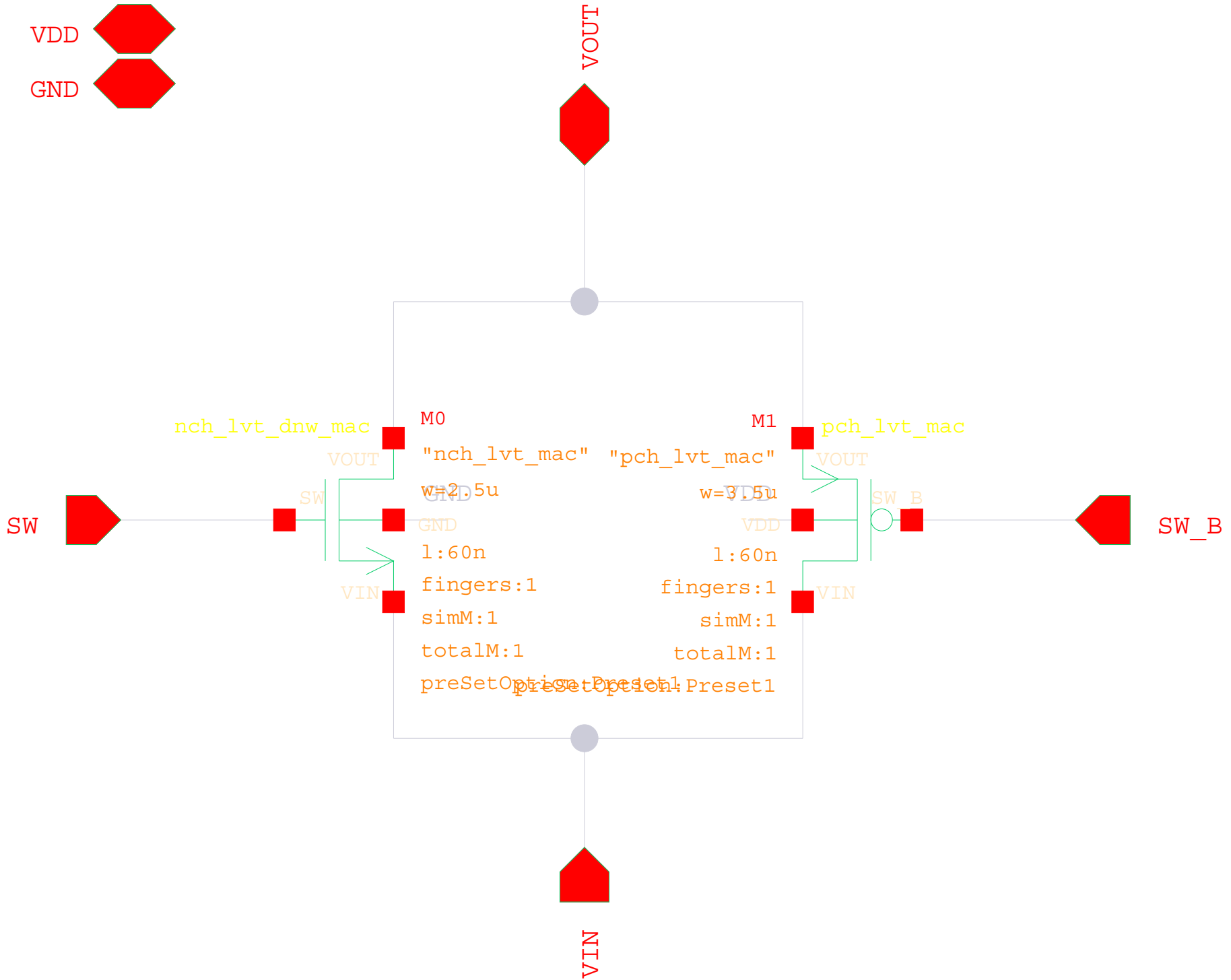
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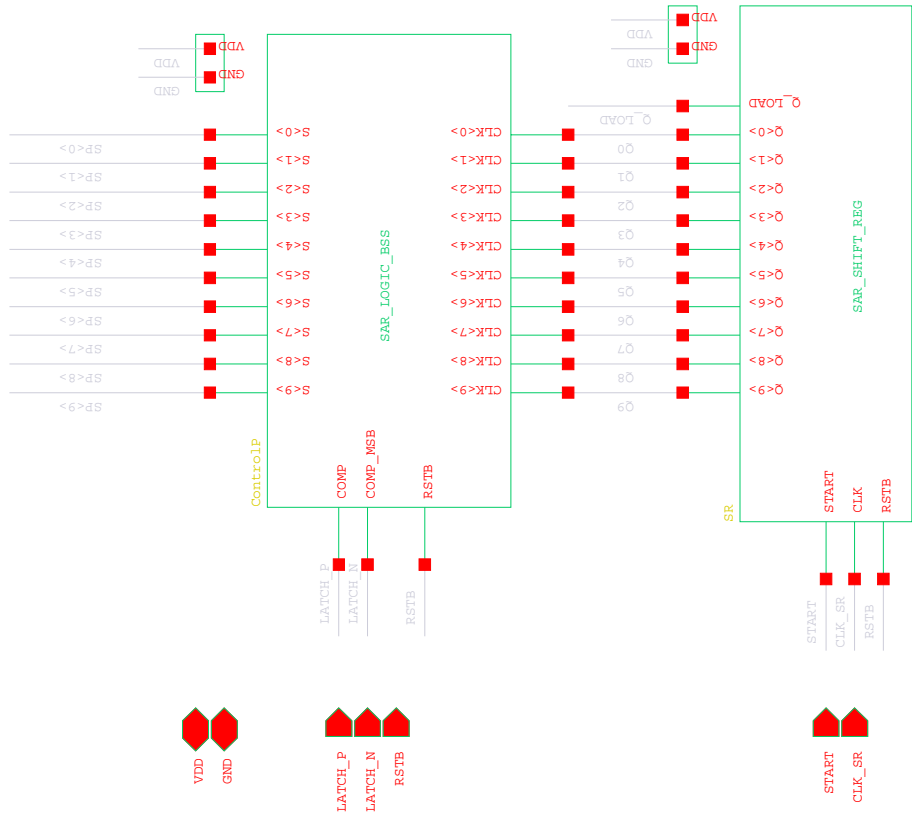
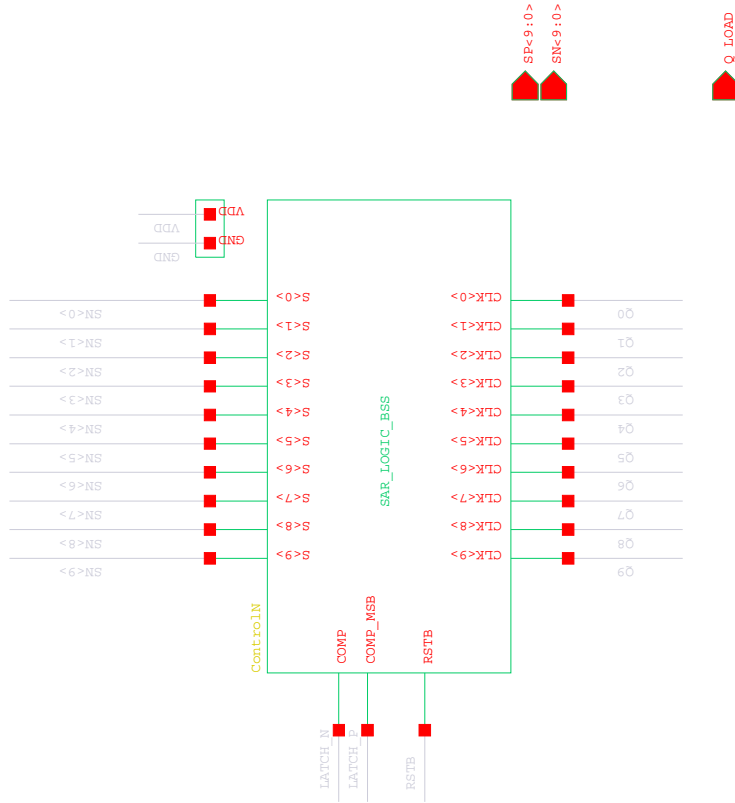
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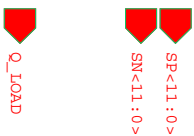
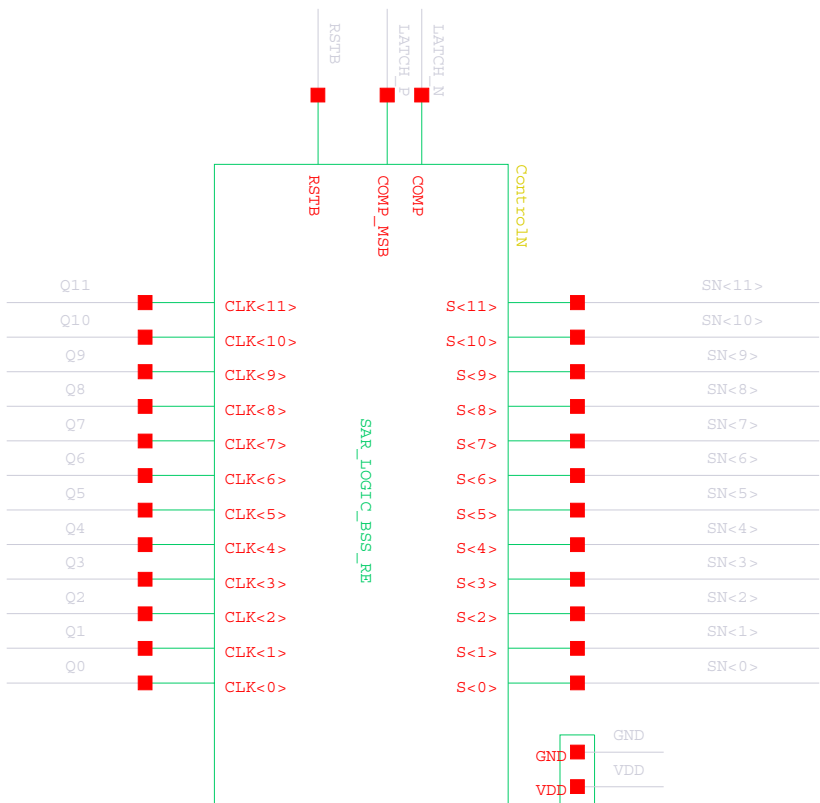
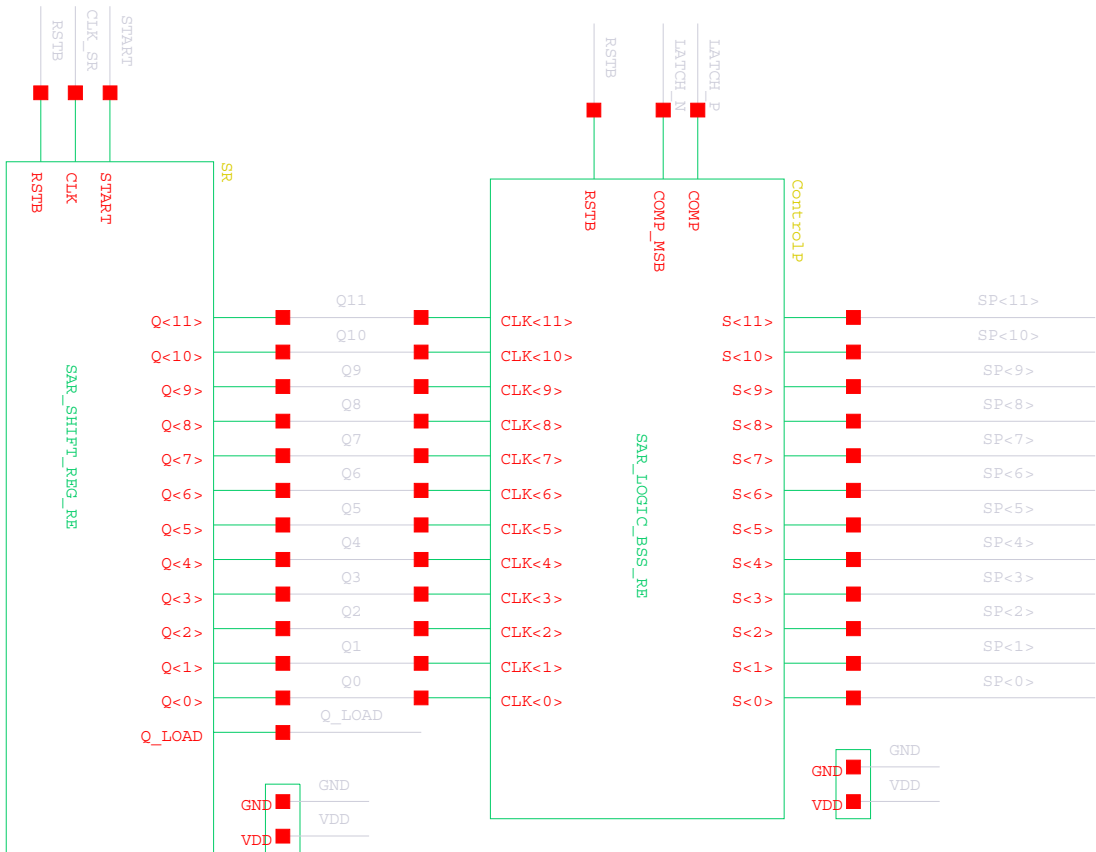
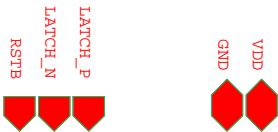
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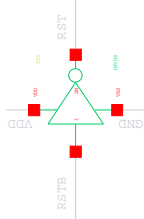
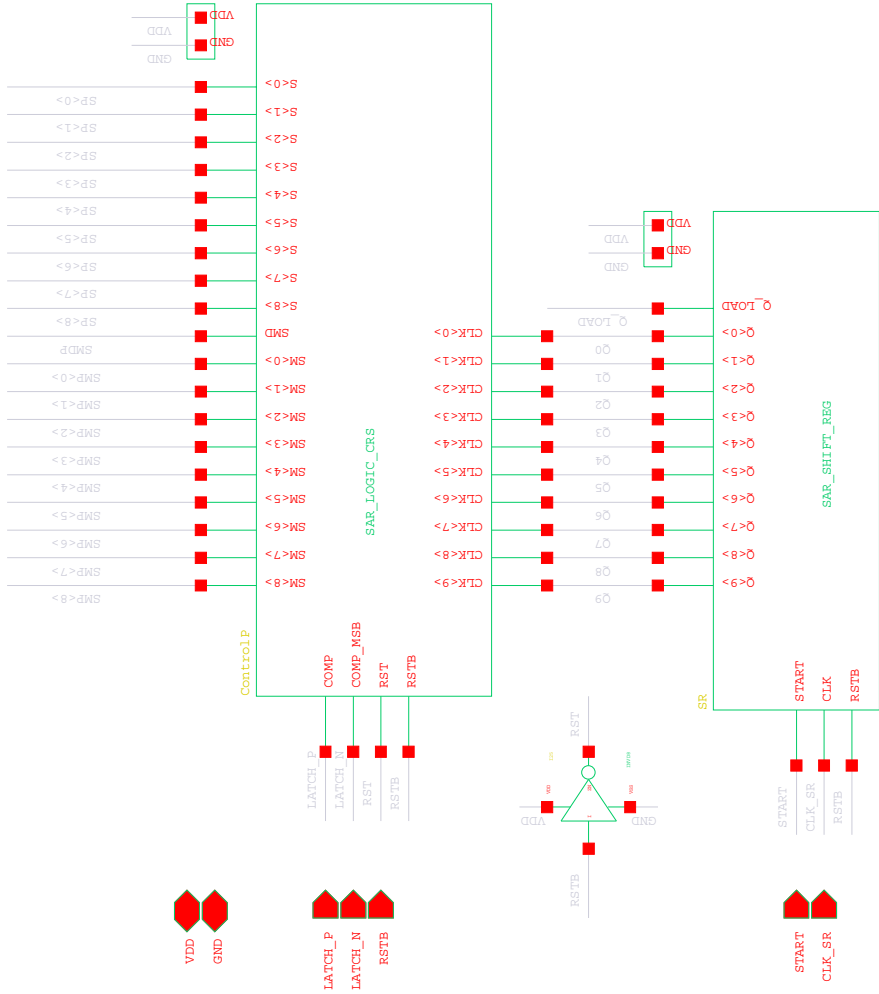
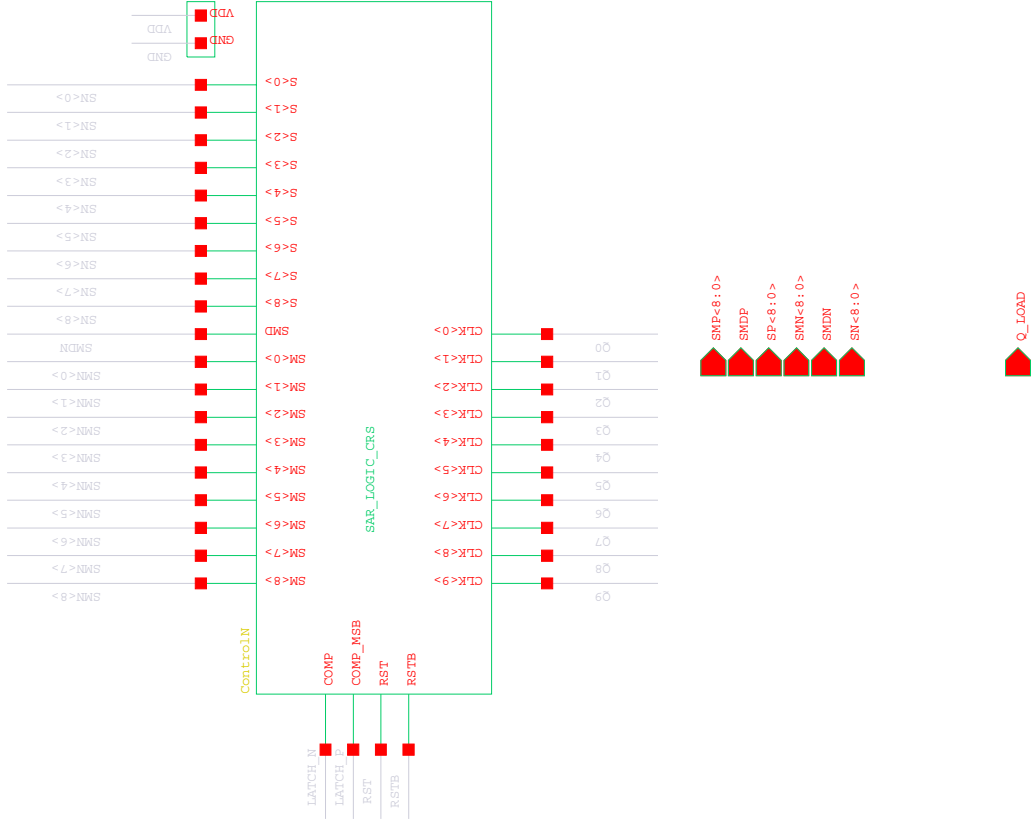
1.026

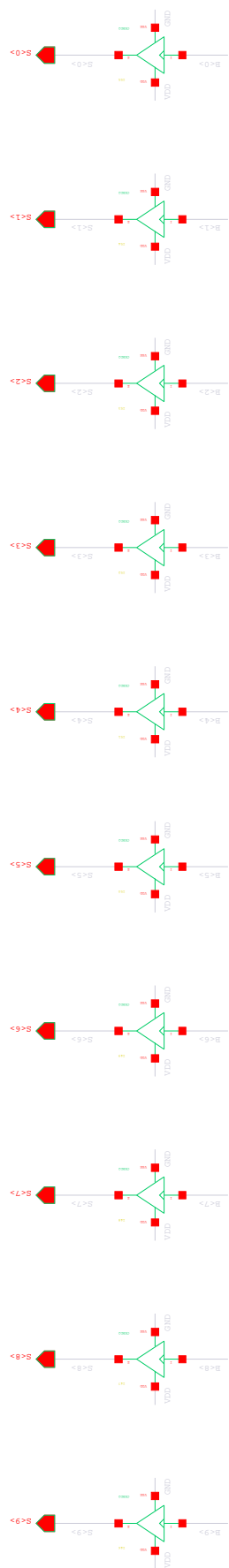
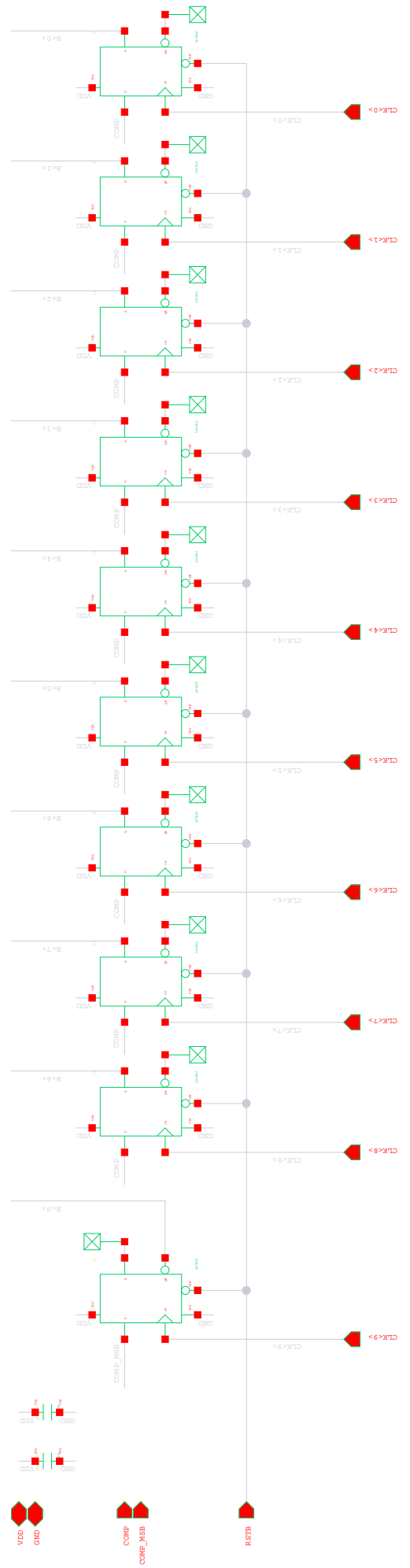
1.027

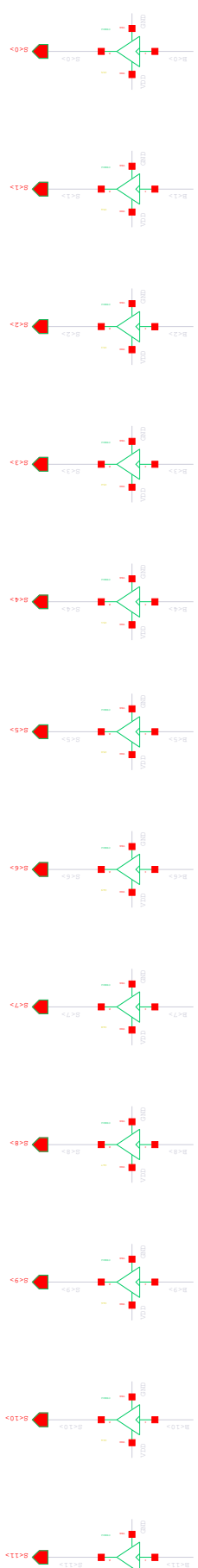
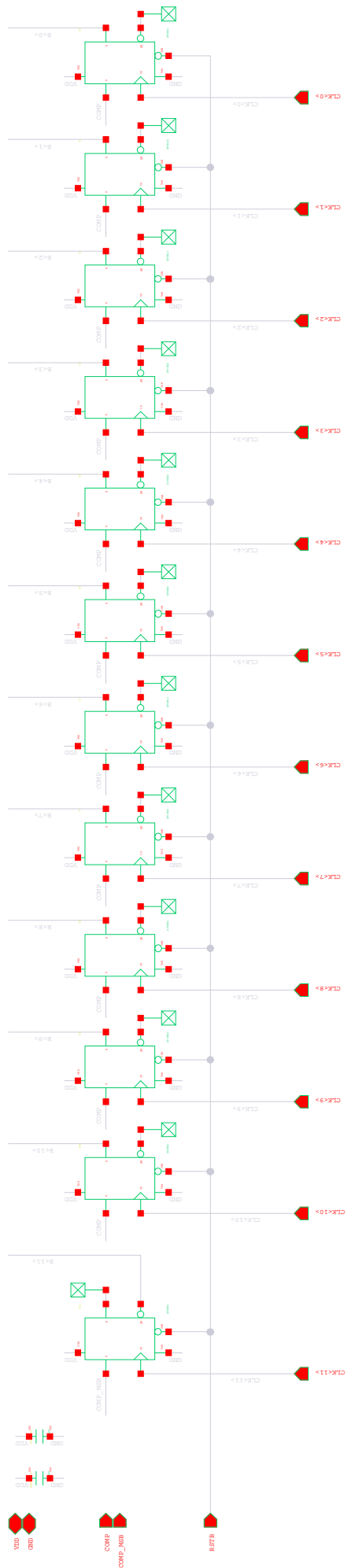












RESET PHASE:

$S_{<*>} = 0$, $SM_{<*>} = 1$

MSB COMPARISON:

If $B_{<9>} = 0$: $SM_{<*>} = 0$ (VREF)

If $B_{<9>} = 1$: $SM_{<*>} = 1$ (GND)

OTHER BITS:

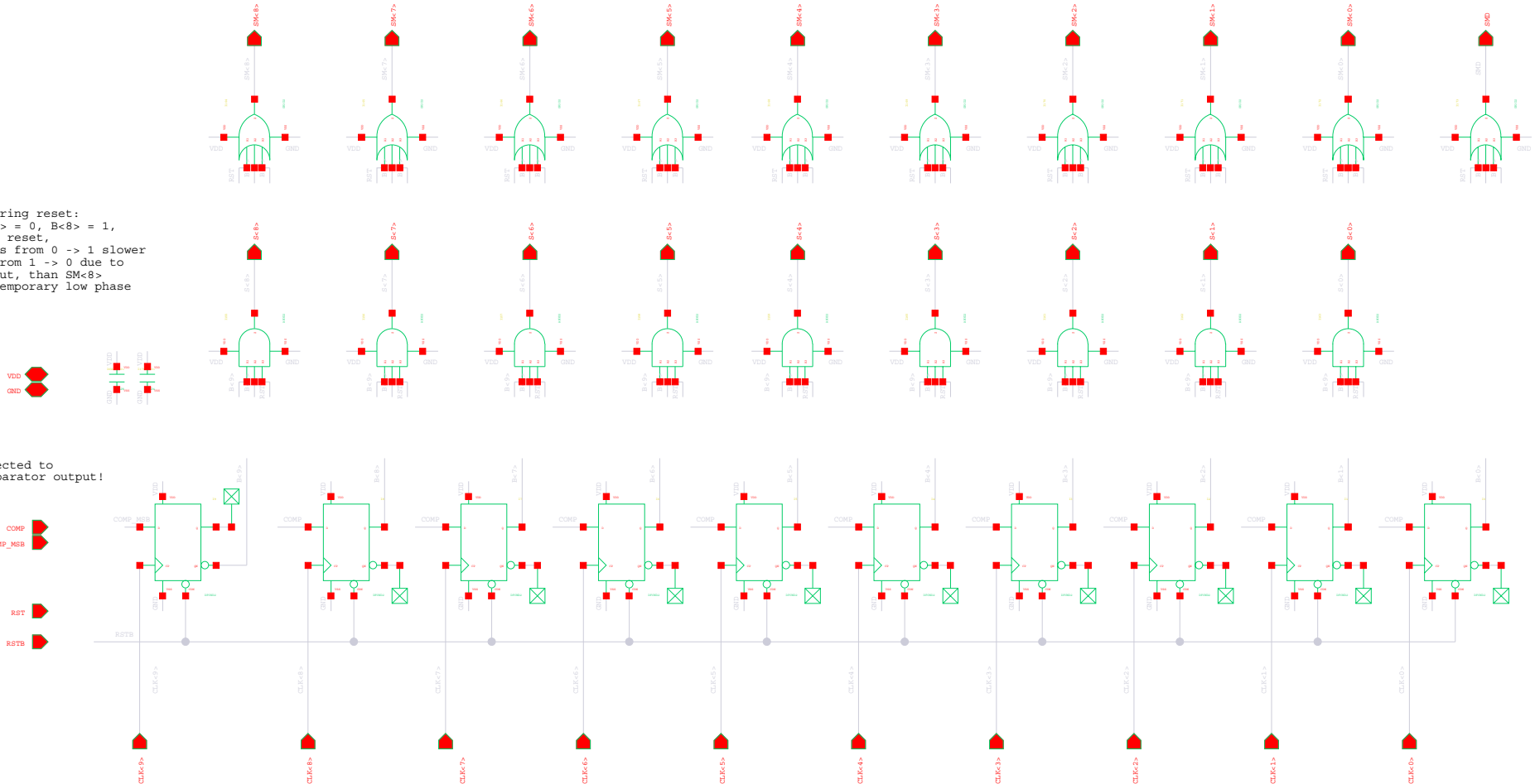
If $B_{<9>} = 0$ & $B_{<*>} = 0$: $S_{<*>} = 0$, $SM_{<*>} = 0$ (No switch on P side, switch N side $S_{<*>}$ to 1)

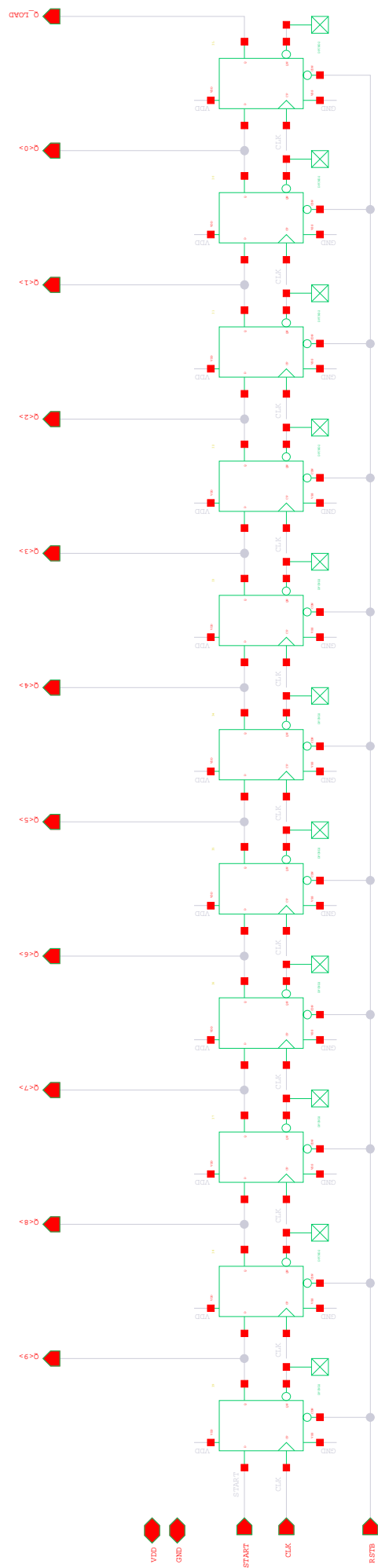
If $B_{<9>} = 0$ & $B_{<*>} = 1$: $S_{<*>} = 0$, $SM_{<*>} = 1$ (Reset P side $SM_{<*>}$)

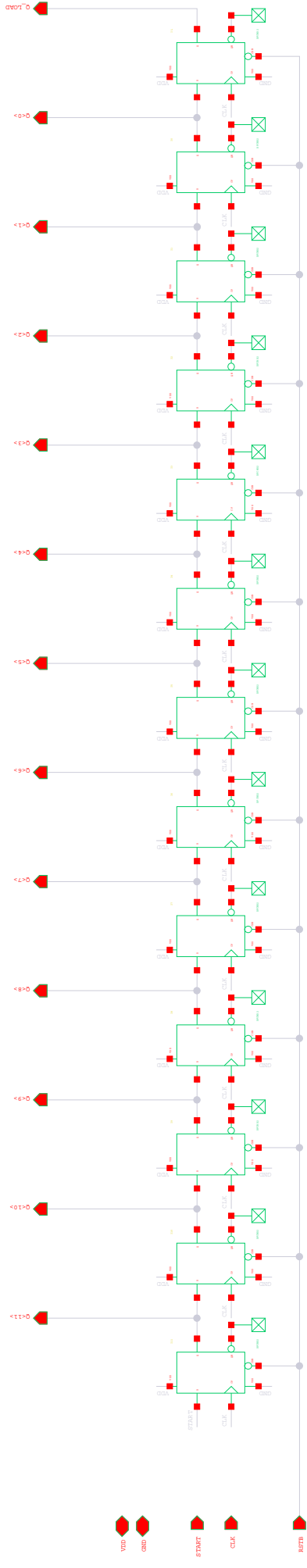
If $B_{<9>} = 1$ & $B_{<*>} = 0$: $S_{<*>} = 0$, $SM_{<*>} = 1$ (Reset N side $SM_{<*>}$)

If $B_{<9>} = 1$ & $B_{<*>} = 1$: $S_{<*>} = 1$, $SM_{<*>} = 1$ (No switch on N side, switch P side $S_{<*>}$ to 1)

Glitches during reset:
e.g. If $B_{<9>} = 0$, $B_{<8>} = 1$,
Then during reset,
 $B_{<9>}$ changes from 0 -> 1 slower
than $B_{<8>}$ from 1 -> 0 due to
higher fanout, than $SM_{<8>}$
will have temporary low phase







VDD
GND

COMP_P

COMP_N

