

# **Measurement report of the ADC-TEST-IC**

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**!! work in progress !!**

**This version is submitted only for reviewing !! the content may be subject to changes !!**

This report summaries the measurement-results and characterization of the ADC-TEST-IC (called : ADC\_CORDIA\_1). This IC consists of 4 variants of the SAR-ADC architecture (briefly described below). The design was successfully carried out by **Tianyang Wang** a former Postdoc-employee at the SILAB of the physical institute (university of Bonn). Please note, the document is not intended to describe the design of the ADCs; it focus, mainly, on the measurement results.

## 1. Cordia project

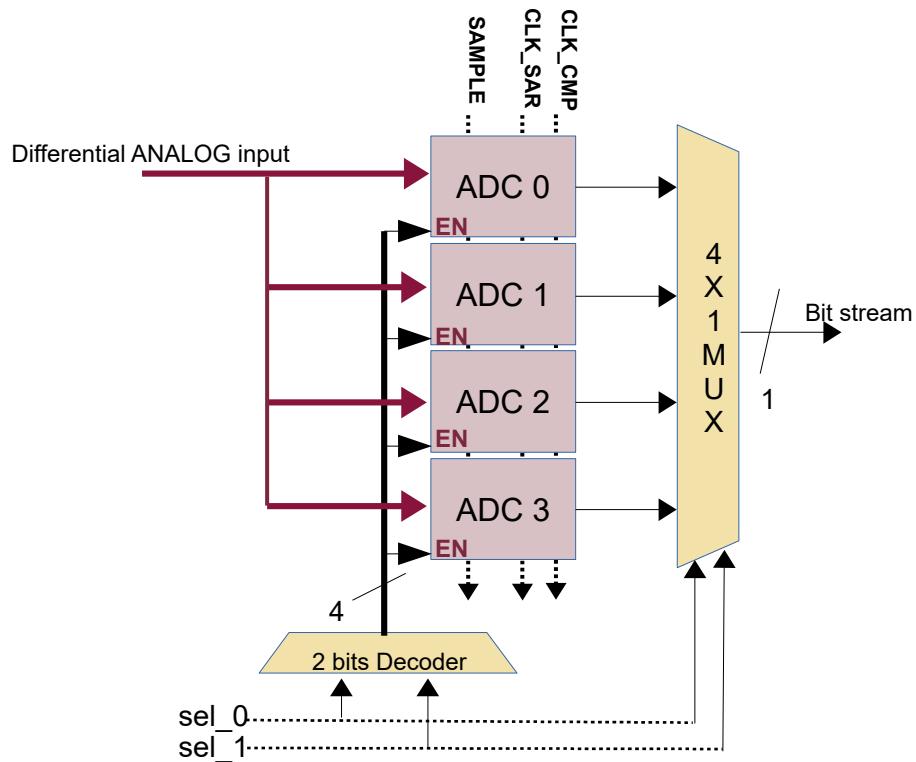
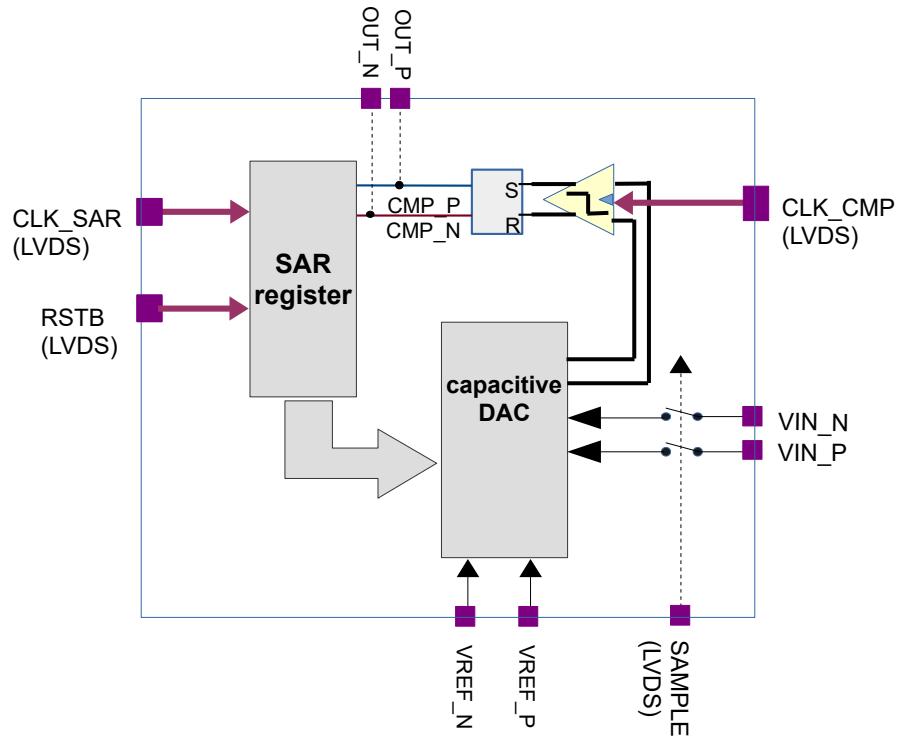
The ADC-TEST-IC was developed in cooperation with DESY (Deutsches Elektronen-Synchrotron) as part of a comment research project called : CORDIA : Continuous Readout Digitising Imager Array. For extended information please refer to [1].

## 2. ADC- Design

The Design aims an ADC with an effective resolution of 10 bits and a sampling rate of 2.5MS/sec. It is based-on the well-known SAR architecture (Successive Approximation Register) with 4 different variants, which are summarized in table 1. As depicted in figure 1, an integrated 2-bits decoder and 4X1 multiplexer allow the selection of the desired ADC. Note that all ADC's implementations are similar (Figure 2), they differs, however, in the scheme of the capacitive DAC (BSS vs. CRS) as well as the use of the redundancy technique (ADC0 and ADC1 vs. ADC2 and ADC3). For more theoretical background please refers to [2-4].

ADC	SEL	Symbol	Description	Bit stream size
ADC0	00	BSS	Bidirectional Single-Sided switching	11
ADC1	01	CRS	Correlated reverse switching	11
ADC2	10	BSS_RE	BSS with <u>redundancy</u>	13
ADC3	11	BSS_AW_RE	BSS attenuated weighting and with <u>redundancy</u>	13

**Table 1:** designed SAR-ADC variants

**Fig. 1:** abstracted diagram of ADC-TEST-IC**Fig. 2:** simplified diagram of SAR-ADC

### 3. Key requirements of the ADC

- Bitstream size : 11 to 13 bits (13 bits when redundancy is used)
- Digital output resolution : 11 Bits
- Aimed effective resolution : 10 Bits
- Maximum Sampling Frequency 2.5MS/sec
- Typical DNL less than 1 LSB (evaluated based on 11 Bits / aimed 10 Bits resolutions)
- Typical DNL less than 1 LSB (evaluated based on 11 Bits / aimed 10 Bits resolutions)
- Noise (1 Sigma)  $\sim 0.6$  LSB (evaluated based on 11 Bits)<sup>1</sup>
- ENOB 9.5 Bits (Typical operation condition) / **not completely tested yet !!**
- Operating ambient temperature : -20 to 85 °C (validated with a measurement-test)
- Typical power consumption (per ADC/rough estimation):  $25\mu\text{A} \times 1.2\text{V} = 30\mu\text{W}$
- For the electrical parameters see table 2

Param.	Description	MIN	TYP	MAX	unit	condition
VIN_P	Positive input voltage	0		1.3	V	VDDD=VDDA=1.2V
VIN_N	Negative input voltage	0		1.3	V	VDDD=VDDA=1.2V
VCM	Common mode voltage	500	600	700	mV	
VDIFF	Differential input voltage (VIN_P-VIN_N) <sup>2</sup>	-0.80		0.80	% VREF	
VDDA	Analog supply (+/- 10%)	1.08	1.2	1.32	V	
VDDD	Digital supply (+/- 10%)	1.08	1.2	1.32	V	
VDDIO	Input/output supply (+/- 10%)	1.08	1.2	1.32	V	
VREF_P	Positive analog reference	n. a.	1.2	1.3	V	VDDD=VDDA=1.2V
VREF_N	Negative analog reference	-100	0	n. a.	mV	VDDD=VDDA=1.2V
VREF	ADC reference (VREF_P-VREF_N)	1.08	1.2	1.32	V	VDDD=VDDA=1.2V

**Table 2:** electrical parameters

1 the theoretical limits of the quantization noise of 10 Bits  $Q_n(1\sigma) = \frac{LSB_{10\text{bits}}}{\sqrt{(12)}} = 2 \times \frac{LSB_{11\text{bits}}}{\sqrt{(12)}}$

2 functional up to 0.84% (validated with test) / 0.8% with reserve (owing to the expected process corners and mismatch)

#### 4. description and configuration of the PINOUT (ADC-TEST-IC )

Figure 3 depicts the configuration of the chip PINOUT. The chip has, in total, 28 PADs with 7 each side. The digital IO-PADs are supplied with VDD<sub>\_IO</sub> /GND<sub>\_IO</sub>, while the chip core contains 2 power domains: Digital and Analog supplied via VDDD/GNDD and VDDA/GNDA respectively. The LVDS (Low-Voltage Differential Signaling) configuration is used for the main digital control signals (SAMPLE, RESB, CLK\_SAR and CLK\_CMP) as well as the bit-stream output. However, since the ADCs selection bits (SEL0, SEL1, and SEL2) are static-signals, they are connected to a simple CMOS input-PAD. The ADC differential analog input is connected to the PADs : VIN<sub>\_P</sub> and VIN<sub>\_N</sub> while the PADs: VREF<sub>\_P</sub> and VREF<sub>\_N</sub> connects the differential input reference.

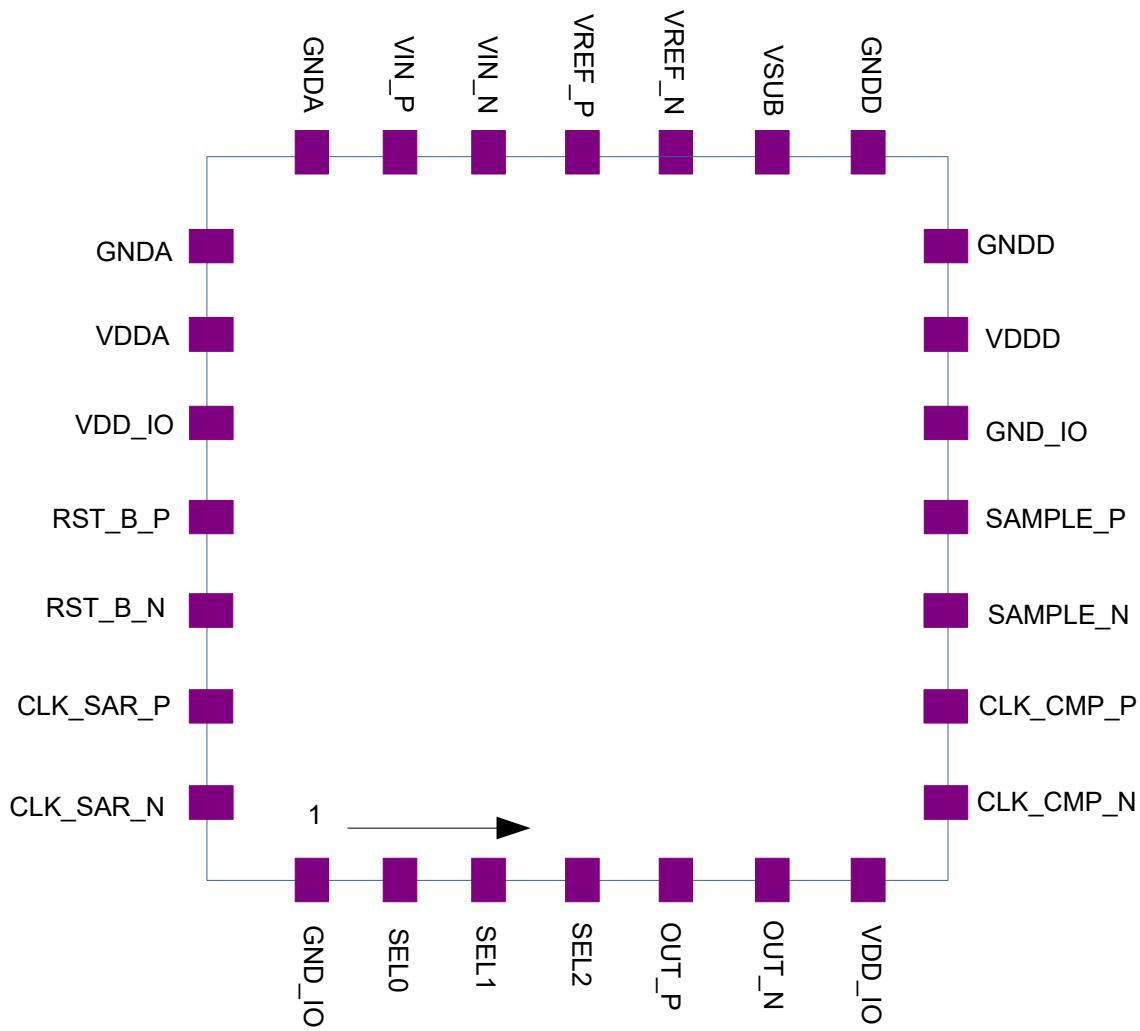


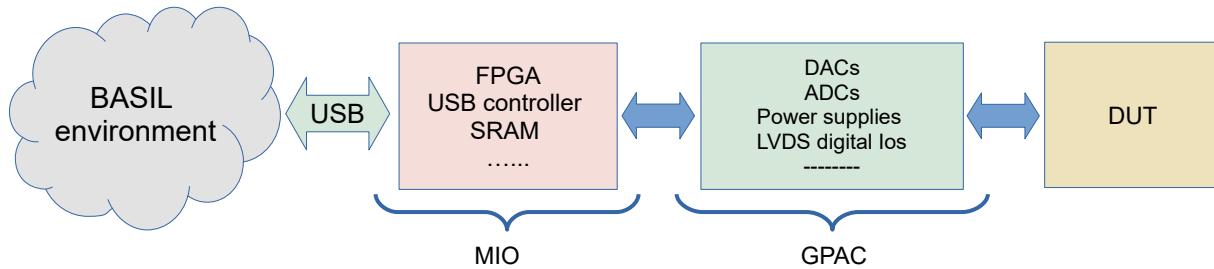
Fig. 3: PINOUT

N	PIN	Description	note
1	GND_IO	Ground of PAD-RING domain	Input/Output PADs
2	SEL0	Select (LSB)	CMOS input
3	SEL1	Select	CMOS input
4	SEL2	Select (MSB)	CMOS input
5	OUT_P	Output bitstream	LVDS output
6	OUT_N	Output bitstream	LVDS output
7	VDD_IO	Supply of PAD-RING domain	Input/Output PADs
8	CLK_CMP_N	comparator clock	LVDS input
9	CLK_CMP_P	comparator clock	LVDS input
10	SAMPLE_N	Sample signal	LVDS input
11	SAMPLE_P	Sample signal	LVDS input
12	GND_IO	Ground of PAD-RING domain	
13	VDDD	Digital supply	
14	GNDD	Digital ground	
15	GNDD	Digital ground	
16	VSUB	Subtract connection (ground)	
17	VREF_N	Positive reference voltage	
18	VREF_P	Negative reference voltage	
19	VIN_N	Positive input voltage	
20	VIN_P	Negative input voltage	
21	GNDA	Analog ground	
22	GNDA	Analog ground	
23	VDDA	Analog supply	
24	VDD_IO	Supply of PAD-RING domain	
25	RST_B_P	Reset signal	LVDS input
26	RST_B_N	Reset signal	LVDS input
27	CLK_SAR_N	SAR clock (shift register)	LVDS input
28	CLK_SAR_N	SAR clock (shift register)	LVDS input

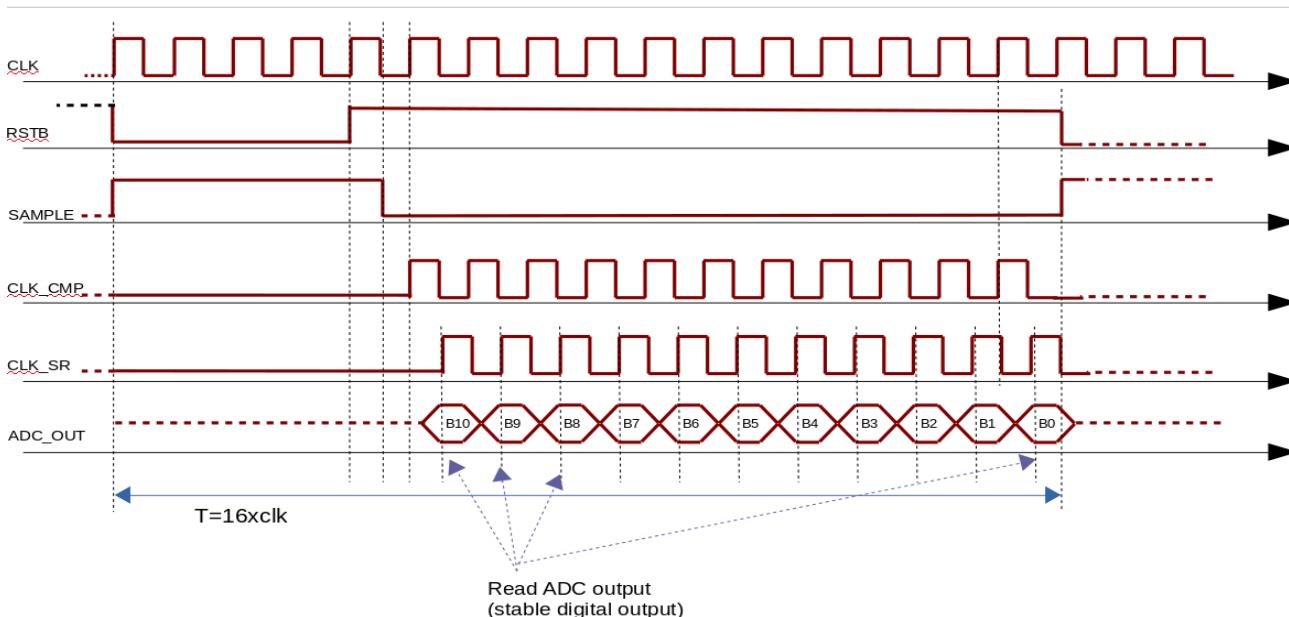
**Table 3:** PINs description

## 5. Measurement setup (soft- and hardware)

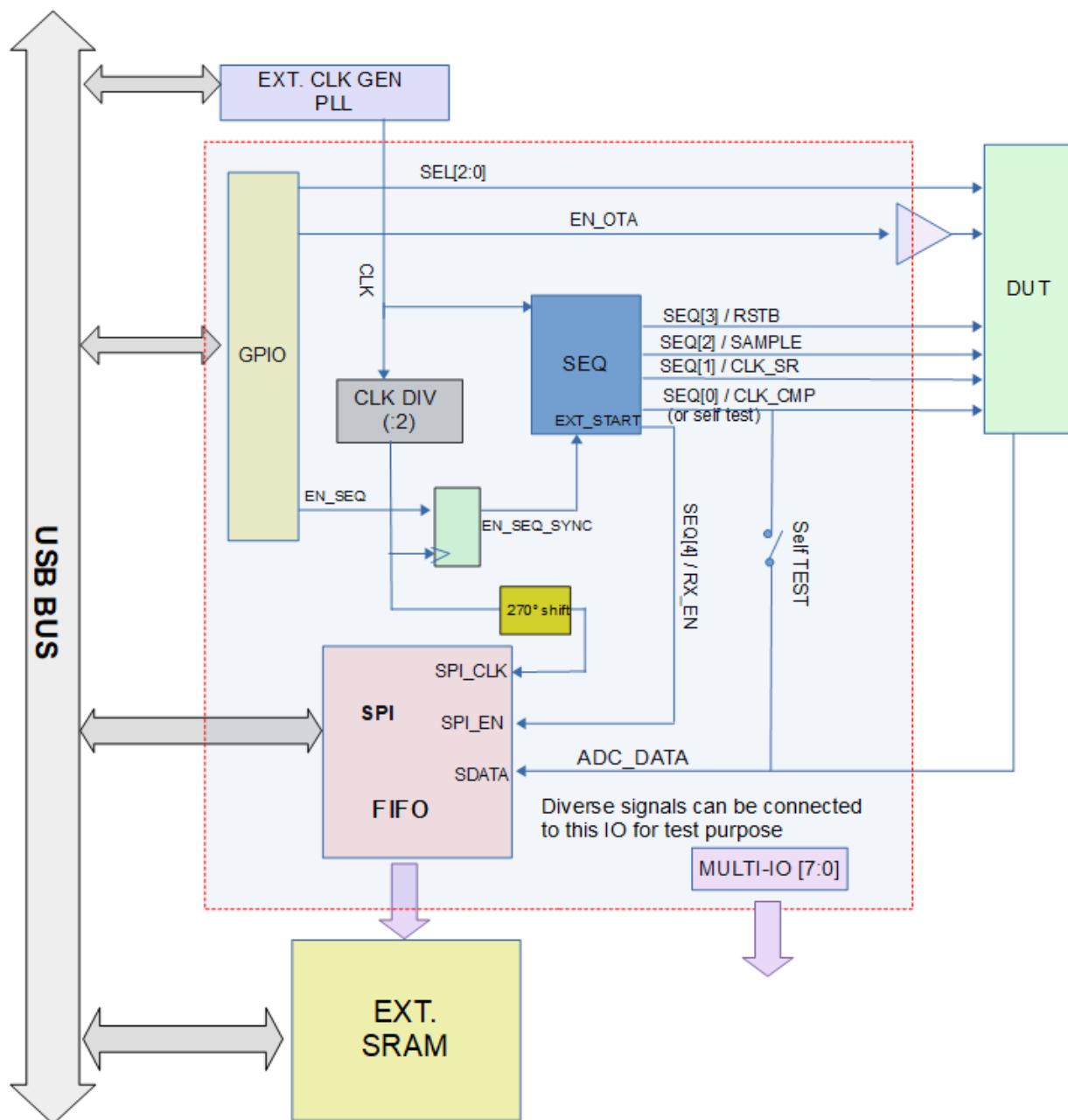
as depicted in figure 4 the test setup consists of an FPGA- and GPAC-board (general purpose analog card) and the DUT-PCB. The system is controlled based on BASIL-system : a data acquisition framework in Python and Verilog (for more information : <https://github.com/SiLab-Bonn/basil>). The FPGA configuration (firmware) generates the ADC control signals (Figure 5 and figure 7) and allows, simultaneously, the data acquisition (ADC's bitstream). This is further illustrated in figure 6. The signals timing is stored in a configurable sequencer (SEQ) allowing the control and the synchronization of A/D conversion cycles. So, the sampling rate and the number of iteration (conversion) can be set to a given values. A measurement frame starts always with the trigger signal: EN\_SEQ. The acquired data (16 bits per conversion) through the SPI (Serial Peripheral Interface) are transferred to an external RAM and read out via USB interface.



**Fig. 4:** diagram of the measurement setup



**Fig. 5:** typical timing diagram (without redundancy)



**Fig. 6:** diagram of the FPGA configuration

## 6. Weights vector (with redundancy)

when redundancy is used (ADC02 and ADC03)<sup>3</sup>, specific weights must be used instead of the usual one :  $W_i = 2^i$  with  $i=0$  to 10 (11 bits). This is owing to the non-binary steps used in the capacitive DAC with redundancy configuration. Table 4 reports the weights vector relative to ADC02 and ADC03. Note that the bit-stream size is 16 bits; 3 out of that are not used (0,1 and 2). The decimal value of the ADC output is computed based on eq. (1).

bit stream (DATA)	BSS_RE   CH=2															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Not valid DATA ADC BIT			12	11	10	9	8	7	6	5	4	3	2	1	0
				MSB	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	LSB
	B12															B0
Wi used in python program	0	0	0	1024	448	256	128	64	32	16	8	4	4	2	1	0
	0	0	0	448	256	128	64	32	16	8	4	4	2	1		
BSS_AW RE   CH=3																
Wi used in python program	0	0	0	1024	444	240	156	84	48	24	12	6	4	2	2	1
	0	0	0	444	240	156	84	48	24	12	6	4	2	2	1	0

Table 4: redundancy weights vector

$$ADC_{OUT} = 1024 + \left( \sum_{i=3}^{14} W_i \times Bw_i \right) + 0.5 (Bw_{15} - 1) \quad (1)$$

with

$$Bw_i = -1 \text{ when } BIT_i = 0 \text{ and}$$

$$Bw_i = 1 \text{ when } BIT_i = 1$$

## 7. measurement and characterization

At this stage, the measurement and characterization are performed using only 4 DUTs (bonded die on PCB). Hence, the results reflect only typical performances and no statistical data are available, at this point. All measurement are performed under typical operation conditions (see section 3); unless otherwise indicated. In addition, the ADC performances are tested against the variations of supplies and temperature (see table 2). This section is organized in two main parts : DC and AC (or dynamic) characterization. In both tests we use the well known standard methods for testing and computing the key parameters, e. g. INL, DNL and ENOB.

Figure 7 shows an oscilloscope-capture of the timing of the control signals (for reference see also figure 6). This configuration is standard for our application and used for all measurements. Further details including timing, FPGA configuration (firmware), entire measurement database can be found under SVN<sup>4</sup>.

<sup>3</sup> for this TEST-ASIC the redundancy is designed for calibration purpose. In general, it is used also to reduce the output uncertainty when wrong decisions occurs during the SAR iterations (e. g. due to comparator settling time).

<sup>4</sup> [https://silab-redmine.physik.uni-bonn.de/repos/cordia/ADC\\_01](https://silab-redmine.physik.uni-bonn.de/repos/cordia/ADC_01)

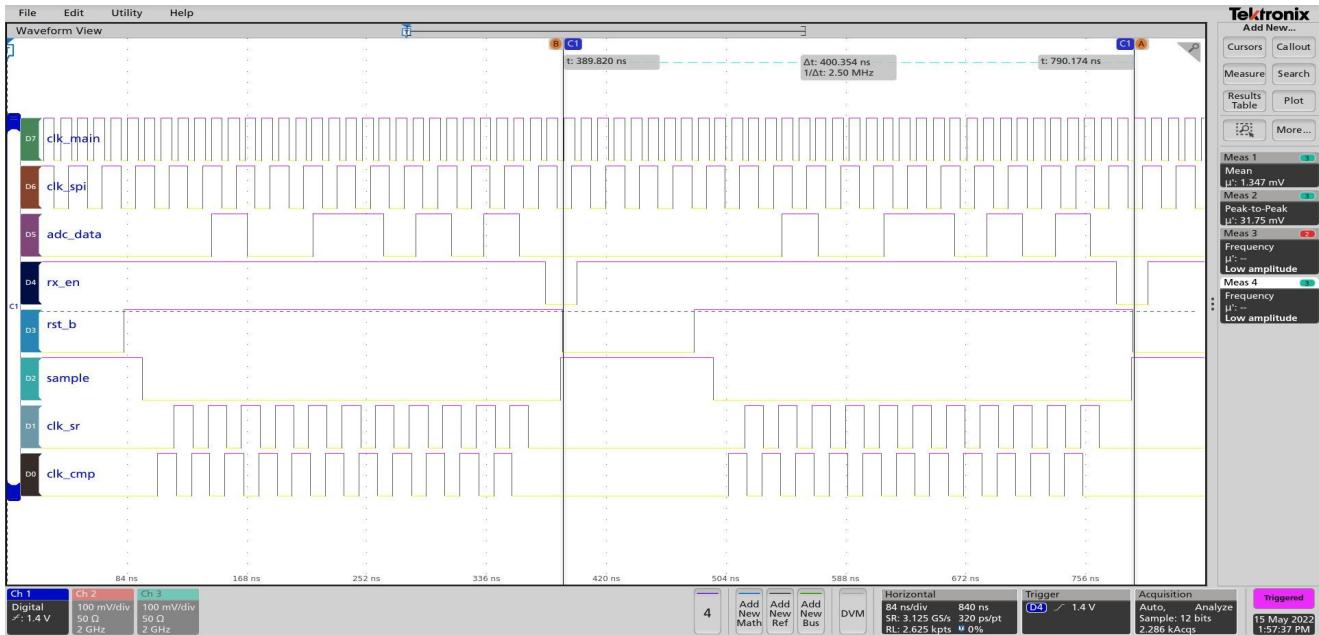
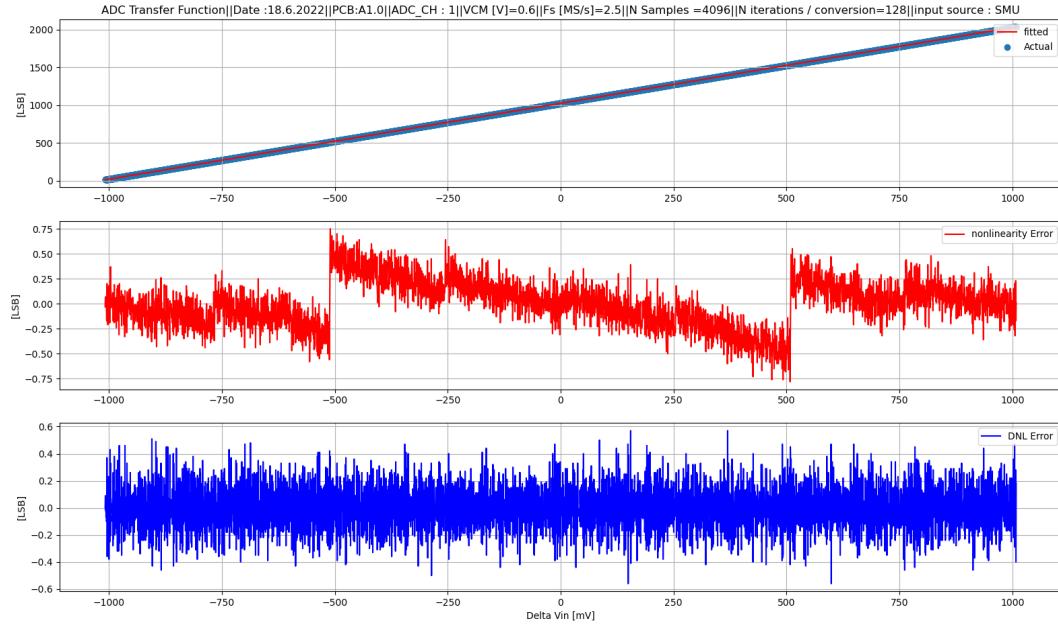


Fig 7: control digital signals

## 7.1 DC transfer function

A higher resolution digital ramp, compared to 11 bits, is applied to the ADCs input. The DC-ramp is generated using high precision SMU device (Source Measure Unit)<sup>5</sup>. For a typical measurement, the input voltage covers the range from nearly -1V to + 1V (~ 85% of the full range : 1.2V) with 4096 steps ( $\Delta V = 2V/4096 \approx 488\mu V$ ); which means twice resolution of the ADC under test. In order to reduce the impact of the noise on the INL/DNL computing, each point is averaged based on 128 iterations. The INL is computed, for each single point, as the difference between the linear regression (using least square method) and the actual data. The DNL, in the other hand, is computed as the difference between 2 successive points compared to the expected ideal step. A typical results are shown in figure 8. Further detailed results of all tested devices (4 DUTs times 4 ADCs) are reported in the section **detailed results**.

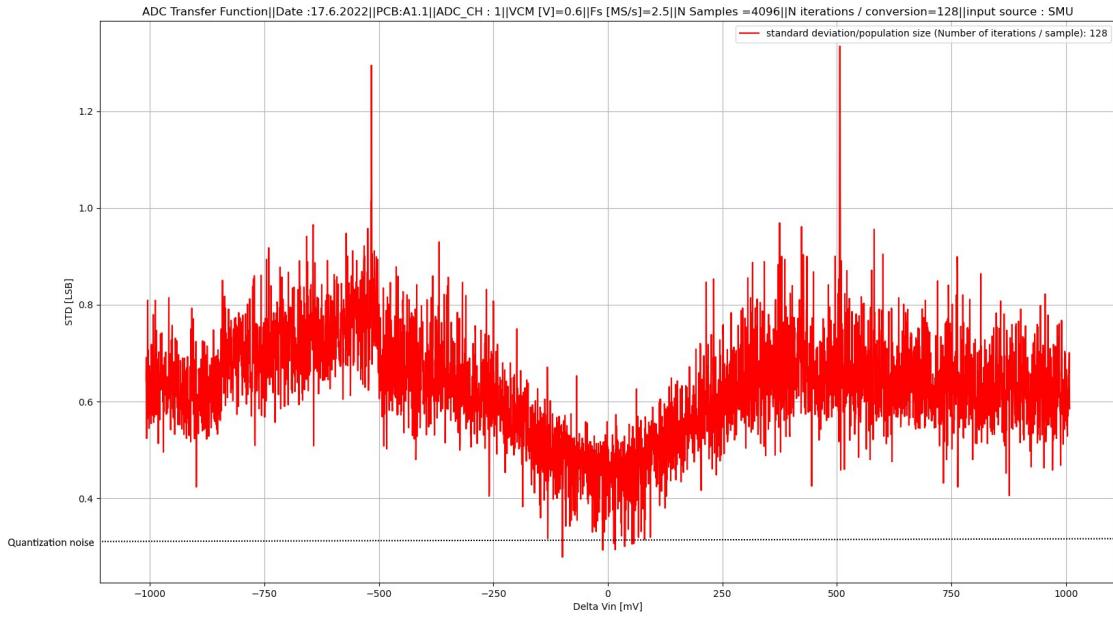


**Fig. 8:** typical DC transfer characterization (ADC01/CRS)

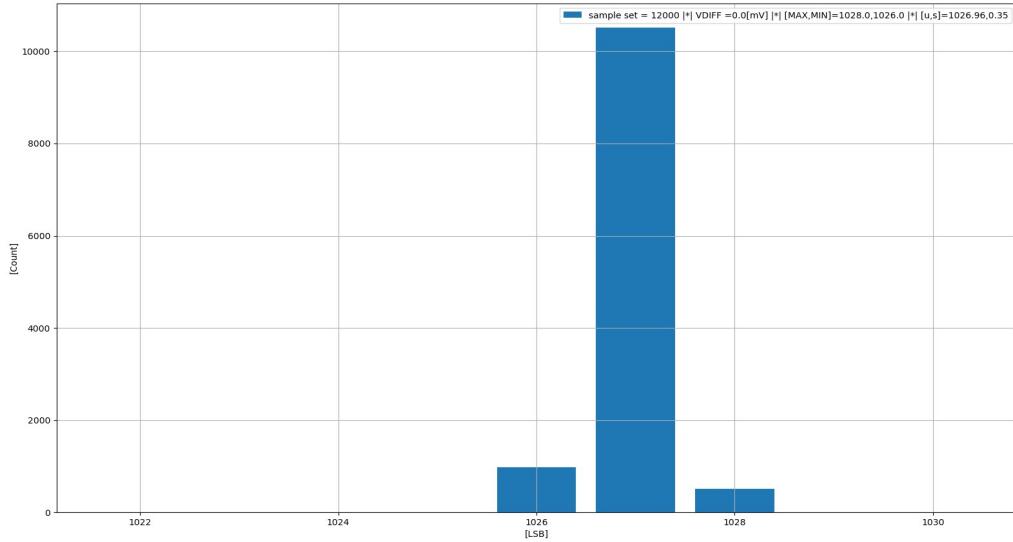
## 7.2 Noise

using the same test-setup, described in the latter section, the noise is evaluated as the standard deviation for each single input voltage (4096 step/ 128 iteration per step). A typical noise behavior is plotted in figure 9. Note that, all ADCs show, nearly, the same behavior (see section detailed results). This is owing, probably, to the CMOS input switches (sampling phase), in which the ON-resistance varies as a function of the input voltage<sup>6</sup>. In addition, the noise behavior is further investigated using the histogram method. This consists of computing the PDF (probability distribution function) of the ADC output @ a given constant input. The aim is to determine the distribution function (Gaussian is expected). Using 12000 successful iterations (conversions), a typical histogram of the ADC output is depicted in figure figure 10 (more results are reported in the section detailed results). From this results it can be inferred that the span of the ADC output lays in the range of 2 LSB (MAX-MIN) with a sigma of 0.35 LSB.

<sup>6</sup> To be further investigated (simulation!)



**Fig. 9:** typical standard deviation (ADC01/CRS)



**Fig. 10:** typical histogram of the ADC output (ADC01/CRS)

### 7.3 Temperature and supplies variation

The limits of the electrical parameters reported in table 2, as well as the operating temperature range (-20 to 85 °C) are tested and validated based on the DC-test-setup described above (see section 7). All

ADCs exhibits a good robustness against temperature and supplies variations. Detailed results are reported in the section: “detailed results”.

#### 7.4 Higher sampling rate

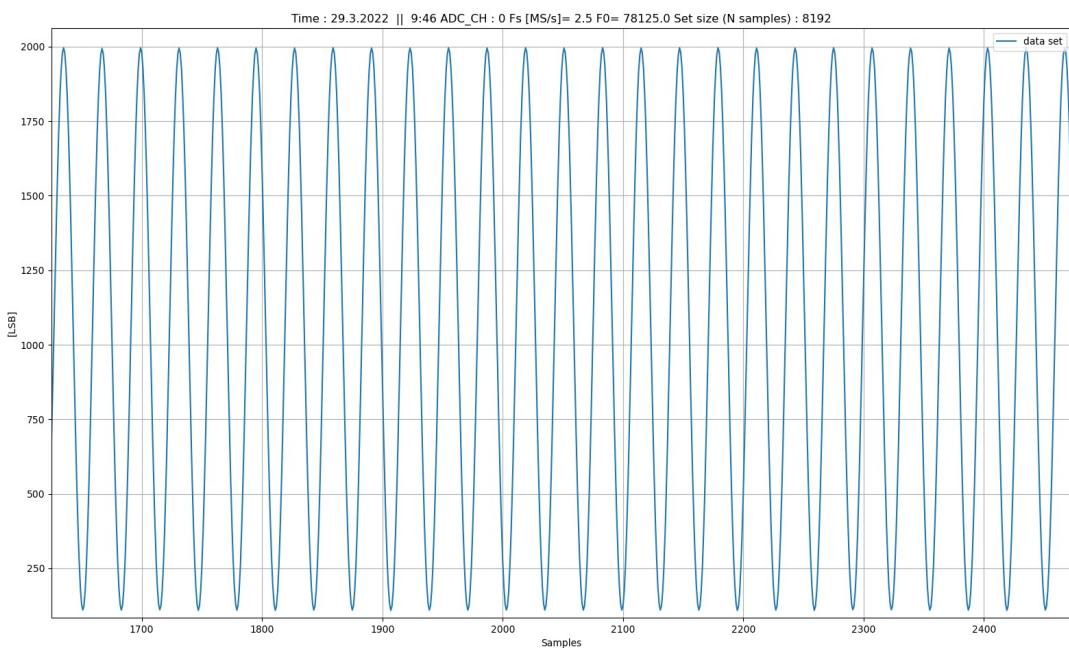
Similar to the test of temperature and supplies variation, the ADCs are tested with higher sampling rate (up to 3MS/sec). Note that the design is optimized for 2.5MS/s ! and so the aim of this test is only to investigate the robustness of the system.

#### 8. AC (dynamic) characterization

ENOB measures the combined effects of all sources of noise and distortion. This parameter provides a figure-of-merit for a given ADC. Most common ENOB test procedure is based on acquiring and analyzing the digital data of a pure sinus<sup>7</sup> analog input. The FFT of the digitized signal is used as an analog spectrum analyzer to measure the magnitude of the various harmonics and noise components.

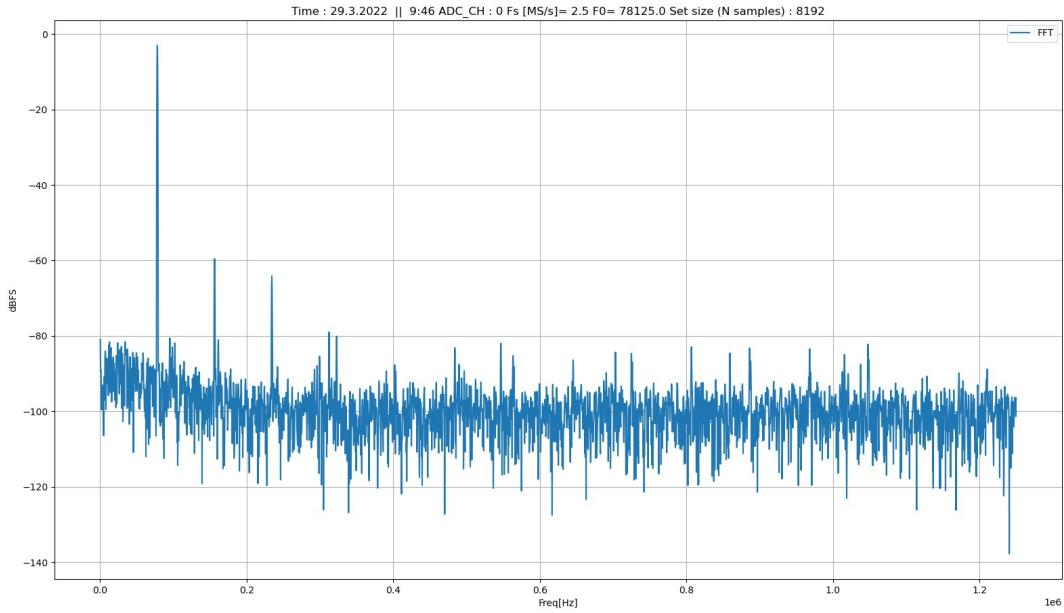
*“!! Work on progress !! at this point ! We were not able to set up a sinus wave with required spectral purity. We have only used an arbitrary function generator (Agilent) with THD in the range of 60dBc. We are working on a solution with 4<sup>th</sup> order bandpass filter! unfortunate the delivery is delayed due to the chips shortage!*

*This section will be updated ”*

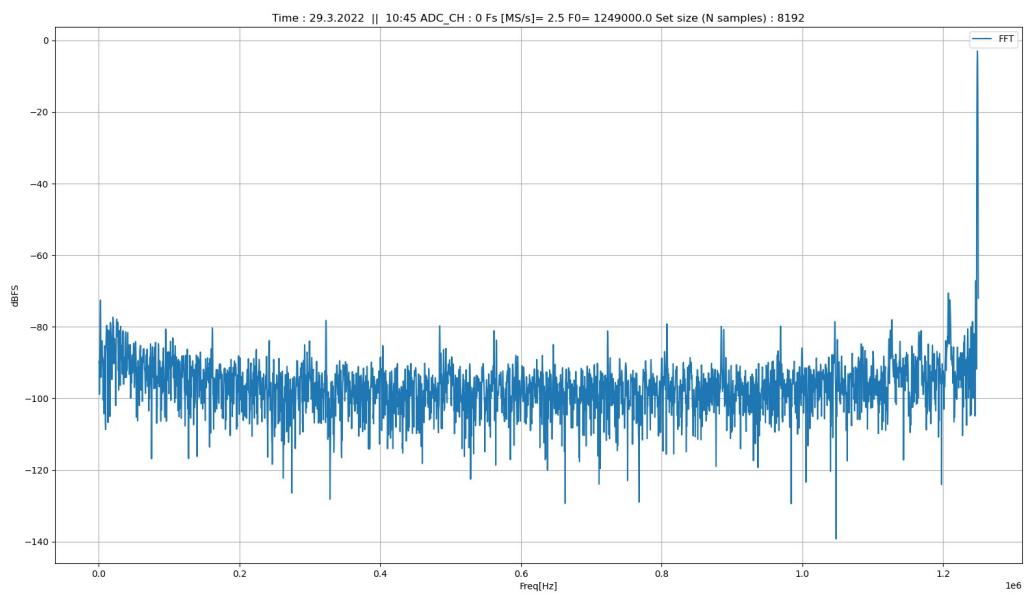


**Fig. 11:** digitized sinus waveform (input frequency  $F_0 = 78.125$  kHz)

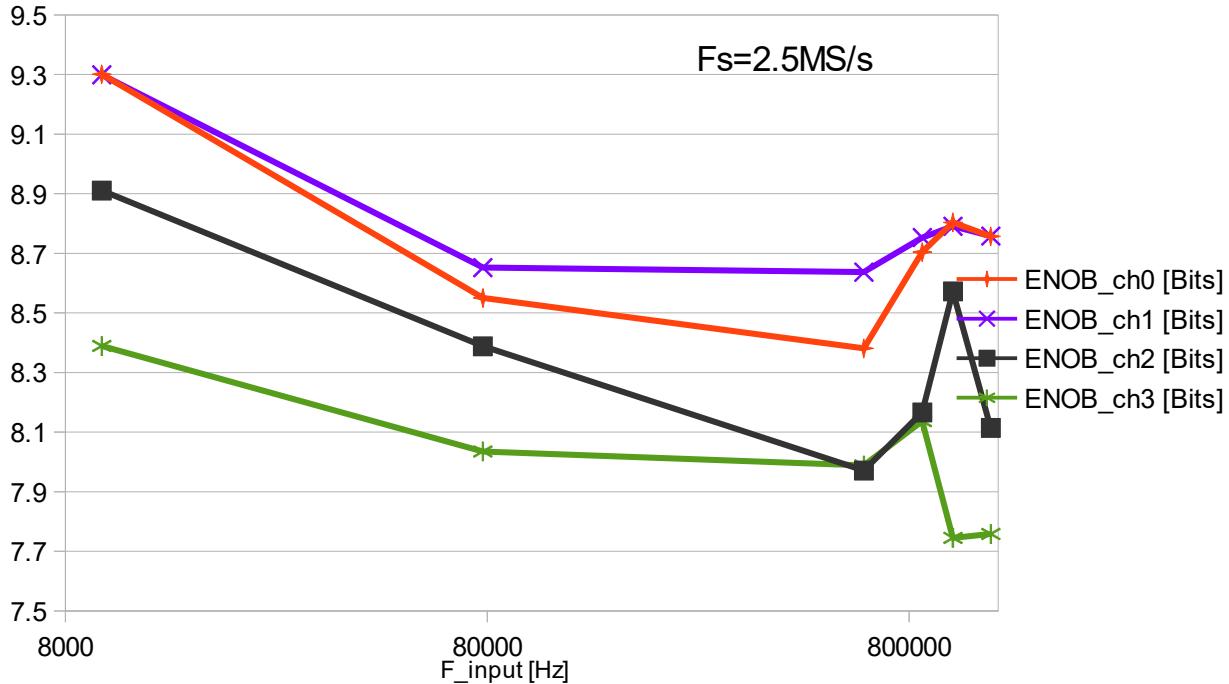
<sup>7</sup> this refers to the spectral purity of sinus signal (THD); for 10 Bit resolution at least 62 dBc is needed



**Fig. 12:** FFT (input frequency  $F_0 = 78.125 \text{ kHz}$ )



**Fig. 13:** FFT (input frequency  $F_0 = 1.249 \text{ MHz}$ )



**Fig. 14:** ENOB vs. input frequency

### comparison and assessment

As mentioned before only 4 DUTs, at this point, are characterized and hence no statistical data are available. Since, both INL and DNL depends on the mismatch between devices (e. g. DAC-Capacitors) as well as the process variation (die -to-die and/or wafer-to-wafer), the current results reflect only a typical performances. Nonetheless, considering the ENOB, noise evaluation and INL/DNL of all tested DUTs, it can be concluded that the 4 ADCs (table 1) exhibit a 10 bits resolution<sup>8</sup>. However, ADC01 (CRS) shows relatively stable behavior with respect to INL/DNL. It is worth mentioning that ADC02/03 (with redundancy) can be further improved with calibrate (by adjusting the weight matrix). All 4 ADCs exhibits the same noise level, which is expected, as the ADC's variants have the same input capacitance, sampling switches and comparator. The latter is the main contributor to the total noise.

<sup>8</sup> evaluated based on 11 Bits / aimed 10 Bits resolutions

ADC01 (CRS) <sup>9</sup>		Description	Condition	MIN	TYP	MAX
DC characteristics	INL [LSB]			n. a.	< 1	No data available
	DNL [LSB]			n. a.	< 1	No data available
	Typical offset [LSB]	Rough estimation <sup>10</sup>		-10		+10
	Typical gain [LSB/1V]	Rough estimation		990	1000	1010
AC (dynamic) characteristics	ENOB		@ Finput = Fs/2		!!!! Bits	

**Table 5:** characteristics of ADC01

## Nomenclature

ENOB	: effective number of bits
THD	: total harmonic distortion
INL	: integral non-linearity
DNL	: differential non-linearity
FFT	: fast fourier transformation
DUT	: device under test

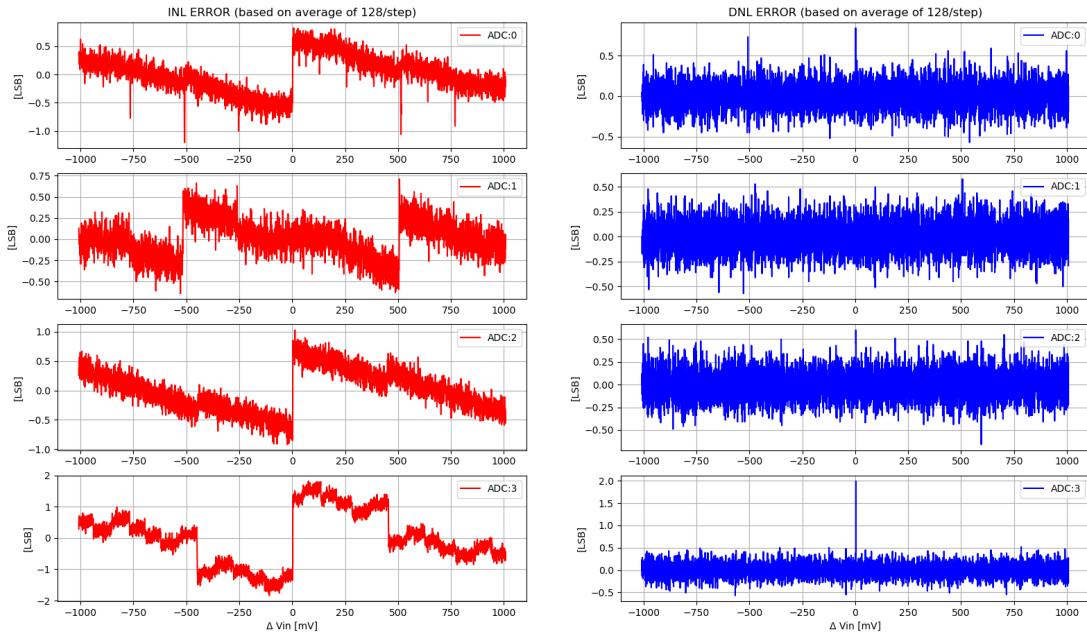
## Reference

- [1] A. Marras a,b , A. Klyuev a,b , T. Laurus a,b , D. Pennicard a,b , U. Trunk a,b , C.B Wunderer a,b ,
- [1] T. Hemperek c , T. Kamilaris c , H. Krueger c , T. Wang c and H. Graafsma a,b,d“Development of CoRDIA: a High-Speed Imaging Detector, for Diffraction-Limited Synchrotron Rings and Continuous-Wave Free Electron Lasers“, 2021 IEEE NSS MIC.
- [2] Jen-Huan Tsai, Hui-Huan Wang, Yang-Chi Yen, Chang-Ming Lai, Yen-Ju Chen, Po-Chuin Huang, Ping-Hsuan Hsieh, Hsin Chen, and Chao-Cheng Lee, “A 0.003 mm 10 b 240 MS/s 0.7 mW SAR ADC in 28 nm CMOS With Digital Error Correction and Correlated-Reversed Switching”, EEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 50, NO. 6, JUNE 2015
- [3] Wan Kim, Student Member, IEEE, Hyeok-Ki Hong, Student Member, IEEE, Yi-Ju Roh, Student Member, IEEE, Hyun-Wook Kang, Student Member, IEEE, Sun-Il Hwang, Dong-Shin Jo, Dong-Jin Chang, Min-Jae Seo, and Seung-Tak Ryu, Senior Member, IEEE, “A 0.6 V 12 b 10 MS/s Low-Noise Asynchronous SAR-Assisted Time-Interleaved SAR (SATI-SAR) ADC”, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 51, NO. 8, AUGUST 2016.
- [4] Chun-Cheng Liu, Member, IEEE, Che-Hsun Kuo, and Ying-Zu Lin, Member, IEEE, “A 10 bit 320 MS/s Low-Cost SAR ADC for IEEE 802.11ac Applications in 20 nm CMOS”, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 50, NO. 11, NOVEMBER 2015

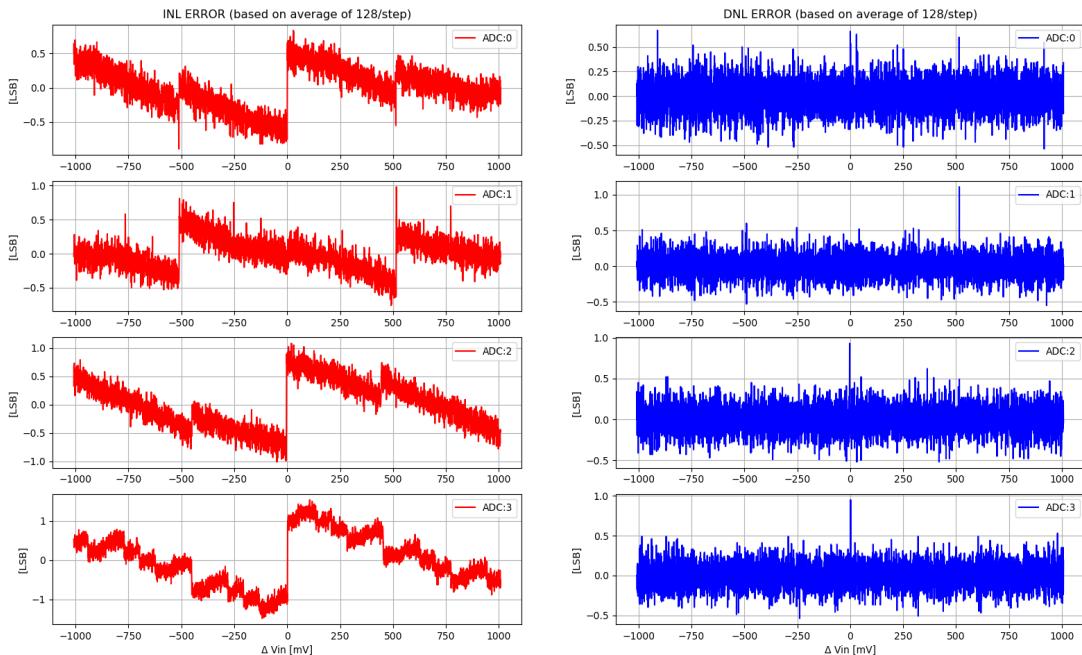
<sup>9</sup> based on the evaluation of only 4 devices ! No statistical data are available<sup>10</sup> guess based on former experience

## detailed measurement results: INL/DNL (4 DUTs X 4 ADCs / Typical)

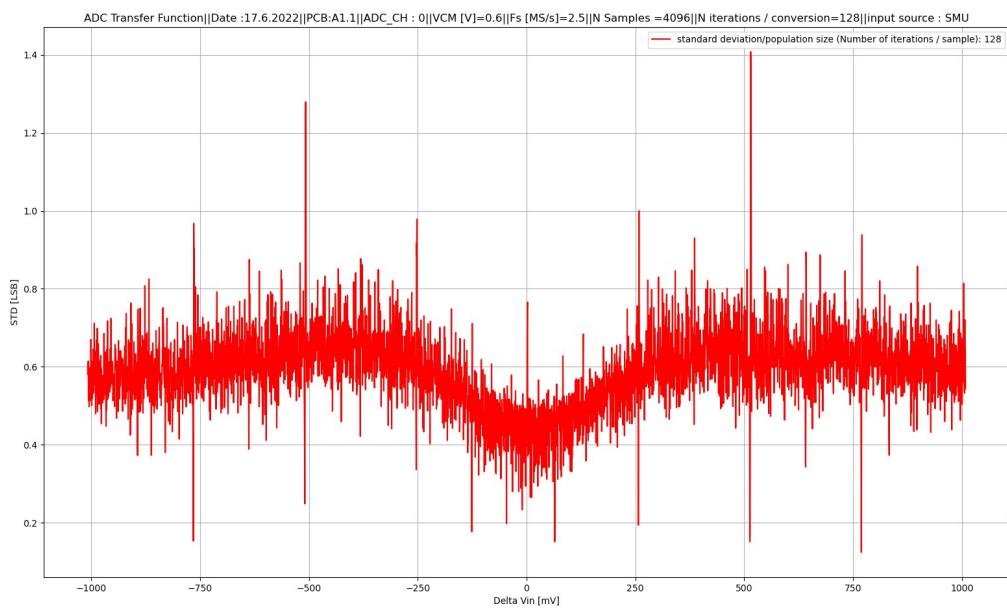
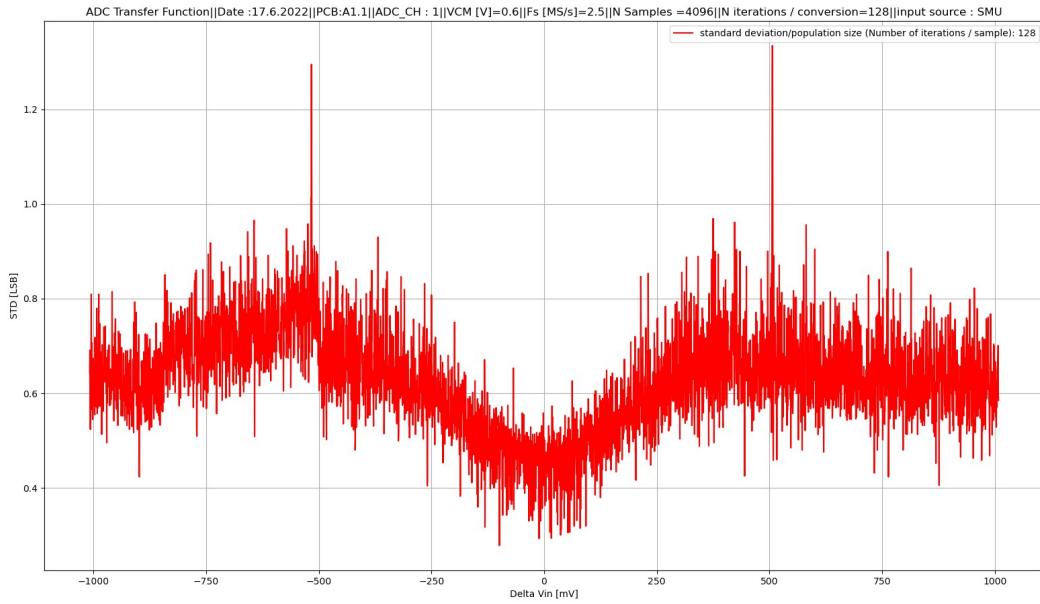
17.6.2022 / DUT:A1.1 (PCB+IC) / Typical operating conditions: room Temp, VCM [V]=0.6, Fs [MS/s]=2.5, Input voltage range : [-1V, +1V], N input steps=4096, number of iterations (conversion cycles per input : 128), input source SMU (Keithley 2602A).

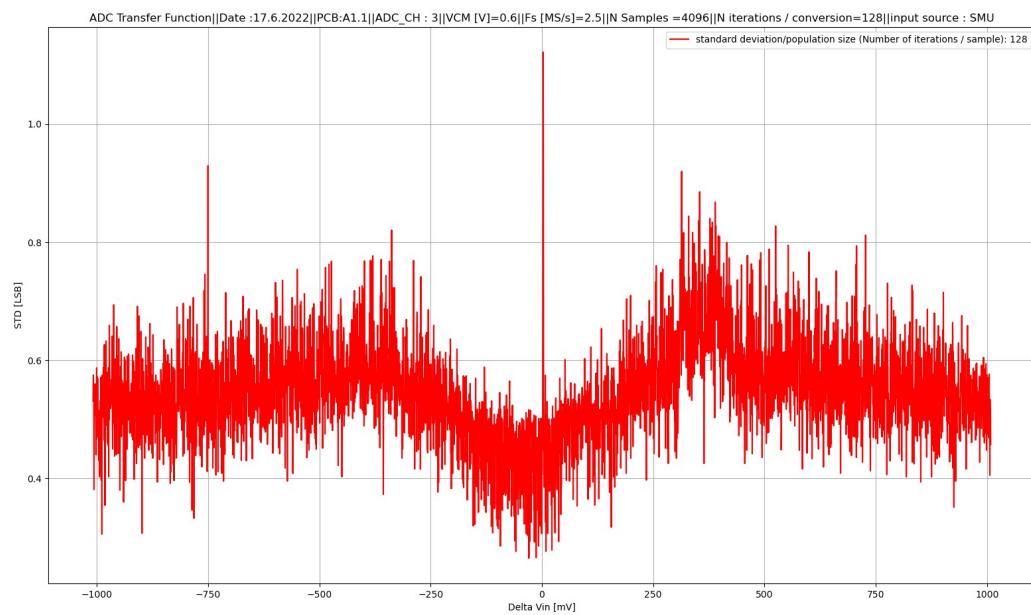
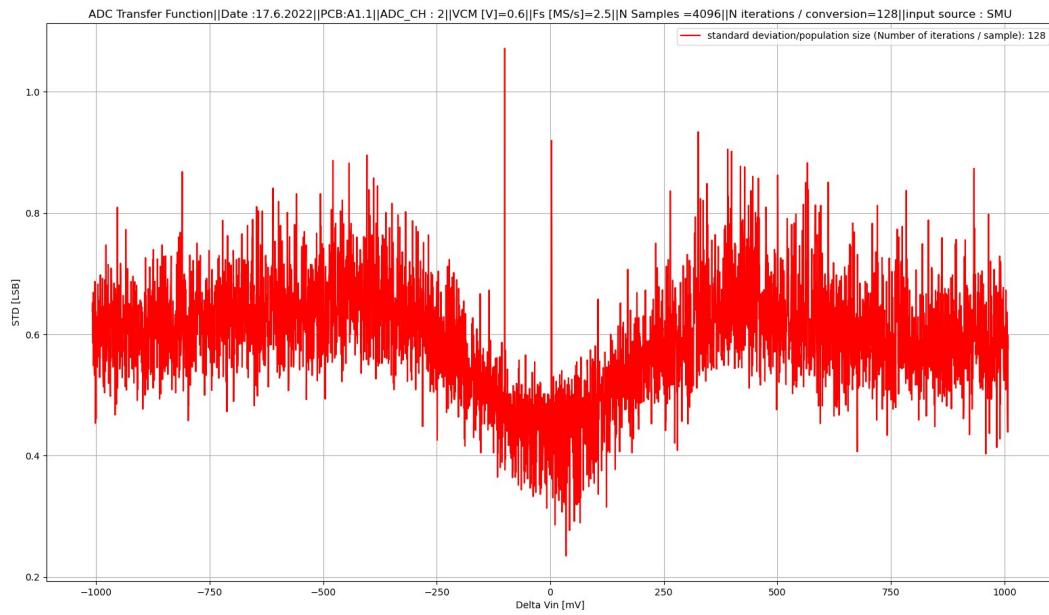


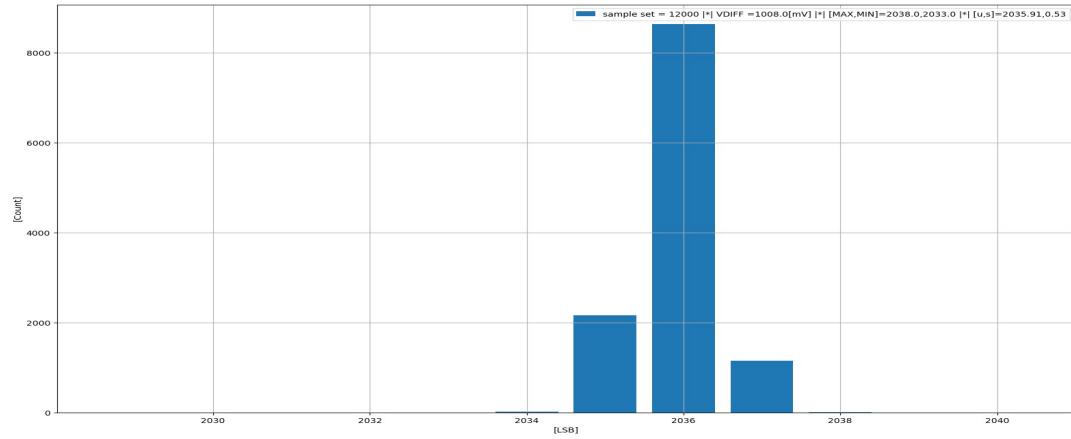
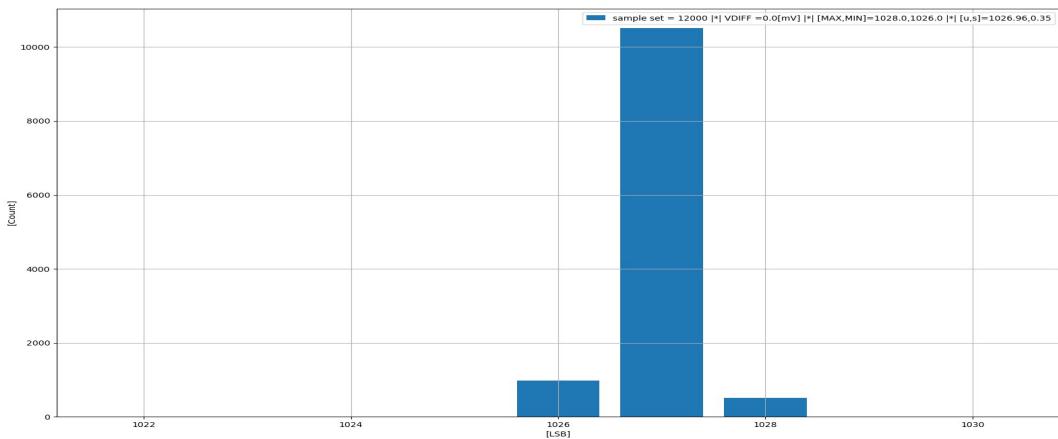
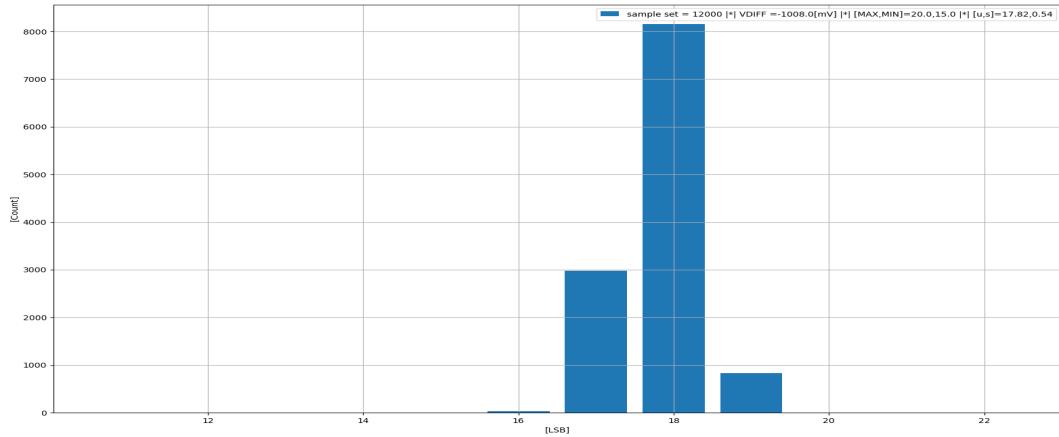
19.6.2022 / DUT:A1.3 (PCB+IC) / Typical operating conditions: room Temp, VCM [V]=0.6, Fs [MS/s]=2.5, Input voltage range : [-1V, +1V], N input steps=4096, number of iterations (conversion cycles per input : 128), input source SMU (Keithley 2602A).



## Noise (4 X ADCs / Typical)

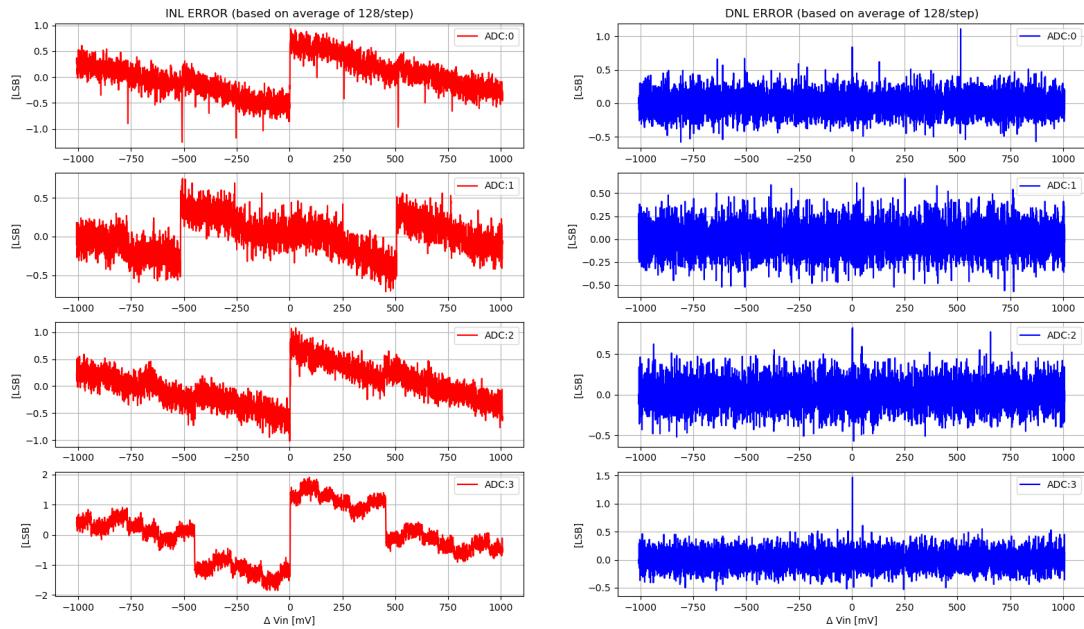




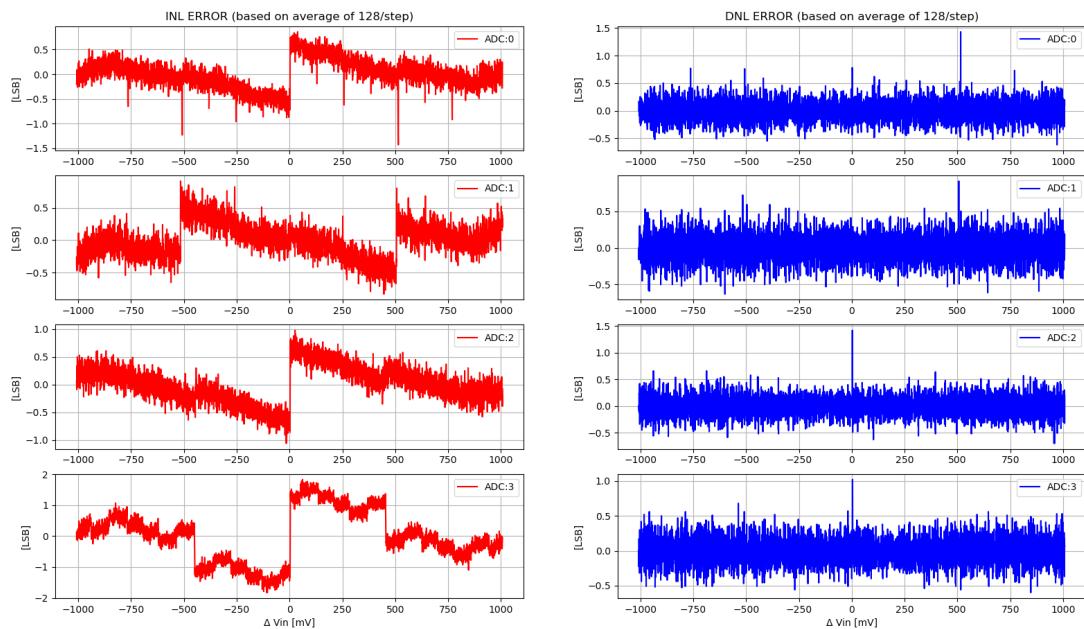
**Noise (Histogram / ADC01 / Typical)**

## Temperature test (INL/DNL / 4 X ADCs)

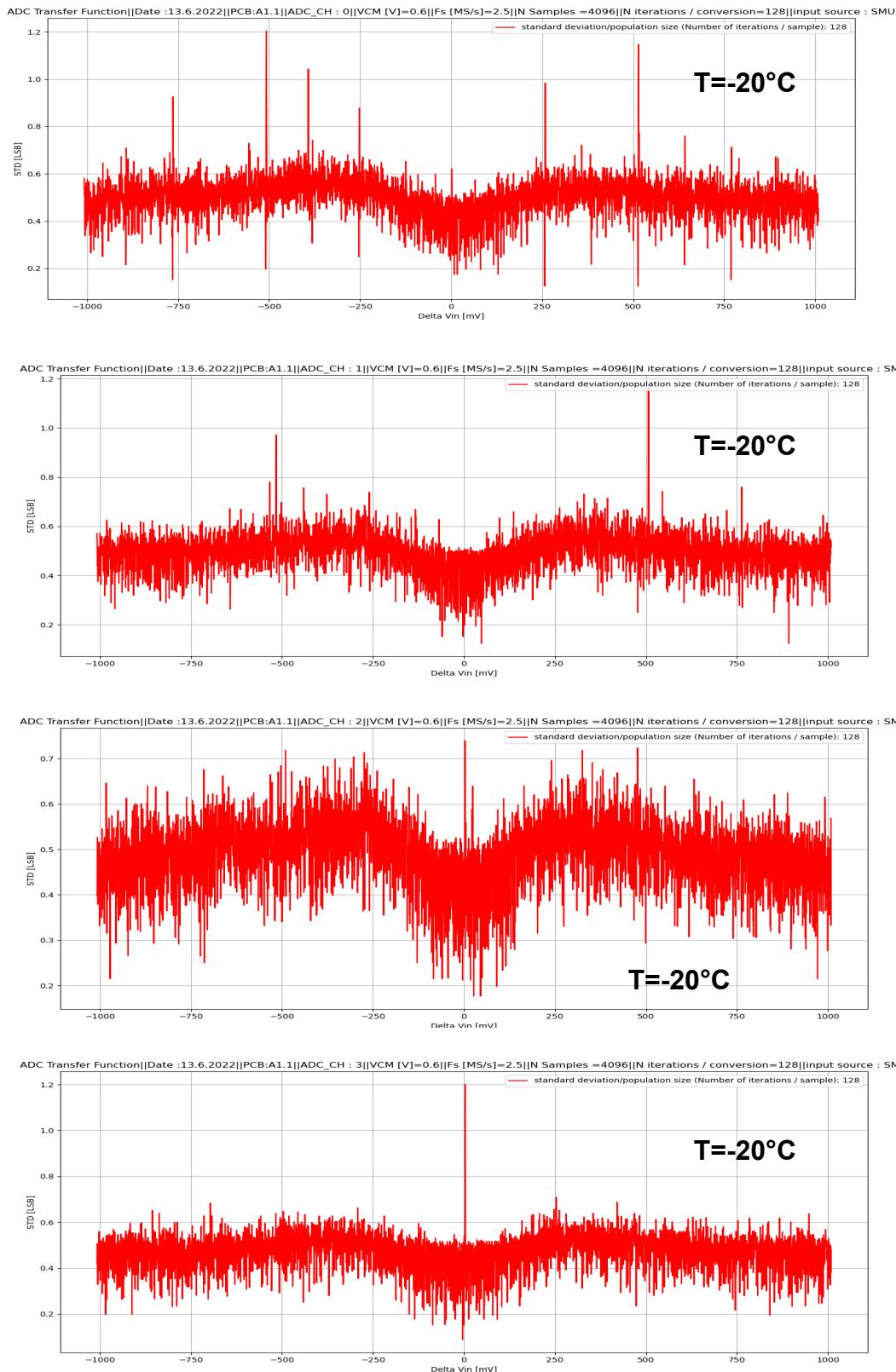
13.6.2022 / DUT:A1.1 (PCB+IC) / Temp = -20 °C , VCM [V]=0.6, Fs [MS/s]=2.5, Input voltage range : [-1V, +1V], N input steps=4096, number of iterations (conversion cycles per input : 128), input source SMU (Keithley 2602A).



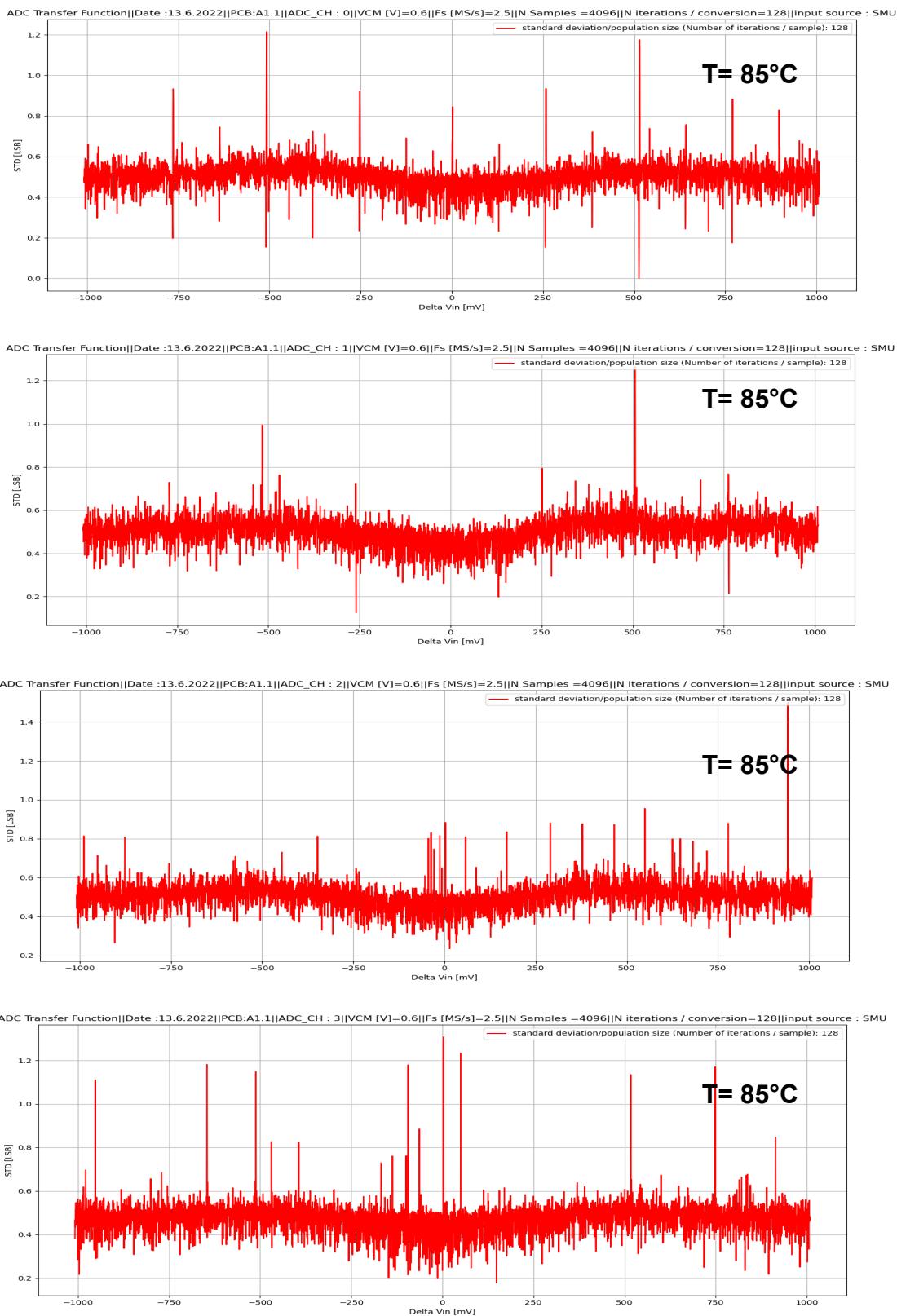
13.6.2022 / DUT:A1.1 (PCB+IC) / Temp = 85°C , VCM [V]=0.6, Fs [MS/s]=2.5, Input voltage range : [-1V, +1V], N input steps=4096, number of iterations (conversion cycles per input : 128), input source SMU (Keithley 2602A).



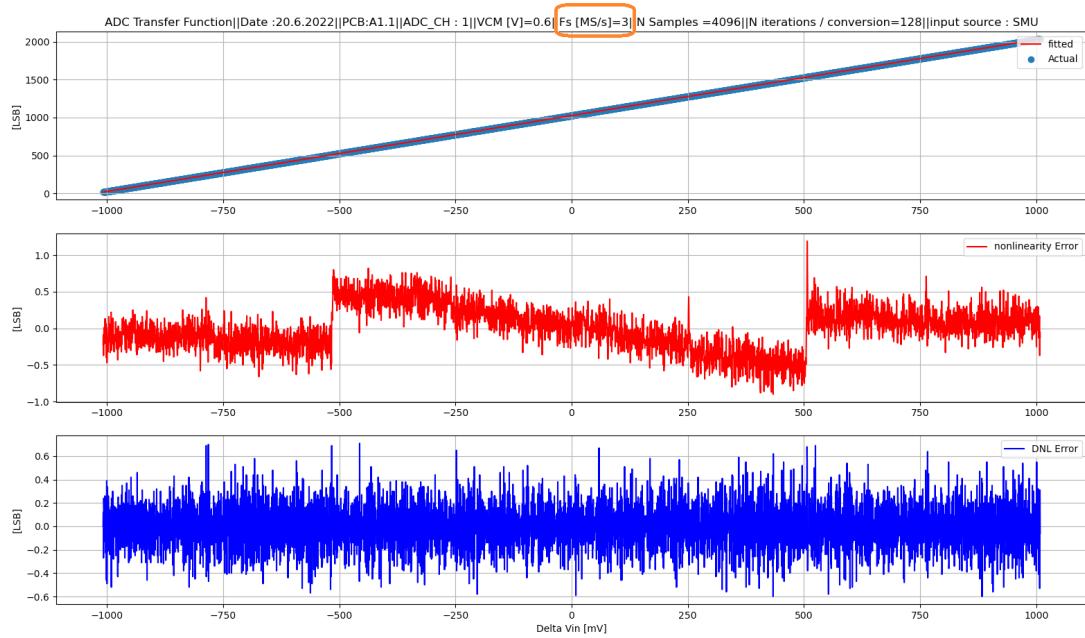
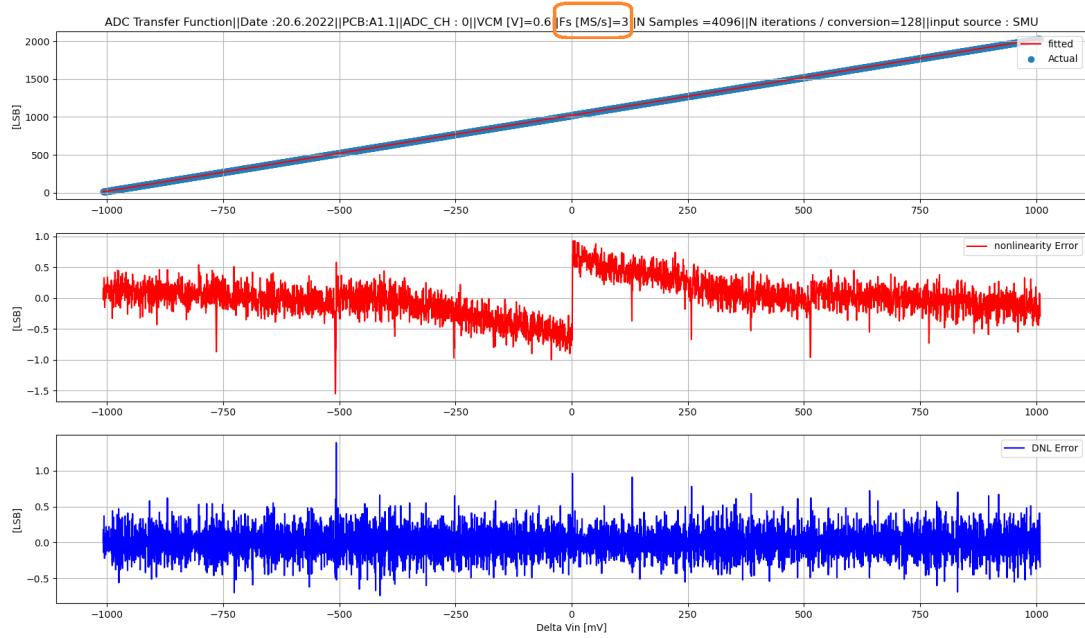
### Temperature test (Noise @ -20 °C / 4 X ADCs)

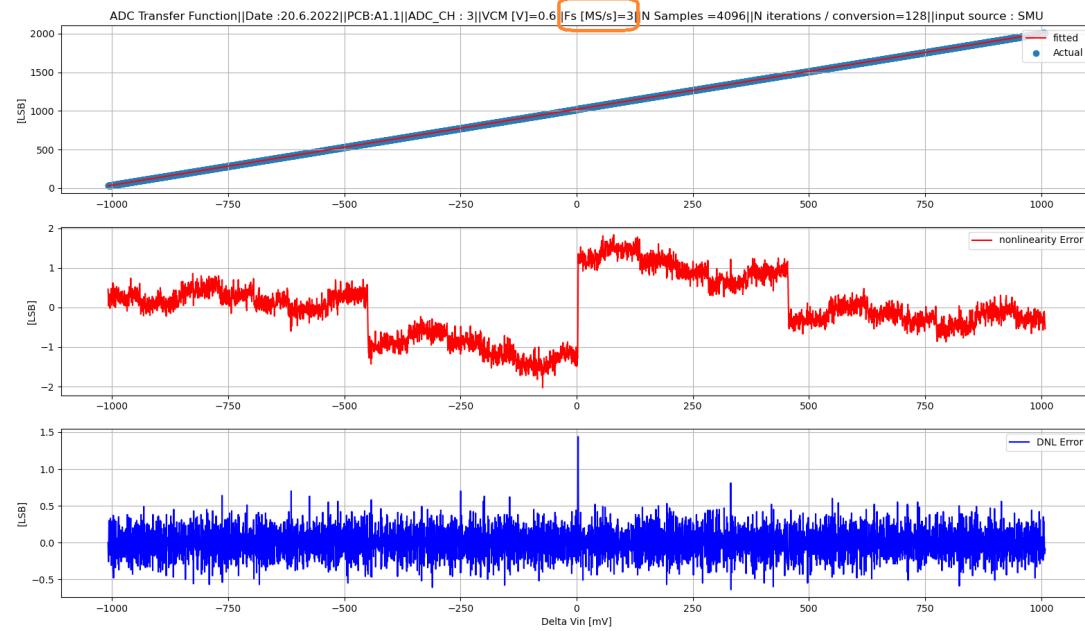
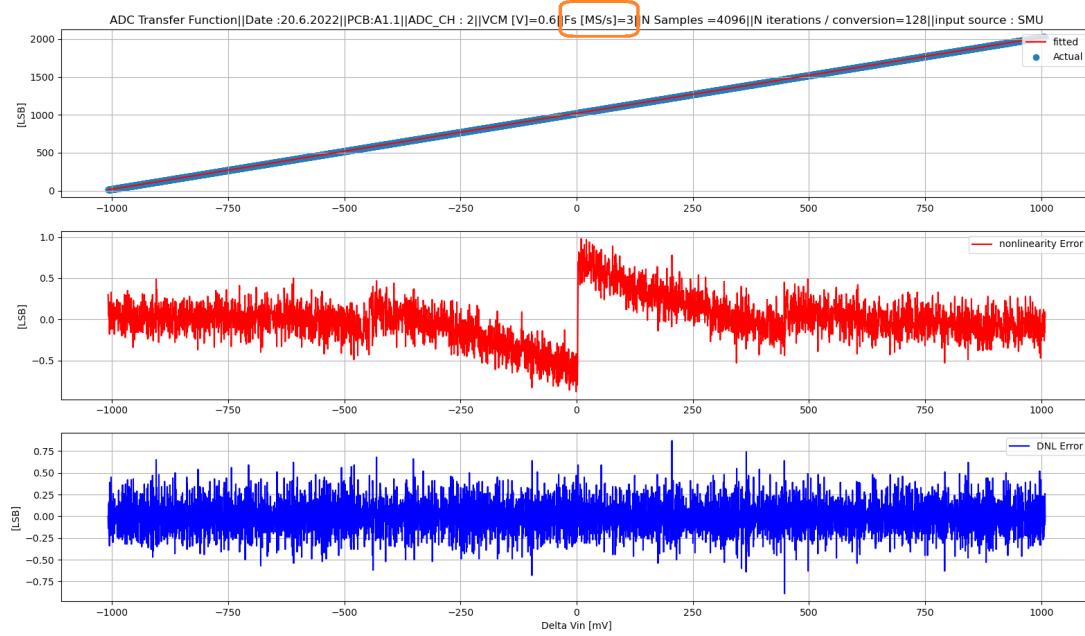


### Temperature test (Noise @ 85 °C / 4 X ADCs)



### Higher sampling rate (INL/DNL / 4 X ADCs)





### High sampling rate (Noise / 4 X ADCs)

