SAR ADC schematic diagram

Title:	SAR ADC		
Project: Embedded System Lab		Drawn by: HK	
		Revision: 1.1	
Date: 09/02/2023	Time: 17:06:51	Sheet 1 of 2	
File: SAR_ADC.SchDoc			

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SI LAB
Silizium Labor Bonn

VDD

R31
470R

D8
1N4148W-7-F

U6
5 VREF   VIN 4
         EN 3
2 GND   NC 1
LM4132AMF-1.8/NOPB

C8
X7R
10u

VDD

R32
100k

U7
OPA354AIDBVT
4 −
5
3 +
2
1

R33
100R

RAMP

RAMP

T1
1 FDN357N
3
2

C9
Film
10n

GND   GND   GND

D9
1N4148W-7-F

U1
TLV7011DBVR
5
+ 3
1
− 4
2

VDD

R34
1k

C10
X7R
100n

GND

VREF

VREF

VDD

C11   C12
X7R   X7R
100n   100n

GND

GND

GND

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Rev 1.1 HK 11/2022

COMP

R4
R3
R5
C5

U2

C1

U3
R1

C7

TSV

ADC INPUT

D7 D6 D5 D4 D3 D2 D1 D0

DAC
bits

U5
C11

U4

C2

UNI
BONN

Embedded
System
Lab

SAR-ADC

SPI

DAC
VREF
RAMP

OUTPUT

C3
C4

T1

R32 U6

C8 R33

R31
C6

C9

R34 C10

C12

U1

ON

R30

D9

U7

D8

R31