
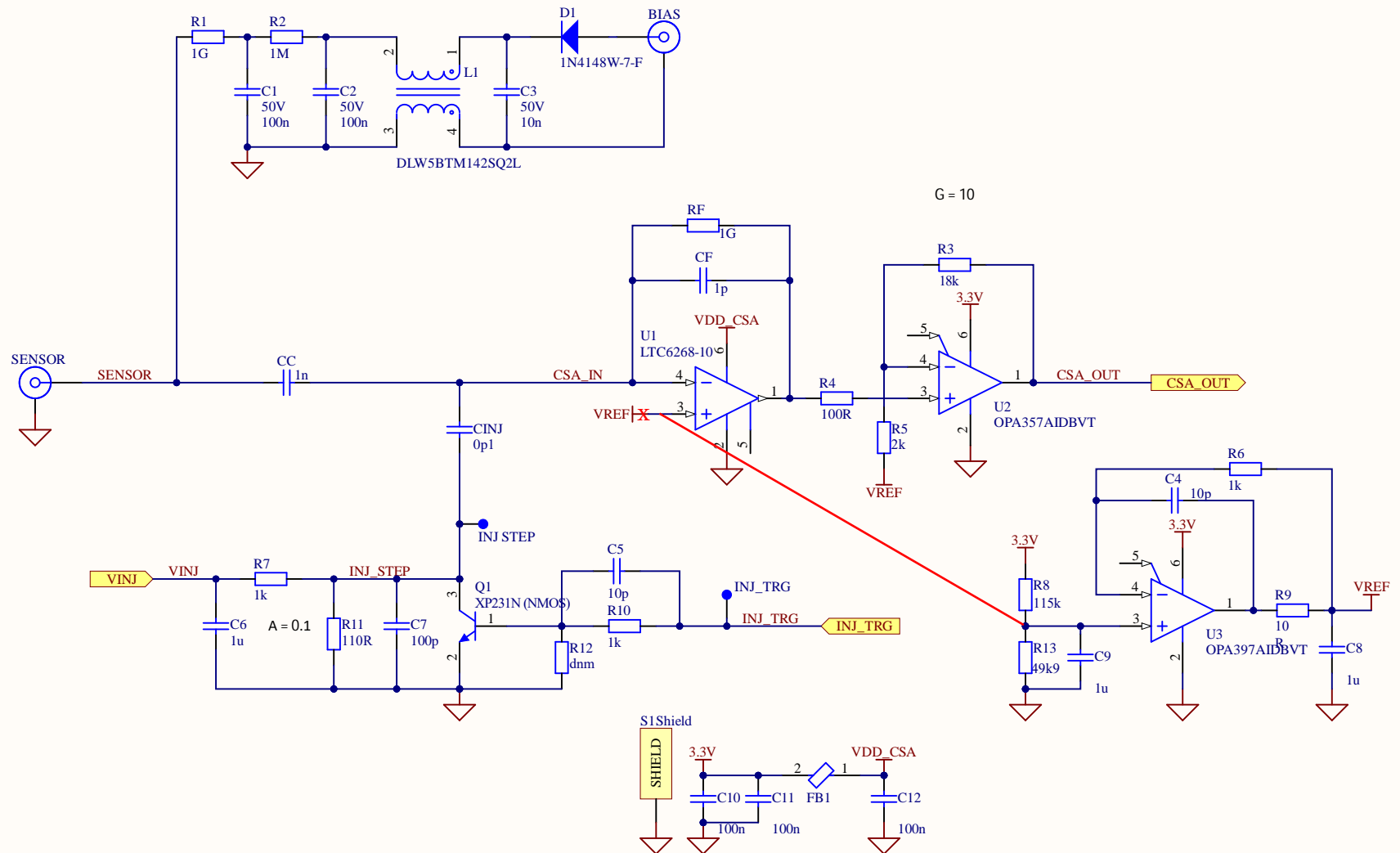
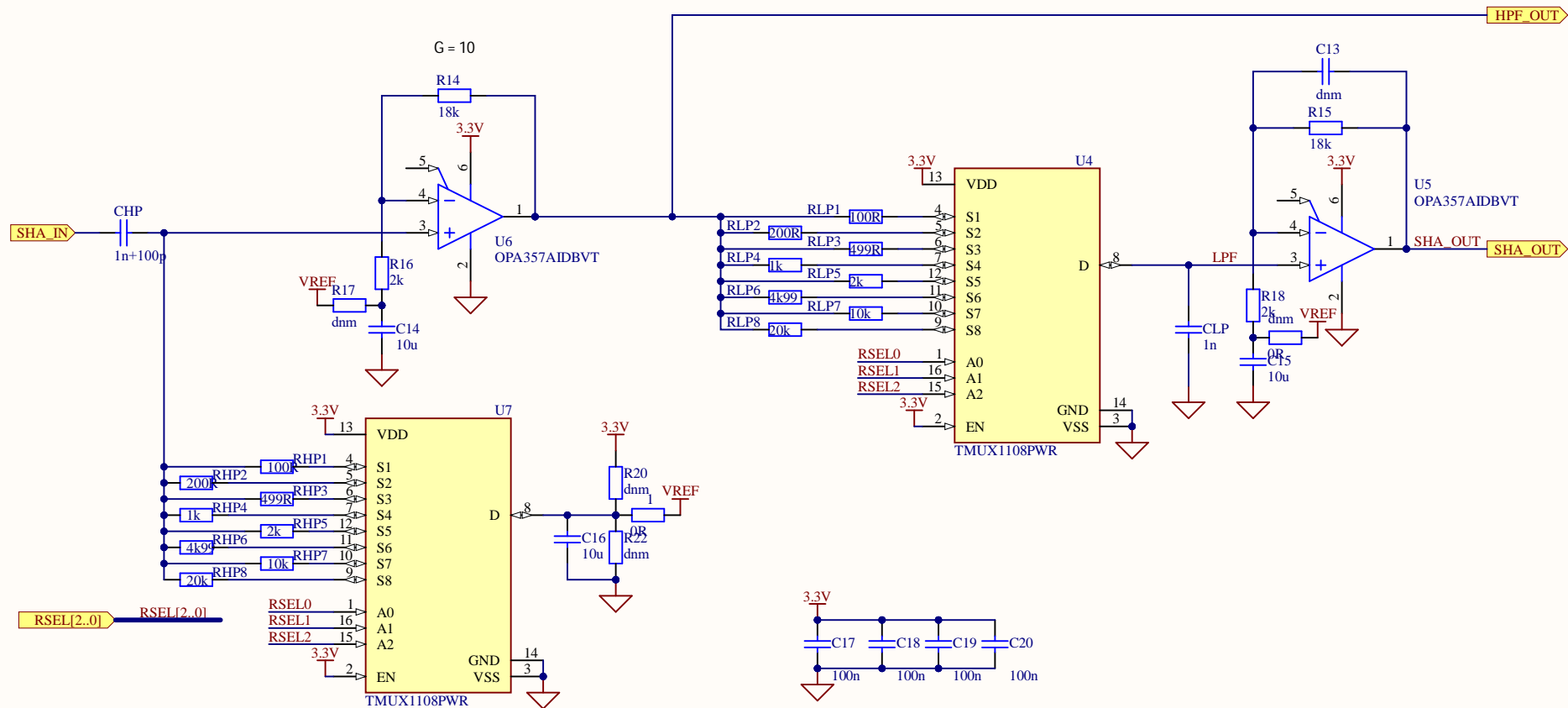
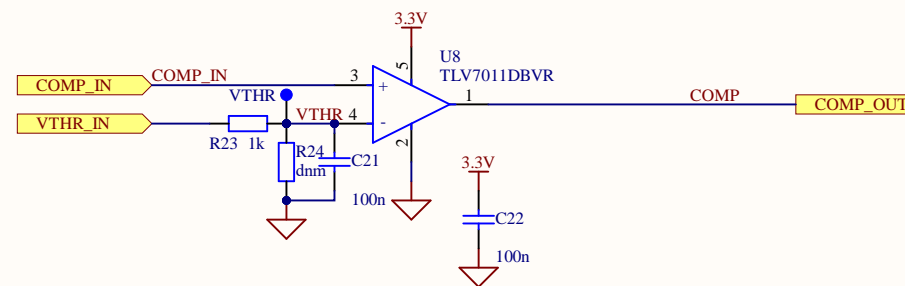


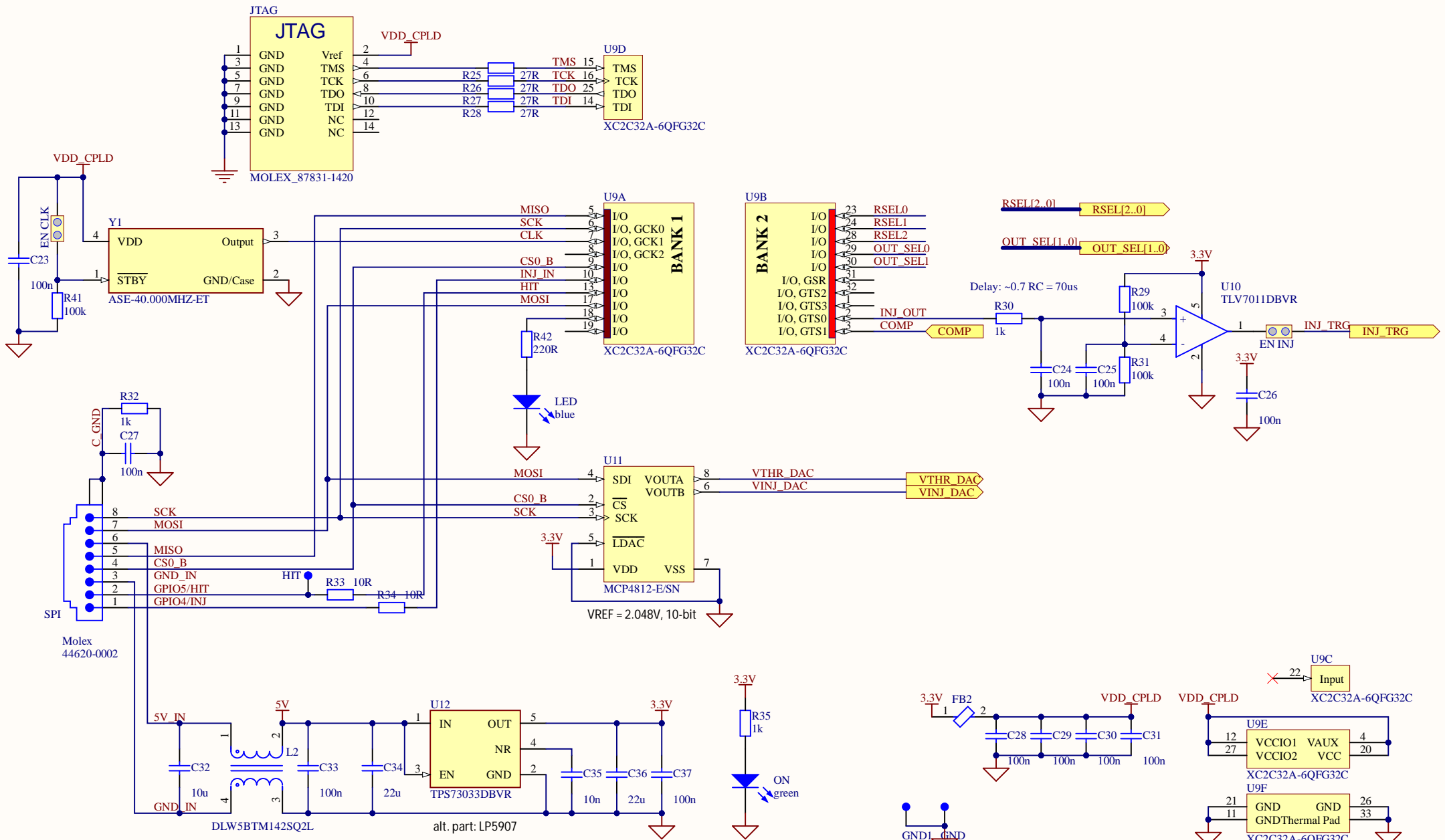
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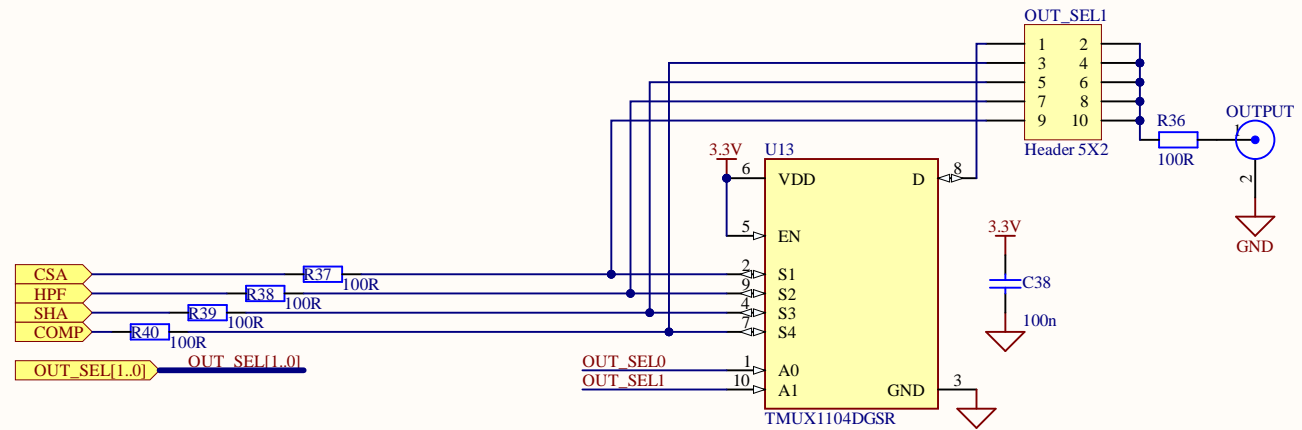
Title: Analog Signal Processing Frontend			 Physikalisches Institut Universität Bonn Nußallee 12 53115 Bonn
Project: Embedded System Lab	Drawn by: HK		
Date: 09/02/2023	Time: 13:29:01	Revision: 1.1	
File: AFE.SchDoc		Sheet 1 of 6	













Embedded  
System  
Lab

Analog  
Front-end

**SI LAB**  
Silizium Labor Bonn  
Rev 1.1 HK /2023

JTAG

EN CLK

FB2

R42

HIT

VTNR

SPI

ON

R35

L2

C32

C33

C34

U12

C35

C36

C24

C25

C26

R29

R30

R31

R32

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