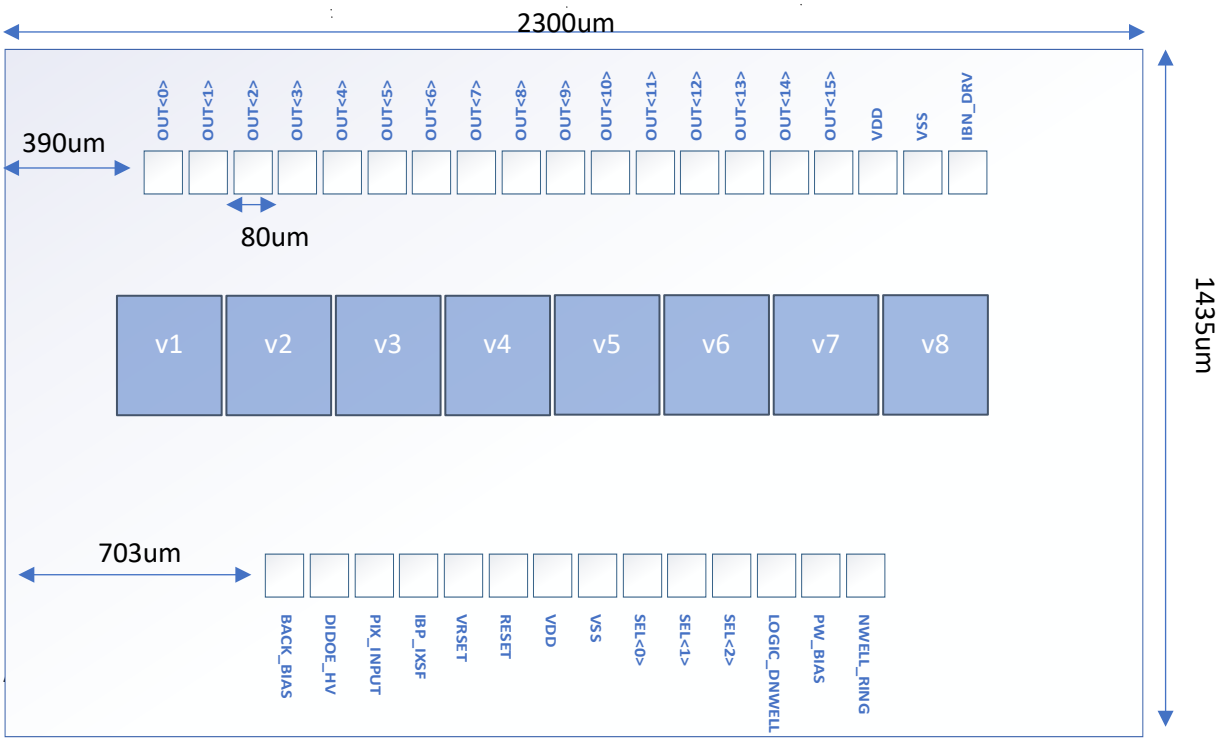
LF – SMALL FILL-FACTOR

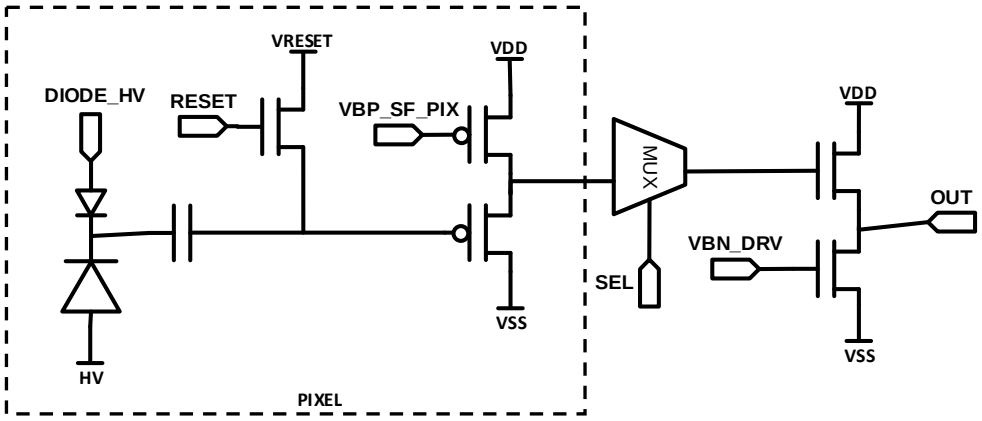
PADRING/IO:



PADLIST:

VDD – POWER 1.2V
VSS – GROUND
OUT<n> - 16 x analog outputs from the pixels (4x4)
IBN_DRV – bias for output driver/source follower (100uA)
BACK_BIAS – Outer guard-ring (P)
DIODE_HV – Diode bias (N)
PIX_INPUT – input of single central pixel array (v1)
IBP_PIXSF – bias of pixel source-follower (10uA)
VRESET – reset voltage
RESET – reset signal (digital)
SEL<n> - selects what array is connected to output (digital)
LOGIC_DNWELL – DNWELL potential of logic part (connected to VDD)
PW_BIAS – Bias of in pixel PWELL/bulk potential (GNC to -6V ? TBD)
NWELL_RING – NWELL ring around the chip connected (connected to VDD)

SCHEMATIC:

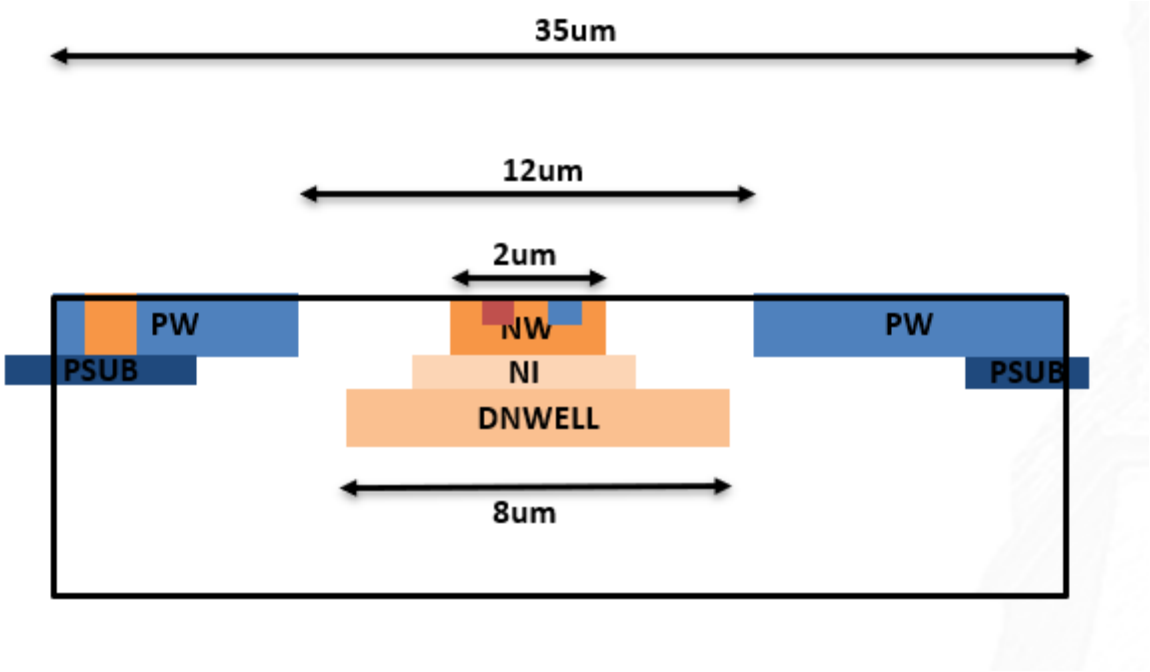


PIXEL ARRAY:

Chip consist of 8-pixel array 6x6 pixels (only inner 4x4 are connected to output). Version connected to output is selected by SEL pins.

Version	Diode opening [um]	AC [fF]	DNELL size [um]	Input W [um]
1	8	6	-	1
2 (1+injection)	8	6	-	1
3	12	12.5	3	1
4	8	6	-	0.5
5	8	10	-	1
6	8	12.5	-	1
7	12	12.5	8	1
8	12	6	-	1

PIXEL CROSS-SECTION:



PIXEL LAYOUT: