Power and Area Efficient Column-Parallel ADC Architectures for CMOS Image Sensors

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Abstract— **The ever-increasing resolution of CMOS imagers has had a profound impact on their analog readout electronics, and, in particular, on their ADC architecture. This paper gives an overview of the development of column-parallel ADCs that enable the high-speed and power-efficient readout of high-resolution CMOS imagers. In particular, the recently proposed multiple-ramp single-slope (MRSS) ADC will be discussed.**

I. INTRODUCTION

In recent years, the resolution of CMOS imagers has steadily increased. This increase has had a significant impact on their design. Apart from the continuous drive towards decreased pixel size, the bandwidth of the imager's readout circuitry must be continuously increased in order to read out larger and larger pixel arrays in the same frame time. As a result, column-level ADCs have become increasingly popular [1,2]. This is because they employ a large number of parallel ADC channels, which facilitates the high speed readout of large pixel arrays.

The design of such a column-level ADC is a very challenging task. In particular, three design targets must be simultaneously met. First, it is imperative that the read-out channels have a uniform response compared to one another. Any difference in response between the column ADCs will be highly visible as vertical stripes in the produced image. These artifacts are even visible if the magnitude of the non-uniformity is lower than that of other temporal noise sources in the read-out circuit. Second, the required chip area for each readout column should be minimized, since the column ADC should have the same width as a pixel on the chip, which is typically less than 10μm. Third, the power consumption of the column ADC should be minimized with an eye towards mobile applications.

The choice of ADC strongly determines how well the above-mentioned design targets can be met. In literature, three types of ADCs have been used in a column-level ADC: the cyclic ADC [1][2], the successive approximation ADC

[3][4] and the single slope ADC [5]-[8]. The latter is clearly the most often used.

In this paper, the column-level single-slope ADC will be reviewed, and the reasons for its popularity will be discussed. Apart from its advantages, the single-slope ADC also has the disadvantage of having a slow conversion speed. A recently introduced alternative ADC architecture [9][10] will be discussed that solves this problem. This architecture, called the multiple-ramp single-slope (MRSS) ADC offers a significantly higher conversion speed while maintaining the advantages of a single-slope ADC.

II. SINGLE-SLOPE ADC ARCHITECTURE

In Fig. 1, a block diagram and timing diagram of a column-level single-slope ADC is depicted. The only analog circuit in each column is a comparator, which compares an input voltage (V_{in1}, V_{in2}, etc.) with a centrally generated ramp voltage V_{ramp}. This ramp voltage spans the entire input range of the ADC. A central digital counter is running synchronously with the ramp voltage. When a column comparator detects that its input voltage equals the ramp voltage, it triggers a digital memory implemented in each column circuit. This memory then stores the counter value output by the central digital counter. Thus, the stored digital word is directly proportional to the input voltage of the column-level ADC.

The main advantage of the column-level single-slope ADC is the simplicity of its column circuit, which is partly due to the fact that the ramp generator can be centrally implemented. This reduces the required chip area of the column circuit to a minimum. A second advantage is that it is relatively easy to ensure uniformity between column circuits: to first approximation, only the comparator offset has to be compensated for, which can be done with an auto-zero technique. However, an important disadvantage of a single-slope ADC is its relatively slow conversion speed. Each n-bit A/D conversion requires 2^n clock periods, compared to only n clock cycles for both SAR and cyclic
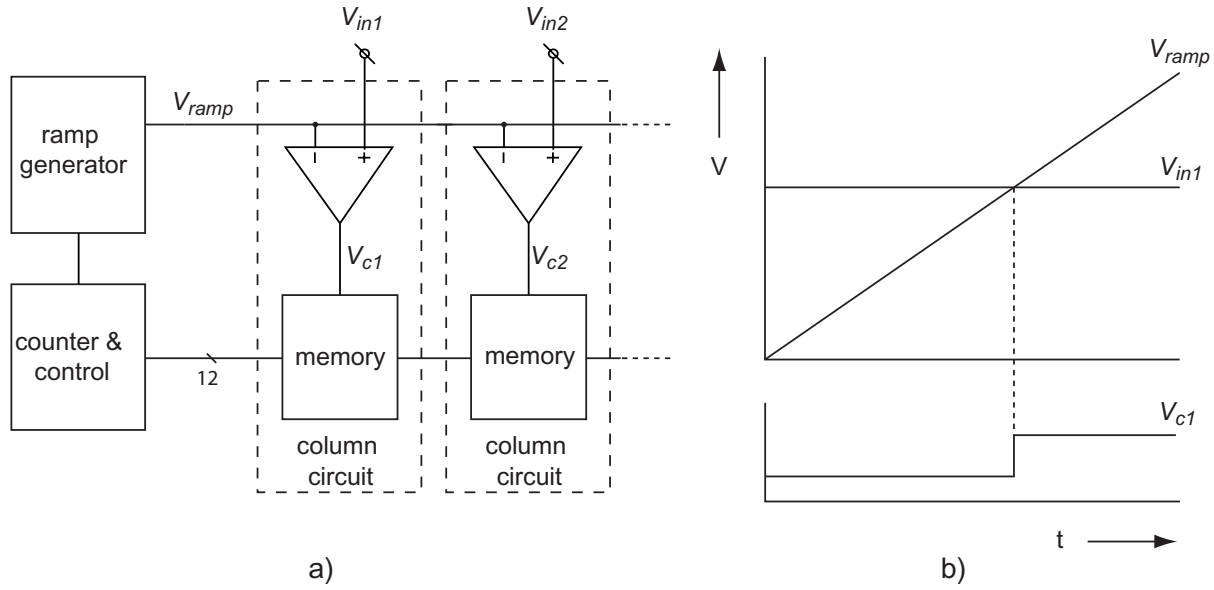

Figure 1.   a) Block diagram of a column-level single-slope ADC b) Corresponding timing diagram

ADCs. This is a serious limitation, particularly for higher (>10 bit) ADC resolutions, which in some cases can force the designer to trade-in ADC resolution for readout speed [8]. While SAR and cyclic ADCs are much faster, these all require much more column-level circuitry, which significantly increases chip area and increases column uniformity problems.

III.   MRSS ADC ARCHITECTURE

The MRSS ADC [9][10] can best be regarded as a cross between a single-slope and a SAR ADC. In both cases, as illustrated in Fig. 2, the A/D conversion is performed by means of a number of comparisons between a dynamic reference signal and the analog input voltage. In the case of a single-slope ADC, the dynamic reference generator outputs a ramp voltage. While this approach is simple and robust, it

Figure 2. Common principle of single-slope and successive approximation ADCs.

requires 2^n comparisons for an n-bit conversion, and is therefore slow. The successive approximation ADC requires only n comparisons, by using a dynamic reference generator whose output depends on the result of previous comparisons. The drawback of this approach in a column-parallel ADC architecture is that it requires feedback between the comparator and the dynamic reference generator, and therefore, the dynamic reference voltage becomes dependent on the input signal. In a column-parallel structure, in which there are several hundreds of comparators, this necessitates the implementation of a reference generator in each column, instead of a single, centrally implemented dynamic reference generator - as is the case in a column-parallel single-slope ADC. This significantly increases chip area, and makes it more difficult to ensure uniformity between columns.

The multiple-ramp single-slope (MRSS) ADC has a faster conversion speed than the single-slope ADC, without requiring a reference generator in each column. This is because the ramp voltage of an MRSS ADC, which spans the entire input voltage range in a single-slope architecture, is divided into m ramps, which each span $1/m$ of the input range. If each column comparator can be connected to the correct ramp (i.e. whose span contains the input signal), all m ramps can be output concurrently, resulting in a shorter conversion time compared to a single-slope ADC. In Fig. 2a, a block diagram of an MRSS ADC is shown. The dynamic reference generator outputs m different ramp voltages. Each column circuit has a set of switches that connects one of the m ramps to the input of the comparator. Compared to the single-slope architecture, the MRSS architecture only requires the addition of some analog switches, as well as some extra digital memory and logic in each column.

In Fig. 2b, the operation of the MRSS architecture is further illustrated with a timing diagram. The A/D
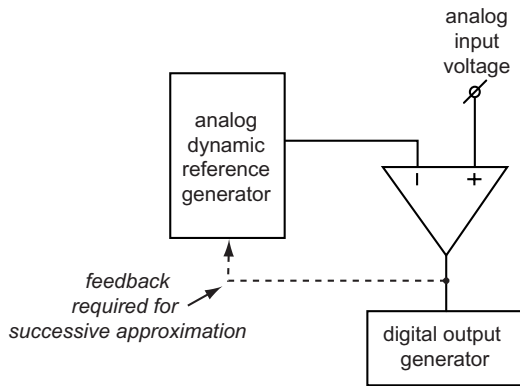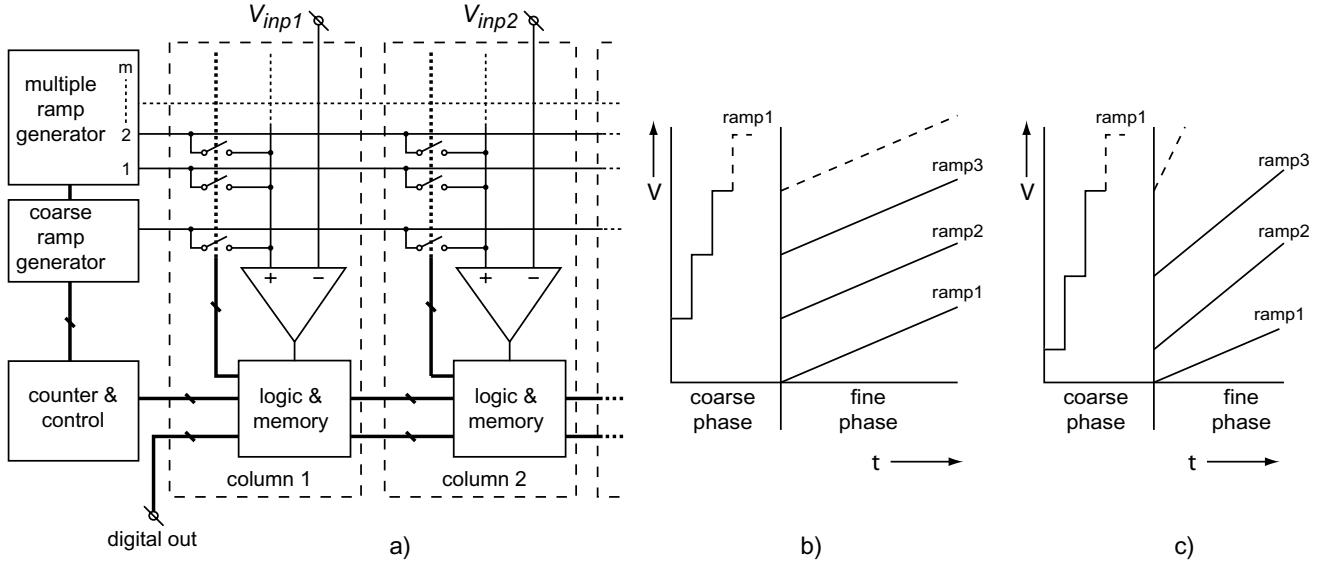
Figure 3. a) Block diagram of a column-parallel multiple-ramp single-slope (MRSS) ADC b) Corresponding timing diagram

conversion is subdivided into a coarse and a fine phase. In the coarse phase, all comparators are connected to a single coarse ramp voltage, and a single-slope A/D conversion is performed. The results of this coarse conversion are stored in the memory in each column. Next, the coarse conversion result is fed back into the analog switches, which connect the correct ramp to each comparator. The fine conversion phase is then performed while all *m* ramps are concurrently output. The fine conversion is essentially a single-slope conversion, but since each comparator is connected to a ramp corresponding to the level of its input signal, each ramp only has to span *1/m* times the ADC input range, and therefore, the conversion can be much faster. The result of the fine conversion is stored in the column memory. The final digital output is a combination of the results of the coarse and fine conversion phases.

If the number of ramps *m* is equal to a power of two, i.e. $m=2^p$, then the total A/D conversion time T_{conv} can be expressed as:

$$T_{conv} = \frac{2^p - 1}{f_{ck}} + \frac{2^q - 1}{f_{ck}} \qquad (1)$$

Where f_{ck} the clock frequency of the counter, and *p* and *q* are integers, $p+q=n$, and *n* is the resolution of the conversion. Therefore, the theoretical minimum conversion time occurs for $p=q$, which would result in a conversion time of 62 clock periods for a 10-bit resolution or 126 clock periods for a 12-bit resolution. However, such a choice for *p* and *q* would imply that 32 or 64 ramps would be required respectively. Two practical problems make it difficult to implement such a large number of ramps. First, regardless of the way the ramp generator is implemented, its outputs must be buffered in order to drive the capacitive load presented by a large number of comparators. Since the number of comparators connected to each ramp is signal-dependent,

each buffer has to be dimensioned for the worst-case situation where it has to drive all the comparators. Therefore, there is a trade-off between the increased speed obtained by using a large number of ramps, and the increased power dissipation of using many ramp buffers.

A second limitation stems from the fact that if each of the *m* ramps only spans *1/m* of the input range, errors in the coarse conversion phase may result in the comparator being connected to the wrong ramp during the fine conversion phase, resulting in dead bands in the final digital output. This problem can be solved by creating some overlap between the different ramps. Subsequently, the digital outputs stored in the coarse and fine memory can be correctly combined with some simple digital processing. The amount of overlap required between successive ramps depends on the expected errors in the coarse conversion phase. Therefore, increasing the number of ramps means that a larger portion of the voltage span of each ramp will be lost in overlap.

In [10], the first prototype imager that uses a column-level MRSS ADC is presented. Using 8 ramps, this prototype achieves a reduction in A/D conversion time of 3.1x compared to a single-slope ADC while only requiring 16% more power. This result underlines the potential of the MRSS ADC to increase conversion speed and thus increase power efficiency in a column-level ADC.

IV. MRMS ADC ARCHITECTURE

A further reduction in conversion time can be achieved by exploiting the presence of photon shot noise in imager signals [11][12]. This is illustrated in fig. 4 and 5. While most noise sources are constant, photon shot noise increase proportional to the square root of the signal, and dominates for higher input signals. Since the quantization noise of the ADC is usually optimized for low-input signals, this means that the ADC essentially *overperforms* for higher input
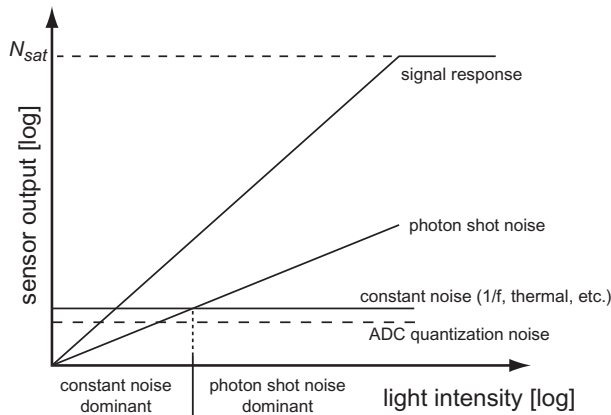
Figure 4. Conceptual logarithmic plot of the sensor's response to light and corresponding noise sources

Figure 5. Exploitation of photon shot noise in an imager ADC, by increasing the quantization step in binary fashion

signals. Therefore, the quantization noise, and thus the quantization step can be increased without reducing the perceived image quality. This can for instance be done by increasing the quantization step in binary fashion (fig. 5), which facilitates the reconstruction of a linear digital code at the ADC output.

In an MRSS ADC, this concept can be implemented by increasing the slopes of some of the ramps, as illustrated in fig. 3c. Since the quantization step in an MRSS ADC is defined by the increase in ramp voltage per clock period, this effectively increases the quantization step. Since the ramps are now running at different slopes, the resulting ADC is called a *Multiple-Ramp Multiple-Slope ADC*. The actual decrease in conversion time depends on three factors: the initial resolution of the ADC, the saturation charge of the pixel, since this determines the relative amount of photon shot noise, and the ratio between photon shot noise and quantization noise that is allowed by the designer. However, published implementations of this concept in a single-slope ADC [11][12] suggest that the reduction can be quite substantial.

V. CONCLUSION

The column-parallel single-slope ADC architecture has evolved in the last years as the preferred solution for increasing the total readout speed of CMOS imagers. The architecture requires only a very simple analog comparator for each ADC channel, reducing chip area, power consumption and uniformity problems. However, it has an important disadvantage of a slow conversion speed. The recently introduced MRSS ADC solves this problem, and can significantly increase the power efficiency of a column-level ADC. A further reduction in conversion time can be made by exploiting the presence of photon shot noise in imager signals, leading to a MRMS ADC.
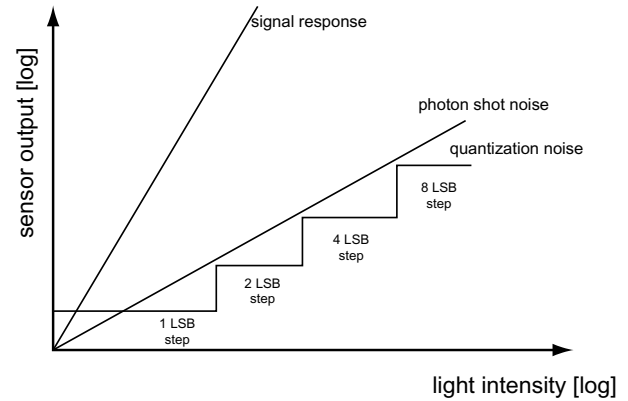
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