15.7 A 2.4-to-5.2fJ/conversion-step 10b 0.5-to-4MS/s SAR ADC with Charge-Average Switching DAC in 90nm CMOS

Chang-Yuan Liou, Chih-Cheng Hsieh

National Tsing Hua University, Hsinchu, Taiwan

Applications of wireless sensor networks and biomedical devices frequently require an ADC with medium resolution (8 to 12b) running at hundreds of kS/s to a few MS/s. Successive-approximation register (SAR) ADCs show convincing performance with inherent low-power operation and high efficiency. DAC switching energy and SAR control logic are the main power-hungry blocks in ADC designs, and this attracts much research interest [1-6]. Set-and-down [1-3], step-wise [4], merged capacitor [5], and input-range-prediction [6] show improved switching-energy efficiency with design penalties such as common-mode shift, extra auxiliary capacitors, extra voltage reference (V_{cm}), and an extra conversion step, respectively. Reducing power with a smaller unit capacitance requires extra calibration to meet accuracy requirements [2-3]. Without the aforementioned drawbacks, this work presents a SAR ADC with FoM performance as low as 2.4fJ/conv-step, and a variable sampling rate optimized by adequately scaling the supply.

In this paper, a 10b 0.5-to-4MS/s asynchronous SAR ADC is proposed and prototyped in 90nm CMOS. The supply voltage is scaled down appropriately (0.4 to 0.7V) for different speeds to minimize power consumption of SAR control and switching energy. Moreover, a charge average switching (CAS) DAC is developed to reduce the switching energy of the DAC without an extra voltage reference and common-mode shift. In near-threshold operation with a scaled-down supply, a double-boosted sample-and-hold (S/H) circuit and a local-boosted switch are implemented for the linearity and accuracy requirements of the 10b ADC.

Figure 15.7.1 shows a circuit diagram of the implemented SAR ADC. It is composed of S/H circuits, 9b DAC arrays, 9b SAR control units, and 5b CAS control units in fully differential form. Top-plate sampling without the MSB capacitor (512C) implementation effectively reduces power and improves speed. For 0.4-to-0.7V operation, a double-boosted S/H design is implemented to achieve a sampling linearity of 11.3-to-12.7b (at Nyquist-rate input) compared to 7.1-to-9.9b for a conventional single-boosted implementation.

The main idea of a CAS DAC is to generate the necessary top-plate voltage shift by charge averaging between the bottom plates of PDAC and NDAC instead of a conventional charging (or discharging) operation. The charge-averaging function is achieved by disabling the switching path from the SAR (by TG_N), and enabling equalization switches from CAS control (by CA_N). In near-threshold operation, the increased turn-on resistance of the equalization switch degrades the speed and accuracy of the charge-averaging operation. Local-boosted control signal generators are implemented for CA_N to guarantee a completed averaging function without loss.

Figure 15.7.2 shows the proposed CAS DAC with a 4b conversion example. During the top-plate sampling phase, the capacitor array of each bit is split into two equal parts (PDAC-H/PDAC-L and NDAC-H/NDAC-L) with different bottom-plate reset levels as V_{ref} and GND, respectively. Since the conversion process is symmetrical at $V_{ip}=V_{in}$, only the $V_{ip}>V_{in}$ condition is illustrated for simplicity. After comparison of input signals on top plates and output MSB = 1, the bottom plates of 2C in PDAC-H and NDAC-L are switched from V_{ref} to GND and GND to V_{ref} simultaneously to generate a $-1/2\ V_{ref}$ shift on top plates. If $V_{ip}-V_{in}<V_{ref}/2$ (MSB-1=0), the subsequent necessary $-1/4\ V_{ref}$ shift on top plates is achieved by connecting the bottom plates of 2C in PDAC-L and NDAC-H through equalization switch turned on by CA_N. The necessary voltage shift ($\pm 1/8\ V_{ref}$) of the following conversion steps (MSB-2) can be all achieved using the CAS operation. This 4b example demonstrates that the DAC switching energy is reduced by 36.2% by enabling the CAS operation instead of switching to a rail in the conversion process.

Figure 15.7.3 shows the CAS switching procedure and resulting switching energy savings. For a 10b SAR ADC with a top-sampling implementation, there are a total of 9 conversion steps. Although the CAS operation can be applied to every DAC bit, the gained efficiency is decreased at lower bits because of the smaller capacitance and the necessary power penalty of the local-boosted circuit. In this design, CAS is applied to the most-significant 5b and activated at conversion steps 2 to 6. The resulting power penalty from additional control and local-boosted circuits is below 3% of the total power consumption of the implemented ADC.

The total numbers (PDAC and NDAC) of switching capacitor (in white) and charge averaging capacitor (in grey) in each conversion step with different input range are illustrated in Fig. 15.7.3. The switching energy curve in conversion phase versus output code shows the power-reduction behavior of the CAS technique. The average energy numbers of well-known techniques in conversion phase are calculated and listed with the differential DAC implementation. Compared to set-and-down [1-3] (255.5 CV_{ref}^2) and MCS [5] (170 CV_{ref}^2) techniques without reset energy, the CAS consumes less energy (88.6 CV_{ref}^2) at the conversion phase with a cost of reset energy (255.5 CV_{ref}^2) at the sampling phase. In low-supply-voltage operation, the required boosted control for reference voltage (V_{cm}) switching of MCS, and the common-mode shift issue of set-and-down, degrade the energy efficiency and linearity, respectively. Moreover, the reduced high-speed charging/discharging operations of CAS in the conversion phase benefit the low dynamic/short-circuit power consumption with smaller switches, the minimized supply disturbance, and the resulting FoM at low-supply operation.

A test chip is fabricated in 90nm CMOS and occupies a core area of 0.0418mm^2 (110×380μm^2). A metal-oxide-metal (MOM) unit capacitor of 5fF is chosen for matching and noise considerations. Based on a tradeoff of power and speed, instead of optimization at variable resolution [3], this ADC achieves a constant resolution of 10b for a variable sampling rate (0.5 to 4MS/s) operated at an adequately scaled supply (0.4 to 0.7V).

Figure 15.7.4 shows the spectrum at Nyquist-rate input with a sampling rate of 0.5 to 4MS/s. The measured SNDR at 0.5MS/s, 1.25MS/s, 2.5MS/s, and 4MS/s are 54.3dB, 55.6dB, 56.2dB, and 56.3dB, respectively. The resulting ENOBs for 0.5 to 4MS/s are 8.72 to 9.05b with a power consumption of 0.5 to 11μW.

Figure 15.7.5 shows the static performance at 0.5MS/s and ENOB versus input frequency. The peak DNL and INL are +0.3/–0.34 LSB and +0.2/–0.51 LSB, respectively. With a wide sampling rate of 0.5 to 4MS/s and corresponding supply of 0.4 to 0.7V, the measured results show a consistent ENOB performance with input frequency ranging from static to Nyquist-rate.

The performance summary and comparison table is shown in Fig. 15.7.6. With the proposed CAS techniques and corresponding design for scaled-down supply operation, the implemented 10b ADC achieves an FoM of 2.4fJ/conv-step at 0.5MS/s and 0.4V supply. For 10b applications with a wide sampling frequency range of 0.5 to 4MS/s, the resulting FoMs range from 2.4 to 5.2fJ/conv-step.

Acknowledgements:
The authors acknowledge the support of National Chip Implementation Center (CIC), Taiwan and Signal Sensing and Application Laboratory (SiSAL), EECS, National Tsing Hua University.

References:
[1] H.-Y. Tai, *et al.*, "A 3.2fJ/c.-s. 0.35V 10b 100KS/s SAR ADC in 90nm CMOS," *IEEE Symp. VLSI Circuits*, pp. 92-93, June 2012.
[2] A. Shikata, *et al.*, "A 0.5 V 1.1MS/sec 6.3fJ/Conversion-Step SAR-ADC with Tri-Level Comparator in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 1022-1030, Apr. 2012.
[3] P. Harpe, *et al.*, "A 7-to-10b 0-to-4MS/s Flexible SAR ADC with 6.5-to-16fJ/conversion-step," *ISSCC Dig. Tech. Papers*, pp. 472-474, Feb. 2012.
[4] M. van Elzakker, *et al.*, "A 10-bit Charge-Redistribution ADC Consuming 1.9μW at 1MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1007-1015, May 2010.
[5] V. Hariprasath, *et al.*, "Merged Capacitor Switching Based SAR ADC with Highest Switching Energy-Efficiency," *IET Electronics Letters*, Apr. 2010.
[6] H.-Y. Huang, *et al.*, "A 9.2b 47fJ/Conversion-step Asynchronous SAR ADC with Input Range Prediction DAC Switching," *IEEE ISCAS*, pp. 2353-2356, May 2012.

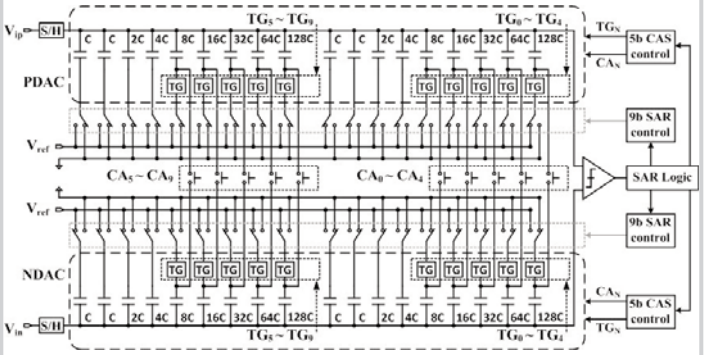


Figure 15.7.1: Circuit diagram of proposed SAR ADC.

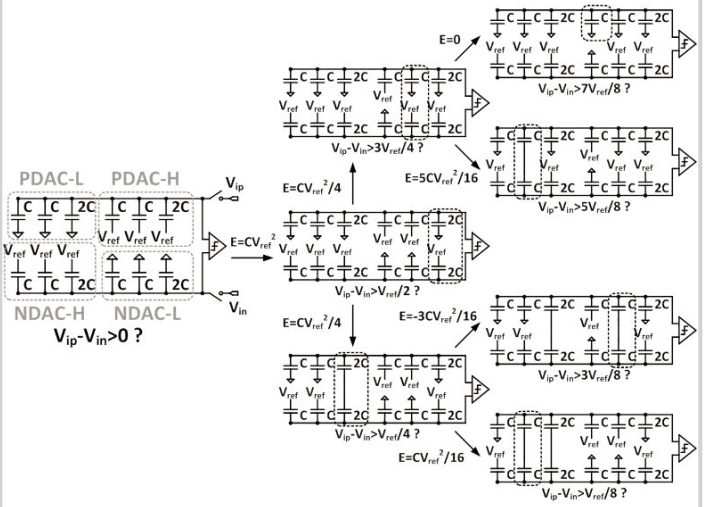
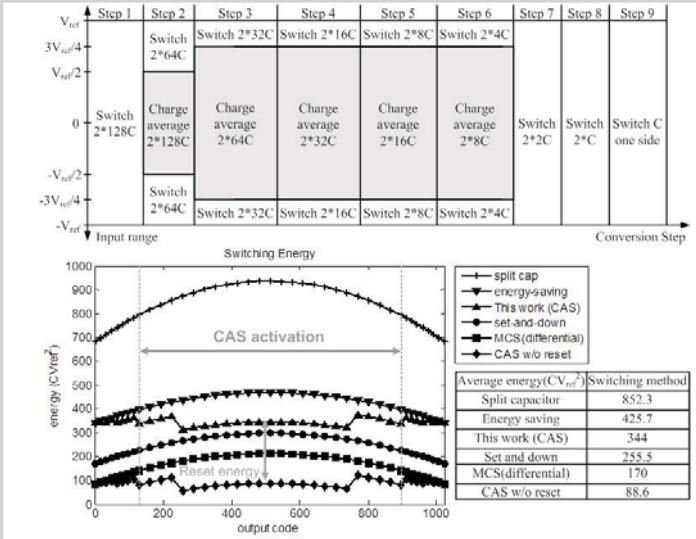


Figure 15.7.2: A 4b conversion example of the CAS DAC switching method.



Average energy(CV_{ref}^2)	Switching method
Split capacitor	852.3
Energy saving	425.7
This work (CAS)	344
Set and down	255.5
MCS(differential)	170
CAS w/o reset	88.6

Figure 15.7.3: DAC switching procedure and switching energy versus output code.

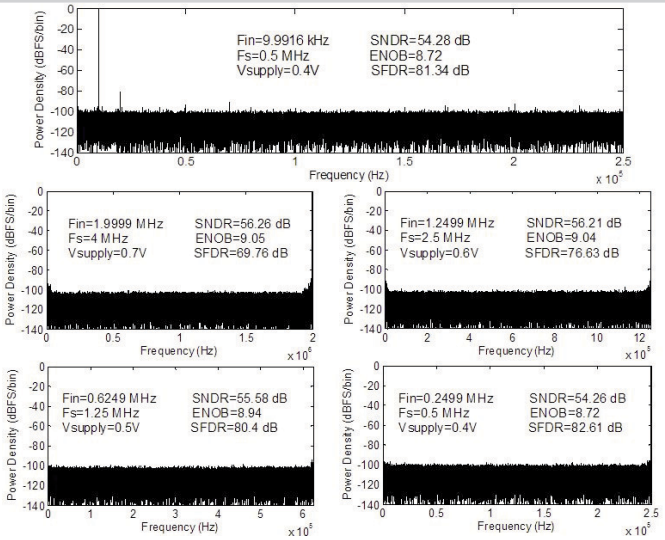


Figure 15.7.4: Measured spectrum and SNDR/SFDR of 10k input at 0.5MS/s (0.4V) and Nyquist-rate input at 0.5MS/s (0.4V) to 4MS/s (0.7V).

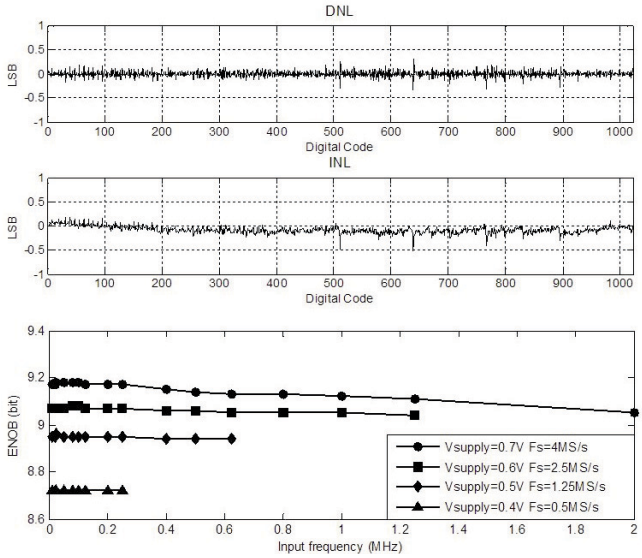


Figure 15.7.5: DNL, INL and ENOB versus input frequency at 0.5 to 4MS/s.

	[1] Tai (Symp. on VLSI-2012)	[4] Elzakker (JSSC-2010)	[2] Shikata (JSSC-2012)	[3] Harpe (ISSCC-2012)	This work			
Technology	90nm	65nm	40nm	90nm	90nm			
Area(mm^2)	0.03	0.026	0.011	0.047	0.042			
Supply voltage(V)	0.35	1	0.5	1.1	0.4	0.5	0.6	0.7
Sampling rate(MS/s)	0.1	1	1.1	4	0.5	1.25	2.5	4
Resolution(bit)	10	10	8	10	10			
Diff. input range(V_{pp})	-	2	-	1.36	0.78	0.98	1.18	1.37
DAC unit capacitor(fF)	-	1	0.5	0.6	5			
DAC Calibration	-	-	Yes	Yes	No			
DNL(LSB)	0.3	0.5	1.4	0.27	0.34			
INL(LSB)	0.6	2.2	1.1	0.42	0.62			
SNDR(dB)@Nyquist	56.3	54.4	46.8	56	54.3	55.6	56.2	56.3
ENOB(bit)@Nyquist	9.06	8.75	7.5	9.01	8.72	8.94	9.04	9.05
Power (μW)	0.17	1.9	1.2	17.44	0.5	1.8	5	11
FOM(fJ/conv.-step) @Nyquist	3.2	4.4	6.3	8.45	2.37	2.93	3.8	5.2

Figure 15.7.6: Performance summary and comparison table.

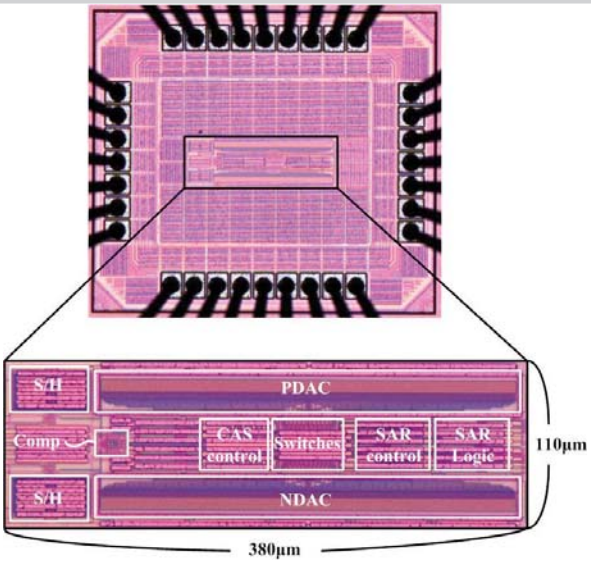


Figure 15.7.7: Die photo of the SAR ADC.

978-1-4673-4516-3/13/$31.00