A 0.3 V 10-bit 1.17 f SAR ADC With Merge and Split Switching in 90 nm CMOS

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***Abstract*—This paper presents a 10-bit ultra-low voltage energy-efficient SAR ADC. The proposed merge-and-split (MS) switching effectively reduces DAC switching energy by 83% compared with conventional one without the need of extra reference voltage (V_{cm}) and the issue of common-mode voltage variation. To maintain good input linearity, a new double-bootstrapped sample-and-hold (S/H) circuit is proposed under an ultra-low voltage of 0.3 V. In addition, by employing asymmetric logic in SAR control, the leakage power is reduced with the penalty of slight conversion speed degradation. The test chip fabricated in 90 nm CMOS occupied a core area of 0.03 mm^2. With a single 0.3 V supply and a Nyquist rate input, the prototype consumes 35 nW at 90 kS/s and achieves an ENOB of 8.38 bit and a SFDR of 78.2 dB, respectively. The operation frequency is scalable up to 2 MS/s and power supply range from 0.3 V to 0.5 V. The resultant FOMs are 1.17-to-1.78 fJ/conv.-step.**

***Index Terms*—Low power, low voltage, SAR ADC.**

I. Introduction

IN THE PAST FEW years, with the advancement of large-scale integrated circuits, there has been a growing interest in the design of wireless sensor network for implantable, portable, and wearable applications. These sensing devices are generally used for detecting and monitoring biomedical or environmental signals such as electrocardiographic (ECG), electroencephalography (EEG), electromyography (EMG), temperature, humidity, sound, and so on. In the sensor nodes, the power should be supplied by energy harvesting technologies to reduce the maintenance cost for battery replacement. Most of the small size energy harvesting devices, such as solar cells, can generate extremely low output voltage, and limited power. Therefore, ultralow-voltage and low-power operation is inevitable for wireless sensor nodes.

The sensed signals are usually digitized by ADCs with moderate resolution (8–12 bits) and sampling rate (1–1000 kS/s). In these applications, ADCs are the most critical and power hungry blocks. Among various ADC architectures, successive approximation register (SAR) ADC shows a better power efficiency. Furthermore, SAR ADC benefits from technology downscaling because of two major reasons: 1) SAR ADC mainly consists of digital circuits which get faster in advanced technologies, and is compatible with digital processors; and 2) SAR ADC is an opamp-free architecture. In other words, SAR ADC does not require high gain and high bandwidth opamps, which consume large static power, and suffer from short channel effect and low supply voltage in advanced process. These reasons arouse many researches on exploring SAR ADC in depth.

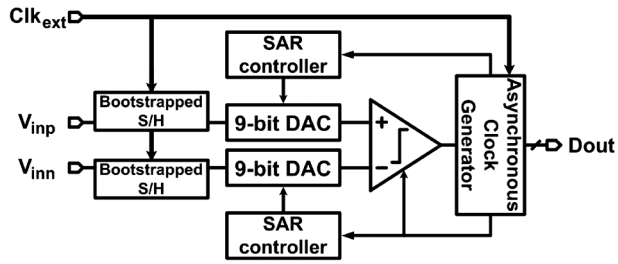

Fig. 1. Common 10-bit asynchronous SAR ADC.

Power consumption in a SAR ADC mainly lies in the DAC network, the comparator, and the SAR control logics, and the leakage current needs to be carefully manipulated as well. Many researches have shown interests in reducing DAC switching power [1]–[5]. Compared to the conventional switching sequence, the energy-saving [1], charge average switching (CAS) [2], set-and-down [3], V_{cm}-based [4], and, partial floating [5] switching sequences reduce switching energy by 69%, 74.8%, 81%, 90%, and 94%, respectively. To reduce comparator noise, data-driven noise reduction [6] and majority vote comparison [7] are proposed. With respect to digital circuit, reducing supply voltage and employing advanced technology is beneficial [1], [2], [6]–[14]. However, analog circuits become challenging in low supply operation due to the reduced signal swing and barely turn-on resistance of MOS switch. In addition, by carefully selecting transistor size and threshold voltage, one could minimize the overall power consumption with the design trade-off between speed (dynamic power consumption) and leakage current (static power consumption).

This brief aims at enhancing SAR ADC power efficiency by pushing down the supply voltage to 0.3 V and proposing low-voltage design techniques. For low voltage design, the simplest SAR architecture is preferred and employed in this work, as shown in Fig. 1. Asynchronous clocking helps frequency scaling because only one external sampling clock (Clk_{ext}) is required. To overcome the nonlinearity degraded by weakly turn-on switch, a new advanced double-boosted sample-and-hold (S/H) is proposed. In addition, a merge-and-split (MS) switching DAC without common-mode voltage shift is developed to reduce the switching energy of DAC network by 83% compared to conventional one. Considering leakage current, asymmetric logics and multi-threshold MOS devices are employed for the optimal SAR control logics with trade-off of speed and leakage power.

Manuscript received April 28, 2014; revised July 14, 2014 and August 04, 2014; accepted August 06, 2014. This research is particularly supported by National Science Council, Taiwan under Contract NSC 102-2221-E-007-132 and 102-2220-E-007-008. This paper was recommended by Associate Editor A. M. A. Ali.

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Digital Object Identifier 10.1109/TCSI.2014.2349571

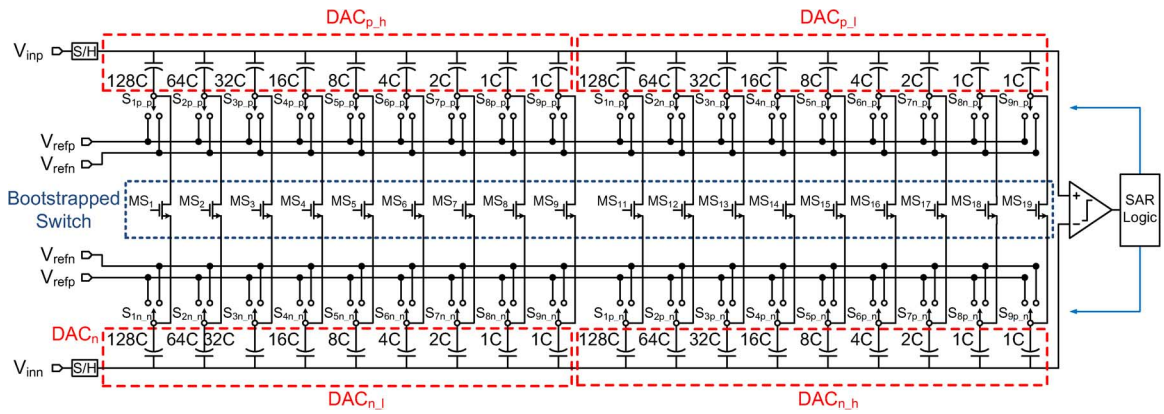

Fig. 2. Block diagram of the proposed 10-bit asynchronous SAR ADC.

The paper is organized as follows. Section II introduces the MS switching method, and Section III describes the design and implementation of the SAR ADC. Measurement results are shown in Section IV and conclusions are given in Section V.

II. Proposed ADC Architecture

Fig. 2 shows the schematic of the proposed 10-bit asynchronous SAR ADC. To suppress supply voltage noise and have good common-mode noise rejection, the fully differential architecture is employed. The DAC array is used as sampling capacitor and its MSB capacitor is split into sub-arrays. Thus, the DAC array is composed of two identical sub-DAC arrays called $\mathrm{DAC_{p(n)\_h}}$ and $\mathrm{DAC_{p(n)\_l}}$, which are connected to $\mathrm{V_{refp}}$ and $\mathrm{V_{refn}}$ at sampling phase, respectively. By doing so, the two DAC arrays can be switched on the opposite side, and maintain constant common-mode voltage at conversion phase. In addition, local boosted switches ($\mathrm{MS_x}$, x = 1–9,11–19) are implemented for MS switching, and only two reference voltages of $\mathrm{V_{refp}}$ (VDD) and $\mathrm{V_{refn}}$ (gnd) are required.

Fig. 3(a) shows CAS DAC switching [2] with a 4-bit example. Since the implementation is symmetrical, only the $\mathrm{V_{inp}} > \mathrm{V_{inn}}$ condition is illustrated for simplicity. During the sampling phase, the input signals are sampled onto the top plates of DAC, while $\mathrm{DAC_{p\_h}}$ and $\mathrm{DAC_{n\_h}}$ are reset to $\mathrm{V_{ref}}$ and $\mathrm{DAC_{p\_l}}$ and $\mathrm{DAC_{n\_l}}$ are reset to 0. After the sampling phase, the comparator makes first decision directly without switching any capacitor, and the result is MSB = 1 (for $\mathrm{V_{inp}} > \mathrm{V_{inn}}$). Then, the 2C of $\mathrm{DAC_{p\_h}}$ and $\mathrm{DAC_{n\_l}}$ are switched to 0 and $\mathrm{V_{ref}}$ to generate a $-1/2$ $\mathrm{V_{ref}}$ shift on top plates. If $\mathrm{V_{inp}} - \mathrm{V_{inn}} > \mathrm{V_{ref}}/2$ (MSB − 1 = 1), the necessary $-1/4$ $\mathrm{V_{ref}}$ shift on top plates is accomplished by switching the 1C of $\mathrm{DAC_{p\_h}}$ and $\mathrm{DAC_{n\_l}}$ to 0 and $\mathrm{V_{ref}}$, respectively. Nevertheless, If $\mathrm{V_{inp}} - \mathrm{V_{inn}} < \mathrm{V_{ref}}/2$ (MSB − 1 = 0), the required 1/4 $\mathrm{V_{ref}}$ shift on top plates is accomplished by merging the 2C in $\mathrm{DAC_{p\_l}}$ and $\mathrm{DAC_{n\_h}}$. The same procedure is conducted until the last bit is finished.

Fig. 3(b) shows the proposed MS DAC switching with a 4-bit example. During the sampling phase, the input signals are sampled onto the top plates of DAC, while $\mathrm{DAC_{p\_h}}$ and $\mathrm{DAC_{n\_h}}$ are reset to $\mathrm{V_{ref}}$ and $\mathrm{DAC_{p\_l}}$ and $\mathrm{DAC_{n\_l}}$ are reset to 0. Next, the comparator makes first decision directly, and the result is MSB = 1 (for $\mathrm{V_{inp}} > \mathrm{V_{inn}}$). Then, all the capacitors of $\mathrm{DAC_{p\_h}}$ and $\mathrm{DAC_{n\_l}}$ are merged to generate a $-1/2$ $\mathrm{V_{ref}}$ shift on top plates. If $\mathrm{V_{inp}} - \mathrm{V_{inn}} > \mathrm{V_{ref}}/2$ (MSB − 1 = 1), the necessary $-1/4$ $\mathrm{V_{ref}}$ shift on top plates is accomplished by splitting the 2C in $\mathrm{DAC_{p\_h}}$ and $\mathrm{DAC_{n\_l}}$ and switching them to 0 and $\mathrm{V_{ref}}$, respectively. Nevertheless, If $\mathrm{V_{inp}} - \mathrm{V_{inn}} < \mathrm{V_{ref}}/2$ (MSB − 1 = 0), the required 1/4 $\mathrm{V_{ref}}$ shift on top plates is accomplished by merging the 2C in $\mathrm{DAC_{p\_l}}$ and $\mathrm{DAC_{n\_h}}$. The same procedure is conducted until the last bit is resolved.

The quantitative energy consumption of CAS and MS methods in each switching step is also shown in the Fig. 3. In the most energy-wasting switching (first step switching), the MS switching applies merging operation instead of switching the 2C to $\mathrm{V_{ref}}$ and 0, respectively, and the energy consumption is $-\mathrm{CV_{ref}^2}$ instead of $\mathrm{CV_{ref}^2}$. In the following switching step, either the merging operation or the new introduced splitting operation is employed to accomplish successive approximation.

For an n-bit SAR ADC, if the probability of each digital output code is equal, the average switching energy of conventional [3], CAS [2], monotonic [3], $\mathrm{V_{cm}}$-based [4] methods can be derived as

$$E_{avg,conv} = \sum_{i=1}^{n} 2^{n+1-2i}(2^i - 1)CV_{ref}^2 \quad (1)$$

$$E_{avg,CAS} = \sum_{i=1}^{n-1} (2^{n-2-2i})CV_{ref}^2 \quad (2)$$

$$E_{avg,mono} = \sum_{i=1}^{n-1} (2^{n-2-i})CV_{ref}^2 \quad (3)$$

$$E_{avg,V_{cm}} = \sum_{i=1}^{n-1} 2^{n-2-2i}(2^i - 1)CV_{ref}^2 \quad (4)$$

The average switching energy for an n-bit SAR ADC using the proposed MS switching procedure can be derived as

$$E_{avg,MS} = -2^{n-4}CV_{ref}^2 + \sum_{i=2}^{n-1} 2^{n-i-3}(1-2^{-i+1})CV_{ref}^2 \quad (5)$$

However, the CAS and MS switching consume reset energy, which can be derived as

$$E_{reset} = (2^{n-2} - 2^{-1})CV_{ref}^2 \quad (6)$$

For a 10-bit case, the CAS, set-and-down, and $\mathrm{V_{cm}}$-based switching procedures consume 88.6, 255.5 and 170.2 $\mathrm{CV_{ref}^2}$, respectively, while the proposed MS switching procedure consumes only -21.6 $\mathrm{CV_{ref}^2}$. Although the CAS and MS switching methods consume less energy than the monotonic and $\mathrm{V_{cm}}$-based switching methods during the conversion phase, they must be pre-charged at the sampling phase and consume reset energy, which is 255.5 $\mathrm{CV_{ref}^2}$. Fig. 4 shows the

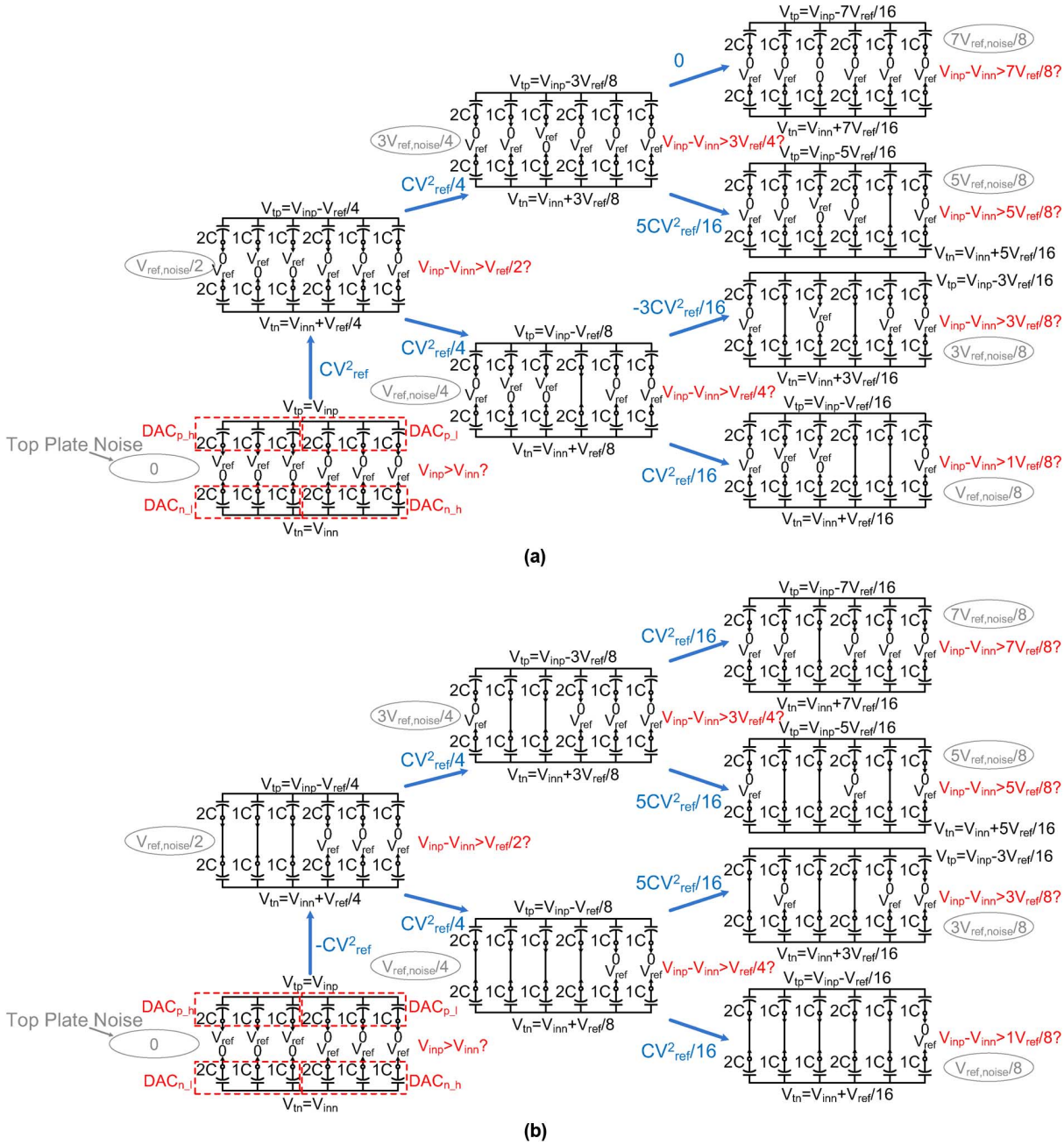

Fig. 3. (a) A 4-bit conversion example of the CAS DAC switching method. (b) A 4-bit conversion example of the proposed MS DAC switching method.

switching energy curves versus output code of MS switching and the other well-known techniques including both sampling and conversion phase and Table I summarizes the features. Compared to set-and-down (255.5 CV^2_{ref}) and CAS (344.1 CV^2_{ref}) techniques, MS (233.9 CV^2_{ref}) switching consumes 8.5% and 32% less energy, respectively. It also solves the common-mode voltage variation issue of set-and-down and hence obviates the distortion at conversion phase. Although V_{cm}-based switching (170.2 CV^2_{ref}) is the most energy-efficient among all techniques, realizing the required extra reference voltage (V_{cm}) at 0.3 V is arduous. Considering the required unit capacitors, MS switching is the same as the other methods and is half of the conventional one.

Assuming the bottom-plate voltage of the being switched capacitor (C_k) on the p-side is V_{pk} and the one on the n-side is V_{nk}, as shown in Fig. 5(a). After merging operation, assuming

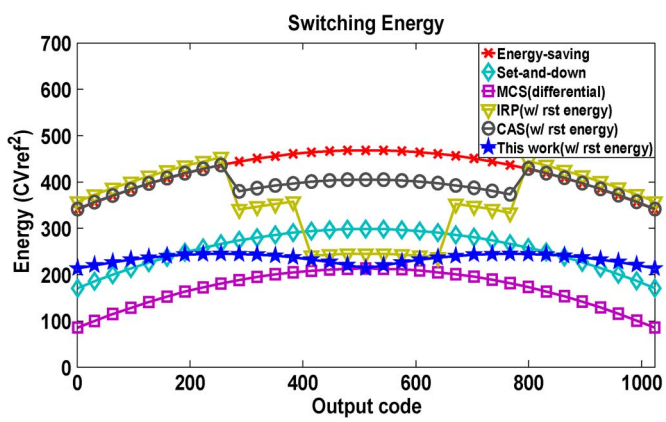

Fig. 4. Switching energy versus output code.

TABLE I
COMPARISON OF DIFFERENT SWITCHING PROCEDURES

Switching procedure	conven tional	set-and -down	V_{cm}-based	CAS	This work
Conversion Energy (CV_{ref}^2)	1365.3	255.5	170.2	88.6	-21.6
Reset Energy (CV_{ref}^2)	0	0	0	255.5	255.5
Total Switching Energy (CV_{ref}^2)	1365.3	255.5	170.2	344.1	233.9
Common-mode Voltage Variation	0	$\frac{V_{ref}}{2}$	0	$\frac{V_{ref}}{1024}$	0
Extra Reference Voltage	No	No	Yes	No	No
No. of Unit capacitors in Capacitor Array	2^n	2^{n-1}	2^{n-1}	2^{n-1}	2^{n-1}

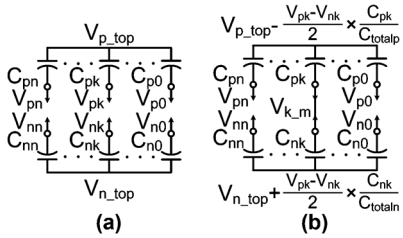

Fig. 5. DAC switching voltage (a) before merging operation. (b) After merging operation.

the capacitor C_{totalp} is equal to C_{totaln}, the voltages on both side then can be calculated as

$$V'_{p(n)\_top} = V_{p(n)\_top} \pm \frac{V_{pk} - V_{nk}}{2} \times \frac{C_{p(n)k}}{C_{totalp(n)}} \tag{7}$$

, where $C_{totalp(n)}$ is the sum of total capacitors ($C_{p(n)0} + C_{p(n)1} + \ldots + C_{p(n)n}$). Hence, the voltage change on top plates is

$$\Delta V_{top} = (V_{pk} - V_{nk}) \times \frac{C_k}{C_{total}} \tag{8}$$

Considering the V_{ref} noise, assuming the V_{pk} is disturbed by noise and becomes $V_{pk} + \Delta V_{noise}$ before merging operation, then the merged voltage (V_{k_m}) would have $\Delta V_{noise}/2$ shift from ideal value, making the comparator input common-mode voltage shift of

$$\Delta V_{\mathrm{comp,common-mode}} = \frac{\Delta V_{noise}}{2} \times \frac{C_k}{C_{total}} \tag{9}$$

However, the voltage change on top plates is still the same as ideal case. That is, the reference voltage variation only causes input common-mode voltage variation during merging operation. Then considering the splitting operation, the V_{k_m} is splitting first and the V_{pk} and V_{nk} are connected to constant voltages, respectively [return to Fig. 5(a)]. The common-mode voltage shift caused by merging operation is erased and becomes the same as the condition before merging operation. In addition, to reduce comparator input common-mode voltage variation, the switch sizes of C_k on both sides are designed the same to cancel out the charge-injection and clock feedthrough effects.

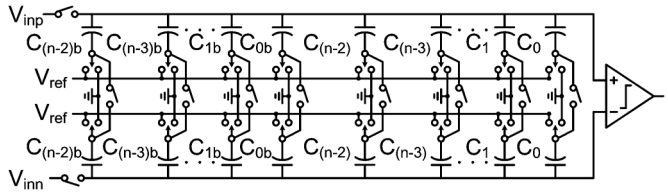

Fig. 6. DAC array of the proposed MS switching.

During comparison phase, the V_{ref} noise would couple to the comparator input via DAC array and the mount depends on the number of capacitors connected to V_{ref}. Therefore, different switching sequence would induce different noise profile. Taking the proposed MS switching as an example, at first comparison the V_{ref} noise on the top plates is 0, because the noises on p-side and n-side are common-mode and canceled out, as shown in Fig. 3(b). At second comparison, if $V_{inp} - V_{inn} > V_{ref}/2$ ($MSB-1=1$), the V_{ref} noise on the top plates is $3V_{ref,noise}/4$. Nevertheless, if $V_{inp} - V_{inn} < V_{ref}/2$ ($MSB-1=0$), the V_{ref} noise on the top plates becomes $V_{ref,noise}/4$. However, by carefully examining the switching sequence of CAS and MS techniques, as shown in Fig. 3, each switching step has the same V_{ref} noise. This is true for V_{cm}-base and monotonic as well. Hence, the linearity degradation due to V_{ref} noise is the same for all these switching methods.

Besides the V_{ref} noise, the mismatch of capacitive DAC array is a main error source which deteriorates ADC linearity. For matching concerns, a large capacitor in the DAC array is usually composed of multiple identical unit capacitors. Due to process variation, the practical capacitance of each unit capacitor deviates from the nominal value. Suppose the unit capacitor is modeled with a nominal value of C_u and a standard deviation of σ_u. Therefore, for n-bit ADC with MS switching, the capacitance of each capacitor, shown in Fig. 6 can be expressed as:

$$\begin{aligned} C_i &= 2^{i-1}C_u + \delta_i (i = 1 \sim n-2) \\ C_{ib} &= 2^{i-1}C_u + \delta_{ib} (i = 1 \sim n-2) \\ C_0 &= C_u + \delta_0 \\ C_{0b} &= C_u + \delta_{0b} \end{aligned} \tag{10}$$

where i is an integer representing the bit position, C_u is the unit capacitance and δ_i is the error term. Assuming that the error distributions of unit capacitors are independent and identically distributed (i.i.d.) Gaussian random variables, the mean and variance of the error terms are

$$\begin{aligned} &\mathrm{E}[\delta_i] = \mathrm{E}[\delta_{ib}] = 0, \mathrm{E}\left[\delta_0^2\right] = \mathrm{E}\left[\delta_{0b}^2\right] = \mathrm{E}\left[\delta_1^2\right] = \mathrm{E}\left[\delta_{1b}^2\right] = \sigma_u^2, \\ &\mathrm{E}\left[\delta_i^2\right] = \mathrm{E}\left[\delta_{ib}^2\right] = 2^{i-1}\sigma_u^2 \end{aligned} \tag{11}$$

The differential input voltage of the comparator before it makes the last decision (i.e., all bits are decided except the LSB) can be expressed as

$$\Delta V_{in}(y) = V_{in} - \frac{S_n \sum_{i=0}^{n-2} C_{ib} - \overline{S_n} \sum_{i=0}^{n-2} C_i + \sum_{i=1}^{n-2} S_{i+1} C_{ib} - \sum_{i=1}^{n-2} \overline{S_{i+1}} C_i}{\sum_{i=0}^{n-2} C_{ib} + \sum_{i=0}^{n-2} C_i} \times V_{ref} \tag{12}$$

where y $= [\mathrm{S_n} \ldots \mathrm{S_1}]$ is the digital estimation, $\mathrm{S_n}$ represents the comparator decision for the nth bit ($\mathrm{S_n} = 0$ or 1), $\mathrm{V_{in}}$ is the input signal difference, and $\mathrm{V_{ref}}$ is the reference voltage. Subtracting the nominal value yields the error INL

$$INL(y) = \frac{V_{error}(y)}{LSB} = \frac{\frac{S_n \sum_{i=0}^{n-2} \delta_{ib} - \overline{S_n} \sum_{i=0}^{n-2} \delta_i + \sum_{i=1}^{n-2} S_{i+1}\delta_{ib} - \sum_{i=1}^{n-2} \overline{S_{i+1}}\delta_i}{\sum_{i=0}^{n-2} C_{ib} + \sum_{i=0}^{n-2} C_i} \times V_{ref}}{LSB} \tag{13}$$

with variance

$$E\left[V_{error}^2(y)\right] = \sum \left[\frac{S_n \sum_{i=0}^{n-2} \delta_{ib}^2 - \overline{S_n} \sum_{i=0}^{n-2} \delta_i^2 + \sum_{i=1}^{n-2} S_{i+1}\delta_{ib}^2 - \sum_{i=1}^{n-2} \overline{S_{i+1}}\delta_i^2}{2^{2n-2}C_u^2} \times V_{ref}^2 \right] \tag{14}$$

For the proposed MS switching procedure, MSB is determined mismatch-independently (INL $= 0$), and worst cases INL occur at the VFS/4 and 3 VFS/4, where VFS means the full scale signal. At these two transitions, the most capacitors are switched. Therefore, the variance of maximum INL error is derived as

$$\begin{aligned}
\sigma_{INL,\max}^2 &= E\left[\frac{\sum_{i=0}^{n-2} \delta_i^2 + \delta_{n-2}^2 + \sum_{i=1}^{n-3} \delta_{ib}^2}{2^{2n-2}C_u^2} \times V_{ref}^2 \right] \\
&= \frac{E\left(\sum_{i=0}^{n-3} \delta_i^2\right) + E\left(4\delta_{n-2}^2\right) + E\left(\sum_{i=1}^{n-3} \delta_{ib}^2\right)}{2^{2n-2}C_u^2} \times V_{ref}^2 \\
&= \frac{\left(3 \times 2^{n-2} - 1\right)\sigma_u^2}{2^{2n-2}C_u^2} \times V_{ref}^2 \\
&\cong \frac{3 \times 2^{n-2}\sigma_u^2}{2^{2n-2}C_u^2} \times V_{ref}^2 = \frac{3\sigma_u^2}{2^n C_u^2} \times V_{ref}^2
\end{aligned} \tag{15}$$

Therefore, the maximum INL of MS switching is

$$\sigma_{INL,\max} = \frac{\sqrt{3 \times 2^{n-2}}\sigma_u}{C_u} \tag{16}$$

The DNL is the difference of two adjacent codes expressed as

$$DNL(y) = \frac{V_{error}(y) - V_{error}(y-1)}{LSB} \tag{17}$$

The maximum DNL of MS switching is the code distance between the middle code transition and its previous one. The error term of middle code is generated at the MSB decision and it is error free with top-plate sampling. Therefore, the variance of the maximum DNL error is derived as

$$E\left[V_{error}^2(2^{n-1}) - V_{error}^2(2^{n-1}-1)\right] = \sum \left[0 - \frac{\sum_{i=0}^{n-2} \delta_i^2 + \sum_{i=1}^{n-2} \delta_{ib}^2}{2^{2n-2}C_u^2} \times V_{ref}^2 \right]$$

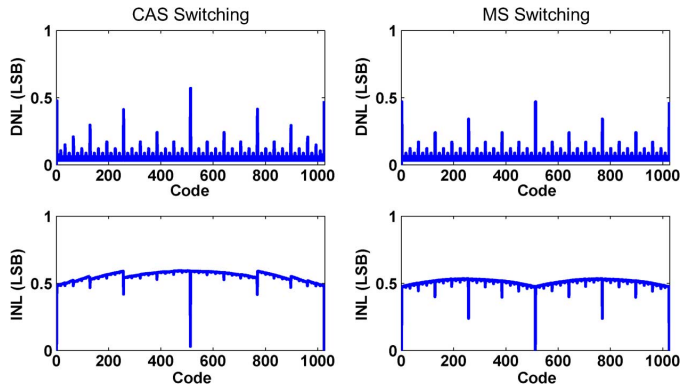

Fig. 7. Static performance with a SAR ADC using CAS switching method and MS switching method.

$$\begin{aligned}
&= \frac{E\left(\sum_{i=0}^{n-2} \delta_i^2\right) + E\left(\sum_{i=1}^{n-2} \delta_{ib}^2\right)}{2^{2n-2}C_u^2} \times V_{ref}^2 = \frac{(2^{n-1}-1)\sigma_u^2}{2^{2n-2}C_u^2} \times V_{ref}^2 \\
&\cong \frac{2^{n-1}\sigma_u^2}{2^{2n-2}C_u^2} \times V_{ref}^2 = \frac{\sigma_u^2}{2^{n-1}C_u^2} \times V_{ref}^2
\end{aligned} \tag{18}$$

Therefore, the maximum DNL of MS switching is

$$\sigma_{DNL,\max} = \frac{\sqrt{2^{n-1}}\sigma_u}{C_u} \tag{19}$$

The same derivation procedures are applied to CAS switching, and the maximum INL and DNL can be expressed as (20) and (21).

$$\sigma_{INL,\max,CAS} = \frac{\sqrt{7 \times 2^{n-3}}\sigma_u}{C_u} \tag{20}$$

$$\sigma_{DNL,\max,CAS} = \frac{\sqrt{3 \times 2^{n-2}}\sigma_u}{C_u} \tag{21}$$

To verify the theoretical analysis above, behavioral simulations for a 10-bit SAR ADC with CAS and MS switching were developed. The only error source is the random mismatch of capacitors and each capacitor cell has a Gaussian random error with a standard deviation of 3%. Fig. 7 shows the root-mean-square (rms) of DNL and INL of 10000 Monte-Carlo runs. As expected, the worst DNL is at the middle code and the worst INL occurs at the VFS/4 and 3 VFS/4 for both CAS and MS switching. The DNL of MS switching is better than CAS switching by a factor of $\sqrt{3/2}$ and the INL by a factor of $\sqrt{7/6}$. Therefore, for the same peak DNL and INL, MS switching can use smaller unit capacitor than CAS switching.

III. Implementation of Key Building Blocks

The fundamental building blocks of the proposed MS switching ADC are two S/H circuits, a dynamic comparator, SAR control logics, and two capacitive DAC networks. The detailed design consideration of the building blocks are described in the following subsections.

A. Double-Bootstrapped Sample-and-Hold

The double-bootstrapped switch shown in Fig. 8 performs the S/H function. With the bootstrapped switch, the gate-source voltage of the sampling transistors ($\mathrm{M_{s1}}$ and $\mathrm{M_{s2}}$) are fixed at the double supply voltage, which makes the on-resistance a small constant value and thus improves the switch linearity.

When clk is high, $\mathrm{C_1}$ and $\mathrm{C_2}$ are pre-charged to VDD. After clk becomes low, $\mathrm{C_1}$ and $\mathrm{C_2}$ are connected in series by a low

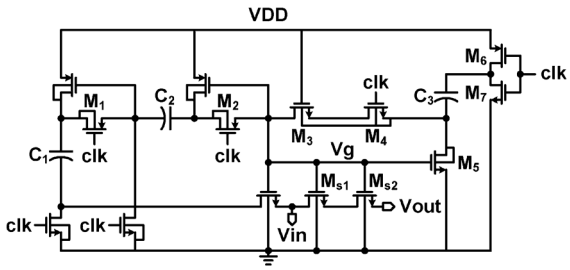

Fig. 8. Double-bootstrapped sample-and-hold.

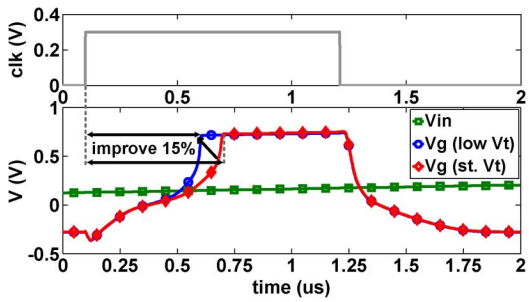

Fig. 9. Transient simulation of S/H turn-on speed with low Vt and with standard Vt at the SS corner.

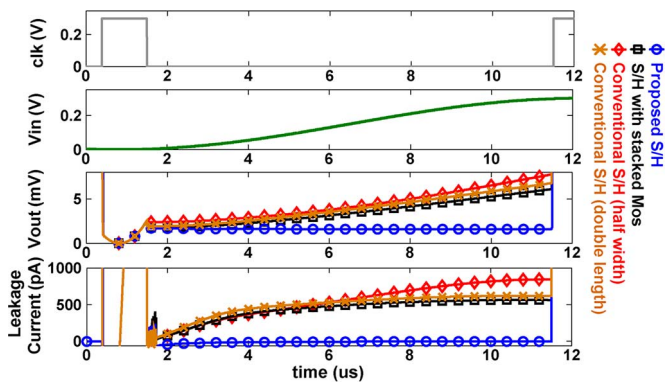

Fig. 10. Transient simulation of S/H at the FF corner.

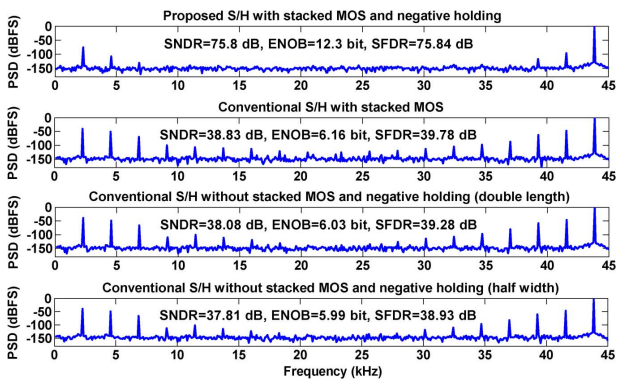

Fig. 11. Simulated FFT plot of S/H at the FF corner.

threshold PMOS (M_1) to improve boosting speed. The transient simulation of the worst case (SS corner) is shown in Fig. 9. Under the same sampling clock, the turn-on speed with low Vt M_1 can improve 15% compared to normal Vt one.

In addition, operating at low sampling frequency, the holding voltage on DAC array will be degraded due to the leakage current. The transient simulation of conventional double-bootstrapped S/H [14] with two switch sizes (half width and double

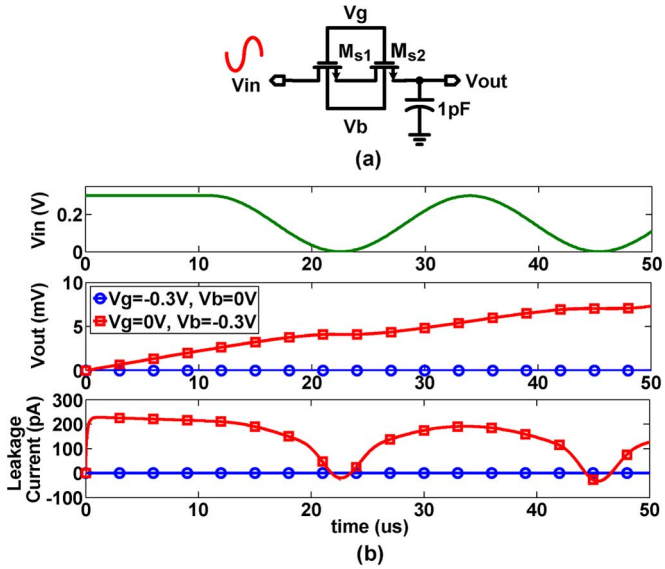

Fig. 12. (a) Simple S/H circuit. (b) Transient simulation of negative gate bias and negative body bias at the FF corner.

length for equal resistance) operated at the FF corner is displayed in Fig. 10. The common used method of stacked MOS (M_{s1} and M_{s2}) [12] is also shown in Fig. 10. The leakage current of stacked MOS is slightly smaller than the one of double length. However, because of large leakage current, the holding voltage changes larger than 1 LSB. With an input signal of common-mode voltage 0.15 V and amplitude 0.3 Vpp, Fig. 11 shows the simulated FFT plot of S/H at the FF corner. Although the stacked MOS can improve linearity, the ENOB (6.16 bit) and SFDR (39.78 dB) are still not enough for 10-bit ADC. Therefore, a modified S/H should be introduced to achieve 10-bit linearity under 0.3 V supply. By adding three MOS ($M_5 - M_7$) and one capacitor (C_3), the negative holding voltage is implemented. From simulation shown in Fig. 10, the leakage current of M_{s2} is reduced from 90 pA to 40 pA under small drain-to-source voltage (V_{ds}) of M_{s2} and the leakage current is kept small under large V_{ds} voltage of M_{s2} as well. As the FFT plot of Fig. 11 shows, the ENOB and SFDR of the proposed double-bootstrapped S/H are improved to 12.3 bit and 75.84 dB, respective. To compare the difference of the proposed negative gate bias and the negative body bias [12], the circuit shown in Fig. 12(a) is used for transient simulation. Assuming Vout is initially 0 V, when Vg is -0.3 V and Vb is 0 V (negative gate bias), the leakage current is 70 fA and keeps constant. However, with the negative body bias case (Vg is 0 V and Vb is -0.3 V), the leakage current is between -40 pA to 220 pA and oscillates with input frequency. Since the threshold voltage of the sampling switch depends on input voltage, the negative body bias would cause input-dependent non-linearity and its resultant ENOB and SFDR with Nyquist rate input are 7.66 bit and 48.86 dB, respectively.

B. Dynamic Comparator With Dummy Input Pair

The conventional dynamic latch typed comparator, shown in Fig. 13 is employed for no static current consumption. When en is low, and en_b is high, the comparator is at reset phase, and the comparator outputs V_{op} and V_{on} are pull high. In addition, the drain and source voltages of input pair (M_1 and M_2) are also reset to VDD to cancel out the coupling effect of C_{gs}

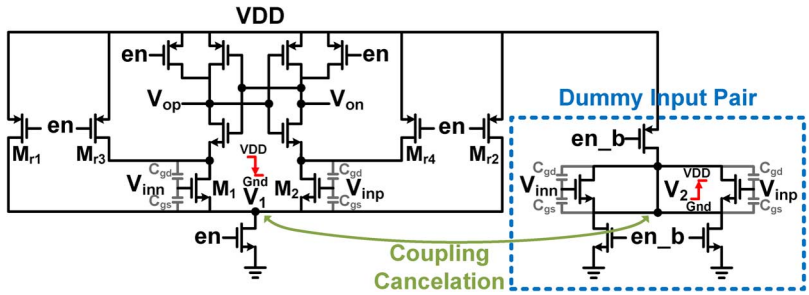

Fig. 13. Schematic of dynamic comparator.

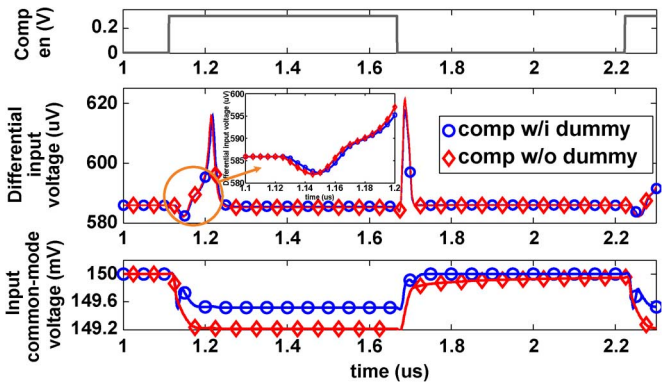

Fig. 14. Transient simulation of dynamic comparator.

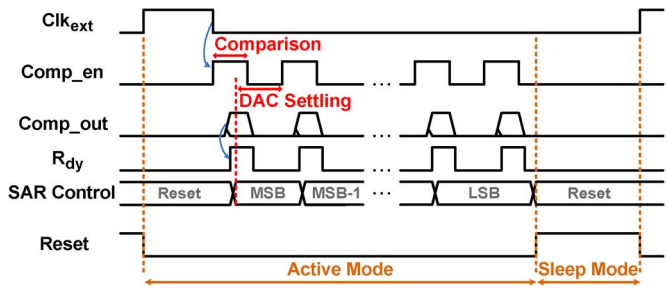

Fig. 15. Timing diagram of the proposed SAR ADC.

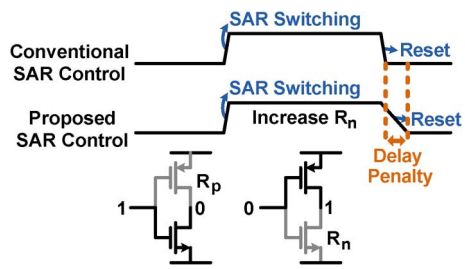

Fig. 16. Waveform of one bit SAR control.

and C_{gd}, and make each comparison have the same initial condition. When en becomes high and en_b becomes low, the comparison starts, and the voltage of V_1 are pulled from VDD to gnd rapidly. Hence, the input common-mode voltage is coupled down by C_{gs} and degrades ADC linearity. To resolve this problem, a dummy input pair is employed, as shown in Fig. 13. The voltage of V_2 is reset to gnd and go to VDD at the beginning of comparison, which makes an opposite coupling effect and maintains the input common-mode voltage constant. Fig. 14 shows the transient simulation of dynamic comparator. The input common-mode voltage variation of the comparator with dummy pair is 38.8% less than the one without dummy pair, and at reset phase, it can rapidly recover to 150 mV with reset switch $(M_{r1} - M_{r4})$. In addition, the differential input voltage variation with dummy pair is less than the one without dummy pair as well.

C. SAR Controls With Asymmetric Logic

Fig. 15 shows a timing diagram of the proposed SAR ADC. At the rising edge of Clk_{ext}, V_{in} is sampled onto the DAC array, and after the falling edge of Clk_{ext}, the ADC starts bit conversion by triggering the first rising edge of comparison clock $Comp\_en$. Beyond this point, the ADC operates in asynchronous mode and the R_{dy} signal indicates the completion of comparisons by its rising edges, and the decision result $Comp\_out$ is passed to SAR Controls directly to increase DAC settling time. As soon as the ADC finishes AD conversion, the ADC enters sleep mode. The self-power gating proposed in [10] can only reduce the leakage current at sleep phase. However, in a full rate SAR ADC, the duration of sleep phase is nearly zero, so the power gating is helpless. In this work, we propose a new technique to reduce the leakage current at active phase by employing asymmetric logic. Fig. 16 shows the waveform of one bit SAR control. The initial value of SAR control is reset to low, and the equivalent resistance R_p of PMOS (turn-off) dominates the leakage current. However, after SAR switching, the waveform would become high and the leakage current is determined by R_n. By increase the resistance of R_n, the leakage current is reduced after SAR switching with the penalty of slower reset speed. In the SAR logic implementation of this work, high Vt devices are used to replace normal Vt devices to increase R_n instead of increasing gate length. Because all the SAR controls are reset at the same time, the conversion speed only degrades slightly. From simulation, the design with asymmetric logic can reduce about 20% power consumption of SAR controls with only 3% degradation of maximum sampling frequency.

D. Capacitive DAC Network

The finger typed metal-oxide-metal (MOM) [9] unit capacitor is used in the DAC network. A 3-bit DAC network layout with previous proposed structure, shown in Fig. 17(a) has large routing error because the routing line near the DAC array has larger parasitic capacitance $(C_1 > C_2 > C_3 > C_4)$, resulting in unequal unit capacitance. To reduce this routing error, the routing lines should be far enough to have little parasitic capacitance. However, the large distance increase the chip area and bottom-plate parasitic capacitance, which increases DAC settling time and power consumption. Instead of increasing distance, this work proposes a modified finger typed MOM capacitor, shown in Fig. 17(b). The shielding structure is incorporated

TABLE II
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART WORKS

	This work			2014 ISSCC [11]	2013 ISSCC [2]	2013 ISSCC [6]	2013 CICC [7]	2012 VLSI [8]
Supply (V)	0.3	0.4	0.5	0.45	0.4	0.6	0.5	0.35
Tech.	90nm			40nm	90nm	65nm	65nm	90nm
Bit	10			10	10	10/12	10	10
Input capacitance (F)	1024f			835.5f	2560f	1024f	N/A	N/A
Fs (Hz)	90k	600k	2M	200k	500k	40k	250k	100k
DNL (LSB)	0.38			0.44	0.34	0.32/0.97	0.36	0.3
INL (LSB)	0.66			0.45	0.51	0.48/1.9	0.47	0.6
ENOB (bit) @ at Nyquist	8.38	8.88	8.97	8.95	8.72	9.4/10.1	8.45	9.06
SNDR (dB) @ at Nyquist	52.2	55.2	55.8	55.63	54.3	58.3/62.5	52.63	56.3
SFDR(dB) @ at Nyquist	78.2	87.9	81.9	76.25	82.6	N/A/68.8	64.1	71
Total Power (W)	35n	372n	1.8u	84n	0.5µ	72µ/97µ	290n	170n
FoM (fJ/c.-s.)	1.17	1.32	1.78	0.85	2.37	2.7/2.2	3.3	3.2
Core area (mm^2)	0.031			0.0065	0.042	0.076	0.072	0.032

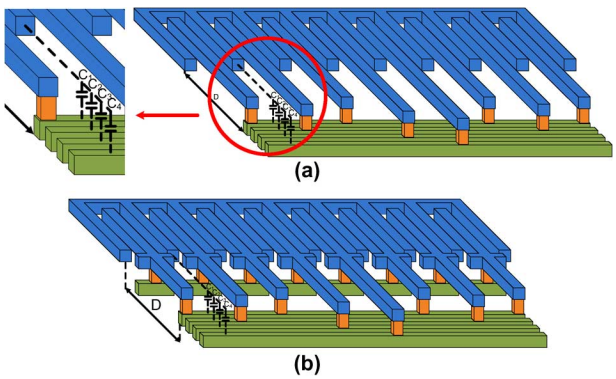

Fig. 17. Layout of 3-bit DAC network. (a) Finger typed metal-oxide-metal (MOM) unit capacitor. (b) Modified finger typed metal-oxide-metal (MOM) unit capacitor.

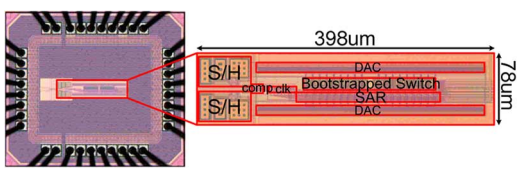

Fig. 18. Die photograph of the proposed SAR ADC.

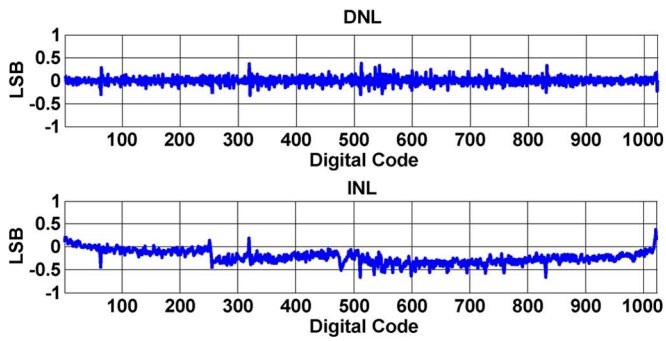

Fig. 19. Measured DNL and INL at 90 kS/s (0.3 V).

into the unit capacitor, which not only increases the unit capacitance but also reduces the undesired parasitic capacitance. The unit capacitor of the proposed SAR ADC is composed of M4-to-M7 layers and has a unit capacitance about 2 fF for capacitor matching and kT/C noise consideration. Therefore, the total sampling capacitance of one capacitor network is 1 pF. The two capacitive DAC networks occupy a total active area of 311 μm $\times$ 22 μm, about 22% of the whole ADC.

IV. MEASUREMENT RESULTS

The proposed 10-bit MS switching SAR ADC was fabricated in 90 nm CMOS technology and the die photograph is shown in Fig. 18 with a core area of 0.031 mm^2 (398 μm $\times$ 78 μm).

A. Static Performance

The static performance of the proposed ADC is evaluated by using a histogram test after applying a slow sinusoid input. Operating at 0.3 V and 90 kS/s, the measured DNL and INL are $+0.38$ LSB/-0.32 LSB and $+0.38$ LSB/-0.66 LSB, respectively, as shown in Fig. 19. The DNL and INL of proposed MS switching are worse than those of CAS switching [2], shown in Table II, mainly because of unit capacitance scaling (5 fF to 2 fF). Theoretically, the DNL and INL would be 2.5 times larger. However, thanks to the DNL and INL improvement induced in Section II, and the proposed modified finger typed MOM capacitor, the DNL and INL (0.38 LSB and 0.68 LSB) are only 1.12 and 1.29 times larger than those (0.34 LSB and 0.51 LSB) of CAS switching, respectively.

B. Dynamic Performance

Fig. 20 shows the measured fast Fourier transform (FFT) plots with an input frequency of close to Nyquist frequency. The resultant SNDR at 90 kS/s, 600 kS/s, and 2 MS/s are 52.18 dB, 55.21 dB, and 55.79 dB, respectively, and the corresponding ENOB are 8.38 bit, 8.88 bit, and 8.97 bit, respective. In addition, all of measured SFDR are above 78 dB, which proves the proposed double-bootstrapped S/H has good linearity under low supply voltage.

Fig. 21 illustrates the SNDR and SFDR as a function of input frequency for supply voltage of 0.3 V–0.5 V. The SNDR drops within 0.3 dB when the input frequency is increased to Nyquist

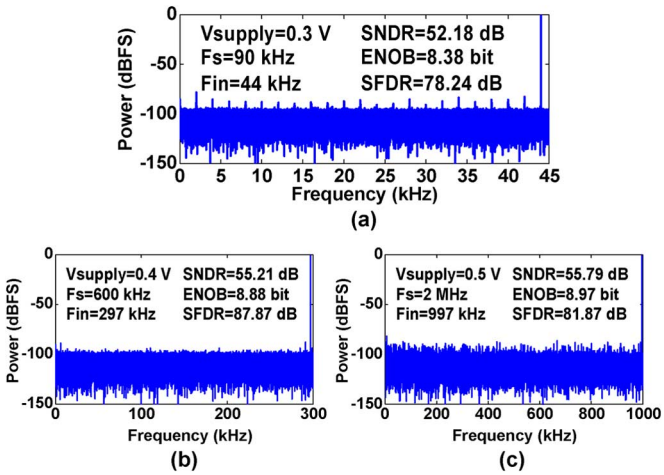

Fig. 20. Measured spectrum and SNDR/SFDR of near Nyquist-rate input at (a) 90 kS/s. (b) 600 kS/s. (c) 2 MS/s.

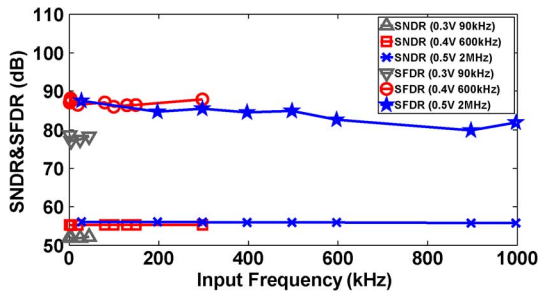

Fig. 21. Measured SNDR&SFDR as a function of input frequency (VDD = 0.3–0.5 V).

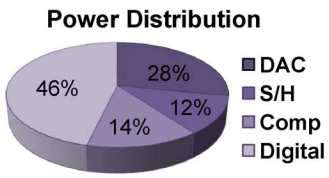

Fig. 22. The power distribution of the prototype for VDD = 0.3 V.

frequency, so the effective resolution bandwidth (ERBW) is higher than Nyquist frequency.

C. Power Consumption and Comparisons

The measured total power dissipation at 0.3 V supply is 35 nW with 11.7% in the S/H, 14% in the comparator, 28.1% in the DAC, and 46.2% in the digital SAR logics, as shown in Fig. 22. The total power consumption at 0.4 V and 0.5 V supply are 372 nW and 1.8 μW, respectively.

To compare the proposed ADC with other state-of-the-art SAR ADCs, the figure-of-merit (FOM) is used.

$$FoM = \frac{Power}{2^{ENOB} \times \min\{Fs, 2 \times ERBW\}} \qquad (22)$$

where F_s is the sampling frequency, ERBW is the effective resolution bandwidth, and ENOB is the effective number of bits at a Nyquist input.

Table II shows a summary of the measured performance and a comparison to other state-of-the-art works. With the proposed MS technique and corresponding design for low supply voltage, the prototype achieves a best FOM of 1.17 fJ/conversion-step at 0.3 V and 90 kHz. Compared to other low-power SAR ADCs, this work with a wide sampling frequency range of 90 kS/s-to-2 MS/s presents FOMs of 1.17-to-1.78 fJ/conversion- step at 0.3 V-to-0.5 V supply and can operate at the lowest supply voltage for 10-bit resolution.

V. Conclusion

In this paper, a 10-bit SAR ADC for biomedical system or sensor network is presented. The proposed energy-efficient MS switching procedure reduces the DAC power consumption without common-mode voltage shift and extra reference voltage. In addition, the new proposed double-bootstrapped S/H improves sampling linearity under ultra-low voltage of 0.3 V. The modified comparator enhances comparison accuracy, and the finger typed MOM capacitor with shielding structure is employed to reduce parasitic capacitance and increase unit capacitance. Furthermore, the asymmetric logic is proposed to take trade-off between leakage current and operation speed at conversion phase. The prototype ADC occupies an active area of 0.031 mm^2, and achieves 90 kS/s-to-2 MS/s operation speeds with FOMs of 1.17-to-1.78 fJ/conversion-step at 0.3 V-to-0.5 V supply.

Acknowledgment

The authors thank MediaTek for supporting of this work and National Chip Implementation Center (CIC) for fabrication of the test chip.

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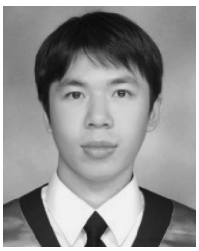

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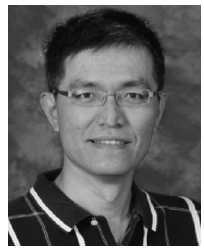

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