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A 10 bit 320 MS/s Low-Cost SAR ADC for IEEE 802.11ac Applications in 20 nm CMOS

Chun-Cheng Liu, *Member, IEEE*, Che-Hsun Kuo, and Ying-Zu Lin, *Member, IEEE*

***Abstract*—This paper presents a low-cost successive approximation register (SAR) analog-to-digital converter (ADC) for IEEE 802.11 ac applications. In this paper, a binary-scaled recombination capacitor weighting method is disclosed. The digital sub-blocks in this ADC are composed of standard library logic cells. The prototype is fabricated in a 1P8M 20 nm CMOS technology. At 0.9 V supply and 160 MS/s, the ADC consumes 0.68 mW. It achieves an SNDR of 57.7 dB and 57.13 dB at low and Nyquist input frequency, respectively, resulting in figures of merit (FoMs) of 6.8 and 7.3 fJ/conversion-step, respectively. At 1 V supply and 320 MS/s, the ADC consumes 1.52 mW. It achieves an SNDR of 57.1 dB and 50.89 dB at low and Nyquist input frequency, respectively, resulting in FoMs of 8.1 and 16.5 fJ/conversion-step, respectively. The ADC core only occupies an active area of 33 μm $\times$ 35μm.**

***Index Terms*—20 nm CMOS, analog-to-digital converter (ADC), IEEE 802.11ac, low cost, low power, redundancy, successive approximation register (SAR).**

I. Introduction

TODAY'S digital life is all about connections. People connect to the internet for daily work, entertainment and communication. The growing number of mobile devices, like smart phones, notebook, tablet, etc., makes our life more convenient. The high data rate applications such as wireless display and rapid media content upload/download are driving the need for high-data-rate wireless local area network (WLAN). Table I shows the evolution of IEEE 802.11 WLAN standards. The IEEE 802.11ac (5th Generation Wi-Fi) is expected to be the mainstream WLAN specification in the next few years. The mandatory channel bandwidths of IEEE 802.11ac system are 20 MHz, 40 MHz, and 80 MHz (80+80 MHz and 160 MHz are optional) [1]. Fig. 1 shows the architecture of a WLAN RX system which includes antenna, mixer, analog filter, I/Q ADCs, digital filter, decimation unit and FFT unit. To reserve some bandwidth margin for digital filtering or decimation, the sampling rate of I/Q ADCs must be higher (2X $\sim$ 4X) than the signal bandwidth. Therefore, the receiver of an IEEE 802.11ac system requires an analog-to-digital converter (ADC) with a sampling rate of 160 to 320 MS/s and a resolution of 8 to 10 bits for sufficient signal bandwidth and signal to noise ratio (SNR).

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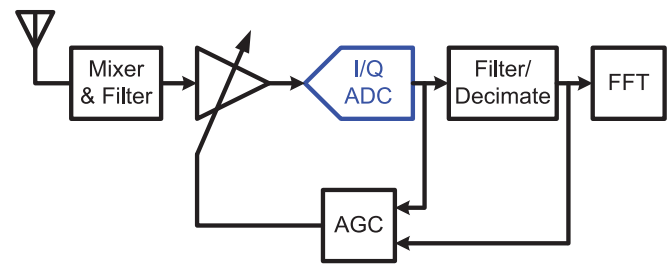

Fig. 1. Architecture of a WLAN RX system.

TABLE I
IEEE802.11 Standards Evolution

Standard	Frequency band	Bandwidth	Modulation	Maximum data rate
802.11b	2.4 GHz	20 MHz	DSSS	11 Mb/s
802.11a	5 GHz	20 MHz	OFDM	54 Mb/s
802.11g	2.4 GHz	20 MHz	DSSS, OFDM	54 Mb/s
802.11n	2.4 GHz, 5 GHz	20MHz, 40MHz	OFDM	600 Mb/s
802.11ac	5 GHz	20MHz, 40 MHz,80 MHz, (80+80 MHz), (160 MHz)	OFDM	1.3Gb/s (6.9Gb/s)

With the progress of CMOS technology, the feature size of CMOS devices is scaled down. The conversion rate of successive approximation register (SAR) ADCs improves with the growing transistor bandwidth. The SAR ADC becomes an attractive ADC architecture in the nanometer scaled CMOS processes. A lot of recent research activity has been invested in this type of ADCs. The asynchronous SAR ADC [2] eliminates the need of high frequency clock and speed up the SAR operation. The passive charge sharing SAR ADCs [3]–[5] works in charge domain and uses only passive circuits to reduce the power consumption of reference buffer. The sampling phase is also enlarged. The redundant SAR ADCs [6], [7] adds extra redundant bit to tolerate a certain range of settling and decision error during bit-cycling, therefore, improves the conversion speed. The time-interleaving SAR ADC [8], [9] enhances the sampling rate. Digital calibration technique [8] overcomes the channel mismatch problem and other nonideal effects in medium-to-high-resolution time-interleaving SAR ADCs. Several energy-efficient switching methods [10], [11] have been proposed to lower the switching energy of the capacitor network. The other techniques, like multibit/step [12], [13], pipelined-SAR [14]–[16], etc., also improve the sampling rate or reduce the power consumption of pipelined ADC. Recently,

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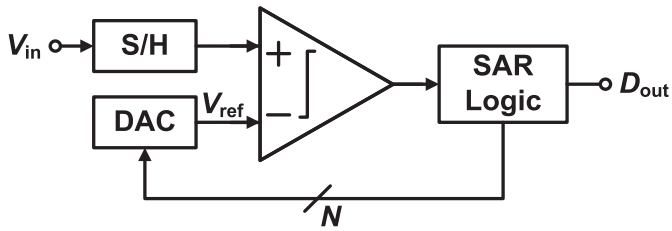

Fig. 2. Architecture of a conventional SAR ADC.

the conversion rate of single-channel SAR ADCs has achieved more than 100 MS/s with the resolutions from 10 to 14 bit [17]–[20]. The SAR ADCs also have the feature of low-power and low-cost that makes it more attractive than the other ADC architectures for the high-speed WLAN systems, especially for those embedded in mobile devices.

This paper presents a binary-scaled recombination capacitor weighting method for SAR ADC [21]. With the proposed capacitor partition algorithm, the reference buffer requirement is relaxed greatly. The prototype ADC achieves a conversion rate of 320 MS/s and an effective resolution bandwidth (ERBW) more than 100-MHz while consumes 1.52-mW dynamic power from 1.0-V supply and 0.9-V reference voltage, and only occupies an active area of 33 μm $\times$ 35 μm in a 20-nm CMOS technology. The remaining part of this paper is organized as follows: Section II describes the comparison of redundant weighting methods for SAR ADC. Section III presents the implementation of proposed SAR ADC and key building blocks. Section IV shows the measurement results of the prototype ADC and the comparison to the state-of-the-art works. Conclusions are given in Section V.

II. Redundant Weighting Methods for SAR ADC

Fig. 2 shows the block diagram of a conventional SAR ADC, which includes a sample and hold (S/H) circuit, a comparator, a SAR logic and a digital-to-analog convertor (DAC). A SAR ADC requires several comparison cycles to complete one conversion. Therefore, it needs a S/H circuit to hold the input signal. The comparator compare the sampled input signal with the DAC reference voltage, then the output of comparator triggers the SAR logic operation. According to the SAR logic, the DAC changes the output voltage. Then, the comparator performs comparison again. The SAR ADC repeats these procedures until the final bit is obtained. For a correct conversion, the difference between the analog signal and digital presentation should be less than 1 LSB. If the difference is larger than 1 LSB, that means there are some errors happened during the conversion.

Fig. 3(a) shows an example of binary search SAR ADC. This is a 4 bit case. Hence, it has sixteen quantization levels. The V_i is the input signal and the bold line is the threshold. The comparator distinguishes the input signal is higher or lower than the threshold and generates one bit digital code. In the first bit cycle, the input signal is lower the threshold. Therefore, the first bit is 0. After the first bit is decided, the number of possible quantization levels is reduced from 16 to 8. That means the effective input range is reduced by a fact of 2. The conversion will repeat

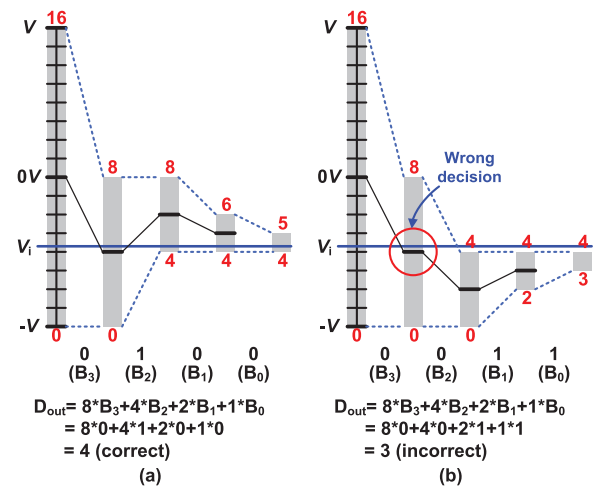

Fig. 3. Conventional binary search: (a) correct conversion; (b) wrong conversion.

until the final bit is obtained. If all bit cycling operations are correct, we can get a correct digital output code. In this case, the digital output code is equal to 4.

If a wrong decision is made before the last cycle as shown in Fig. 3(b), even if the remaining decisions and their corresponding DAC switching are correct, the difference between the input and reference in the last cycle is still larger than one LSB, resulting in performance degradation. To make sure the conversion is correct, the DAC setting error must be less than 0.5-LSB in each bit-cycling. It takes a long time for MSB capacitors and reference voltage to stabilize. Otherwise, the nonsettled DAC may result in wrong decisions and degrade the ADC performance. The long settling time limits the conversion rate of SAR ADCs especially in high resolution cases. To improve the settling speed, the binary SAR ADC needs a power hungry on-chip reference buffer to fast settling of reference voltage, or directly uses external reference voltages [10], [11]. However, the SAR ADC consumes pretty large dynamic current. It needs large decoupling capacitors to minimize the variation on reference voltage. In the nanometer scaled CMOS process, the area of on-chip decoupling capacitors is usually much larger than the core area of SAR ADCs. To avoid a strong reference buffer or large area on-chip decoupling capacitors, some redundant weighting methods [6], [7] for the SAR ADC are proposed to speed up conversion by increasing extra bit-cycles to alleviate the DAC and reference settling requirement during bit-cycling.

A. Nonbinary Weighting Method

In the nonbinary SAR ADCs [6], the effective input range is reduced by a factor smaller than 2 in each bit-cycle. Fig. 4(a) shows the concept of nonbinary search algorithm. This is also a 4 bit case. The effective input range is reduced by a factor small than 2 after each bit cycles. For example, after the first bit cycles, the number of possible quantization levels is reduced from 16 to 9. Fig. 4(b) shows a wrong decision happened during the conversion. If the remaining bit cycling operations are all correct, it is possible to get a correct digital

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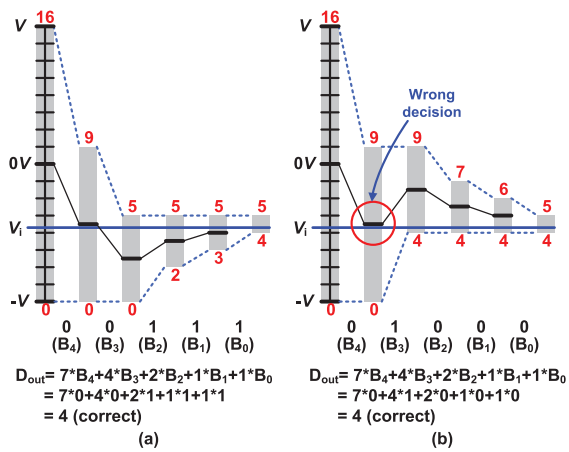

Fig. 4. Nonbinary search: (a) correct conversion; (b) conversion with wrong decision.

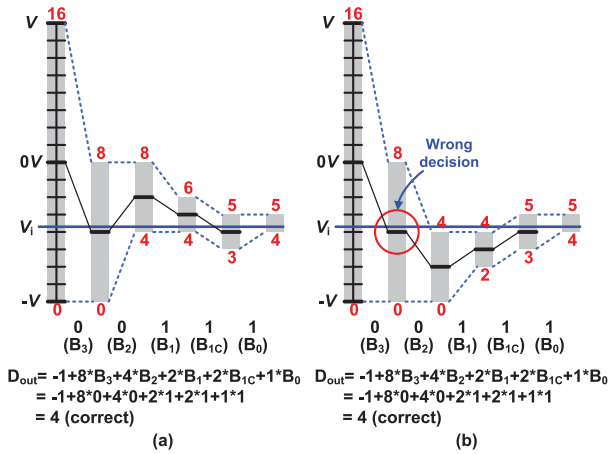

Fig. 5. Binary-scaled compensation: (a) correct conversion; (b) conversion with wrong decision.

output code at the cost of extra bit cycles. In this 4 bit example, it needs 5 bit cycles to complete the conversion.

The nonbinary SAR ADC generates more decision levels than a conventional one. There are several digital codes representing the same input voltage, meaning different switching procedures can lead to the same result. Hence, a certain range of error does not have influence on the conversion result. Comparator can do comparison before the DAC and reference voltage is well settled. Hence, the bit-cycling time can be reduced. Even the no-binary SAR ADC needs extra bit cycles, the total conversion time still can be improved.

However, the nonbinary architecture needs extra hardware, including control circuits, a ROM to store the bit weightings and an arithmetical unit to calculate the sum. Moreover, the nonbinary scaled bit weighting is not favored for layout matching, which may limit the linearity of the DAC network.

B. Binary-Scaled Compensation Weighting Method

In the binary-scaled error compensation SAR ADC [7], some binary-scaled capacitors are inserted in the original binary DAC network to provide compensative voltage values. Fig. 5(a) shows the concept of the binary-scaled error compensation algorithm. Like the binary search, the effective input range is reduced by a factor of 2. But in some bit cycles, the input range does not reduce but shift to compensate for some errors. With the extra compensative bit cycles, there are multiple digital presentations for an input voltage. Different output codes can lead to the same result. Even a wrong decision happened during the conversion, as shown in Fig. 5(b). It is still possible to get a correct digital output code.

This is a simpler way to overcome the DAC settling issues with less design and hardware overhand. Only the compensative capacitors and the digital error correction logic added to perform the compensation function and compute the binary output codes. However, the extra compensative capacitors increases the sampling capacitance and results in a smaller input range. The mismatch between the compensative capacitors and the corresponding digital value also degrades the linearity of the ADC.

C. Proposed Binary-Scaled Recombination Weighting Method

For an N bit redundant SAR ADC, it needs M bit cycles ($M > N$) to convert an N bit digital code. The DAC capacitor array comprises $M+1$ capacitors, (C_{M} to C_1 descending in size, C_0 is a termination capacitor with the same size of a unit capacitor). The total capacitance C_{M} to C_0 is defined as C_{total}, and V_{R} is the reference voltage. The maximum tolerable settling error range during switching the capacitor C_{n} can be expressed as

$$V_{\max_\mathrm{error}_n} = V_R \cdot \left(\sum_{i=0}^{n-1} \frac{C_i}{C_{\mathrm{total}}} - C_n\right). \tag{1}$$

Therefore, each capacitance in a redundant SAR ADC must satisfy

$$C_n \le C_{n-1} + \cdots + C_1 + C_0, (M \ge n > 1). \tag{2}$$

According to the redundancy principle, we proposed a binary-scaled recombination weighting method without adding extra compensative capacitors and with less circuit overhead than the previous techniques. For an N bit proposed SAR ADC, the $M+1$ capacitors in DAC array are composed of only 2^N capacitor cells. To make the MSB capacitor C_M has a certain range of redundant margin, the MSB capacitor C_M only includes $2^{N-1} - 2^P$ $(N-1 > P)$ capacitor cells, which is less than half of C_{total}. The 2^P capacitor cells removed from the MSB capacitor C_{M} are distributed into $r(M > r > P)$ groups. In each of the r groups, the number of capacitor cells is a power-of-2 number. The r groups are selectively allocated to r different capacitors among C_{M-1} to C_1. Therefore, C_n, one of the capacitors from C_{M-1} to C_1, has either 2^{n-j} or $(2^{n-j} + 2^k)$ capacitor cells, where $2^{n-j} \neq 2^k$, and C_n must satisfy (2).

Take a 10 bit case, for example. There are 2^{10} quantization levels for the proposed weighting method to arrange. The MSB capacitor with half of the total bit weights (2^9) is split into two groups, $480(2^9 - 2^5)$ and $32(2^5)$. Next, $32(2^5)$ cells are split into $8(2^3)$, $8(2^3)$, $4(2^2)$, $4(2^2)$, $4(2^2)$, $2(2^1)$, $1(2^0)$ and $1(2^0)$, respectively. Those weights are added to the LSBs groups. The new weighting ratio of C_{11} to C_1 are $480(2^9 - 2^5)$, $256(2^8)$, $128(2^7)$, $72(2^6 + 2^3)$, $40(2^5 + 2^3)$, $20(2^4 + 2^2)$, $12(2^3 + 2^2)$,

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TABLE II
COMPARISON OF REDUNDANT METHODS

	Non-binary [6]		Binary-scaled Compensation [7]		Binary-scaled Recombination			
	12-bit cycles to convert 10-bit		13-bit cycles to convert 10-bit		11-bit cycles to convert 10-bit		12-bit cycles to convert 10-bit	
number of bit-cycling	bit weighting	redundant range (LSB)	bit weighting	redundant range (LSB)	bit weighting	redundant range (LSB)	bit weighting	redundant range (LSB)
1	447	130	512	146	480	64	480	64
2	251	75	256	146	256	32	256	32
3	142	42	128	146	128	32	128	32
4	80	24	128	18	72	16	72	16
5	45	14	64	18	40	8	40	8
6	25	9	32	18	20	8	20	8
7	14	6	16	18	12	4	12	4
8	8	4	16	2	8		6	4
9	5	2	8	2	4		4	2
10	3	1	4	2	2		2	2
11	2		2	2	1		2	
12	1		2				1	
13			1					

$8(2^2+2^2=2^3)$, $4(2^1+2^1=2^2)$, $2(2^0+2^0=2^1)$ and $1(2^0)$, respectively. This example takes 11 bit-cycles to convert 10 bits. The digital output can be expressed as

$$\begin{aligned} D_{\text{out}} = & B_{10}\times(2^9-2^5)+B_9\times(2^8)+B_8\times(2^7) \\ & +B_7\times(2^6+2^3)+B_6\times(2^5+2^3) \\ & +B_5\times(2^4+2^2)+B_4\times(2^3+2^2) \\ & +B_3\times(2^3)+B_2\times(2^2)+B_1\times(2^1)+B_0\times(2^0). \end{aligned}$$

Take another case as an example. It takes 12 bit-cycles to convert 10 bits. The MSB capacitor is split into $480(2^9-2^5)$ and $32(2^5)$. Next, $32(2^5)$ cells are split into $8(2^3)$, $8(2^3)$, $4(2^2)$, $4(2^2)$, $2(2^1)$, $2(2^1)$, $1(2^0)$, $2(2^1)$ and $1(2^0)$, respectively. Those weights are added to the LSBs groups. The new weighting ratio of C_{12} to C_1 are $480(2^9-2^5)$, $256(2^8)$, $128(2^7)$, $72(2^6+2^3)$, $40(2^5+2^3)$, $20(2^4+2^2)$, $12(2^3+2^2)$, $6(2^2+2^1)$, $4(2^1+2^1=2^2)$, $2(2^0+2^0=2^1)$, $2(2^1)$ and $1(2^0)$, respectively. The digital output can be expressed as

$$\begin{aligned} D_{\text{out}} = & B_{11}\times(2^9-2^5)+B_{10}\times(2^8)+B_9\times(2^7) \\ & +B_8\times(2^6+2^3)+B_7\times(2^5+2^3) \\ & +B_6\times(2^4+2^2)+B_5\times(2^3+2^2) \\ & +B_4\times(2^2+2^1)+B_3\times(2^2)+B_2\times(2^1) \\ & +B_1\times(2^1)+B_0\times(2^0). \end{aligned}$$

In the proposed redundant method, the MSB weights can be expressed as a difference of two power-of-2 numbers $(2^{N-1}-2^P)$. Except the MSB weights, the other bit weights can be expressed as a sum of two or only one power-of-2 numbers. The method doesn't need extra compensative capacitors and the digital error correction logic is very simple to realize.

Table II shows the comparison of redundant range with different redundant methods. The arrangement of redundancy is more flexible with the proposed binary-scaled recombination algorithm. We can design the number of bit-cycling and the redundant range for each bit cycling and according to the reference buffer and DAC settling. The redundant ranges of the two examples of the proposed methods are smaller than the previous cases. This is because the redundant range of MSB is sufficient for our circuit implementation. To get a larger redundant range, we can remove more bit weight from MSB weighting, and add the reduced weightings to the other LSB weightings.

With the redundancy, the noise requirement of the comparator in the proposed SAR ADC can be relaxed in the MSBs bit-cycling. Exclude the settling issues of reference buffer and DAC circuit, the maximum noise relaxed range for each bit-cycling is about quarter (for 4 sigma variation) of redundant range in Table II. Similar to the ADC in [4], the proposed SAR ADC still needs a low-noise comparator in the last few LSBs bit-cycling to achieve sufficient SNR. To simplify the design and avoid the offset problem between coarse and fine comparator, we only use one low-noise comparator in this SAR ADC implementation.

The proposed technique also relaxes the settling requirement of reference buffer and DAC circuit. It reduces the power consumption of reference buffer and improves the operation speed of SAR ADC. However, the requirement of capacitor mismatch in CDAC cannot be moderated, because the mismatch between real and ideal capacitance value of each unit capacitor cell is not changed with the proposed technique.

III. IMPLEMENTATION OF PROPOSED SAR ADC AND BUILDING BLOCKS

Fig. 6 shows the architecture of the proposed SAR ADC, which consists of a comparator, two bootstrapped switches, two capacitor arrays, SAR control logic and digital error correction logic (DEC). Similar to a monotonic switching SAR ADC [10], the ADC sampled input signal on the top plates of capacitor arrays. Therefore, the 10 bit ADC only needs 2^9 capacitor cells in each capacitor array. The bottom plates of the capacitor cells are either connected to reference voltage or ground. A CMOS inverter can perform the DAC switching with very simple control logic. This ADC adds two extra redundant bit-cycles to alleviate the DAC settling problem and speed up the conversion. The 2^9 capacitor cells will be arranged into 11 capacitor groups C_{11} to C_1 with the proposed binary-scaled recombination weighting method. Fig. 7 shows how to weight the 11 capacitor groups. The MSB capacitor group $256(2^8)$ is split into two groups, $240(2^8-2^4)$ and $16(2^4)$. Next, $16(2^4)$ is split into $4(2^2)$, $4(2^2)$, $2(2^1)$, $2(2^1)$, $1(2^0)$, $1(2^0)$, $1(2^0)$ and $1(2^0)$. Those groups are added to the LSBs capacitor groups. The new capacitor weighting ratios are $240(2^8-2^4)$, $128(2^7)$, $64(2^6)$, $36(2^5+2^2)$, $20(2^4+2^2)$, $10(2^3+2^1)$, $6(2^2+2^1)$, $3(2^1+2^0)$, $2(2^0+2^0=2^1)$, $1(2^0)$ and $1(2^0)$. The effective bit weights of the 12 bits are 480, 256, 128, 72, 40, 20, 12, 6, 4, 2, 2, 1. The digital output can be expressed as

$$\begin{aligned} D_{\text{out}} = & B_{11}\times(2^9-2^5)+B_{10}\times(2^8)+B_9\times(2^7) \\ & +B_8\times(2^6+2^3)+B_7\times(2^5+2^3) \\ & +B_6\times(2^4+2^2)+B_5\times(2^3+2^2) \\ & +B_4\times(2^2+2^1)+B_3\times(2^2)+B_2\times(2^1) \\ & +B_1\times(2^1)+B_0\times(2^0). \end{aligned}$$

A. S/H Circuit

The proposed SAR ADC samples the input signal via the bootstrapped switches at the top plates of capacitors. When the bootstrapped switch is turned off and the SAR ADC is in bit-cycling, the signal couples to the sampling capacitors through

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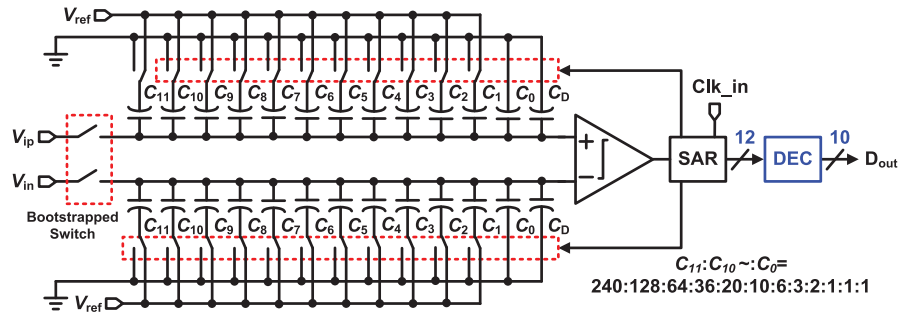

Fig. 6. Architecture of proposed SAR ADC.

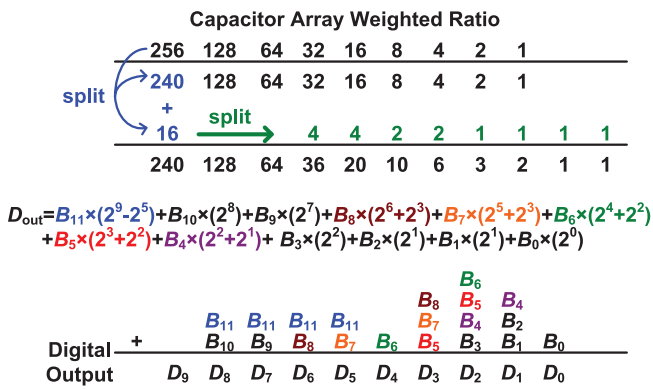

Fig. 7. Capacitor array weighting used in the SAR ADC.

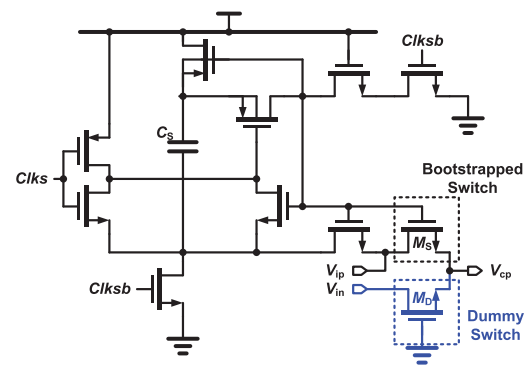

Fig. 8. Bootstrapped switch with a dummy.

the metal routing parasitic capacitor and the drain-source capacitor C_{DS} of the sampling transistor M_{S}. The coupling effect degrades the ADC performance. The work [10] utilizes a cross-coupled metal-oxide-metal (MOM) capacitor to neutralize the effect. However, with process variation, the coupling effect could not be totally cancelled. In this works, an identical dummy transistor M_{D} is added to the bootstrapped switch as shown in Fig. 8. The dummy switch is always off, and the drain and source of the dummy switch are connected to the opposite input signal and the sampling capacitor arrays, respectively. In Fig. 9(a), without this dummy switch, any variation of input signal will directly coupled to the sampling capacitor arrays. The variation on the single side sampling capacitor arrays will disturb the ADC bit-cycling. In Fig. 9(b), with the identical dummy switch, any variation of input signal will be coupled to dual sampling capacitor arrays. The coupling effect will be eliminated mutually and has no influence on the SAR conversion result in this differential ADC.

We run a transient simulation of the S/H circuit to demonstrate the effective of the dummy switch. Assume that the metal parasitic capacitance between the drain and the source of sampling transistor is 0.5 fF. When the sampling switch turned on, the input is connected to a 3.2 MHz signal source. After the sampling switch turned off, the input frequency changed to 75 MHz. Fig. 10 shows the FFT spectrum of simulation results with and without the dummy switch. With the dummy switch, the interference frequency has not influence to the result. Without the dummy switch, the interference frequency of 75 MHz appears in the spectrum and decreases the SNDR from 68.8 dB to 55.0 dB.

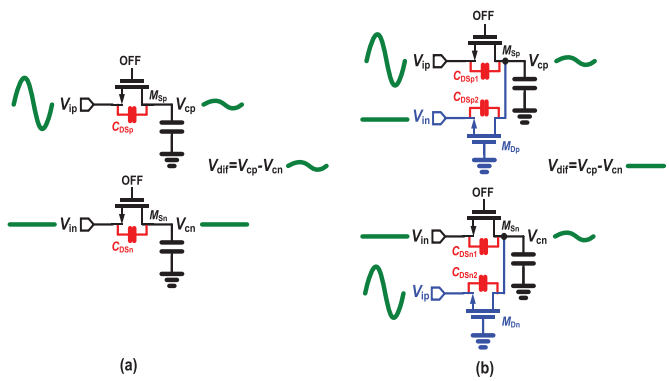

Fig. 9. Coupling effect: (a) without a dummy transistor; (b) with a dummy transistor.

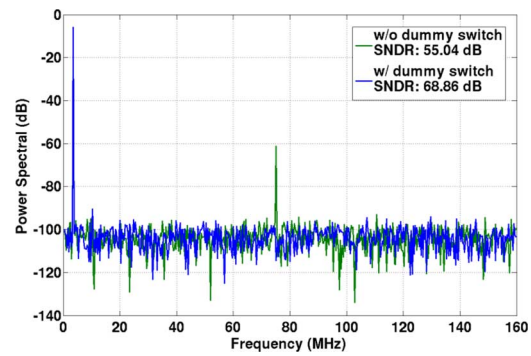

Fig. 10. FFT spectrum of simulation results with and without the dummy switch.

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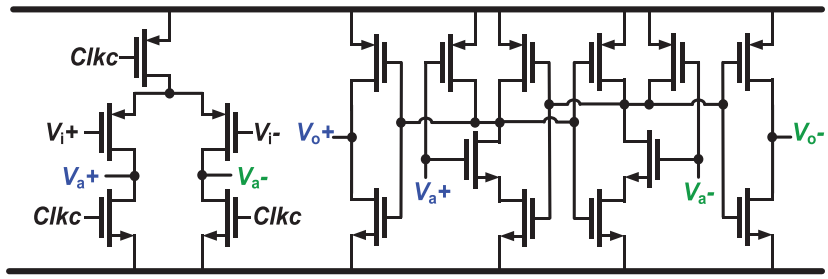

Fig. 11. Schematic of a dynamic two-stage comparator.

B. Dynamic Two-Stage Comparator

A high-speed, low-power and low-noise comparator is crucial for the SAR ADC. To satisfy those considerations, a dynamic two-stage comparator composed of a dynamic preamplifier stage [22] and a dynamic latch is used in this prototype ADC. The detail schematic of the dynamic two-stage comparator is shown in Fig. 11. To work properly with a gradually decreasing common-voltage, the pre-amplifier utilizes a p-type input pair. When *Clkc* is high, the pre-amplifier outputs $V\mathrm{a}+$ and $V\mathrm{a}-$ are reset to ground. When *Clkc* goes to low, $V\mathrm{a}+$ and $V\mathrm{a}-$ are charged from low to high dependent on the input voltages $V_\mathrm{i}+$ and $V_\mathrm{i}-$. The pre-amplifier transfers the difference of two voltage signals into a difference of timing. The dynamic latch performs a timing comparator and generates a digital output according which input signal goes high first. The comparator does not consume any static power. Hence, it is very energy efficient.

C. Capacitor Array

The DAC capacitor array occupies most of the area, usually more than 50% of the whole ADC. The layout of the capacitor array becomes critical to reduce the area of ADC. Fig. 12 shows two metal-oxide-metal (MOM) capacitor cell structures. The structure in Fig. 12(a) has some similarities with the capacitor cell in [10]. The top plate of the capacitor cell is enclosed by bottom plate to reduce the parasitic of top plate. However, the parasitic capacitor between each bottom plate increases to the switch buffers. The space between each unit cell also occupies extra area. Fig. 12(b) shows the proposed capacitor cell. The bottom plate of the capacitor cell is enclosed by the top plate, and the top plates of all capacitor cells are combined together. Therefore, the capacitor array is very compact and has smaller area and gradient effect, that resulting in better matching. We can use a smaller capacitance to achieve 10 bit linearity. When the capacitance reduced, the DAC switch size can also be reduced for the same settling time.

D. Digital Error Correction Logic

The digital error correction logic converts the 12 bit redundant codes into 10 bit binary codes. Fig. 13 shows the logic implementation of digital error correction circuit, which consists of 10 full adders, 10 D-type flip-flops (DFFs) and 2 multiplexers. When the skip_sel is set to high, the last bit-cycling operation is skipped and the total number of bit-cycles is reduced to 11. The conversion time is improved at the cost of missing two quantization levels.

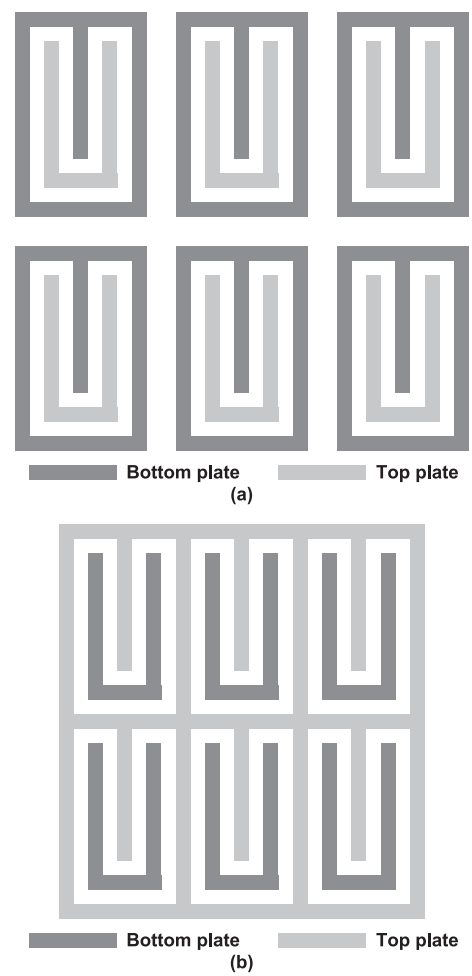

Fig. 12. Structure of capacitor array: (a) top plate encolsed by bottom plate; (b) bottom plate enclosed by top plate.

E. Standard Library Based Design

Many sub-circuits in the proposed SAR ADC are digital, includes comparator cycling timing loop logic, SAR control logic, digital error correction logic and DAC switches. In advance CMOS technology, many dummy devices are added to ensure the device property in full custom design and layout. The extra dummy cells result in extra area overhead, larger routing resistance and parasitic capacitance to main devices. The digital standard library logic cells provided by foundry have verified device properties, regular and compact layout size. Therefore, we use

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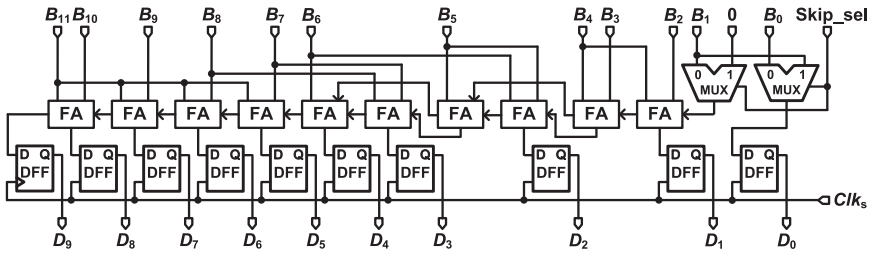

Fig. 13. Implementation of digital error correction logic.

the digital standard logic cells to construct the digital sub-circuits in the proposed ADC. With the standard cell, we can run prelayout simulation with detail layout parasitic. The parasitic effect in those digital sub-circuits can be taken into consideration during prelayout design and simulation. That can reduce a lot of iterations between layout modification and postlayout simulation. Moreover, with the standard cell based design, the layout of each standard cell is already available. Those digital sub-blocks also can use CAD tool for auto-routing. Hence, the layout effort is relaxed very much. Therefore, the develop time and cost are reduced greatly.

F. Reference Generator

For a traditional binary SAR ADC with 10 bit resolution and hundreds of MHz sampling rate, the reference buffer and capacitor DAC network must settled in few tens of pico-seconds. It needs a reference buffer with several tens GHz bandwidth. The current consumption of the wide bandwidth buffer may dissipate few tens mA, which is much higher than the current consumption of SAR ADC. The power hungry reference buffer reduces the low-power attractiveness of SAR ADC. With the help of the proposed binary-scaled recombination redundant algorithm, the bandwidth requirement of reference buffer is relaxed greatly.

Fig. 14 shows the schematic of reference buffer adopted for the proposed SAR ADC. A 30 μA static current through a 30 kΩ resistance generates a 0.9 V voltage. The transistors M_2 and M_3 mirror 12 times current from M_1, and the currents through two 2.5 kΩ resistances generates a pair of 0.9 V reference voltage for I/Q channel ADCs. The open-loop topology has the benefit of small output impedance, wide bandwidth, low noise, and small area. It is very suitable for such high resolution and high speed ADC.

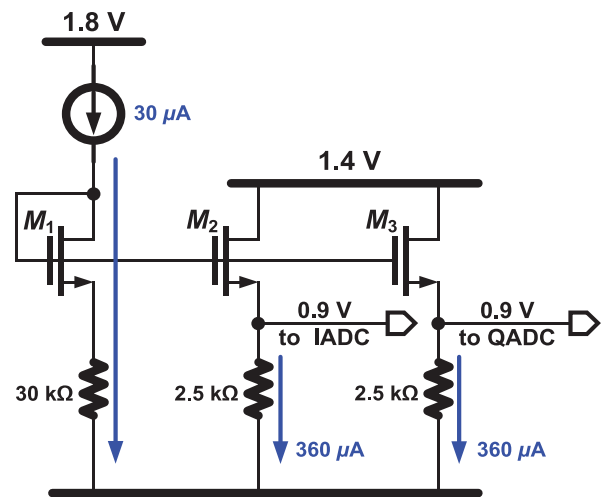

Fig. 14. Implementation of reference buffer.

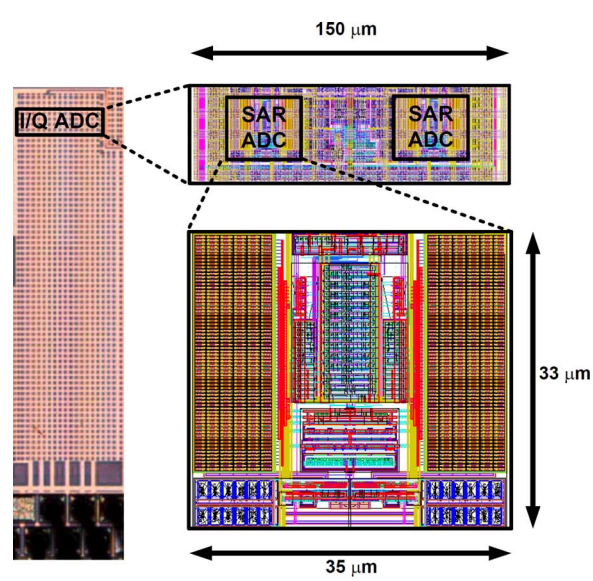

Fig. 15. Chip micrograph and layout zoomed-in view of the SAR ADC core.

IV. Measurement Results

The prototype ADC is fabricated in a 1P8M 20-nm CMOS technology. Fig. 15 shows the chip micrograph and the layout zoomed-in view of the ADC core which only occupies an active area of 33 μm $\times$ 35 μm. Different from the other works [10], [11] achieving almost rail-to-rail input range to improve SNR. The prototype ADC adopts only 1-$V_{P\text{-}P}$ input swing due to the limited linear range of the on-chip front-end circuits. The supply (0.9-V to 1-V) and reference voltage (0.9-V) of the SAR ADC are provided by an internal LDO and a reference generator (consuming only 0.36 mA static current). The total sampling capacitance is 540 fF where the capacitance in the main DAC is about 300 fF and the capacitance of dummies and parasitic is 240 fF.

At 160 MS/s sampling rate mode, the supply voltage is set to 0.9-V to save power, and the sampling time is 50% duty of clock cycle. The dynamic power consumption in the condition is 0.68 mW (S/H and comparator 67%, SAR control logic 23%, DAC reference 7%, and DEC 3%). Most power is

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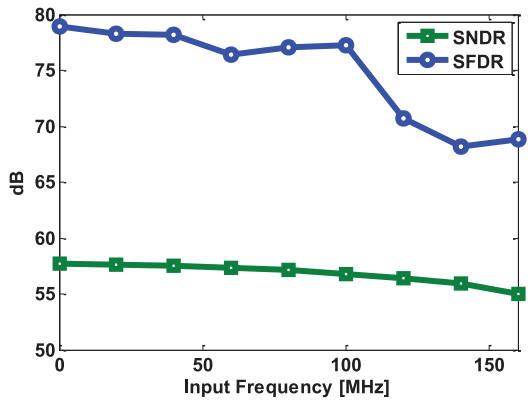

Fig. 16. Measured performance versus input frequency at 0.9 V and 160 MS/s.

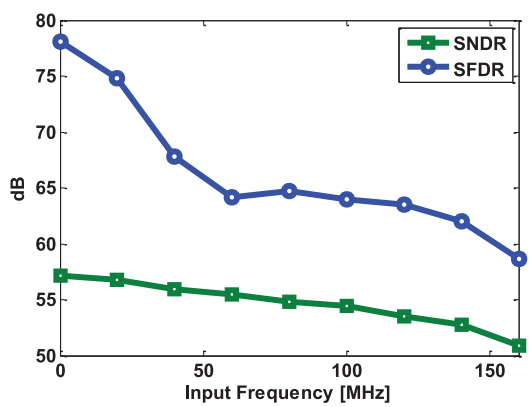

Fig. 17. Measured performance versus input frequency at 1.0 V and 320 MS/s.

dissipated in the comparator to improve SNR. Fig. 16 plots the measured SNDR and SFDR values versus the input frequency at 160 MS/s. At low input frequency, the measured SNDR and SFDR are 57.7 dB and 78.9 dB, respectively. The resultant ENOB is 9.29 bits. When the input frequency increases to Nyquist frequency, the measured SNDR and SFDR were 57.1 dB and 77.1 dB, respectively. The effective resolution bandwidth (ERBW) is higher than 160 MHz. According to Walden FoM equation

$$\mathrm{FoM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} \times f_s}. \tag{3}$$

The resultant FoMs are 6.8 and 7.3 fJ/conversion-step at low and Nyquist frequency, respectively.

To achieve 320 MS/s sampling rate with a 1 V supply, the 12th bit-cycle of SAR conversion is skipped to extend sampling time. The sampling time is about 40% of clock cycle in this condition, and the power consumption is 1.52 mW. Fig. 17 plots the measured SNDR and SFDR values versus the input frequency at 320 MS/s. At low input frequency, the measured SNDR and SFDR are 57.1 dB and 78.1 dB, respectively. The resultant ENOB is 9.20 bits. When the input frequency increases to Nyquist frequency, the measured SNDR and SFDR were 50.9 dB and 58.6 dB, respectively. The ERBW is higher than 100 MHz. The resultant FoMs are 8.1 and 16.5 fJ/conversion step at low and Nyquist frequency, respectively. The sampling bandwidth

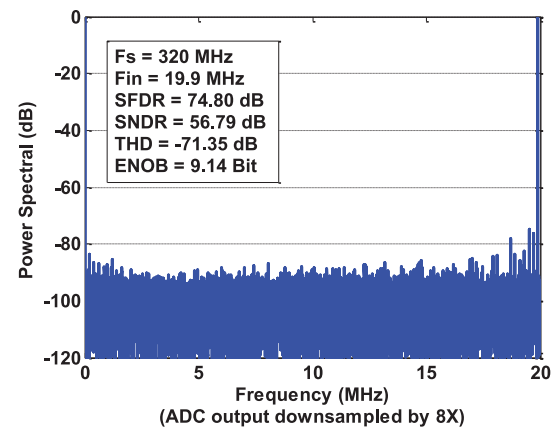

Fig. 18. FFT plot with 19.9-MHz input frequency at 320 MS/s.

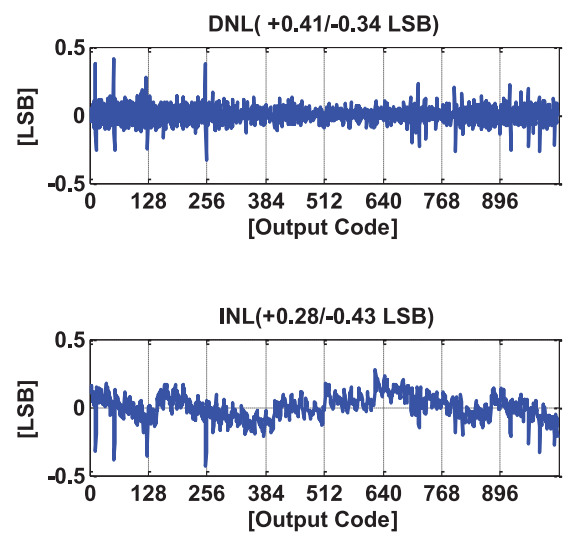

Fig. 19. Measured DNL and INL.

TABLE III
SUMMARY OF PERFORMANCE

Specification (Unit)	Experimental Result	
Technology	20nm 1P8M CMOS	
Resolution (bit)	10	
Supply Voltage (V)	0.9	1
Sampling Rate (MS/s)	160	320
Sampling Duty-cycle (%)	50	40
Total Bit-cycle (cycles)	12	11
Input Range (V_{P-P})	1	
Sampling Capacitance (fF)	540	
Active Area (μm^2)	1155	
DNL / INL (LSB)	-0.34~0.41 / -0.43~0.28	
ENOB (bit)	9.29	9.20
Power (mW)	0.68	1.52
FoM@ DC (fJ/Conv.-step)	6.8	8.1
FoM@ Nyquist (fJ/Conv.-step)	7.3	16.5

is limited by the resistance in ADC test path (includes the ESD protection resistor, routing resistor and switch on-resistor, total about 500 Ω according to postlayout extraction), which slows down the slewing during ADC sampling. Fig. 18 shows the FFT plot at 19.9-MHz input and 320 MS/s sampling frequency. The measured SNDR, SFDR, THD are 56.8 dB, 74.8 dB and −71.3 dB, respectively.

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TABLE IV
COMPARISON TO STATE-OF-THE-ART WORKS

	[7] ISSCC'10	[15] VLSI'12	[16] VLSI'13	[19] ASSCC'13	[23] VLSI'11	This Work	
Architecture	SAR	Interleaving Pipelined-SAR	Interleaving Pipelined-SAR	SAR	Pipelined	SAR	
Technology (nm)	65	65	28	40	90	20	
Resolution (bit)	10	10	11	10	10	10	
Sampling Rate (MS/s)	100	500	410	200	320	160	320
Supply Voltage (V)	1.2	1.2	0.9	0.9	1.2	0.9	1
Input Swing (V_{P-P})	2	2.4	1.8	1.8	-	1	
Power (mW)	1.13	8.2	2.1	0.82	40	0.68	1.52
SNDR (dB)	59.0	55.4	59.8	57.2	53.0	57.7	57.1
Area (mm^2)	0.026	0.046	0.11	0.013	0.46	0.0012	
FoM@ DC (fJ/Conv.-step)	15.5	34	6.5	7.0	390	6.8	8.1
FoM@ Nyquist (fJ/Conv.-step)	21.9	45.2	11.4	13.9	780	7.3	16.5

Fig. 19 shows the measured static performance at 160 MS/s. The DNL is within $-0.34/+0.41$ LSB and the INL is within $-0.43/+0.28$ LSB. A summary of the ADC performance is listed in Table III.Table IV compares the proposed ADC with the state-of the-art ADCs. With similar conversion rate and resolution, the proposed SAR achieves similar FOM with only 1-V_{P-P} input signal swing and 10 X smaller area compared to those works. The prototype ADC is the fast and smallest 10 bit non-interleaving SAR ADC so far.

V. CONCLUSION

In this paper, a binary-scaled recombination redundant algorithm is proposed to overcome the reference buffer and DAC settling issue in high-speed SAR ADCs. A small size but well matched MOM capacitor cell is used in this prototype to reduce the total sampling capacitance and the active area. The standard library based design helps to reduce the design and layout time of digital sub-circuits. The prototype ADC achieves 320 MS/s operation speed with an ERBW more than 100 MHz. It achieves a FoM of 8.1 fJ/conversion-step and only occupies an active area of 0.052 mm^2 in a 20-nm CMOS technology. The experimental results demonstrate the power and hardware efficiency and also high-speed potential of the proposed SAR ADC and make it suitable for the IEEE 802.11ac applications.

ACKNOWLEDGMENT

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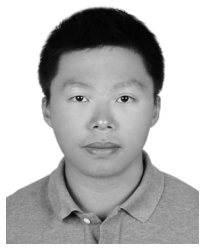

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