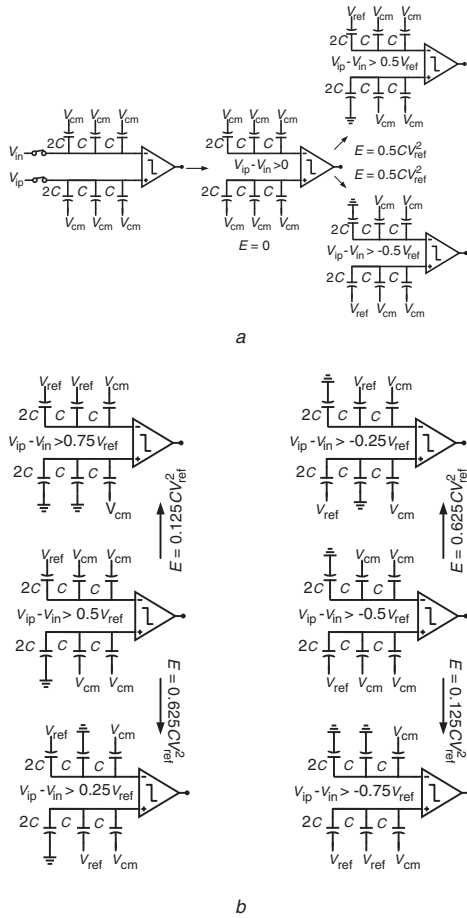


# Merged capacitor switching based SAR ADC with highest switching energy-efficiency

V. Hariprasath, J. Guerber, S.-H. Lee and U.-K. Moon

A modified merged capacitor switching (MCS) scheme is proposed for the successive approximation register (SAR) analogue-to-digital converter (ADC). The conventional MCS technique previously applied to a pipelined ADC improves signal processing speed and, with use in the SAR ADC, this scheme achieves lowest switching energy among existing switching schemes. The MCS scheme achieves 93.4% less switching energy as compared to the conventional architecture.

**Introduction:** The capacitive array digital-to-analogue converter (D/A) in the feedback path of the SAR ADC approximates the sampled input voltage after every comparison. The conventional capacitor array switching scheme of the SAR ADC is energy inefficient [1] in performing this approximation. This Letter explains the MCS scheme [2] for a SAR ADC and enumerates the advantages of this scheme in comparison with the present techniques.



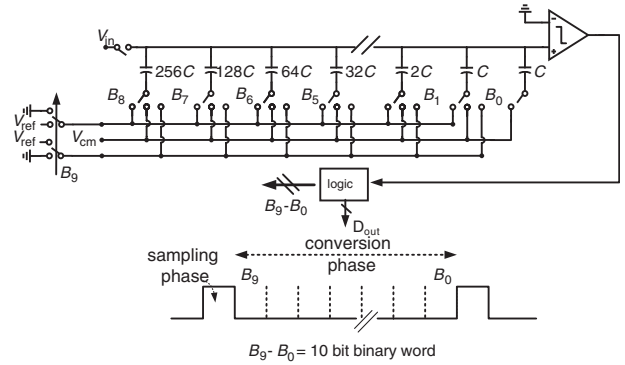
**Fig. 1** Merged capacitor switching scheme and energy consumption

**Merged capacitor switching scheme:** The energy consumption of a 3-bit conventional switching scheme is described in [3]. The energy consumption is quite different for the ‘UP’ and ‘DOWN’ transitions [1]. In particular, the conventional SAR switching scheme consumes five times more energy for a ‘DOWN’ transition as compared to the corresponding ‘UP’ transition, as illustrated in [3]. This inefficiency in switching energy leads to increased power consumption, dynamic settling errors in references and in turn limits the speed of the converter. A three-level capacitor array D/A with series capacitor coupling was used in [4] to partially address some of the above inefficiencies with the added cost of calibration and additional digital complexity.

A 3-bit MCS scheme is shown in Figs. 1a and b. The input is sampled onto the virtual node. The first comparison does not consume any switching energy as compared to the conventional scheme. Further, ‘UP’ and ‘DOWN’ transitions are symmetrical and consume equal

energy. In particular, ‘UP’ and ‘DOWN’ transitions consume energy of  $0.5 CV_{ref}^2$  J.

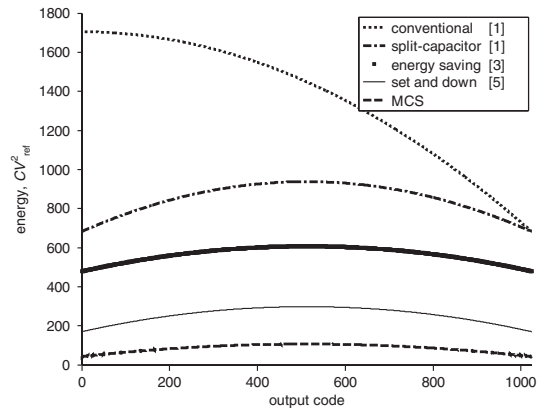
A single-ended implementation of the proposed 10-bit ADC implementation of the MCS SAR is shown in Fig. 2. The switching network, number of cycles and logic complexity is the same as that of the conventional switching scheme. The following Sections elaborate on switching energy and matching requirements for a 10-bit MCS SAR.



**Fig. 2** 10-bit MCS-SAR ADC

**SAR switching energy:** The average energy required for charging and discharging the SAR capacitor array determines the efficiency of the switching scheme [1]. The average switching energy for different switching schemes [1, 3, 5] was compared through a behavioural simulation of a 10-bit SAR ADC. The switching energy efficiency for different schemes is discussed below.

The behavioural simulation of average switching energy for different schemes is shown in Fig. 3. With respect to the conventional switching technique, the split-capacitor scheme [1] achieves 37.4% ( $E_{avg} = 852.3 CV_{ref}^2$ ), the energy-saving scheme [3] achieves 58.7% ( $E_{avg} = 563.8 CV_{ref}^2$ ) and the set and down scheme [5] achieves 81% ( $E_{avg} = 255 CV_{ref}^2$ ). However, these switching schemes achieve energy savings at the cost of increased digital switching complexity, common mode variation and matching requirements.



**Fig. 3** Switching energy comparison

The MCS scheme is 93.4% ( $E_{avg} = 84.7 CV_{ref}^2$ ) more efficient than the conventional switching scheme and is the highest reported switching energy efficiency among existing methods. Average switching energy for the different switching schemes and the proposed switching scheme is given below:

$$\text{conventional scheme [1]} \quad E_{avg} \simeq \sum_{i=1}^n 2^{n+1-2i} (2^i - 1) CV_{ref}^2 \text{ J} \quad (1)$$

$$\text{energy saving scheme [3]} \quad E_{avg} \simeq 3.2^{n-3} + \sum_{i=3}^n 2^{n+1-2i} (2^{i-1} - 1) CV_{ref}^2 \text{ J} \quad (2)$$

$$\text{set and down scheme [5]} \quad E_{avg} \simeq \sum_{i=1}^n 2^{n-2-i} CV_{ref}^2 \text{ J} \quad (3)$$

$$\text{MCS scheme } E_{\text{avg}} \simeq \sum_{i=1}^{n-1} 2^{n-3-2i} \times (2^i - 1) C V_{\text{ref}}^2 J \quad (4)$$

**INL and DNL requirements:** The unit capacitor in the SAR ADC capacitor array is typically limited by matching requirements. The variation in unit capacitors was assumed to be Gaussian distributed ( $N(0, \sigma^2)$ ), where  $\sigma$  is the standard deviation of matching between unit capacitors. Assuming  $V_{\text{ref}}$  and GND as the reference levels for the capacitor array D/A, the INL and DNL requirement for an 'n' bit conventional converter can be derived as follows:

$$V_{\text{out}}(n) = \frac{\sum_{i=1}^{n-1} (C_i + \Delta C_i) b_i}{C_{\text{total}}} V_{\text{ref}} = D_{\text{out}} V_{\text{ref}} \quad (5)$$

$$DNL(n) = V_{\text{out}}(n) - V_{\text{out}}(n-1), \text{INL}(n) = V_{\text{out}}(n) - V_{\text{ideal}}(n) \quad (6)$$

$$E(DNL^2)_{\text{max}} = 2^n \sigma^2, \quad \sigma_{DNL, \text{max}} = 2^{n/2} \sigma \quad (7)$$

$$E(INL^2)_{\text{max}} = 2^{n-2} \sigma^2, \quad \sigma_{INL, \text{max}} = 0.5 \times 2^{n/2} \sigma \quad (8)$$

where  $D_{\text{out}}$  is the output code of the ADC, and  $V_{\text{out}}(n)$ ,  $\Delta C_i$ ,  $C_{\text{total}}$  are the reference voltage, mismatch and total capacitance of the capacitive array D/A. The total capacitance was assumed to be constant for all the switching schemes. The INL and DNL requirements for the different switching schemes are shown in Table 1.

**Table 1:** INL and DNL comparison for 10bit SAR ADC

Switching scheme	$\sigma_{INL, \text{max}}, \text{LSB}$	$\sigma_{DNL, \text{max}}, \text{LSB}$
Conventional [1]	$16\sigma$	$32\sigma$
Split-capacitor [1]	$16\sigma$	$\frac{32\sigma}{\sqrt{2}}$
Energy saving [3]	$16\sigma$	$32\sigma$
Set and down [5]	$16\sigma$	$32\sigma$
MCS	$\frac{16\sigma}{\sqrt{2}}$	$\frac{32\sigma}{\sqrt{2}}$

The unit-capacitance for MCS SAR is twice that of the conventional SAR ADC when sized for the same  $kT/C$  noise consideration, which

results in improved INL and DNL performance as compared to a conventional architecture.

**Conclusions:** A three-level capacitor switching scheme is proposed for SAR ADC. This switching scheme achieves the highest switching energy efficiency among the existing switching schemes while reducing static linearity requirements. The MCS scheme also has relaxed matching requirements for the capacitor array without increasing the complexity of digital logic and switches.

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