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# A Two-Stage Weighted Capacitor Network for D/A-A/D Conversion

Y. S. YEE, L. M. TERMAN, AND L. G. HELLER

*Abstract*—**A two-stage weighted capacitor network for A/D and D/A conversion utilizing a feedback amplifier is described. The two-stage weighted capacitor DAC requires a smaller range of capacitor values than the conventional weighted capacitor DAC and is not subject to the nonlinear effects of parasitic capacitance. Experimental results of such a DAC implemented using a conventional n-channel metal-gate MOS process are presented. A discussion of the comparative accuracy and area of one- and two-stage weighted capacitor DAC's on the basis of capacitor tracking is given.**

## I. INTRODUCTION

The use of a weighted capacitor network for A to D conversion has been reported by McCreary and Gray [1]. More recently, the use of a two-stage weighted capacitor D to A converter (WCDAC) has been discussed by Yee [2] and Ohri and Callahan [3], [4]. This paper describes the design and operation of a two-stage WCDAC that is somewhat different from that given by Ohri and Callahan, and also presents a discussion of the comparative accuracy and area of one- and two-stage WCDAC networks.

The circuit is shown in Fig. 1. It consists of two weighted capacitor stages connected by a coupling capacitor $C_S$. A high-gain amplifier is connected in its inverting configuration with the $2C$ capacitor fed back from the output to the negative input. Because of the negative feedback and high gain of the amplifier, the input node of the amplifier is a virtual ground during a DAC operation, and the amplifier serves to integrate charge injected onto the input node. Nonlinear capacitor effects are virtually eliminated since the input node of the amplifier is a virtual ground, and the common node of the second stage is fabricated on the metal side of the capacitors, eliminating nonlinear diffusion capacitance on the node. The function of charge integration while the input node acts as a virtual ground potential can also be accomplished by connecting the node to the source of a bucket brigade device. However, this allows only a single polarity output.

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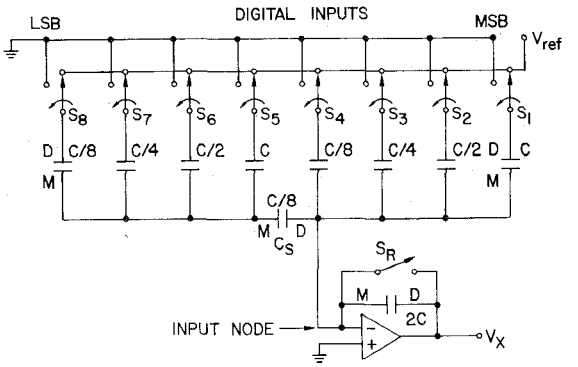


Fig. 1. A two-stage weighted capacitor DAC. "*D*" indicates the diffused capacitor plate, and "*M*" indicates the metal capacitor plate.

In the circuit of Fig. 1 all capacitor values are an integral multiple of the smallest capacitor. This permits fabrication of the larger capacitors by replication of the minimum capacitor, which is advantageous to eliminate capacitor tracking errors due to process biases [1]. The D to A conversion cycle is accomplished by initially resetting the $2C$ capacitor with $S_R$ and setting the input switches to $V_{\text{ref}}$. After $S_R$ is opened, the switches associated with input "1's" are switched to ground, and the amplifier integrates the charge coupled into the input node. Inputs 5-8 couple the correct charge to the input node because it is a virtual ground.

Offsets in the DAC system can be cancelled by adding sufficient low-order bits to the DAC to achieve the desired granularity, determining the necessary input bit pattern to cancel the offset in a preconditioning cycle, and then adding that input to subsequent conversions. The low-order bits may be added by extending the range of the DAC with additional capacitors, or by a network connected in parallel to the input node of the amplifier. The preconditioning cycle can be performed periodically to adaptively take into account changes due to ambient or aging.

## II. EXPERIMENTAL RESULTS

An 8-bit DAC with two four-capacitor stages was fabricated and tested. An extra bit of dynamic range is achievable since the DAC can provide both positive and negative outputs simply by initializing the digital input switches at either $V_{\text{ref}}$ or ground during the reset phase of a DAC operation.

On the test chip metal-to-diffusion capacitors were used, with the metal plates connected as indicated in Fig. 1 to reduce nonlinear effects. More specifically, the series capacitor $C_S$ is fabricated with the diffused plate connected to the input node, and the metal plate of the $2C$ feedback capacitor is also connected to the input node. In the test circuit, $S_R$ is implemented with a simple MOS device switch, and a dummy device is included for first-order cancellation of the turn-off transient coupled into the $2C$ capacitor. The elemental capacitor in the two-stage network consists of two square MOS capacitor structures with the diffused plates connected together on one side to form a rectangular capacitor element. All other capacitors in the network are formed by repeating this basic element. This layout approach is taken to enhance accuracy by cancelling edge etch bias effects and effects due to unwanted thick oxide capacitance, as well as undesirable effects due to mask misalignment.

Only the two-stage weighted network was fabricated on the test site. The amplifier and the switching arrangements were provided off-chip, although these could be put on-chip in

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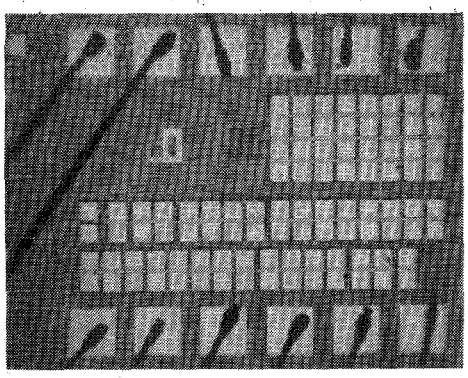


Fig. 2. Photomicrograph of the two-stage weighted capacitor DAC test site.

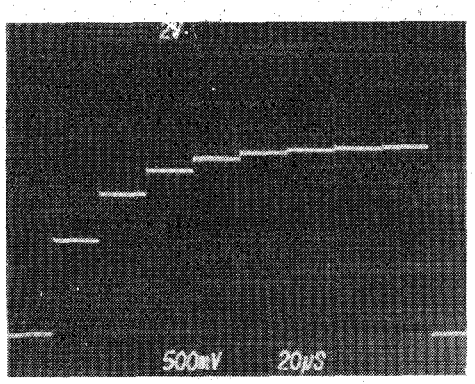
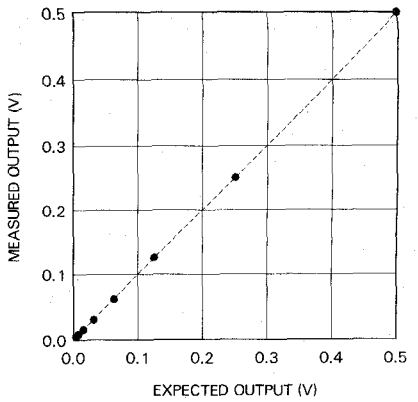
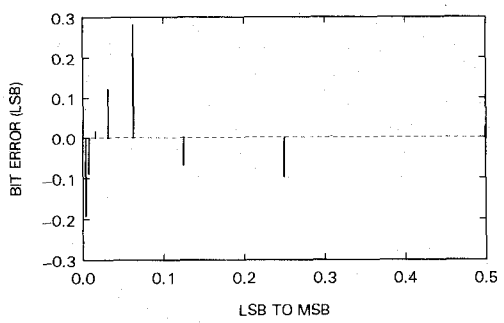



Fig. 3. DAC output. Full scale is 2 V.




(a)




(b)

Fig. 4. (a) 8-bit two-stage weighted capacitor DAC overall accuracy. (b) 8-bit two-stage weighted capacitor DAC bit-scan linearity plot.

practice [5], [6]. Although not included on this test site, the addition of a metal border structure surrounding all the MOS capacitors to provide identical etching boundary conditions for each side of every capacitor should further enhance tracking accuracy.

The test site was fabricated using a conventional metal-gate n-channel MOSFET process with 0.22 mil (5.5 $\mu$m) metal linewidths and 680 Å thin oxide. Capacitor $C$ has a value of about 16 pF. The silicon area occupied by the DAC network is about 40 X 25 mils. A photomicrograph of the test site is shown in Fig. 2. The experimental waveform for cumulative DAC output as progressively lower order bits are switched in is shown in Fig. 3. As indicated in Fig. 4 and Table I, experimental results showed that the DAC has a linearity better than 8 bits, and an overall accuracy of approximately 8 bits ($\pm\frac{1}{2}$ LSB). The accuracy was measured by sampling and holding each step and measuring the step sizes with an accurate digital voltmeter.

## III. Effect of Capacitor Tracking on Accuracy

It is of interest to compare the potential accuracy and area of the two-stage weighted capacitor DAC and the conventional single-stage approach, both implemented using the feedback amplifier, shown in Fig. 5. Nonlinear capacitance effects are virtually eliminated with the pinning of the input node by the amplifier and appropriate layout. The major remaining source of error is capacitor tracking. The two-stage WCDAC requires a range of capacitor values smaller by $2^{n/2}$ for $n$ bits. This may, or may not, result in a significant area or accuracy improvement, depending upon the sources of tracking errors, their distribution, variation with capacitor size, etc.

One limiting case occurs as tracking error between capacitors approaches zero; adequate DAC accuracy can be obtained using equal minimum capacitors in both circuits, and the total capacitance required for the two-stage WCDAC will be smaller by approximately $(\frac{1}{2})\ 2^{n/2}$. The area will be small by essentially the same ratio.

An alternate model is to assume that wafer dimensions have some random variation $\Delta L$ which is independent of $L$ and is normally distributed (this will be called the constant $\Delta L$ model). The resulting variation in capacitor values will then also be normally distributed. Since larger capacitors are

TABLE I
8-Bit Two-Stage Weighted Capacitor DAC Overall Accuracy

| | Measured Output $V_x$ (V) | Expected Output $V_x$ (V) | Error $\Delta V$ (mV) |
|---|---|---|---|
| 1 (MSB) | .5000 | .5000 | 0 |
| 2 | .2503 | .2500 | + .3 |
| 3 | .1251 | .1250 | + .1 |
| 4 | .0612 | .0625 | -1.3 |
| 5 | .0305 | .03125 | - .7 |
| 6 | .0153 | .0156 | - .3 |
| 7 | .0079 | .0078 | + .1 |
| 8 (LSB) | .0044 | .0039 | + .5 |

Total (+) Error = 1.0 mV ~1/4 LSB

Total (-) Error = 2.3 mV ≳1/2 LSB

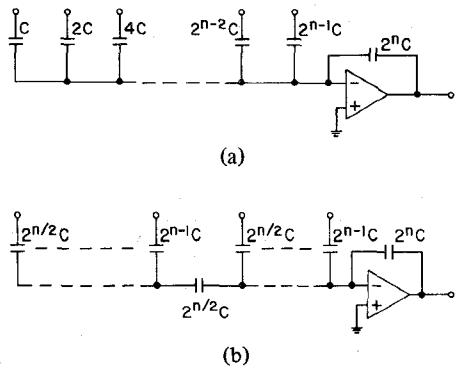



Fig. 5. (a) One-stage WCDAC. (b) Two-stage WCDAC.

made by replicating an elemental capacitor, any consistent error (such as from process biases) will not affect accuracy; only random variations between capacitors will contribute, and for tracking considerations the mean of $\Delta L$ may be taken as zero. The effective standard deviation $\sigma$ of a sum of normally distributed elements is the square root of the sum of the squares of the standard deviations of the individual elements:

$$\sigma_{\text{eff}} = \sqrt{\sigma_1^2 + \sigma_2^2 + \cdots}. \tag{1}$$

Let $\Delta C_0$ be the standard deviation of the elemental capacitor. A capacitor made up of $n$ elemental capacitors will have a standard deviation given by $\Delta C = \sqrt{n}\Delta C_0$. It follows that

$$\Delta C_i \propto \sqrt{C_i} \tag{2a}$$

$$\frac{\Delta C_i}{C_i} \propto \frac{1}{\sqrt{C_i}}. \tag{2b}$$

These expressions are valid whether a large capacitor is made up of $n$ smaller capacitors or is one capacitor with dimensions $\sqrt{n}$ larger. For the single capacitor case, $C \propto L^2$, $\Delta C \propto 2L\Delta L$, and thus $\Delta C \propto \sqrt{C}$ as in (2a).

For the single-stage WCDAC the standard deviation of the smallest capacitor is $\Delta C_0$, that of the next is $\sqrt{2}\Delta C_0$, and so forth up to that of the largest capacitor $\sqrt{2^{n-1}}\Delta C_0$. Applying (1), and normalizing the resulting output error voltage $\Delta V$ to the nominal maximum output signal $V_{\text{MAX}}$,

$$\left.\frac{\Delta V}{V_{\text{MAX}}}\right]_{\text{I}} = \frac{\Delta C_0}{(2^n - 1)C_0}\sqrt{2^{n-1} + 2^{n-2} + \cdots + 2 + 1}$$

$$= \frac{2^{n/2}}{(2^n - 1)}\frac{\Delta C_0}{C_0}\sqrt{\left(1 + \frac{1}{2^{n/2}}\right)\left(1 - \frac{1}{2^{n/2}}\right)} \tag{3a}$$

where $V_{\text{MAX}}$ is the signal when all the input capacitors are switched. The subscript I refers to the one-stage WCDAC; the subscript II used below refers to the two-stage WCDAC. In the first parenthetical expression under the radical sign, the "1" and "$1/2^{n/2}$" terms are the contributions of the high-order $n/2$ capacitors and the low-order $n/2$ capacitors, respectively. It is evident that the contribution of the low-order group is minor for practical values of $n$.

Similarly, for the two-stage WCDAC

$$\left.\frac{\Delta V}{V_{\text{MAX}}}\right]_{\text{II}} = \frac{\Delta C_0}{(2^n - 1)C_0}\sqrt{(2^{n-1} + 2^{n-2} + \cdots + 2^{n/2}) + \frac{1}{2^n}(2^{n-1} + 2^{n-2} + \cdots + 2^{n/2})}$$

$$= \frac{2^{n/2}}{(2^n - 1)}\frac{\Delta C_0}{C_0}\sqrt{\left(1 + \frac{1}{2^n}\right)\left(1 - \frac{1}{2^{n/2}}\right)} \tag{3b}$$

ignoring, for simplicity, the error due to the coupling capacitor between stages. As before, the two terms in the first parenthetical expression under the radical are the contributions due to the high-order and low-order stages. Again the effect of the low-order capacitors is minor.

For the constant $\Delta L$ model, if a two-stage WCDAC is designed with a given accuracy, a one-stage WCDAC can be designed with the same size high-order capacitor which will have essentially the same accuracy, but which will require about half the area (since area is proportional to the total capacitance in the network). This is quite plausible, as the higher order capacitors dominate the error voltage $\Delta V$, and if the $n/2$ low-order capacitors are disregarded, the two circuits are identical, and thus will have the same error for the same size capacitors. If the areas are made the same by reducing the size of the capacitors in the two-stage WCDAC by a factor of two, the error will increase by $\sqrt{2}$, as seen from (2a).

Some limited data which we have obtained indicate that $\Delta L$ decreases as $L$ increases. A simple model is to take $\Delta L$ proportional to $1/L$. This results in $\Delta C$ being constant, independent of capacitor size, and $\Delta C_i/C_i$ is proportional to $1/C_i$. Then, for the single-stage WCDAC

$$\left.\frac{\Delta V}{V_{\text{MAX}}}\right]_{\text{I}} = \frac{2^{n/2}}{(2^n - 1)}\frac{\Delta C_0}{C_0}\sqrt{\left(1 + \frac{1}{2^{n/2}}\right)\left(1 - \frac{1}{2^{n/2}}\right)} \tag{4a}$$

as before, and for the two-stage WCDAC

$$\left.\frac{\Delta V}{V_{\text{MAX}}}\right]_{\text{II}} = \frac{2^{n/4}}{(2^n - 1)}\frac{\Delta C_0}{C_0}\sqrt{\left(1 + \frac{1}{2^n}\right)\left(1 - \frac{1}{2^{n/2}}\right)}. \tag{4b}$$

Thus,

$$\frac{\Delta V_{\text{I}}}{\Delta V_{\text{II}}} \cong 2^{n/4}$$

for the same areas; increasing the elemental capacitor size in the one-stage WCDAC to give the same accuracy, the area ratio becomes

$$\frac{A_{\text{I}}}{A_{\text{II}}} \cong 2^{n/4-1}.$$

The advantage for the two-stage WCDAC in this model arises from making the elemental capacitor as a single capacitor larger by $2^{n/2}$ than the elemental capacitor for the single-stage case.

It is not clear which of the above models most closely approximates reality. No data on capacitor tracking are available in the literature, and in any case it could vary, depending upon the individual facility and process used. Our measurements of capacitor tracking were made on a small sample. However, because it requires a smaller range of capacitor values for a given number of bits, the two-stage WCDAC may permit smaller area or better accuracy than the single-stage WCDAC in a practical manufacturing environment.

## ACKNOWLEDGMENT

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## Realization of an All-Pass Network with a New Simple Circuit

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*Abstract*–**This correspondence shows the realization of the first-order all-pass network with a new simple circuit. This circuit can be integrated and used at frequencies less than about 4 MHz.**

All-pass networks have been usually constructed by using operational amplifiers [1]–[4]. We constructed the network using a new simple circuit. Fig. 1 shows an all-pass network. $Tr_1$ and $Tr_2$ which form a p-n-p-n structure constitute negative impedance circuit. $Tr_2$ is constructed by two matched high $\alpha$ n-p-n transistors, as shown in Fig. 1, to provide a compound n-p-n transistor whose equivalent $\alpha$ is almost equal to 0.5. $R_{g1}$ and $R_{g2}$ are bias resistors for the negative impedance circuit. The circuit formed by $Tr_3$, $R_{b1}$, $R_{b2}$, and $R_e$ is a voltage-controlled current source in an ac operation and is a constant current source in a dc operation. Fig. 2 shows its ac equivalent circuit. The voltage transfer function of the network in Fig. 2 is

$$\frac{V_2}{V_1}=\frac{\alpha_3}{R_e}\frac{(R_p-R_c-r_d)-j\omega C_pR_p(R_c+r_d)}{1+j\omega C_pR_p}. \tag{1}$$

When

$$R_c+r_d=R_p/2$$

and $\alpha_3R_p/2R_e$ is set equal to $H$, then (1) can be written as

$$\frac{V_2}{V_1}=H\frac{1-j\omega C_pR_p}{1+j\omega C_pR_p}\equiv e^{-(\alpha+j\beta)}. \tag{2}$$

Thus (2) is exhibiting the all-pass property of this network. $R_p$, $C_p$, and $r_d$ which are equivalent network elements defined

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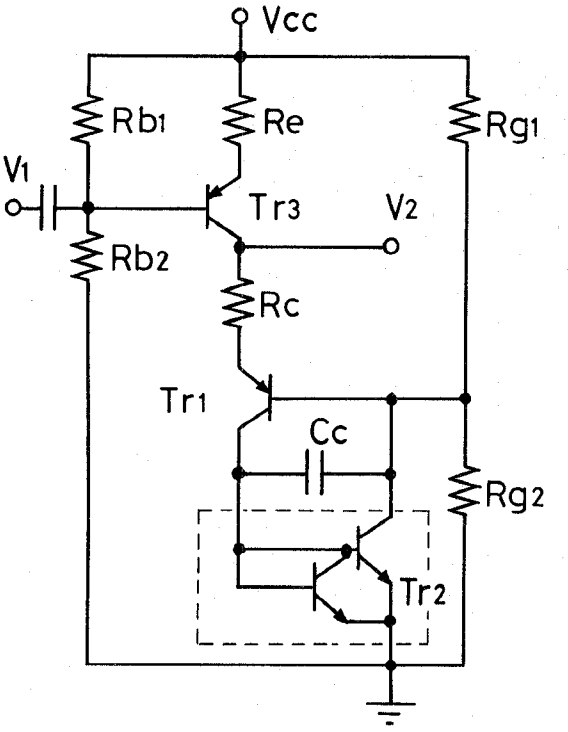


Fig. 1. All-pass network circuit.

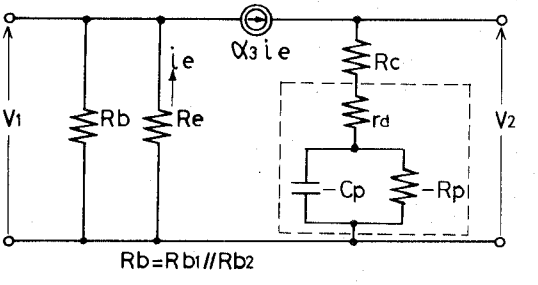


Fig. 2. AC equivalent circuit of Fig. 1.

in the derivation of Fig. 2 are given by

$$R_p=\left(\frac{\alpha_1+\alpha_2-1}{1-\alpha_2}+\frac{r_{e2}}{R_g+r_{e2}}\right)R_g \tag{3}$$

$$C_p=\frac{(R_g+r_{e2})^2}{\{(\alpha_1+\alpha_2-1)(R_g+r_{e2})+(1-\alpha_2)r_{e2}\}R_g}C_c \tag{4}$$

$$r_d=r_{e1}+\frac{r_{e2}R_g}{r_{e2}+R_g} \tag{5}$$

where

$$R_g=\frac{R_{g1}R_{g2}}{R_{g1}+R_{g2}}$$

$\alpha_1$ = common-base small-signal current gain of the p-n-p transistor $Tr_1$,
$\alpha_2$ = equivalent common-base small-signal current gain of the compound n-p-n transistor $Tr_2$,
$r_{e1}$ = emitter resistance of the p-n-p transistor $Tr_1$,
$r_{e2}$ = equivalent emitter resistance of the compound n-p-n transistor $Tr_2$.