Mead Education

Advanced Engineering Course on

Low-Power Analog IC Design

EPFL Premises, Lausanne, Switzerland
August 29 – September 2, 2022

Friday, September 2, 2022

Kofi Makinwa, TU Delft, Netherlands

- **Micropower ADCs**

Micropower ADCs

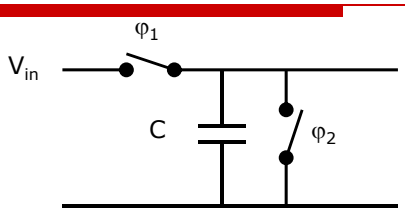
Kofi Makinwa

Electronic Instrumentation Laboratory
Delft University of Technology
Delft, The Netherlands

What is a Micropower ADC?

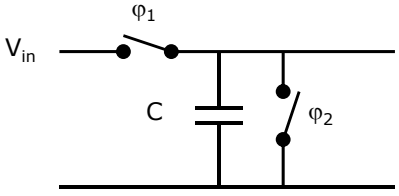
- One that draws less than 1mW
  ➔ a few hundred μAs from a 1V supply
- So not very fast: f_s <100MHz
  charging 1pF with 100μA ➔ 10ns for a 1V swing
- Typical applications:
  - sensor interfaces
  - battery monitoring circuits
  - medical devices
  - short-range radios

Fundamental Limits (Power)



- Cap is charged and discharged ➔ $P_{min} = CV_{FS}^2 \bullet f_S$
- So micropower design
  ➔ reduce caps, reduce swing and reduce frequency
- Main limitations are kT/C noise and mismatch
- Note: Continuous-time circuits avoid kT/C noise limitations but are usually much less accurate

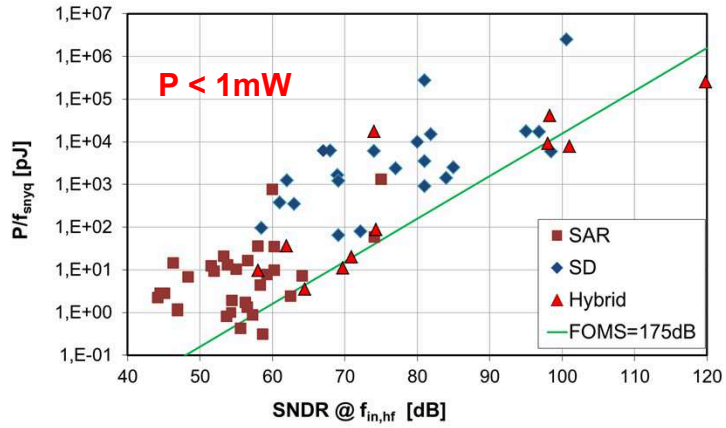
Fundamental Limits (Efficiency)



- Inband noise: $V_n^2 = (kT/C)\bullet(f_{NYQ}/f_S)$
- Signal energy: $V_{in}^2 = (V_{FS}/2)^2/2$
- So SNR = $V_{in}^2 / V_n^2 = (CV_{FS}^2/8kT)\bullet(f_S/f_{NYQ})$
- But $E_{min} = P_{min}/f_{NYQ} = CV_{FS}^2 \bullet (f_S/f_{NYQ})$ = **8kT*SNR**

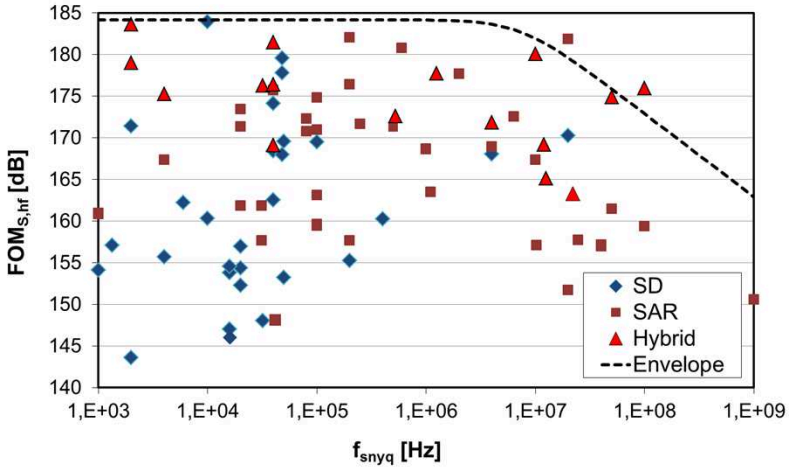
- Linear trade-off between Energy and SNR
- Schreier figure of merit (FOM_S) = $(SNDR)_{dB}$ + 10log(BW/P)

Energy vs. SNDR by Architecture



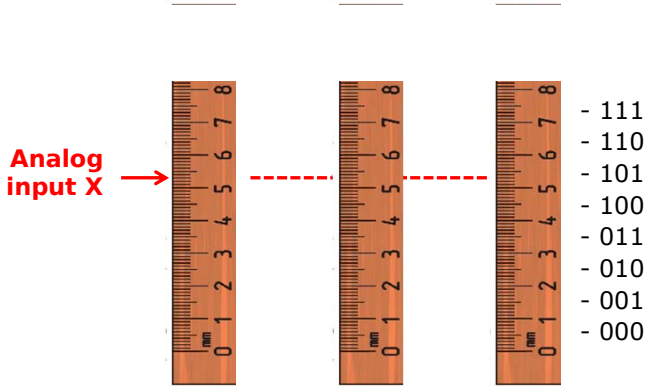
- B. Murmann, "ADC Performance Survey 1997-2016," [Online]
- Micropower ➔ SAR or ΣΔ ADCs (> 10 bits)

BW vs. Efficiency by Architecture



- Micropower **and** BW > 100kHz ➔ SAR or Hybrid ADCs

3-bit Successive Approximation



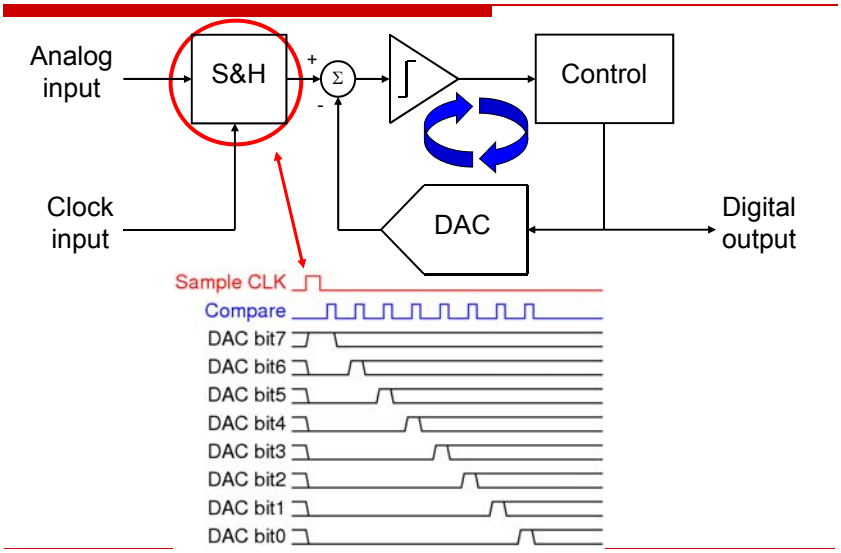
SAR ADCs

SAR ADC = Cap DAC and Comparator

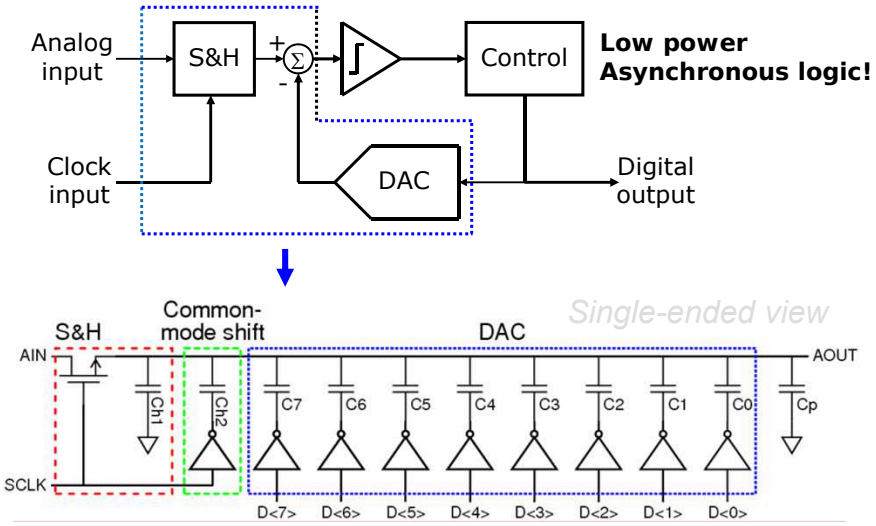
- Only one active component
- Scaling & calibration allows tiny unit caps (< 0.5fF)
  ➔ CV^2 power is dramatically reduced
- But matching limits resolution (and accuracy) to
  < 12b unless calibration is used ➔ nm-CMOS

- Case Study
  - P. Harpe et al., "A 30fJ/Conversion-Step 8b 0-to-10MS/s Asynchronous SAR ADC in 90nm CMOS," ISSCC 2010

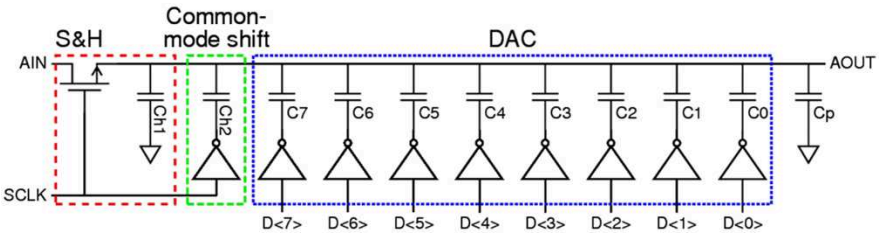
SAR ADC Architecture



Switched Capacitor Architecture



Capacitor Sizing



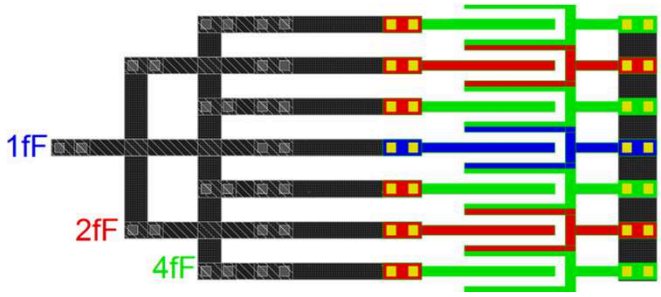
- C_{h1}: 0.5pF
- C_{h2}: 0.25pF
- kT/C-related SNR: 65dB

- C_{dac} (sum $C_7 \cdots C_0$): 0.25pF
- C_p (parasitics): 0.25pF

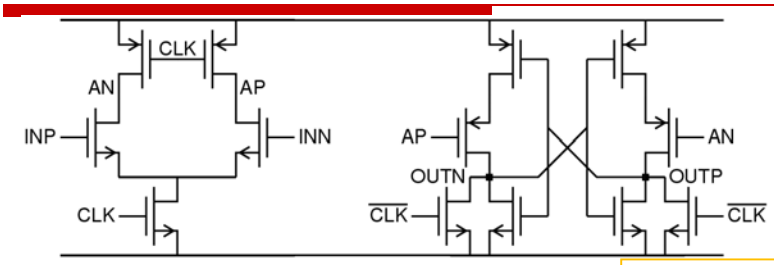
➔ Precise 1fF unit element required

Capacitor Implementation

- Custom 1fF cap ➔ m4 to m7 stacked, min. width/spacing
- Symmetric layout for matching

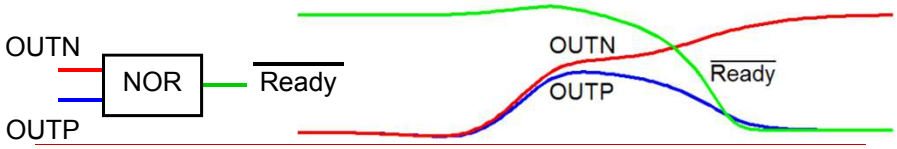


Comparator Design

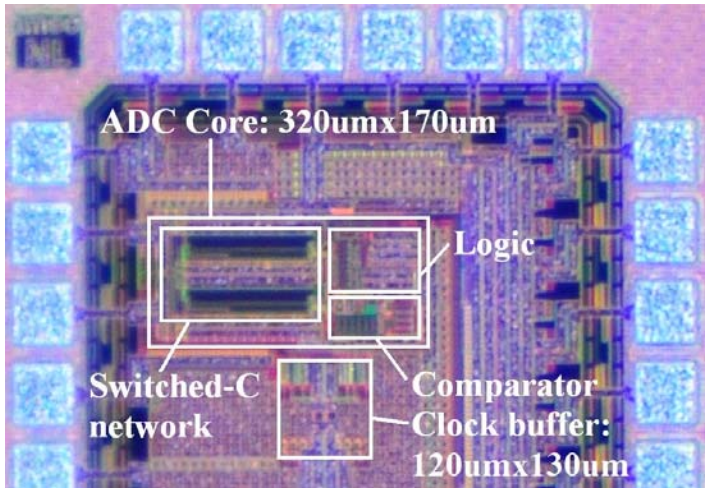


Van Elzakker, ISSCC 2008

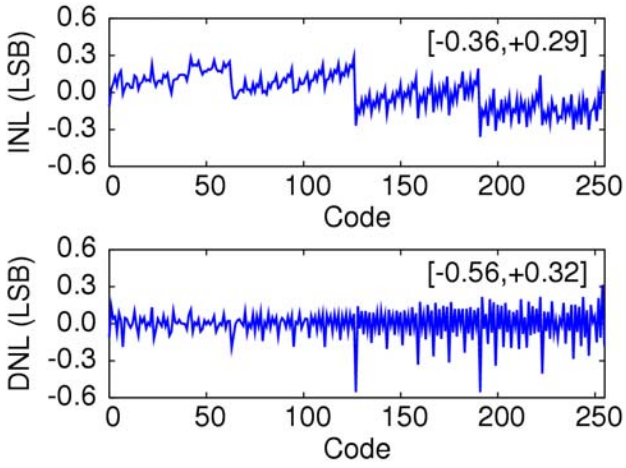
- Dynamic design ➔ power ∝ sampling rate
- NOR on differential output generates READY-flag for asynchronous logic



Layout ADC (90nm CMOS)

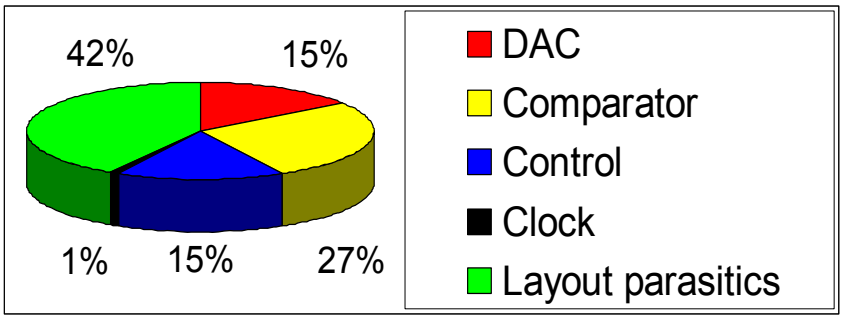


Measured INL/DNL



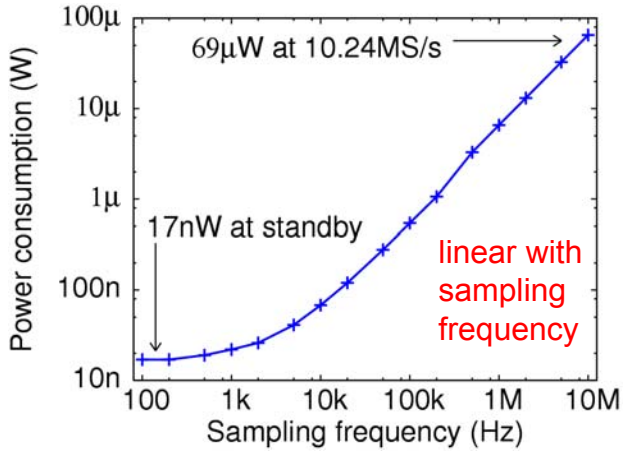
- INL_{max} = 0.36LSB, DNL_{max} = 0.56LSB

Simulated Power Breakdown



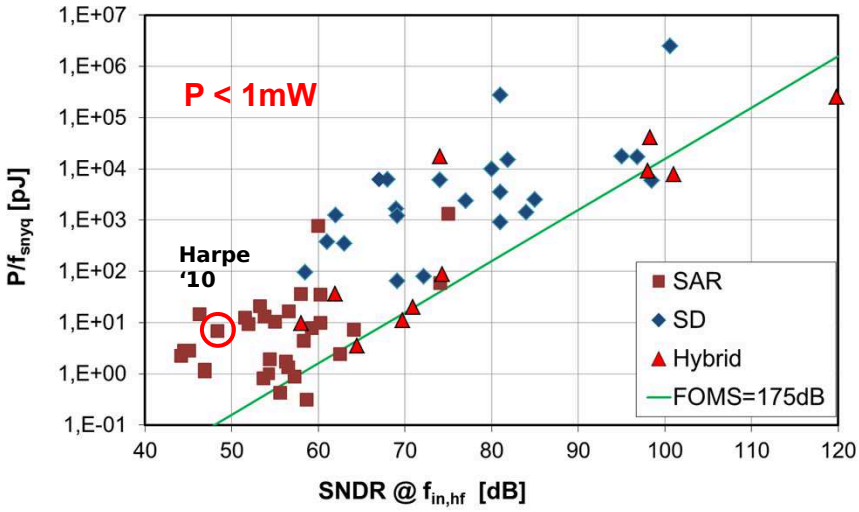
- Power consumption is dominated by layout parasitics, mainly digital interconnect

Measured Power Consumption



- 30fJ/conv-step FoM maintained from 10kS/s to 10MS/s

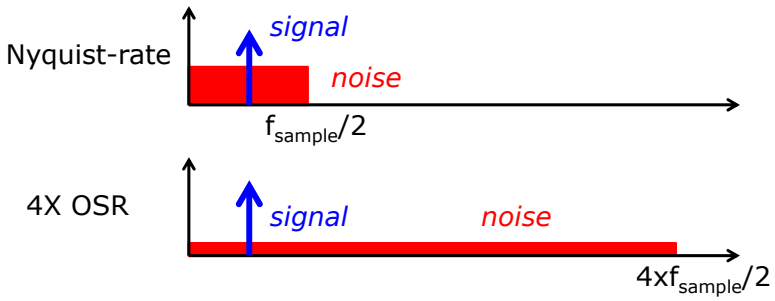
Benchmarking



Further Developments

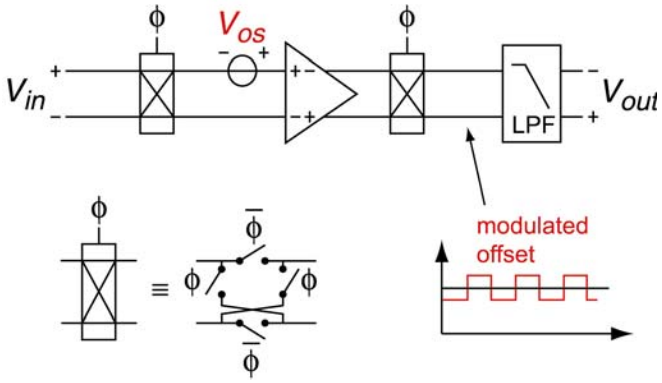
- Lower power ➔ smaller DAC caps (< 0.5fF)
- Lower power ➔ Variable comparator power
  - coarse conversions ➔ low power
  - fine (critical) conversions ➔ higher power OR multiple conversions plus averaging / majority voting)
- Lower power ➔ Optimized DAC switching schemes
  - Minimize energy needed to charge/discharge DAC caps
- Higher resolution
  - Scaling ➔ better lithography
  - Calibration ➔ up to 20b resolution
  - Oversampling & noise-shaping

Over-Sampling



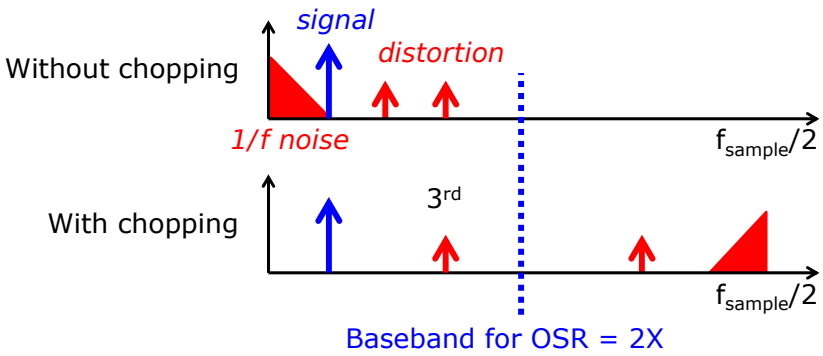
- Flexible trade-off between BW and resolution
- 4x over-sampling ➔ 6dB increase in in-band SNR
- Case Study
  - P. Harpe et al., "An Oversampled 12/14b SAR ADC with Noise Reduction and Linearity Enhancements Achieving up to 79.1dB SNDR," ISSCC 2014

Chopping (1)



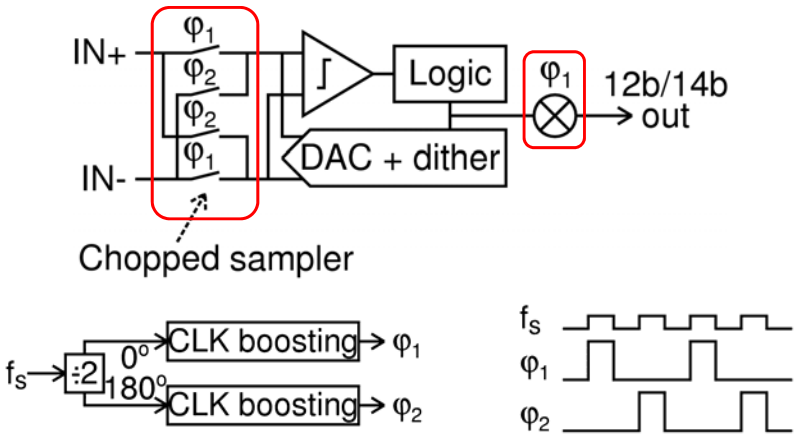
- Modulates Offset (and 1/*f* noise) away from DC
- LPF needed to remove up-modulated ripple

Chopping (2)



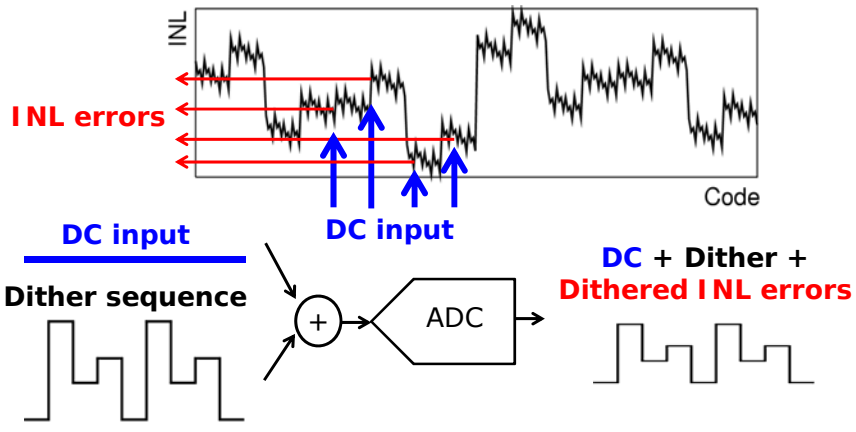
- Chopping also mitigates **even-order** distortion
- Decimation filter removes up-modulated ripple

Chopping Implementation



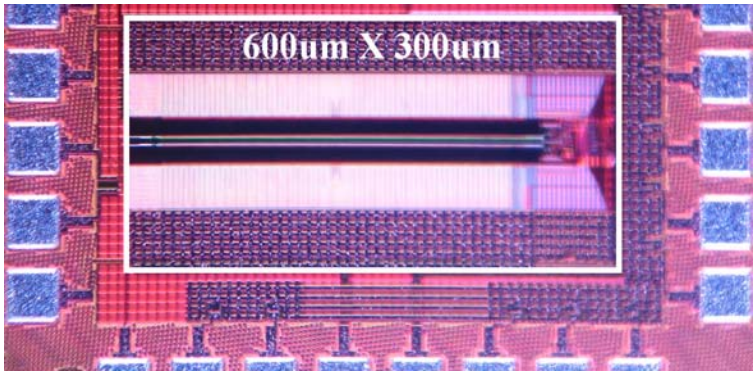
- Negligible power/area overhead

Dither



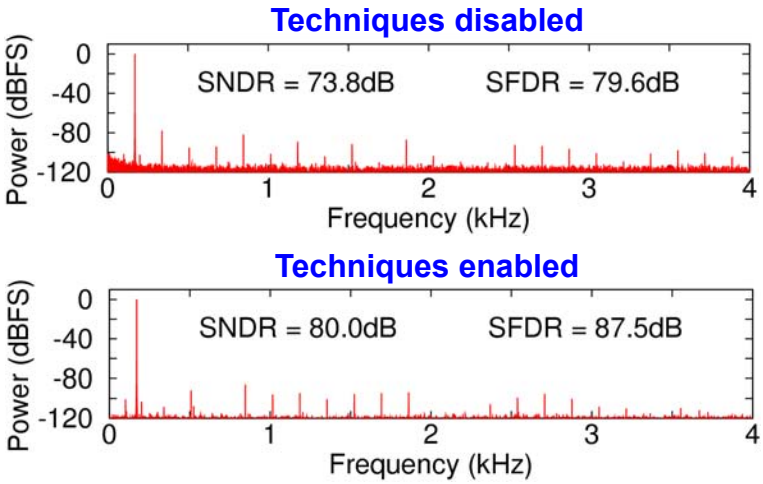
- Add deterministic dither **before** AD conversion
  ➔ modulate INL/DNL errors out of band

Die Photo, 65nm CMOS



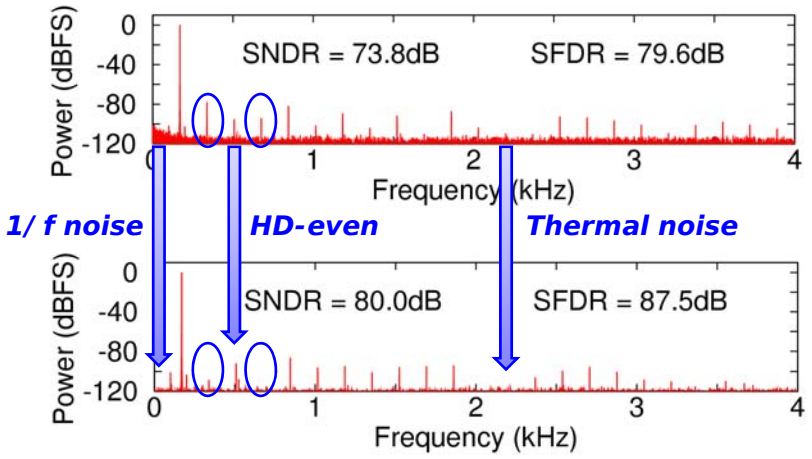
- Total area: 0.18mm^2
- Area includes supply/reference decoupling caps

Measurement Results

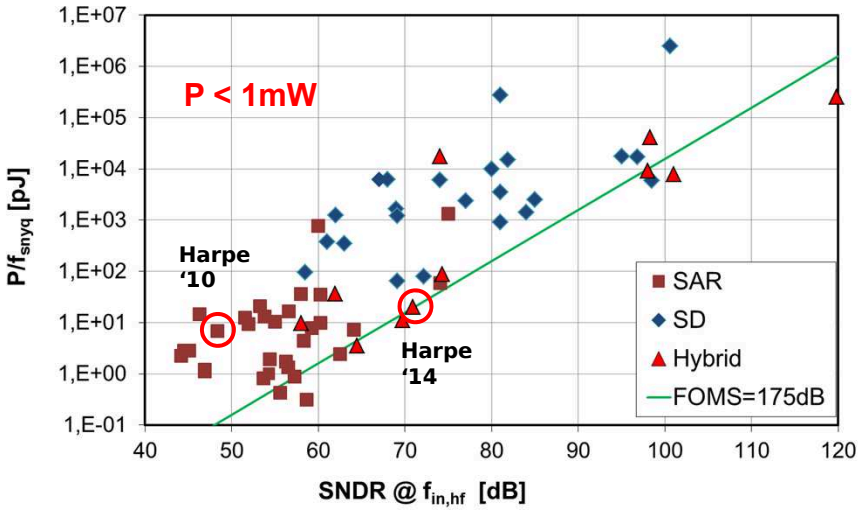


- *14b mode, 128kS/s, 16X OSR, f_{in} = 169.22Hz*

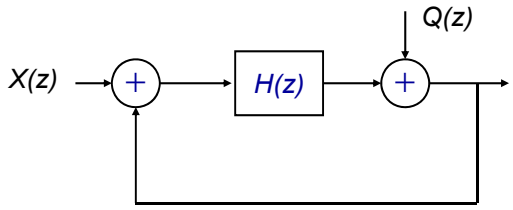
Measurement Results



Benchmarking



ΣΔ Modulator: Linear Model



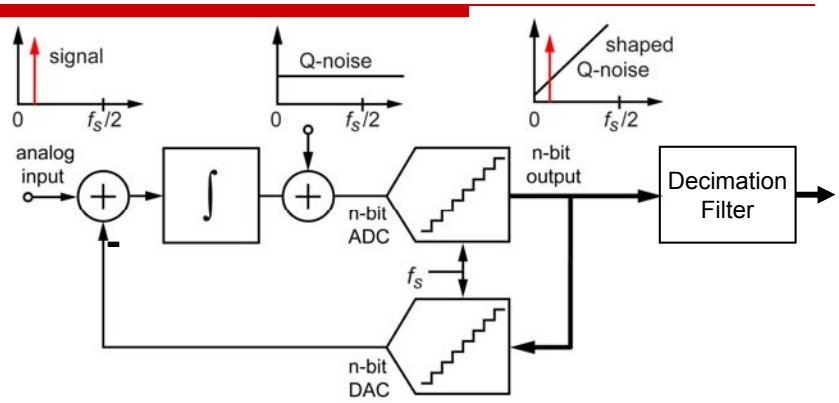
Signal transfer function (STF)

$$Y(z) = X(z)\frac{H(z)}{1+H(z)} + Q(z)\frac{1}{1+H(z)}$$

Noise transfer function (NTF)

- Quantization errors Q(z) are assumed to be white
  ⇒ un-correlated with X(z) (approximately true!)
- STF ~ 1 **if** |H| >>1
- NTF ~ HPF **if** H = LPF ⇒ noise shaping!

Sigma-Delta (ΣΔ) ADC Basics



- Integrator's gain suppresses Q-noise near DC
- Over-sampling further reduces the in-band Q-noise
- A simple (linear) 1-bit ADC and DAC are often sufficient

Sigma-Delta (ΣΔ) ADCs

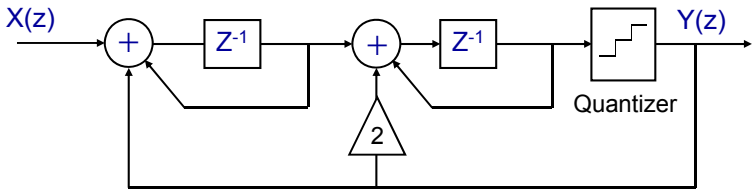
ΣΔ ADC = one critical amplifier + relaxed comparator

- One more active component
- Over-sampling (OSR = f_s/f_{NYQ})
  ⇒ more energy (CV^2*f_s), but less noise (kT/C/OSR)
- Resolution is not matching limited
- Another advantage …

"The beauty of a delta-sigma converter is that you don't have to understand all of it to make it work."

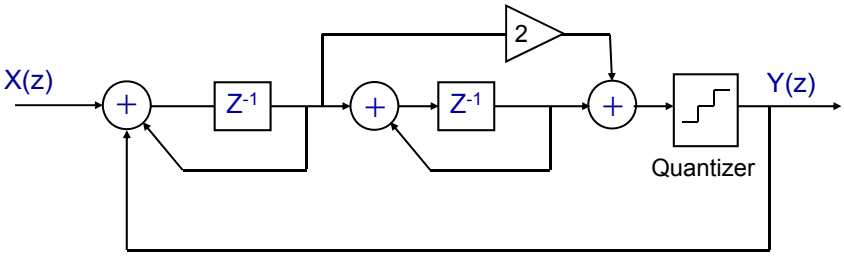
- Willy Sansen

Feedback Topology



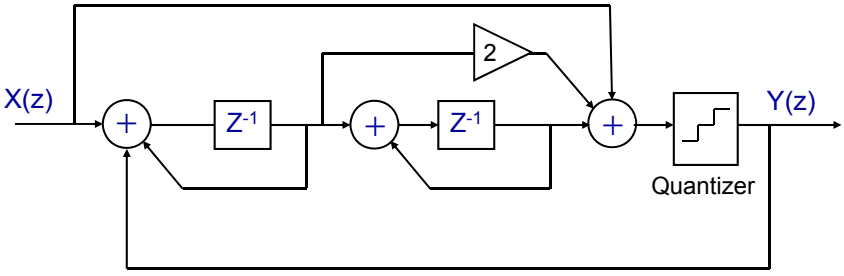
- Classic architecture
- But feedback to the output of the 1st integrator
  ⇒ 1st integrator's output ~ X(z) ⇒ large swing
- STF is Low Pass ⇒ suppresses out-of-band signals

Feed-Forward Topology



- Output of 1st integrator contains high-pass filtered input signal and quantization noise ⇒ lower swing
- But the STF exhibits HF peaking (3x at $f_s/2$)
  ⇒ Out-of-band signals may overload the quantizer

Low-Distortion Topology



- Feeding the input signal directly to the quantizer
  ⇒ loop filter only processes Q-noise ⇒ low swing
- STF is now all-pass (=1), but timing is tricky
- J. Silva et al., "Wideband low-distortion delta-sigma ADC topology," Electronics Letters, June 2001.

Micropower ΣΔ ADC Design

Design strategies

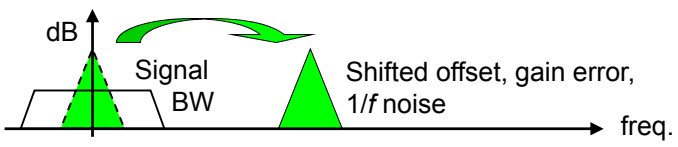
- Reduce amplifier swing ⇒ "The Swing is the Thing"
- Use power-efficient amplifiers (especially the 1st)
- Size caps for thermal noise and use dynamic techniques (inherent averaging!) to reduce offset

Case study

- Y. Chae and G. Han, "Low Voltage, Low Power Inverter-based Switched-Capacitor Delta-Sigma Modulator," JSSC, Feb. 2009.
- Uses the Low-distortion topology + auto-zeroing ⇒ inverters can be used as simple and power efficient amplifiers

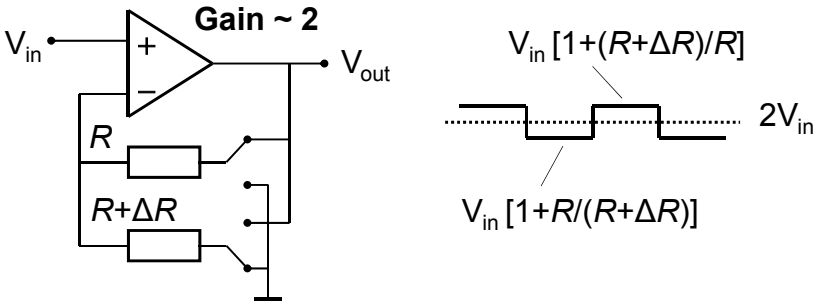
Dynamic Techniques

- Static errors such as offset, 1/*f* noise and gain error can be modulated out of the signal BW
- The resulting AC ripple can elegantly be removed by (notches in) the modulator's decimation filter



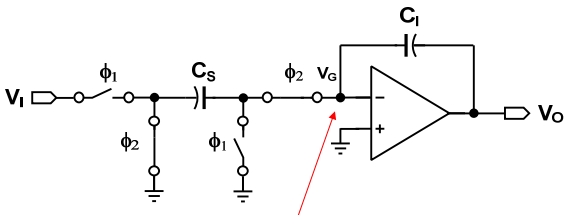
- Auto-zeroing and auto-calibration can also be used to suppress offset and mismatch errors
- **Energy-efficient** manner of improving performance

Dynamic Element Matching (DEM)



- Gain error = $(\Delta R/R)/2 \Rightarrow$ 0.05% with precision layout!
- Resistor swapping $\Rightarrow$ Gain error ~ $(\Delta R/R)^2/2$ = 0.5ppm!
- Up-modulated gain error can be removed by a LPF
- For multiple elements, e.g. in DACs, up-modulated error can even be shaped! $\Rightarrow$ Data weighted averaging (DWA)

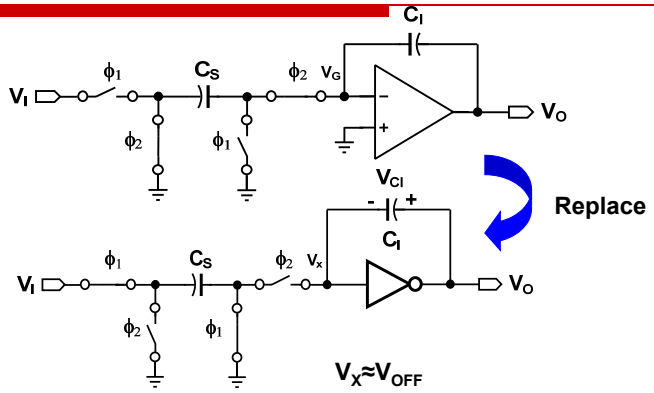
Switched-Capacitor Integrator



SC circuit utilizes the virtual ground formed by the Opamp

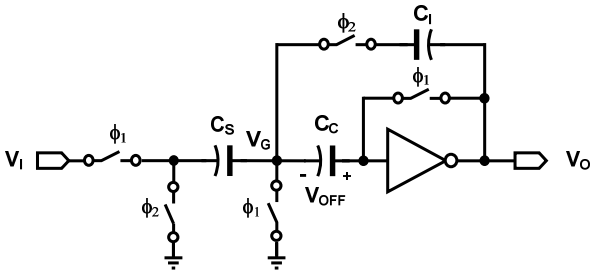
- The Opamp is the major power consuming block
- Voltage scaling $\Rightarrow$ Op Amp design is challenging

Inverter-Based Integrators?



☺ Low voltage operation
☹ Unpredictable offset voltage
☹ No virtual ground

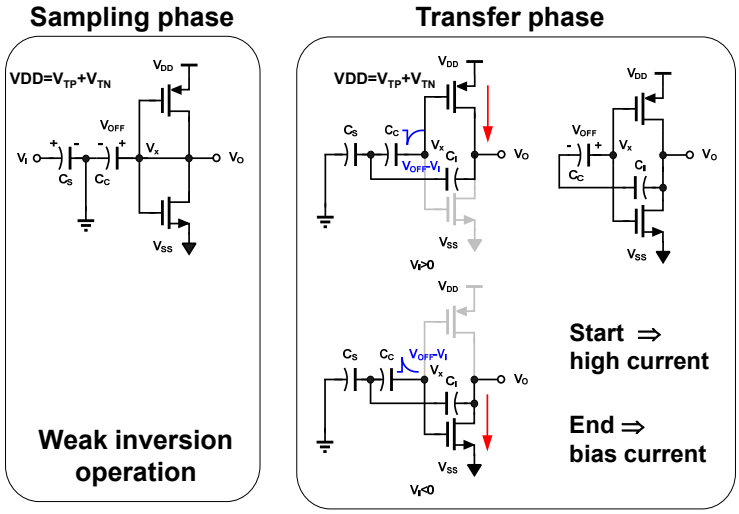
An Inverter-Based Integrator



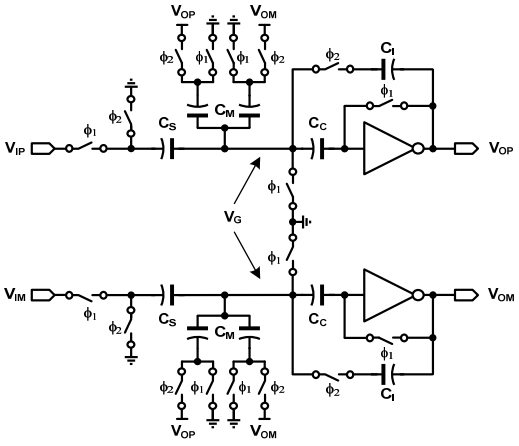
Auto-zeroing

- Phase 1: Amplified offset (and 1/*f* noise) stored on C_C while input signal V_I is sampled on C_S
- Phase 2: Charge on C_C is transferred to C_I
- Inverter offset is stored on C_C => V_G = virtual ground

Class-C Operation



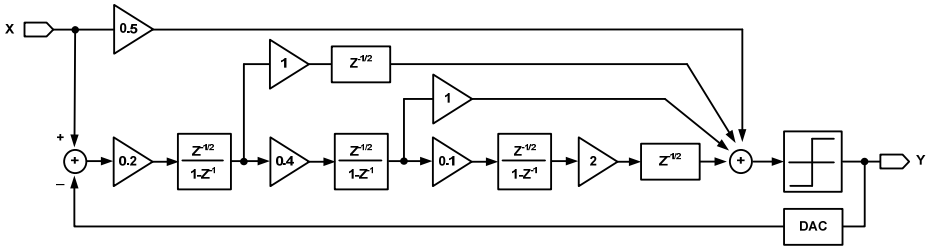
Pseudo-Differential Configuration



- Auto-zeroing ⇒ no offset mismatch problems, but PSRR?

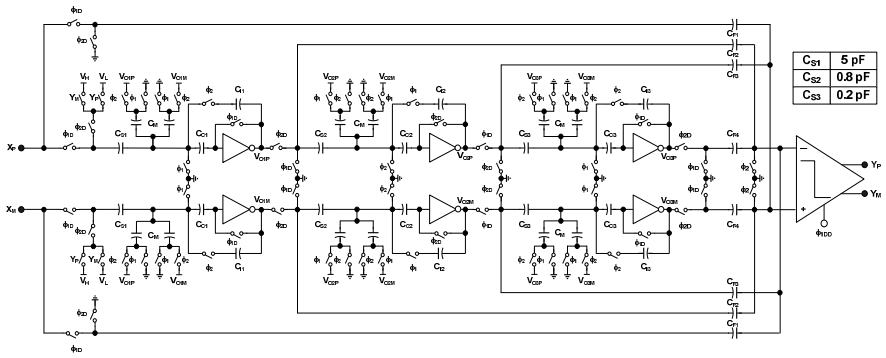
Modulator Topology

3rd order low-distortion topology



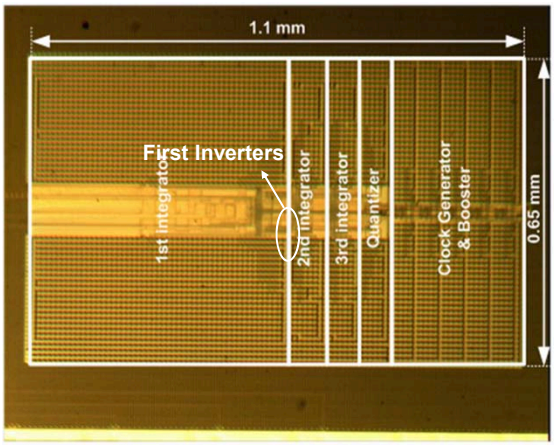
- Relaxed amplifier DC-gain & output swing
  ⇒ inverters can be used!

Schematic Diagram



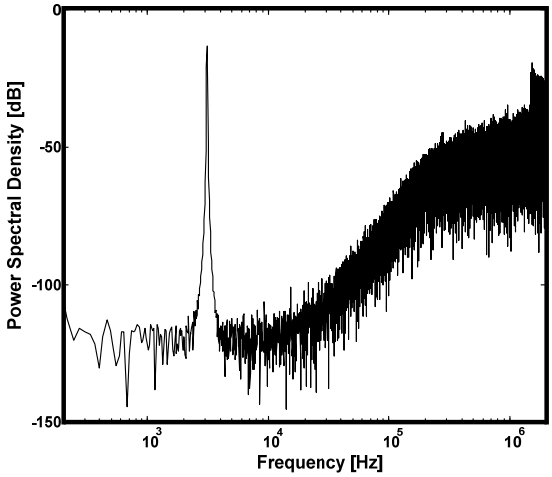
- Active components: only 6 inverters and a comparator

Chip Microphotograph



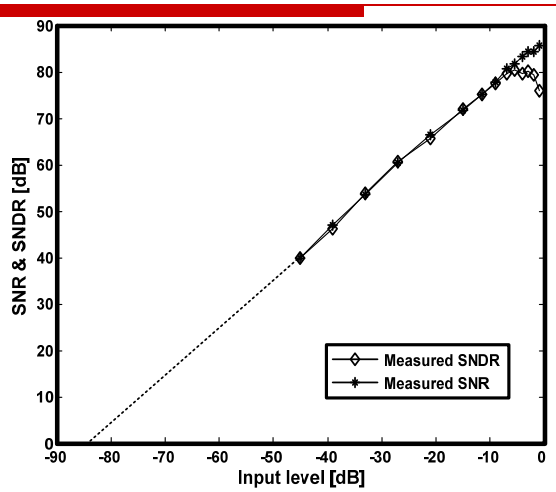
- kT/C noise ⇒ area is dominated by capacitors

Measured Output Spectrum



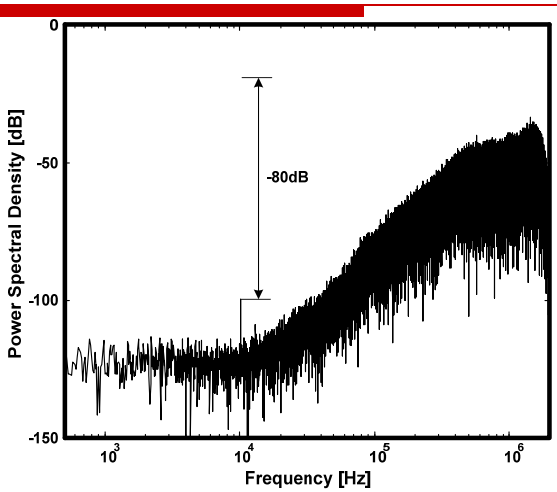
-12dBFS, 3.2-kHz sinusoidal input

Measured SNR & SNDR



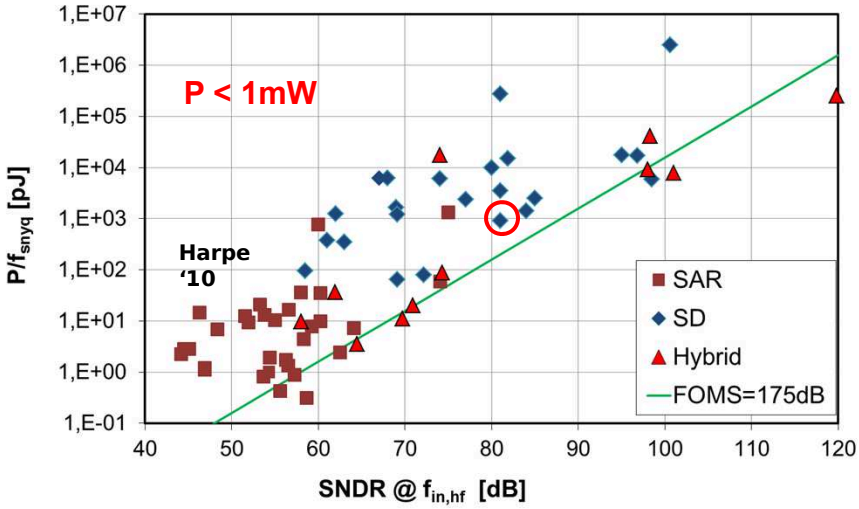
81-dB peak SNDR, 84-dB peak SNR

Measured PSRR



Input shorted and -20dBFS sinusoidal power noise

Benchmarking

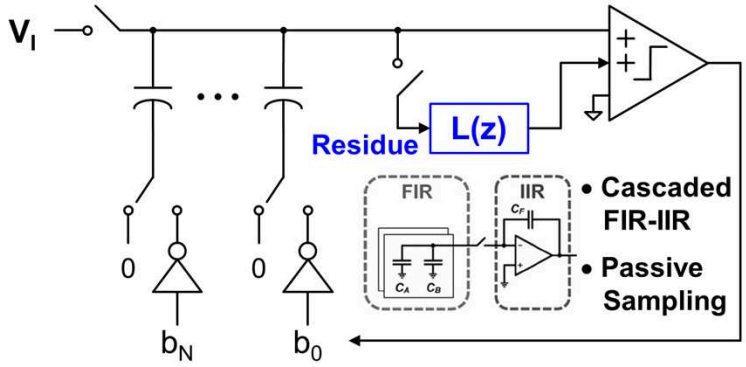


Noise-Shaping in SAR ADCs

- Noise-shaping increases the benefits of over-sampling
- With N^{th} order noise-shaping,
  2x over-sampling ➔ 6N+3 dB improvement in SNR
- But how to do this in a simple (scalable) manner?

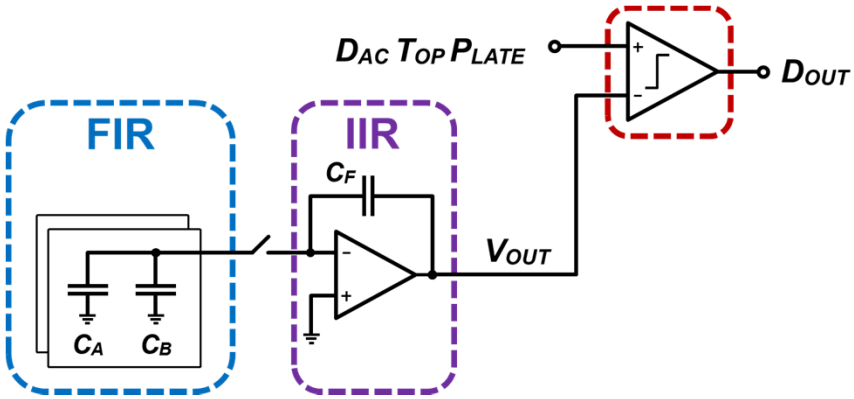
- Case Studies
  - J. Fredenburg et al., "A 90MS/s 11MHz Bandwidth 62dB SNDR Noise-Shaping SAR ADC", ISSCC 2014

Noise-Shaping Concept



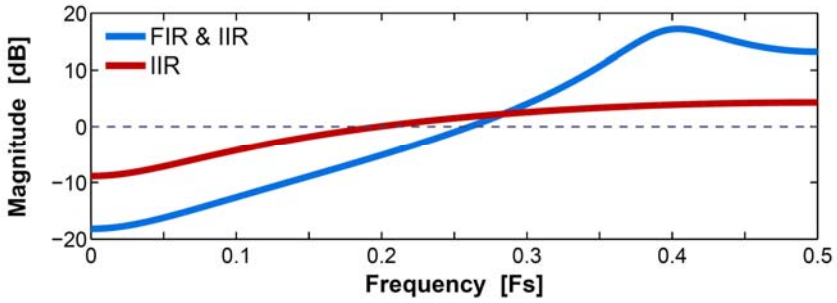
- Extra step at the end of a SAR conversion ➔ analog residue is present at the comparator input!
- Extra comparator input ➔ summing node

Noise-Shaping Filter



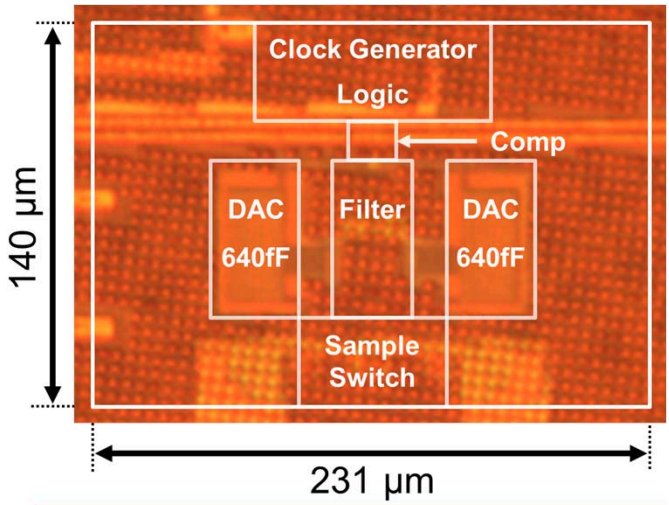
$$V_{OUT}(z) = \left[\frac{C_A}{C_F}z^{-1} + \frac{C_B}{C_F}z^{-2}\right]\frac{\kappa_A}{1-\kappa_A z^{-1}}V_{RES}(z)$$

Noise-Shaping Filter



- IIR filter built around a **simple** one-stage opamp
  ➔ low gain ➔ κ_A = 0.6 ➔ poor noise-shaping
- FIR filter + IIR filter ➔ improved noise-saping
- 10-dB Noise Suppression @ OSR = 8

Die Micrograph



65nm CMOS

8-bit DAC

0.03 mm^2

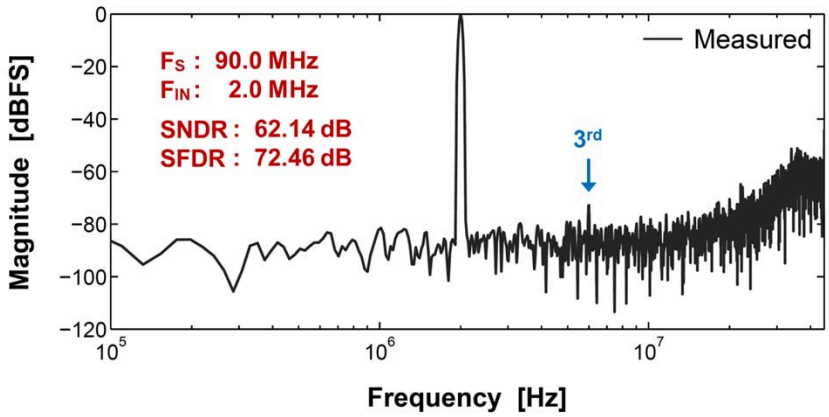
11 MHz BW

800µW

10 bit ENOB

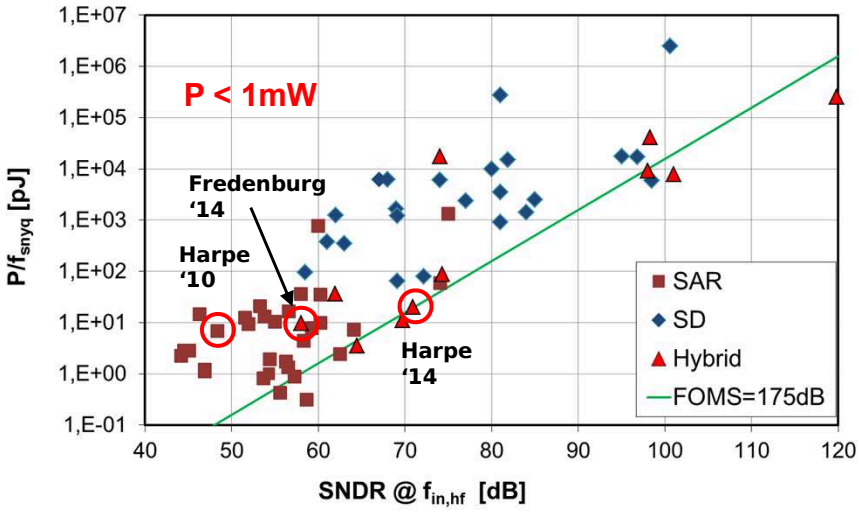
36 fJ/conv-step

Measurement Results

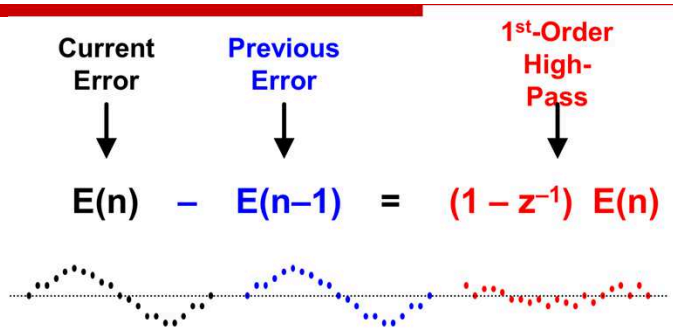


- Noise-shaping is clearly achieved …

Benchmarking

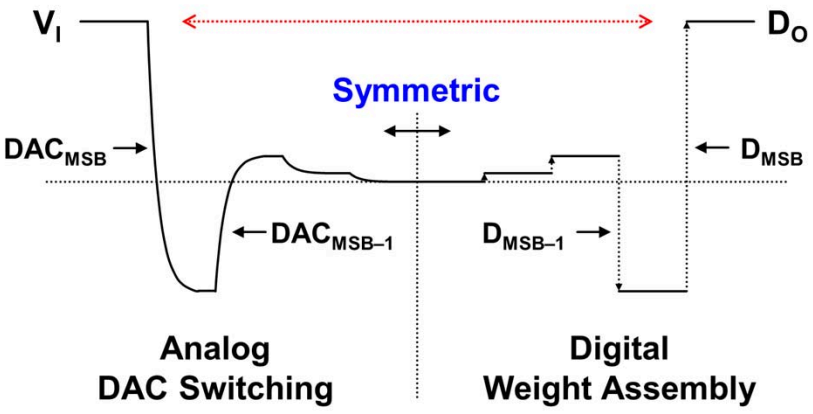


Shaping DAC Mismatch Errors?



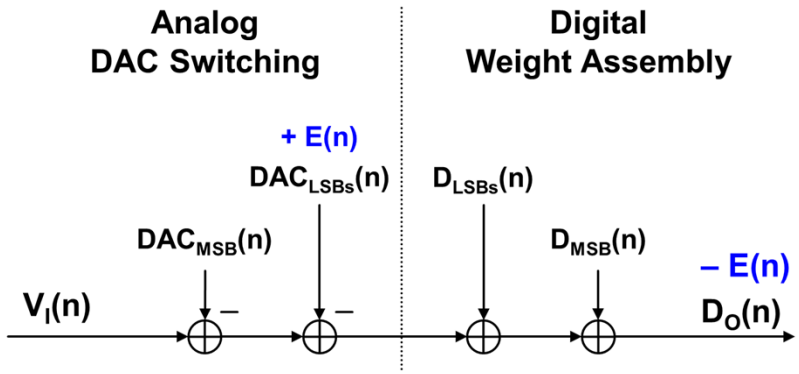
- Use mismatch noise-shaping to mitigate LF DAC errors
- Case Study
  - Yun-Shiang Shu et al., "An Oversampling SAR ADC with DAC Mismatch Error Shaping Achieving 105dB SFDR and 101dB SNDR over 1kHz BW in 55nm CMOS", ISSCC 2016

Ideal SAR ADC operation



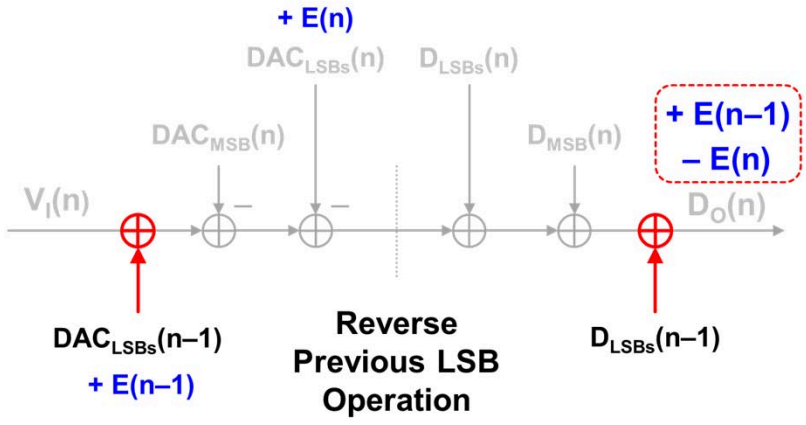
- DAC errors ➔ digital result <> analog input

Non-Ideal SAR ADC operation



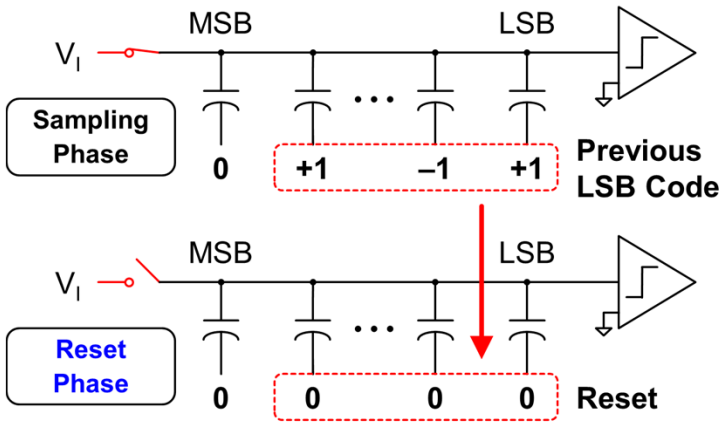
- LSB-Dependent Mismatch Error Sequence

DAC Mismatch Error Shaping (MES)



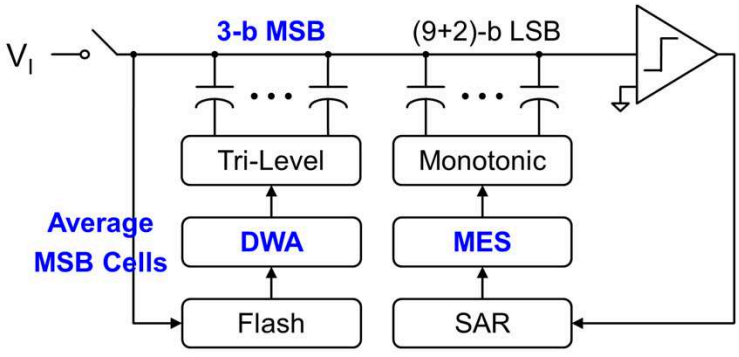
- Add DAC LSBs (and previous error) to the analog input!

MES Implementation



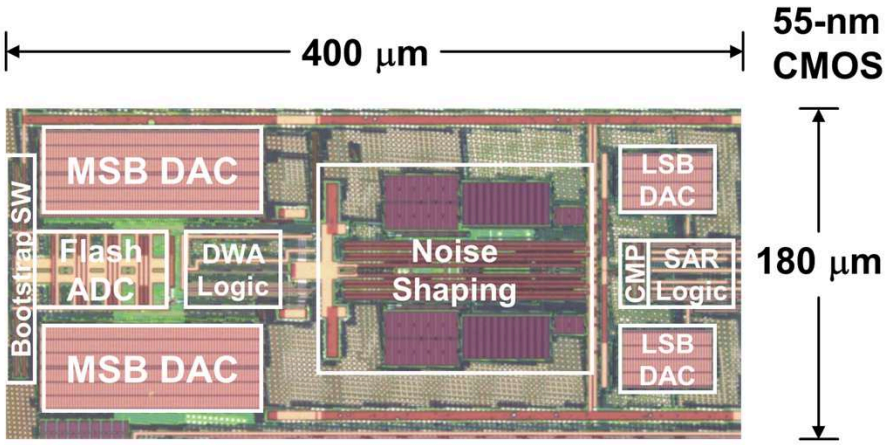
- **One** extra step adds analog input to previous DAC LSBs

MES Prototype



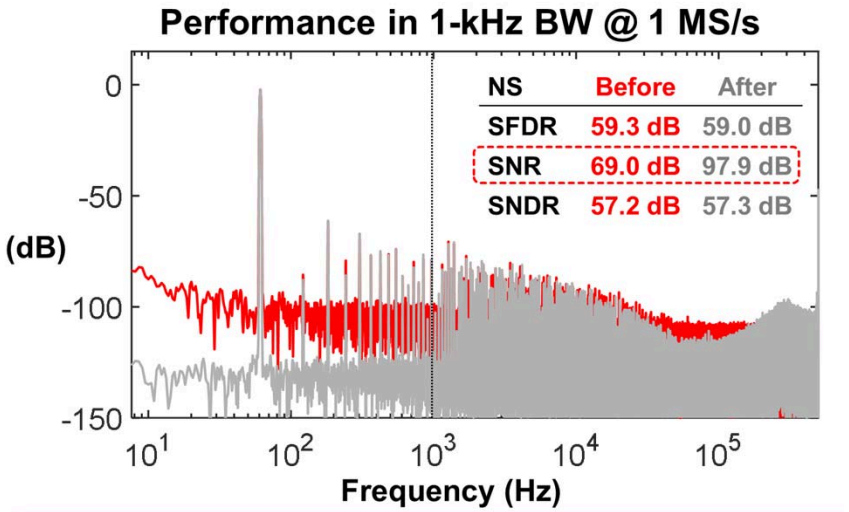
- Adding all LSBs to analog input ➔ 6dB loss in DR
- So data-weighted averaging (DWA) is used for 3 MSBs

Chip Micrograph

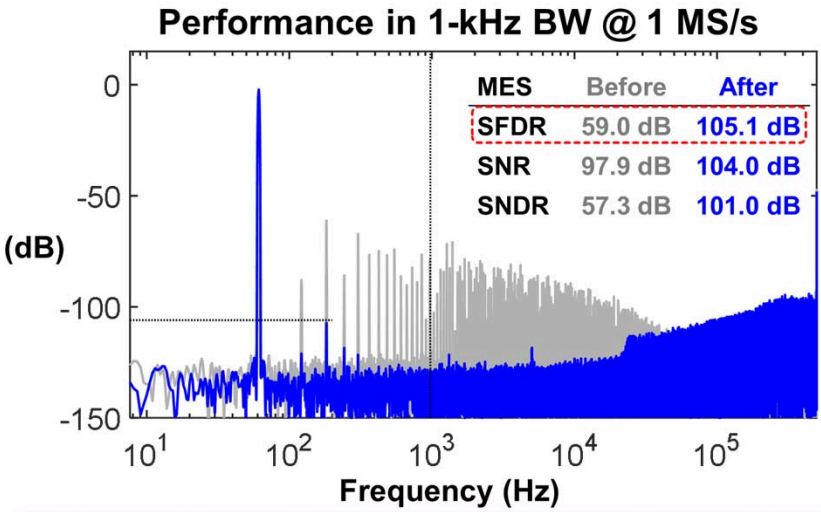


- Separate MSB & LSB DACs to verify effectiveness of MES

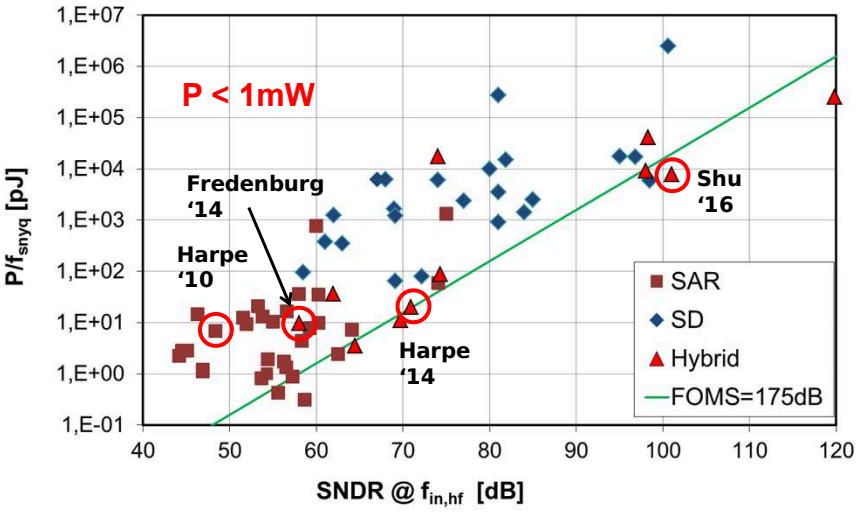
Measurements Before/After NS



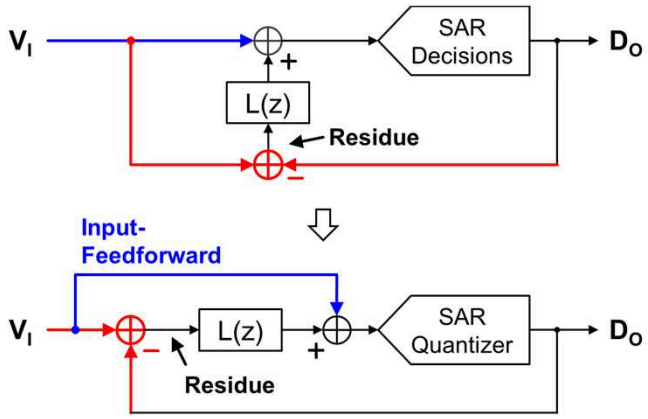
Measurements Before/After MES



Benchmarking



SAR or Sigma-Delta (ΣΔ) ADC?



- Noise-shaping SAR = Multi-bit ΣΔ ADC
- Input feedforward ➔ small residue ➔ simple amplifiers

NS-SAR vs ΣΔ ADCs

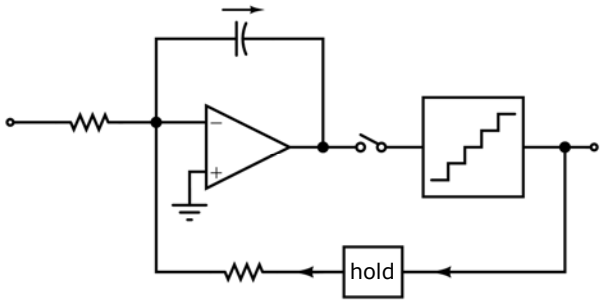
Noise-shaping SAR ADCs

- High-resolution (8-12b) DAC
- Cap DAC ➔ kT/C noise, **strong** input/reference buffers
- Need anti-alias filtering

ΣΔ ADCs

- Low-resolution (1-4b) DAC
- High-order noise-shaping (up to 5^{th})
  ➔ lower OSR, wider BW
- Discrete-Time (DT) ΣΔ ADCs ➔ kT/C noise, **strong** input/reference buffers
- Continuous-Time (CT) ΣΔ ADCs ??

Continuous-Time ΣΔ ADCs



- Sampling **after** loop filter ⇒ built-in anti-alias filtering
- First integrator typically has resistive inputs
  ⇒ simple input/reference buffers
- But width of DAC pulse is important ⇒ jitter sensitivity
  ⇒ multi-bit DAC (+ DWA to maintain linearity)

Incremental ADCs

- Are ΣΔ ADCs whose integrators are **reset** at the start of every conversion
- Result is a **high-resolution** Nyquist-like ADC that produces the same result for the same DC input
- Used for quasi-static signals e.g. in sensor readout and instrumentation applications
- Unlike conventional ΣΔ ADCs can be easily multiplexed between multiple input channels

  - J. Markus, J. Silva, and G. C. Temes, "Theory and Applications of Incremental Delta Sigma converters," IEEE TCAS I, vol. 51, no. 4, pp. 678–690, Apr. 2004.

Micropower Incremental ADCs

ΣΔ ADC = one critical amplifier + relaxed comparator

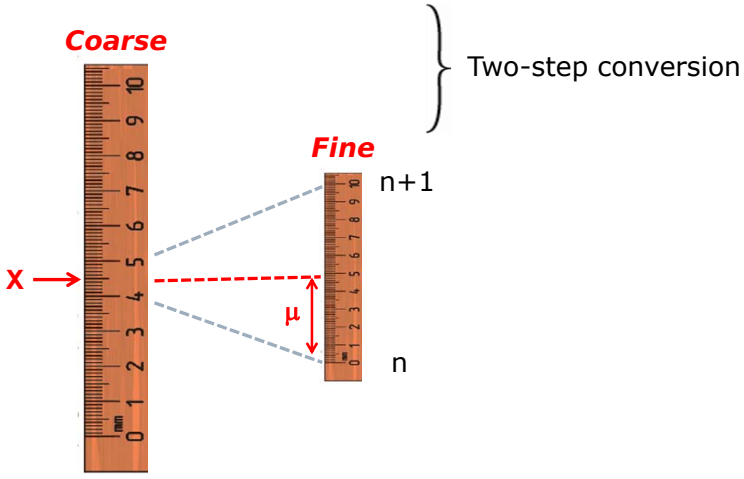
Design strategy

- Reduce loop filter swing ➔ power-efficient amplifiers (especially the 1st) ➔ "The Swing is the Thing"
- Use dynamic techniques (inherent averaging!) to mitigate offset, 1/*f* noise and **DAC mismatch**

- Case Study
  - Y. Chae et al., "A 6.3μW 20bit Incremental Zoom-ADC with 6ppm INL and 1μV Offset," ISSCC 2013.

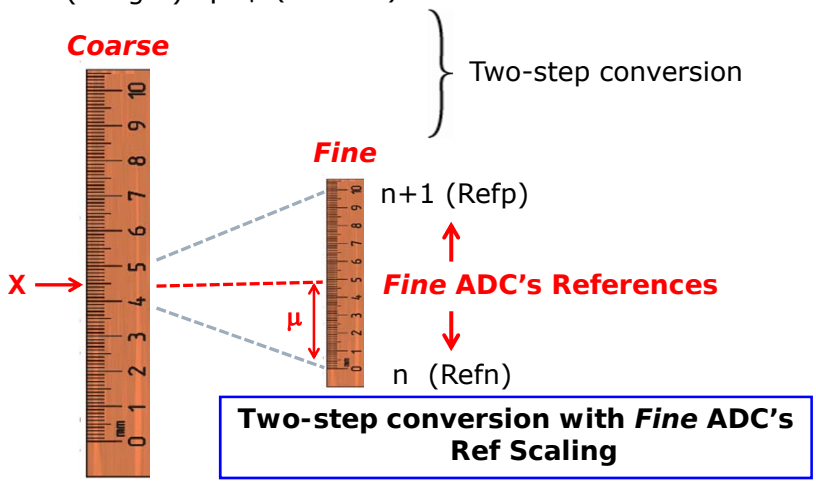
Zoom ADC Principle

X = n (integer) + μ (fraction)



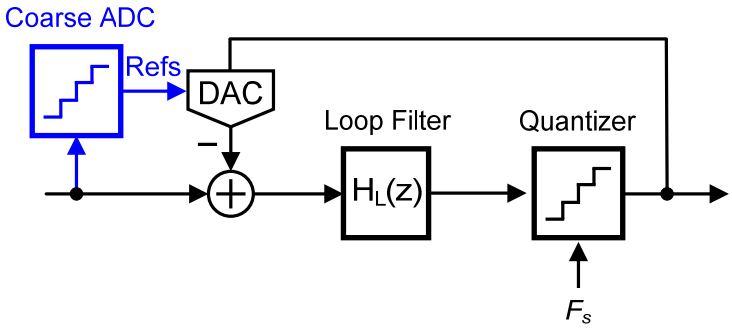
Zoom ADC Principle

X = n (integer) + μ (fraction)



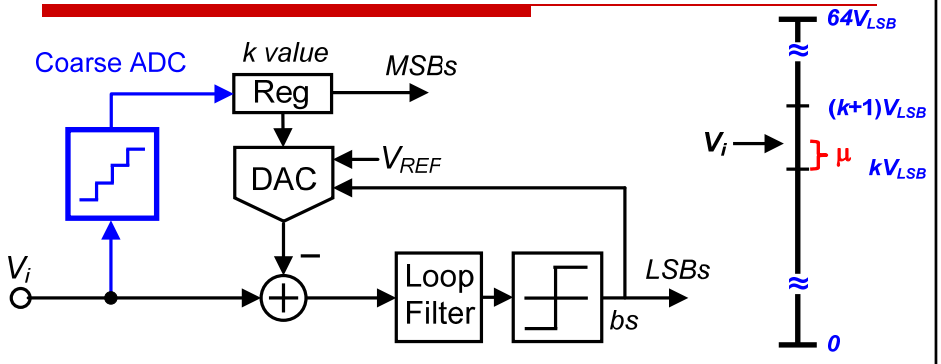
Zoom Conversion with ΣΔ ADC

X = n (integer) + μ (fraction)



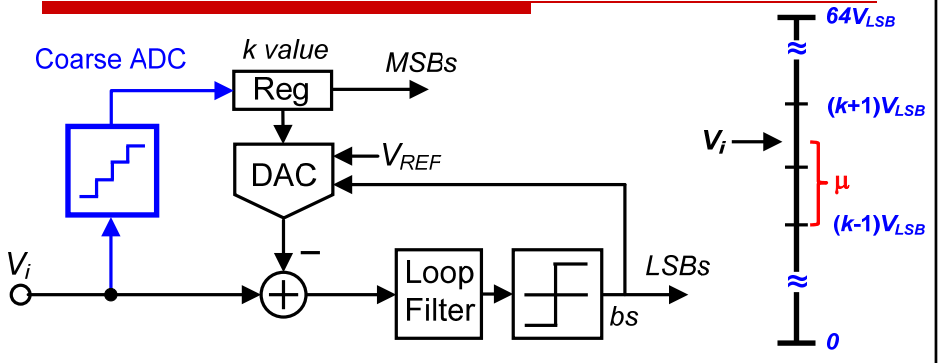
- Coarse conversion: Quickly finds "n" with Nyquist ADC
- Fine conversion: Accurately finds "μ" with ΣΔ ADC
- ΣΔ ADC's input = SAR ADC's Q-noise ➔ relaxed design

20b Incremental Zoom-ADC



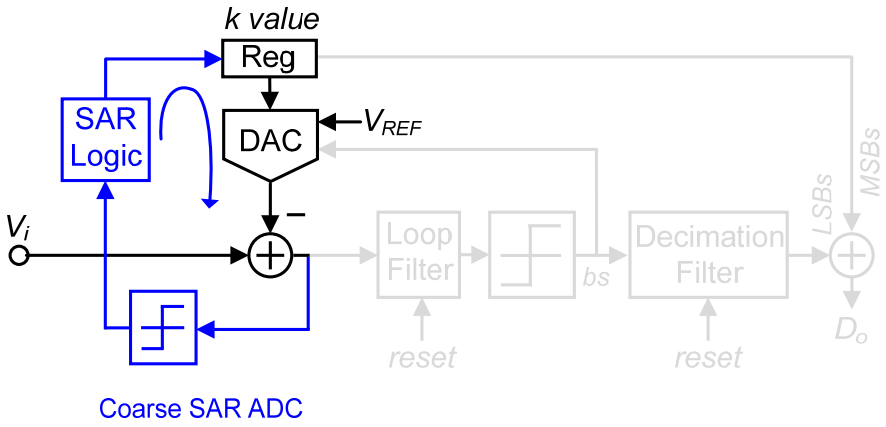
- Coarse ADC determines the references of ΔΣ ADC's DAC
- Errors in the coarse ➔ incorrect *n* & clipping in fine step

20b Incremental Zoom-ADC



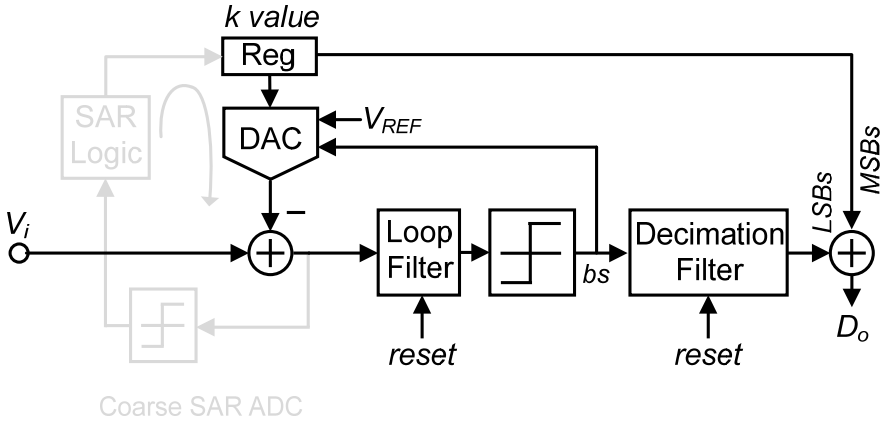
- Coarse ADC determines the references of ΔΣ ADC's DAC
- Coarse ADC errors ➔ incorrect *n* & clipping in fine step
- Fine conversion range is doubled ➔ No clipping!

20b Incremental Zoom-ADC



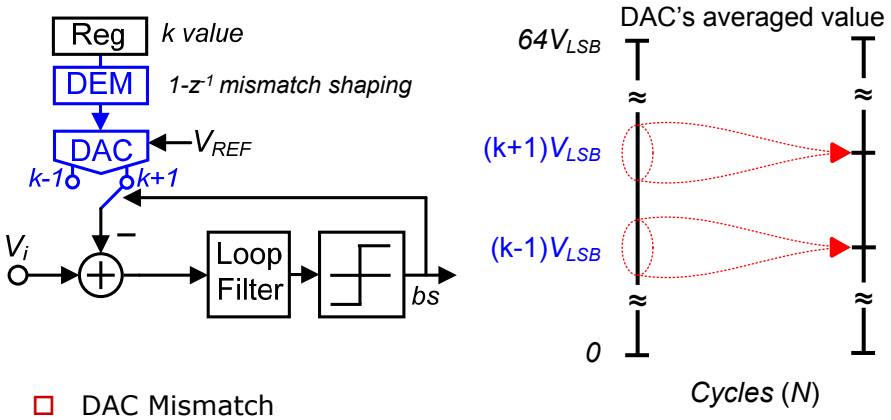
- Incremental applications: DC input ➔ Hardware sharing
- Coarse ADC: 6b SAR ADC reuses feedback DAC

20b Incremental Zoom-ADC



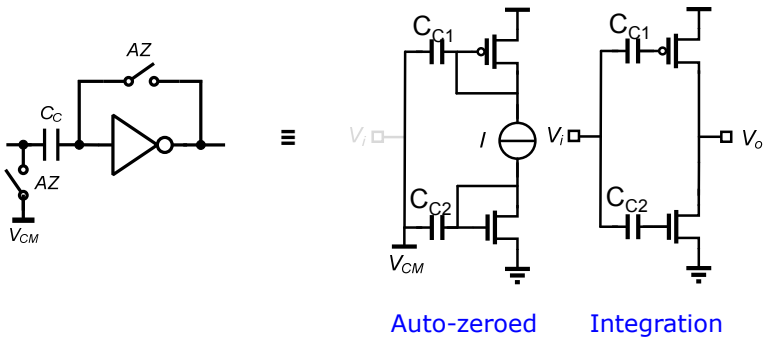
- Incremental ADC: Loop/Decimation filter are reset first
- ΔΣ ADC: 2nd order modulator with relaxed loop filter

DAC with DWA



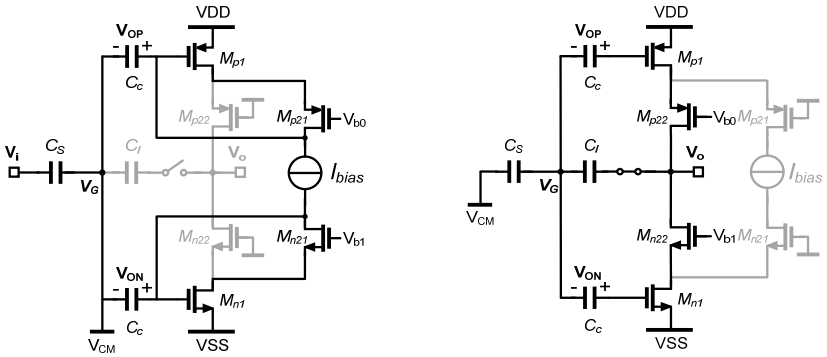
- DAC Mismatch
  - Mitigated by DWA (data-weighted averaging)
  - DAC's averaged outputs become precise over cycles (N)

Inverter-based Integrator



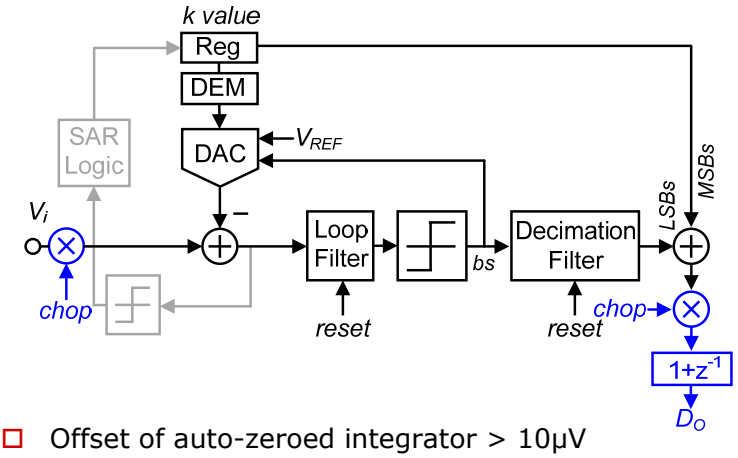
- Two auto-zeroed inverters ➔ pseudo-differential amplifier
  - 1/*f* noise reduction, Max gm/I ratio
- PVT variations of inverter-based circuits
  - Floating I source enhances the immunity to PVT

Inverter-based Integrator



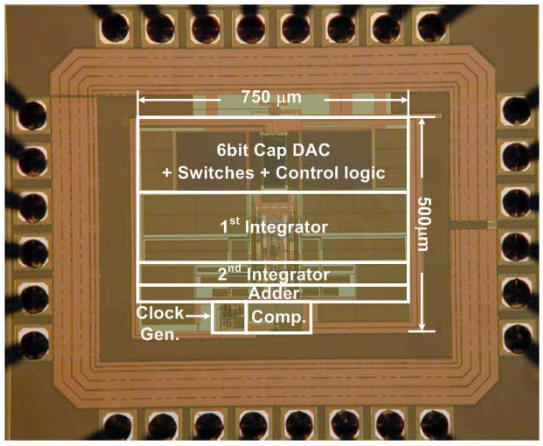
- Biased switches ➔ High gain cascode configuration
- Floating I_{bias} ➔ Translinear bias circuit

System Level Chopping



- Offset of auto-zeroed integrator > 10μV
  - System-level chopping ➔ sub-1μV offset

Chip Micrograph

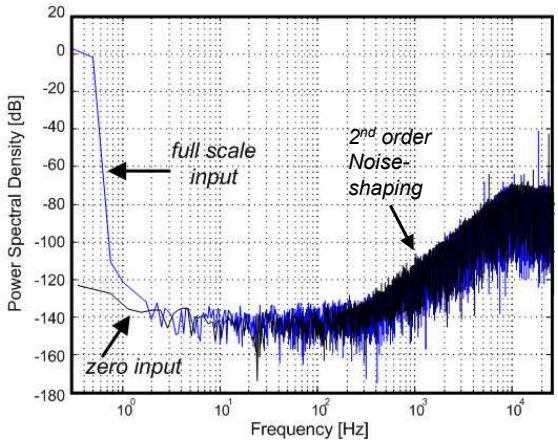


160nm CMOS

0.375 mm^2

6.3µW

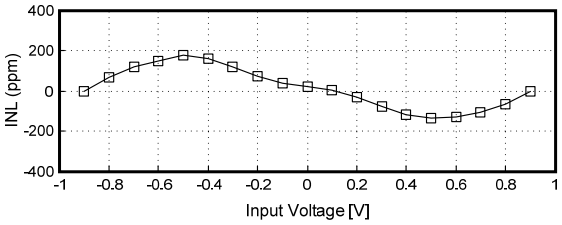
Measured Output Spectrum



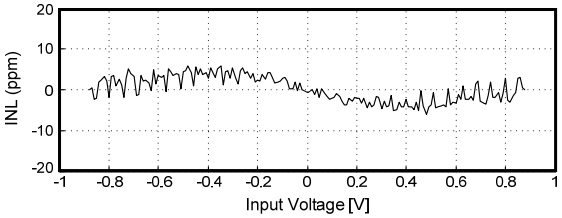
- Free-running ΣΔ Modulator with DEM on ➔ no tones
- Low out-of-band noise ➔ simple $sinc^2$ decimation filter

Measured INL

Without DEM

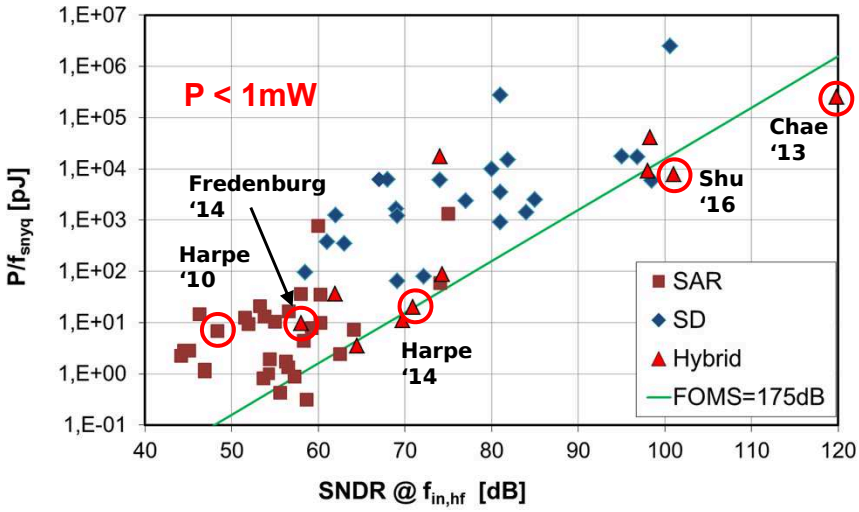


After DEM

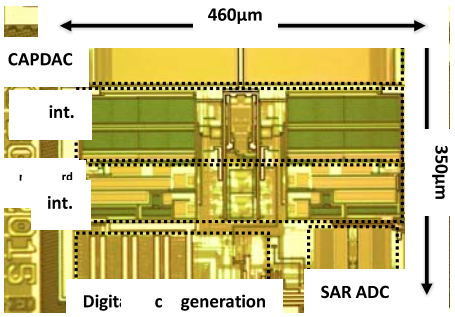


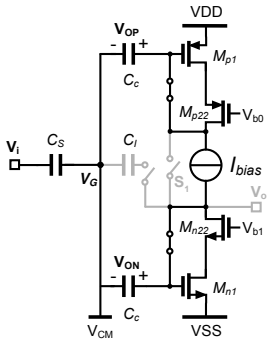
- INL improvement (180ppm ➔ 6ppm)

Benchmarking



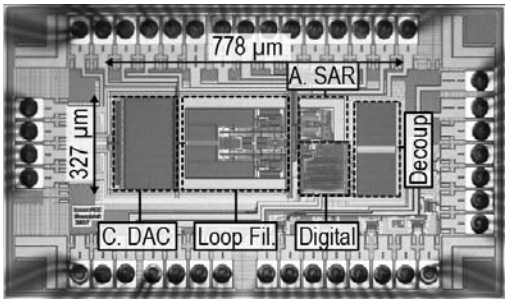
Dynamic Zoom ADC (2016)

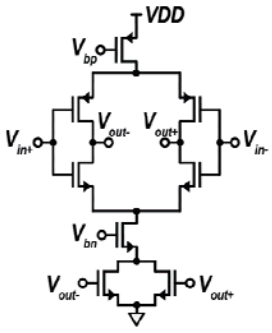




- SAR and ΣΔ ADCs run concurrently
- **Simpler** inverter-based OTA saves power
  - [Gonen, ISSCC '16, JSSC '17]

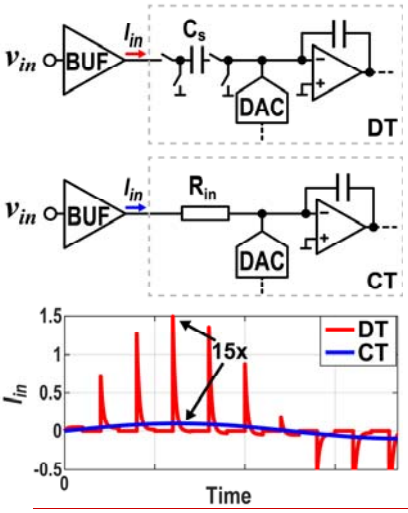
Dynamic Zoom ADC (2018)





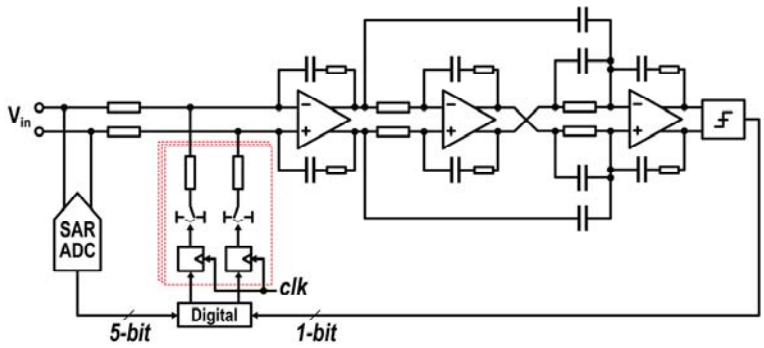
- Asynchronous SAR ⇒ lower power, faster updating of ΣΔ ADCs references ⇒ even less swing
- **So** current-reuse OTA with static biasing ⇒ less power
  - [Karmakar, ISSCC '18]

DT vs CT ADCs



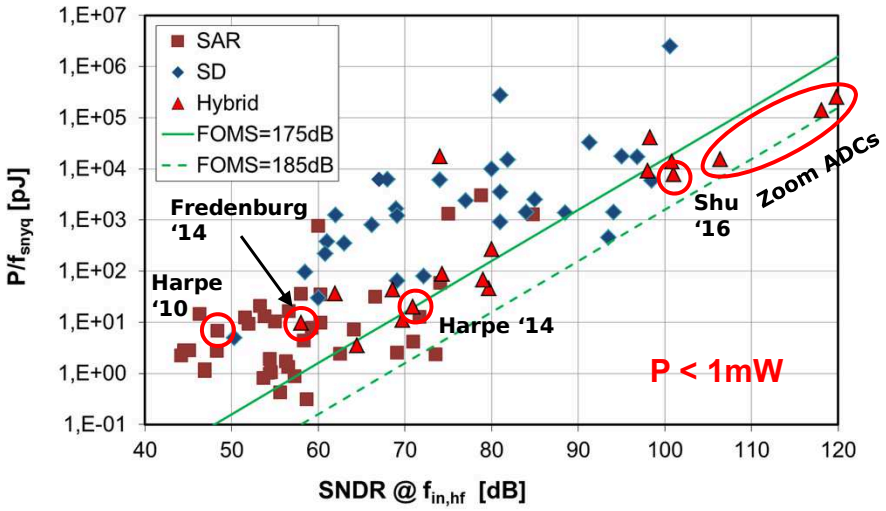
- Discrete-time (DT)
  ⇒ "spiky" input current
  ⇒ high-power driver
  (> ADC power!)
- Continuous-time (CT)
  ⇒ lower input current
  ⇒ low-power driver

CT Dynamic Zoom ADC (2019)



- CT loop filter ⇒ easier to drive, anti-alias filtering
- ISI? ⇒ dual FF DAC drive ⇒ matched rise/fall times
  - [Gonen, VLSI '19]

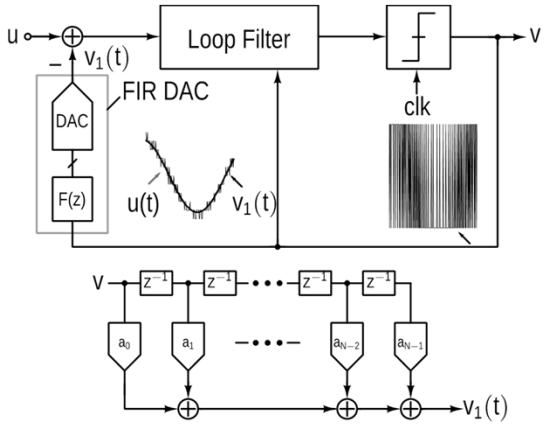
Benchmarking (2019)



FIR-DAC

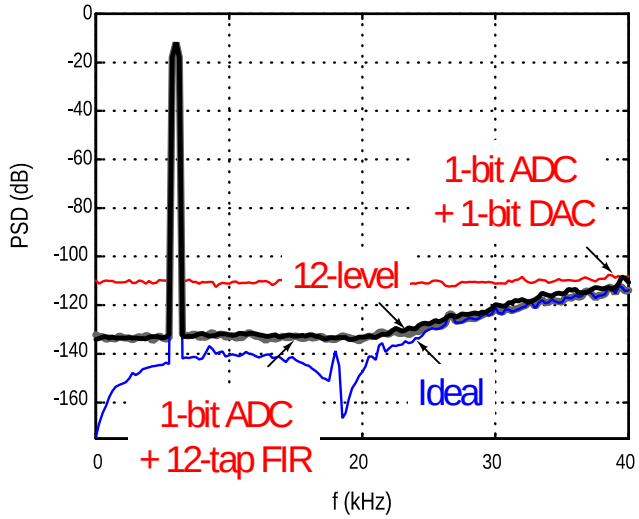
- Continuous-Time (CT) ΣΔ ADCs ➔ built-in anti-alias filtering, simpler buffers, more efficient amplifiers (relaxed settling), **but** jitter sensitive
- Multi-bit DAC ➔ smaller DAC steps ➔ mitigates jitter sensitivity at the expense of linearity
- FIR-DAC ➔ filter the output of a 1b ADC/DAC
- Case Study
  - S. Billa et al., "A 280μW 24kHz-BW 98.5 dB-SNDR chopped single-bit CT ΣΔM achieving< 10Hz 1/f noise corner without chopping artifacts," ISSCC 2016

FIR-DAC Linearity

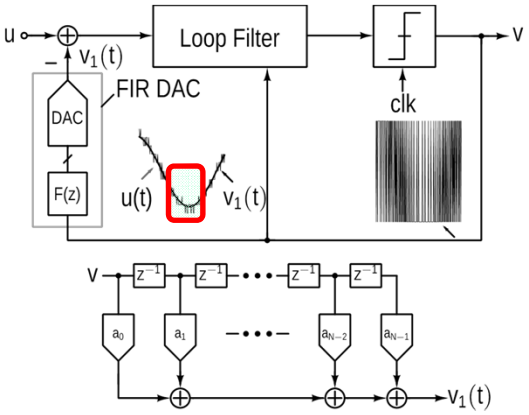


- F(z) filters the output of a linear 1b quantizer
- Quasi-digital implementation ➔ maintains 1b linearity

FIR-DAC Implementation

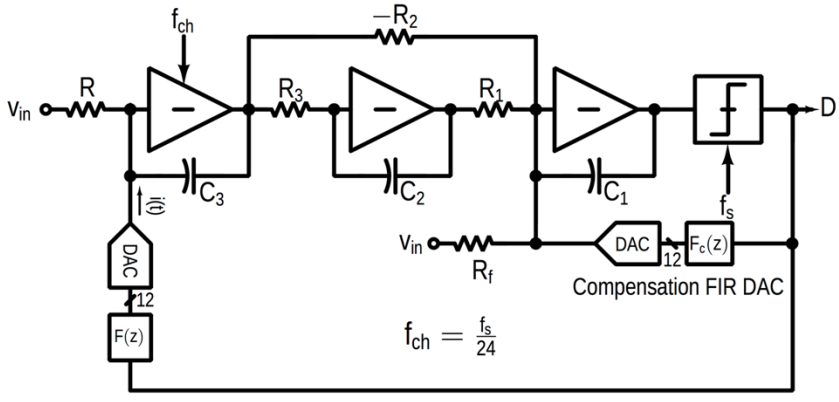


FIR-DAC Implementation



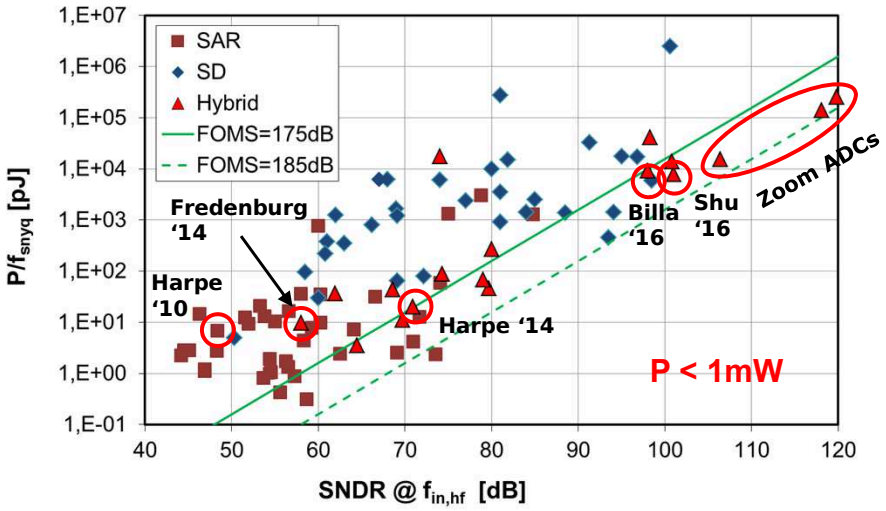
- Reduced loop-filter swing ($u-v_1$) ➔ jitter insensitivity, better linearity, power-efficient amplifiers

3rd Order CTDSM Architecture



- Second DAC compensates for FIR-DAC delay
- Active RC integrators (the 1st is chopped)

Benchmarking (2019)



Summary

- Micropower ADCs ➔ SAR or ΣΔ ADCs
- SAR ADCs are lower power, but their resolution is limited to 10-12b without calibration
- More resolution can be achieved by the use of over-sampling and noise-shaping
- Chopping and/or mismatch shaping ➔ higher resolution
- Use of low-swing topologies facilitates the use of power efficient amplifiers e.g. inverters and dynamic amplifiers
- Hybrid architectures that combine SAR and ΣΔ ADCs ➔ low power **and** high resolution!

Acknowledgements

- Pieter Harpe, Jeffrey Fredenberg, Yun-Shiang Shu, Youngcheol Chae and Shanthi Pavan

  For generously sharing their slides

- Thank-You for Your Attention!

- Any questions?

Recent Literature (1)

Sensor Interfaces with Micropower ADCs

- K. Souri et al., "A CMOS Temperature Sensor With a Voltage-Calibrated Inaccuracy of ±0.15 °C (3σ) from -55 to 125 °C," JSCC 2013
- H. Ha et al., "A 160 nW 63.9 fJ/conversion-step Capacitance-to-Digital Converter for Ultra-Low-Power Wireless Sensor Nodes," ISSCC 2014
- S. Oh et al., "15.4b Incremental Sigma-Delta Capacitance-to-Digital Converter with Zoom-in 9b Asynchronous SAR," VLSI 2014
- S.H. Shalmany et al., "A ±5 A Integrated Current-Sensing System With ±0.3 % Gain Error and 16 µA Offset, JSSC 2016
- C.-C. Tu et al., "A 0.06mm2 ± 50mV Range -82dB THD Chopper VCO-Based Sensor Readout Circuit in 40nm CMOS," VLSI 2017

Recent Literature (2)

Micropower SAR ADCs

- M. van Elzakker et al., "A 10-bit Charge-Redistribution ADC Consuming 1.9 μW at 1 MS/s," JSSC 2010
- A. Shikata et al., "A 0.5 V 1.1 MS/sec 6.3 fJ/Conversion-Step SAR-ADC With Tri-Level Comparator in 40 nm CMOS," JSSC 2012
- P. Harpe et al., "A 10b/12b 40 kS/s SAR ADC With Data-Driven Noise Reduction Achieving up to 10.1b ENOB at 2.2 fJ/Conversion-Step," JSSC 2013.
- H-Y. Tai et al., "A 0.85 fJ/conversion-step 10b 200kS/s Subranging SAR ADC in 40nm CMOS," ISSCC 2014
- Y.-S. Hu et al., "A 510nW 12-bit 200kS/s SAR-Assisted SAR ADC Using a Re-Switching Technique," VLSI 2017
- A. AlMarashli et al., "A 107 dB SFDR, 80 kS/s Nyquist-Rate SAR ADC Using a Hybrid Capacitive and Incremental ΣΔ DAC," VLSI 2017

Recent Literature (3)

Noise-shaping SAR ADCs

- K. Obata et al., "A 97.99 dB SNDR, 2 kHz BW, 37.1 μW Noise-Shaping SAR ADC with Dynamic Element Matching and Modulation Dither Effect," VLSI 2016
- Z. Chen et al., "A 9.35-ENOB, 14.8 fJ/Conv.-Step Fully-Passive Noise-Shaping SAR ADC," VLSI 2016
- W. Guo et al., "A 12b-ENOB 61μW noise-shaping SAR ADC with a passive integrator," ESSCIRC 2016
- S-E. Sieh et al., "A 0.44fJ/conversion-step 11b 600KS/s SAR ADC with Semi-Resting DAC," VLSI 2016
- Z. Chen et al., "A 2nd Order Fully-Passive Noise-Shaping SAR ADC with Embedded Passive Gain," A-SSCC 2016
- M. Miyahara et al., "An 84 dB Dynamic Range 62.5-625 kHz Bandwidth Clock-Scalable Noise-Shaping SAR ADC with Open-Loop Integrator using Dynamic Amplifier," CICC 2017
- W. Guo et al., "A 13b-ENOB 173dB-FoM 2nd -Order NS SAR ADC with Passive Integrators," VLSI 2017

Recent Literature (4)

Micropower ΣΔ ADCs

- J. de Melo et al., "0.7 V 256 μW ΔΣ Modulator With Passive RC Integrators Achieving 76 dB DR in 2 MHz BW," VLSI 2015
- I. Khan et. al, "A Low-Power Gm-C based CT ΔΣ Audio-Band ADC in 1.1V 65nm CMOS," VLSI 2015
- B. Gonen et al., "A 1.65mW 0.16mm2 Dynamic Zoom-ADC with 107.5dB DR in 20kHz BW," ISSCC 2016
- A. Sanyal et al., "A 18.5-fJ/step VCO-Based 0-1 MASH DS ADC with Digital Background Calibration," VLSI 2016
- C. de Berti et al., "A 106 dB A-Weighted DR Low-Power Continuous-Time Sigma Delta Modulator for MEMS Microphones," JSSC 2016
- S. Lee et al., "A 300-μW Audio ΔΣ Modulator With 100.5-dB DR Using Dynamic Bias Inverter," TCAS-I 2016
- M. Jang et al., "A 55μW 93.1dB-DR 20kHz-BW Single-Bit CT ΔΣ Modulator with Negative R-Assisted Integrator Achieving 178.7dB FoM in 65nm CMOS," VLSI 2017

Recent Literature (5)

- Y. Zhang et al., "A Two-Capacitor SAR-Assisted Multi-Step Incremental ADC with a Single Amplifier Achieving 96.6 dB SNDR over 1.2 kHz BW," CICC 2017
- S. Li and N. Sun, "A 0.028mm2 19.8fJ/step 2nd-Order VCO-Based CT ΔΣ Modulator Using an Inherent Passive Integrator and Capacitive Feedback in 40nm CMOS," VLSI 2017
- S. Karmakar et al., "A 280μW dynamic-zoom ADC with 120dB DR and 118dB SNDR in 1kHz BW," ISSCC 2018
- H. Chandrakumar, D. Marković, "A 15.2-ENOB Continuous-Time ΔΣ ADC for a 7.3μW 200mVpp-Linear-Input-Range Neural Recording Front-End," ISSCC 2018
- C. Lee et al., "A 1.2V 68μW 98.2dB-DR Audio Continuous-Time Delta-Sigma Modulator," VLSI 2018
- B. Gonen et al., "A Low Power Continuous-Time Zoom ADC for Audio Applications," VLSI 2019