10.6 A 1.2V 10b 20MSample/s Non-Binary Successive Approximation ADC in 0.13μm CMOS

Franz Kuttner

Infineon Technologies AG, Microelectronics Design Centers Austria, Villach, Austria

Improvements in technologies and design make it possible to use successive approximation ADCs for video applications, where sample frequencies of at least 10MSample/s are necessary. The advantages by changing the structure of the ADC from subranging or pipelined to successive approximation are decreased power dissipation, small area, and high reusability.

The speed of the DAC and the comparator limits the conversion time of a SA-ADC. An n-bit ADC must take n decisions for every conversion, and every decision must be as accurate as the final result of the conversion. The time which the DAC needs to settle to ½ LSB is approximately: $t = \tau \times \ln(1/2 \times 1/2^n)$

The time for the comparator decision depends on the voltage step at the beginning of the comparison time. The recovery time increases for large voltage jumps. So, if the design is changed so that the result is insensitive to small errors in the decisions with the highest voltage jumps, the conversion-time can be improved. This leads to converters with redundant codes.

Converters with redundancy use codes with bases smaller than 2 (not binary). There are several digital codes for every input voltage, so small errors do not affect the conversion result. A DAC with a non-binary network is normally the key element of such an ADC. A charge redistribution ADC can be build by non-binary scaling of DAC capacitor sizes (1 2 4 8…) by using instead a smaller factor e.g. 1.85 ($1\ 1.85\ 1.85^2\ 1.85^3\ 1.85^4$…). Due to the redundancy, the conversion needs additional clock cycles, but the clock frequency can be increased, so that the overall conversion time gets smaller.

This ADC uses a capacitor array driven by a thermometer code. The redundancy is not in the DAC, but is calculated in the digital part of the converter.

Figure 10.6.1 shows the ADC block diagram consisting of a differential input buffer, a differential capacitor array, a comparator, and a digital part.

The voltage which should be measured is switched via the buffer to the capacitor array. The capacitor array samples this voltage. Therefore, the capacitor array is the DAC and the sample-and-hold capacitor of this ADC. This double function is an advantage because this saves power and area. The offset of the comparator is compensated in the sample phase. During conversion, the comparator compares the voltages on the top plates of the capacitor array with the sampled voltage on these plates.

Conversion is started by comparing the sampled voltage with half of the reference voltage by switching the buffered Vrefp and Vrefn voltages to half of the capacitors respectively. For a 10b ADC this is the test whether the digital result is larger or smaller than 512. At the next clock cycle a binary weighted SA-ADC executes the comparison with ¾ or ¼. But, for this converter, the result of the first decision does not mean that the input voltage is greater or smaller than half of the reference voltage. A logical one ('1') means only that the input voltage is greater than half the reference voltage minus some error tolerance (e.g. 12.7%). So the next comparison is not done with 256 or 768. A '1' means that the code is greater than 512 minus 12.7%, so the next comparison is with the middle of the next range 447…1024 = 735. A '0' means, that the code is smaller than 512 plus 12.7%, so the next comparison is with 288. Therefore error of the first conversion can be up to 65LSB of the 10b code.

The bit weights (447 251 142 80 45….) are stored in a ROM. During every conversion step, an arithmetical unit calculates the numbers for the possible next two compare values. Depending on the comparator result, one of these numbers is switched by a multiplexer to the DAC. This multiplexer is able to change the D/A code during the comparison cycle, if the comparator result is not valid (meta stable state).

The 10b binary code is feed to a differential 10b capacitor array, whose upper 8b are driven by a thermometer code and the two lowest bits are binary coded. The 256 capacitors of the upper 8b are located in a 16*16 array, where each capacitor has its own local decoder (Figure 10.6.2). The local decoders are driven by 16 wires for the line, and 16 wires for the column information, so the decoders have only to decode 4 binary bits to 16 thermometer wires. For this 16 thermometer wires metal 1 and metal 2 are used in the layout (Figure 10.6.3). The metal 2 layer is also used to shield the capacitor (build with metal 3 and 4) from the thermometer-coded drive wires. The technique with local decoders and capacitors exploits the 0.13μm technology used, because the local decoder is small enough to fit under the capacitors, and the technology offers at least 4 metal layers. Figure 10.6.3 shows that not only the vertical capacitance between metal3 and metal4, but also the higher lateral capacitance between the metal 4 lines is used. The unit size of one capacitor is 1.5fF, resulting in ~2*400fF total capacitor.

There are several advantages of driving the capacitors with a thermometer code. Differential linearity of the converter is inherently good. Current consumption from the reference is lower, because one great capacitor is not switched to Vrefn and another capacitor switched to Vrefp. (e.g. 10000 ➔ 01000). Only the difference is switched.

To show the improvement by the redundancy, three converters with different ROM content are implemented. The first is binary coded, like a conventional SA-ADC, and needs 10 clock cycles for conversion. The second is able to correct errors up to ±6.4% and needs 11 clock cycles. The third is able to correct errors up to ±12.7% with a conversion time of 12 clock cycles. Figure 10.6.4 shows the effect on a converted sine wave at 20MHz sampling frequency and 320MHz clock frequency.

Figure 10.6.5 shows a die micrograph. The converter is fabricated in a single-poly, four-metal, 0.13μm standard copper CMOS process and occupies 0.08mm², including on-chip input- and reference-buffer. A PLL (0.048mm²), to generate the clock for the ADC, and 1.2V bandgap reference are implemented on the same chip. The converter consumes 10mA at 1.2V, 8mA for the buffer, and 2mA for the comparator.

Figure 10.6.6 shows measurement results (SNR and THD) for sample frequencies from 0.2 to 30MHZ and analog input frequencies from 1/16 of the sample frequency to the Nyquist frequency. For supply voltages between 1.08 and 1.65V and sample frequencies up to 20MHz the SNR is >50dB, sufficient for video application. THD is >60dB. At low frequencies, the second harmonic increases because of the balun located at the analog input. Over 5MHz strobe frequency, a sinewave generator with poor performance is used.

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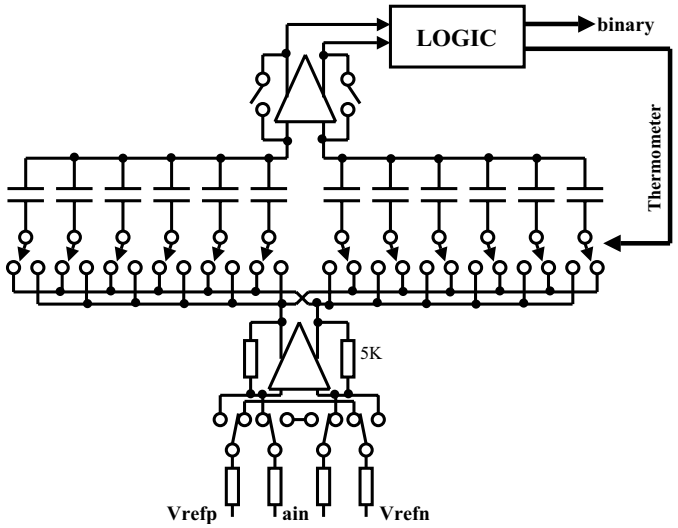

Figure 10.6.1: ADC.

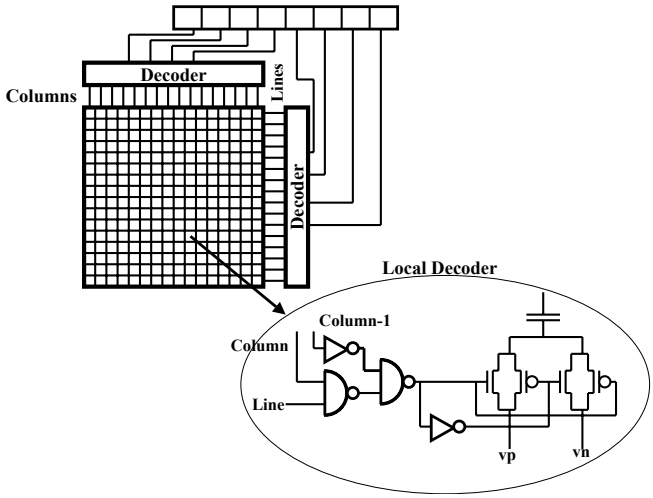

Figure 10.6.2: Capacitor array.

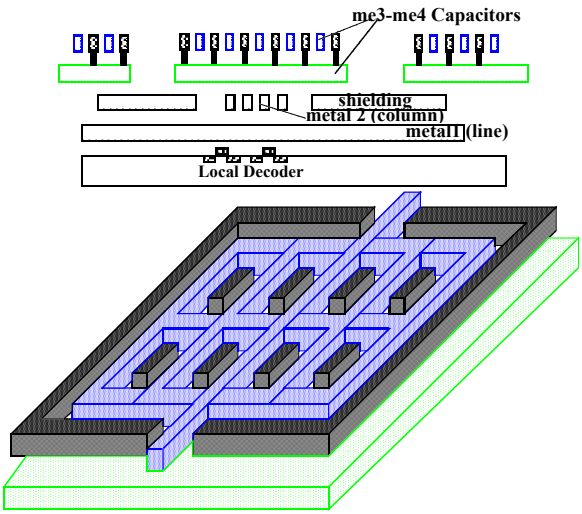

Figure 10.6.3: Topology of capacitor array cells.

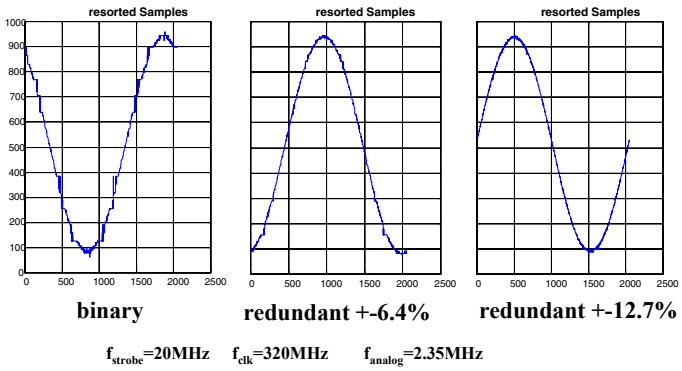

Figure 10.6.4: Effect of redundancy.

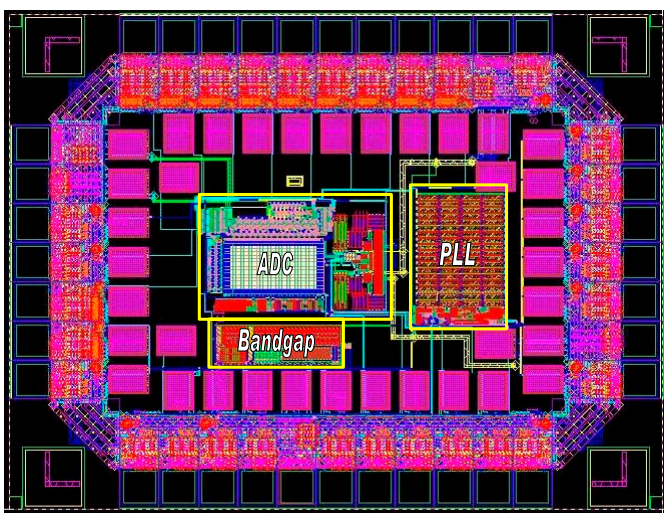

Figure 10.6.5: Die micrograph.

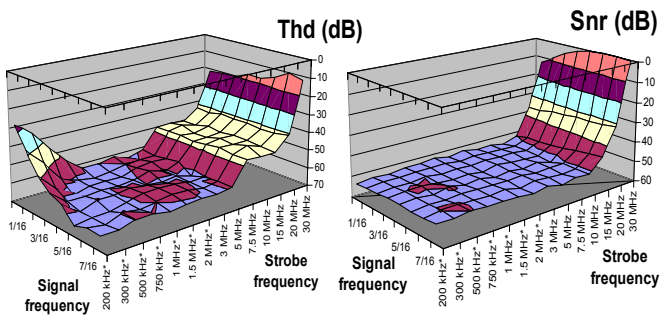

Figure 10.6.6: THD and SNR versus signal and strobe frequency.

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