# Low-Power SAR ADC Design: Overview and Survey of State-of-the-Art Techniques

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***Abstract*— This paper presents an overview for low-power successive approximation register (SAR) analog-to-digital converters (ADCs). It covers the operation principle, error analysis, and practical design issues. Furthermore, this paper provides a comprehensive survey of state-of-the-art low-power design techniques for every circuit block in the SAR ADC, including comparator, capacitive digital-to-analog converter (DAC), and SAR logic. The goal of this paper is to provide a useful overview to SAR ADC designers who want to improve the energy efficiency targeting low-to-medium speed applications.**

***Index Terms*— Analog-to-digital converter (ADC), successive approximation register (SAR), low power, energy efficiency.**

## I. Introduction

WHILE information has been increasingly processed in the digital domain, the physical world remains analog. Whenever these two domains meet each other, for example, in wireline/wireless communication, data storage, and a broad range of sensor applications, we need conversion between analog and digital signals. As a result, analog-to-digital converters (ADCs) are essential building blocks in almost all electronic systems.

In the span of several decades, research and development led to the emergence of a few widely used ADC architectures, such as the flash, pipeline, successive approximation register (SAR), and $\Delta\Sigma$ ADCs. Each finds its own application sweet-spot considering the target bandwidth and resolution. This paper will focus on the SAR ADC, which is traditionally used in medium-to-high resolution and low-to-medium speed applications. Although the SAR ADC architecture was invented more than 40 years ago [1], it did not draw significant attention from researchers back then due to its speed limitation and its relatively heavy use of logic gates when each gate counts in the energy consumption. Nevertheless, exactly because of its mostly digital architecture, it benefits more from technology scaling than other ADC architectures does, leading to its renaissance starting from around 2006 when the CMOS technology entered the 65nm node. Fig. 1 lists published ADC papers at ISSCC and VLSI conferences from 2000 to 2021 [2], which reveals that the dominant ADC architecture by choice over the past decade has been SAR and its hybrid (marked as black diamonds).

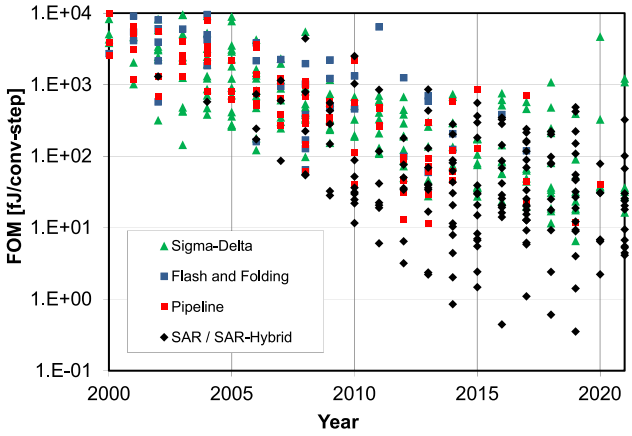


Fig. 1. ADC energy efficiency (FoM) over the years [2].

Benefiting from technology scaling, ADC has increased its energy efficiency dramatically. A widely adopted metric to characterize the ADC energy efficiency is the Walden figure-of-merit (FoM), defined as [3]:

$$FoM = \frac{Power}{2 \cdot BW \cdot 2^{ENOB}} \tag{1}$$

where $BW$ stands for the input signal bandwidth and $ENOB$ is the effective number of bits. By normalizing the power

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consumption against the speed and resolution, FoM represents the energy needed for each conversion step, with a unit of Joule per conversion step. As shown in Fig. 1, the ADC energy efficiency has improved from roughly 3-pJ/conversion-step (the best number reported in 2000) to 0.4-fJ/conversion-step (the best number reported in 2019). This represents an improvement of 7,500 times over 20 years. In other words, the ADC energy efficiency has been improving at a pace of 2 times every 1.5 years. It is apparent from Fig. 1 that the latest most power efficient ADCs are SAR ADCs. This explains why SAR ADC is the popular choice in a broad range of applications, such as Internet-of-Things (IoT), industry, healthcare, and scientific systems, especially when high energy efficiency is a critical demand.

While technology scaling has certainly been a major driving force behind this significant energy efficiency improvement, it is not the only factor. The typical process nodes for ADC designs are 0.35 $\mu$m and 40 nm in the year of 2000 and 2021, respectively. The estimated energy reduction solely due to technology advancement, as characterized by $CV^2$, is about 100 times (3× for voltage scaling and 10× for capacitance scaling). To achieve the total 7,500 times improvement in the ADC FoM, the remaining 75 times improvement comes from sheer engineering ingenuity, i.e., designers' innovations on both architectural and circuit levels. Indeed, researchers have invented many important design techniques that enable this substantial energy reduction. This paper aims to provide a comprehensive survey of these low power design techniques. Due to the constraint on the number of pages, it cannot provide an exhaustive review of all published ADC papers. Nevertheless, the authors aim to cover most important works to the best of their knowledge. The goal of this paper is to provide a useful overview to SAR ADC designers who are interested in improving the energy efficiency of their designs.

This paper is organized as follows. Section II introduces the basics of a SAR ADC. Section III discusses the major error sources, and provides a comprehensive overview of factors that limit SAR ADC's energy efficiency.

A SAR ADC core consists of three major circuit blocks: a comparator, a capacitive digital-to-analog converter (DAC), and a SAR logic. In a well-optimized low-power SAR ADC, the power consumption of each block is comparable. Thus, to significantly reduce the total power, it is necessary to lower the power of each building block. Hence, Section IV, Section V, and Section VI showcase the latest power reduction techniques for each block, respectively. Finally, Section VII reviews the SAR energy efficiency evolution, and Section VIII summarizes the state-of-the-art SAR ADC trends and challenges.

## II. SAR ADC Fundamentals

### A. SAR Principle

The SAR ADC uses successive approximation to find the digital representation of an analog input. For an input with no prior knowledge, the most-efficient search algorithm is binary search, which is adopted in the SAR ADC design [4]–[6]. It includes two core functions: search voltage generation and comparison. This translates to the three core functional components in a SAR ADC: a DAC that generates the comparison voltage $V_{dac}$, a SAR logic that configures the DAC, and a comparator that makes the decision.

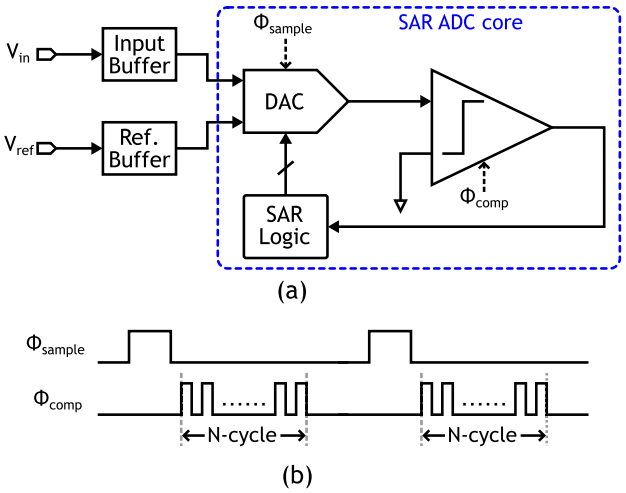


Fig. 2. Simplified (a) block and (b) timing diagrams of a SAR ADC.

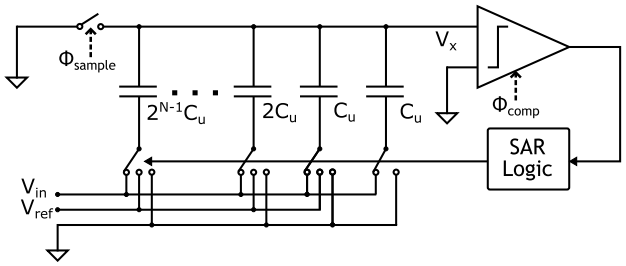


Fig. 3. Simplified classic SAR ADC implementation [1].

### B. SAR ADC Block Diagram and Operation

A simplified block diagram of an $N$-bit SAR ADC is shown in Fig. 2. In addition to the three core functional blocks mentioned above, an input buffer is used to ensure sufficient drivability and linearity of $V_{in}$, and a reference buffer is used to provide a low-noise $V_{ref}$ for DAC to produce a clean comparison voltage $V_{dac}$. The timing diagram shows that a SAR conversion includes a sampling phase where $V_{in}$ is sampled on the DAC, and a conversion phase where $N$ comparisons are made for an $N$-bit A/D conversion.

McCreary and Gray [1] reported the classic implementation of the SAR ADC, as shown in Fig. 3. The DAC is implemented by an array of binary-weighted capacitors with the unit size $C_u$. It realizes the inherent subtraction $(V_{in} - V_{dac})$ for the SAR conversion. During the sampling phase, the input pre-charges the bottom plate of the capacitor array, while the top plate is connected to ground. As a result, a total charge of $Q_{tot} = -2^N C_u \cdot V_{in}$ is sampled at the top plate. After the sampling phase, the SAR conversion starts by connecting the bottom plate of the largest capacitor $2^{N-1}C_u$ to $V_{ref}$ and the remaining plates to ground. Due to the charge conservation at the $V_x$ node, the voltage during the

first conversion cycle can be calculated as:

$$V_x = \frac{V_{ref}}{2} - V_{in} \tag{2}$$

By comparing it with 0, we are equivalently comparing $V_{in}$ with $V_{ref}/2$. Based on the result of this decision, the SAR logic re-configures the DAC and makes $V_x$ successively approach 0, thereby realizing the digitization of $V_{in}$.

The bottom-plate sampling scheme is adopted in this implementation, which suits well for high-linearity data converters due to its mitigation of charge injection [7], [8]. Recently, with transistor feature size decreasing, the charge injection issue has been largely relieved. As a result, the bootstrapped top-plate sampling scheme became increasingly popular owing to its simple implementation, especially for low-to-medium precision converters [9]–[14].

## III. SAR ADC Noise Analysis

There are various types of errors in a SAR ADC that can degrade its effective resolution. While some can be addressed by circuit techniques (e.g., clock bootstrapping for sampling nonlinearity [7]–[14] and calibration for capacitor mismatches [15]), others are more fundamental (e.g., thermal noise). In a well-designed SAR ADC, its signal-to-noise-and-distortion ratio (SNDR) should be limited not by distortion, but by noise. The reduction of noise typically requires increased power consumption. For a SAR ADC with clean peripherals (e.g., sampling clock, input driver, and reference voltage), its noise is typically dominated by the sampling $kT/C$ noise and the comparator thermal noise. To provide an overview, this section discusses common noise sources in a SAR design.

### A. Sampling Error

Accurate sampling is the foundation of the SAR conversion. There are two major error sources during the sampling process: clock jitter and sampling noise.

The jitter is mainly contributed by the thermal noise in the clock generation circuits, e.g., phase-locked loop (PLL) and clock drivers. Assuming $\sigma_t$ is the rms value of the timing error $\Delta t$, the jitter limited SNR is given by [5], [16], [17]:

$$SNR_{jitter} = 20 \cdot \log\left(\frac{1}{\omega_{in} \cdot \sigma_t}\right) \tag{3}$$

Notice that to increase the jitter limited SNR by 6 dB, $\sigma_t$ has to be reduced by 2 times. Hence, a low-jitter clock is necessary for the ADC to achieve high resolution.

Another major error source is the widely-known sampling $kT/C$ noise. It is contributed from the sampling switch. With the sampling capacitor of $C_{dac}$, the total sampled noise $\overline{v_{n,out}^2}$ can be calculated as:

$$\overline{v_{n,out}^2} = \frac{kT}{C_{dac}} \tag{4}$$

For $C_{dac}$ of 1 pF, $\sqrt{\overline{v_{n,out}^2}} = 64\ \mu$V at the room temperature of 300 K. For an ADC input signal of 1-V peak-to-peak, at least 52-fF $C_{dac}$ is needed to ensure 10-bit resolution (i.e., a $kT/C$ noise limited SNR of 62 dB). The requirement on $C_{dac}$ increases exponentially with the target resolution. For example, a 14-bit resolution ADC would demand more than 13-pF of $C_{dac}$. A large $C_{dac}$ greatly increases the power, area, and design complexity of the entire ADC system.

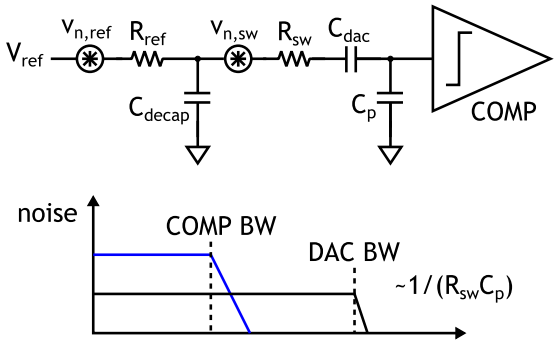


Fig. 4. Reference and DAC noise model.

Besides that, the ADC input buffer contributes extra noise during the sampling phase, which is also integrated and sampled onto $C_{dac}$. Thus, care must be taken in the design of the input buffer to ensure that its noise is sufficiently low [18].

### B. Reference Noise and DAC Noise

During the SAR conversion phase, the reference buffer and DAC switches contribute noise. Their noise models are shown in Fig. 4. $v_{n,ref}$ represents the reference buffer output noise. Since $v_{n,ref}$ directly adds to the reference voltage, it is usually made sufficiently small by design. In addition, a large decoupling capacitor $C_{decap}$ is usually placed at the reference buffer output. $C_{decap}$ is often much bigger than $C_{dac}$ to ensure fast DAC settling. It also filters out $v_{n,ref}$. As a result, with careful design, the reference buffer noise is usually much smaller than the DAC switch noise, and can be ignored in practice.

The DAC noise PSD is set by the DAC switch resistance $R_{sw}$. The noise bandwidth depends on the combination of $C_{dac}$ and the top-plate parasitic $C_p$. Since they are series-connected and $C_{dac}$ is much larger than $C_p$, the total integrated DAC noise is approximately $kT/C_p$, which can be quite large. Fortunately, not all of it affects the comparator decision. In practice, to ensure a fast DAC settling, the DAC switch resistance $R_{sw}$ is usually made very small, leading to a wide DAC bandwidth (i.e., $1/R_{sw}C_{dac}$). In low-to-medium speed SAR converters, comparator bandwidth is usually designed to be relatively small to minimize its noise. Therefore, a large portion of the DAC noise is filtered out by the comparator. The effect of the DAC noise can be significantly suppressed and become negligible for low-to-medium resolution applications.

### C. Comparator Noise

The comparator is the key circuit block that converts an analog voltage into a digital output. It plays a critical role in defining the SAR ADC performance. A comparator usually consists of a pre-amplifier that amplifies the input signal, followed by a latch that uses positive feedback to resolve the final decision. The effect of the pre-amplifier is to attenuate

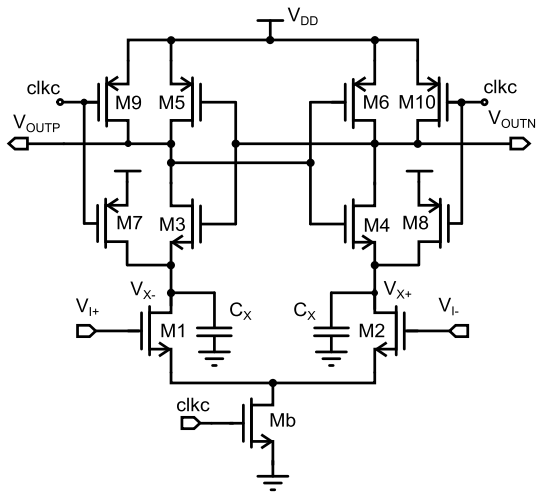


Fig. 5. The schematic of strong-arm latch.

the large offset, noise, and kickback from the latch. With a sufficient pre-amplifier gain, the comparator noise are typically set by its pre-amplifier.

The conventional design adopts a static pre-amplifier (e.g., a common-source amplifier). Comparing to a dynamic one, it offers larger gain, stronger common-mode and power-supply rejection and more robustness against process, voltage, and temperature (PVT) variations. Nevertheless, it consumes static current, which often results in low energy efficiency.

To save power, dynamic pre-amplifiers are becoming increasingly popular. Fig. 5 shows the schematic of the Strong-Arm latch [19]–[21]. It has been widely used as the comparator in a SAR ADC over the past decades. The input pair, $M1/M2$, and the tail device, $Mb$, form an implicit dynamic pre-amplifier. The cross-coupled inverter on the top serves as the latch. The operation of the Strong-Arm latch can be divided into the pre-amplification phase and the latch regeneration phase, separated by the turn-on of the PMOS cross-coupled pair [22].

The analyses in [22]–[25] show that the pre-amplifier noise of the Strong-Arm latch can be expressed as:

$$\overline{v_{n,pre}^2} \approx \frac{I_D}{g_m} \cdot \frac{4kT\gamma}{V_{thn}C_x} \tag{5}$$

where $V_{thn}$ is the NMOS threshold voltage that sets the pre-amplification time. To minimize noise, the $g_m/I_D$ of the input pair can be increased by biasing it in the weak inversion, but it has an upper limit of $q/nkT$, where $n$ is the subthreshold slope factor. In addition, increasing $g_m/I_D$ often results in reduced speed [22]. The other effective way to reduce the comparator noise is to enlarge the loading capacitor $C_x$, but it directly increases the comparator power consumption.

## IV. Comparator Power Reduction

This section first reviews low-power design techniques for a standalone comparator. Then, it surveys techniques that take advantage of the architectural property of the SAR ADC to reduce the total comparator power consumption.

### A. Standalone Low-Power Comparator Design Techniques

*1) Low-Power Voltage-Domain Comparators:* The Strong-Arm latch can be considered the baseline comparator design. It is simple and widely used, but it has limitations in the performance, including energy efficiency and speed. Over the past decades, researchers have developed several advanced dynamic comparators that outperform the Strong-Arm latch in various aspects.

One such design is the two-stage dynamic comparator proposed by Schinkel *et al.* [26]. It separates the latch stage from the pre-amplifier stage. As a result, it greatly accelerates the latch regeneration speed, reducing comparator delay. Nevertheless, the drawback is that the input transistor of the latch starts from the linear region, which reduces the effective inter-stage gain. This results in increased noise and offset coming from the latch. To overcome this issue, Miyahara *et al.* [27] and Van Elzakker *et al.* [28] modified the topology of the latch to ensure the latch input transistors start from the saturation region, leading to a higher gain and reduced comparator noise and offset. Another effective technique to boost the gain, as presented by Hsieh and Hsieh [29], is to use cascaded input pairs. By vertically stacking three input pairs, it equivalently increases the pre-amplification time by threefold, achieving a 3 times gain. Overall, its comparator energy efficiency is improved by 2 times thanks to the further attenuated latch noise.

The aforementioned techniques achieve higher energy efficiency by increasing the effective pre-amplification gain. However, the pre-amplifier load $C_x$ discharges completely to ground during comparison, consuming a fixed energy of $2 \cdot C_x \cdot V_{DD}^2$. Since large $C_x$ is required to suppress the noise, as indicated in (5), the pre-amplifier consumes the majority of the power in a low-noise comparator design, e.g., approximately 80% in [26], [28]. Hence, there is a strong need to improve the energy efficiency of the pre-amplifier itself.

To save the pre-amplifier reset power, Liu *et al.* [30] presented a bi-directional dynamic comparator. As shown in Fig. 6, the pre-amplifier stage consists of both NMOS and PMOS input pairs. During the first half of the pre-amplification phase, the PMOS pair switches on so that the pre-amplifier loads are charged up from ground. Once they cross half $V_{DD}$, the PMOS side turns off, and NMOS pair turns on to perform the second half of the pre-amplification. As a result, the pre-amplifier loads return to their initial condition, which avoids the reset power. It only consumes an energy of $C_x \cdot V_{DD}^2$ while realizing the same gain and noise performance as the conventional design. Theoretically, it can improve the pre-amplifier energy efficiency by 2 times. Limited by the extra circuits needed for operation control, the overall comparator energy efficiency improvement is 1.5 times compared to that of a Strong-Arm latch. To further improve this, Tang *et al.* [31] combines bi-directional pre-amplifier with a common-gate stage of [32]. On top of the reset power saving, it extends the pre-amplification time and realizes a 3 times gain boost. Yet, the overall efficiency improvement is still limited by extra circuits.

In the conventional dynamic pre-amplifier design, the loading capacitors are fully discharged despite the fact that

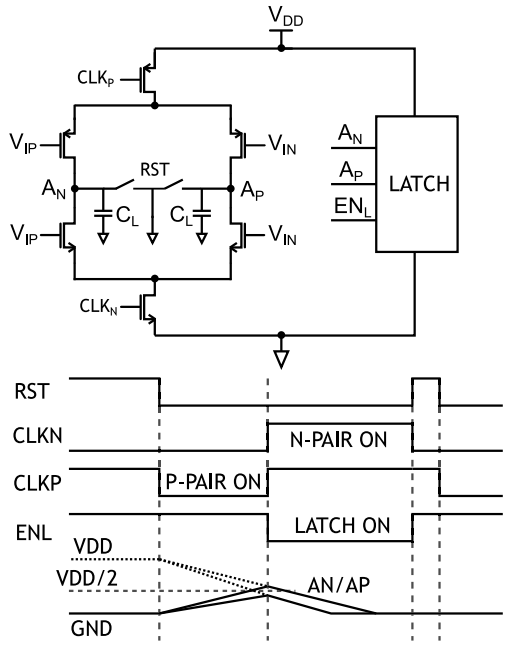


Fig. 6. The bi-directional dynamic comparator [30].

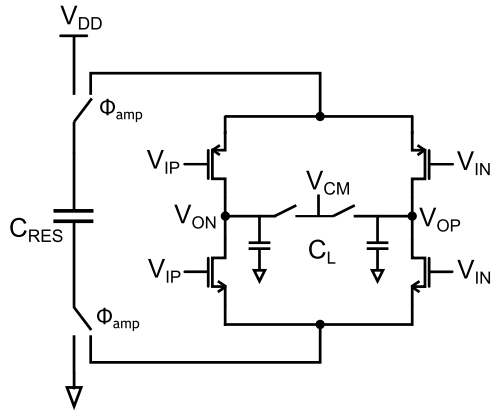


Fig. 7. The floating inverter amplifier [34].

only the initial portion contributes to the noise reduction [24], [25]. Bindra *et al.* [33] proposed a dynamically-biased pre-amplifier to address this issue. By providing a degeneration capacitor, $V_{GS}$ of the input pair keeps decreasing, and eventually, the input pair is cut off. It prevents fully discharging the load. In addition, the reduced $V_{GS}$ boosts the $g_m/I_D$ during the pre-amplification phase, which increases gain and reduces noise. This work achieves over 2.5 times energy efficiency boost compared to its predecessor in [28].

Tang *et al.* [34] further improved the energy efficiency by introducing the floating inverter amplifier (FIA). As shown in Fig. 7, it adopts a CMOS input stage which naturally realizes current reuse. By powering the FIA with a floating reservoir capacitor, it provides a constant output common-mode voltage, which elongates the pre-amplification time and increases the gain. It also avoids the common-mode discharge of the loading capacitor, thus saving considerable energy. In addition, the isolated power domain provided by the reservoir capacitor

TABLE I
COMPARATOR PRE-AMPLIFIER COMPARISON

| Pre-amp Architecture | Speed | Area Efficiency | Pre-amp Gain | Energy Efficiency* | Sensitivity ** |
|---|---|---|---|---|---|
| Conventional | Good | Good | Poor | Poor | High |
| Dynamic Biasing | Poor | Fair | Fair | Fair | High |
| Bi-directional | Fair | Fair | Poor | Fair | Medium |
| FIA | Poor | Poor | Good | Good | Low |

* Pre-amp's thermal noise suppression in terms of power consumption
** Sensitivity against input CM/PVT variations

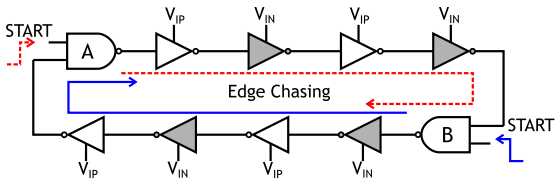


Fig. 8. The edge-pursuit comparator [41].

makes the amplification insensitive of the input common-mode voltage and PVT variations. The reservoir capacitor also provides dynamic biasing similar to [33], which boosts the pre-amplifier $g_m/I_D$. Combining all these merits, it realizes a robust dynamic comparator with greater than 7 times energy efficiency improvement compared to that of the Strong-Arm latch.

Table I gives a qualitative evaluation of state-of-the-art comparator pre-amplifiers. The conventional pre-amplifier excels with great speed and simplicity, and is still widely used. When targeting energy efficient applications, the FIA is a promising choice by offering high gain, great energy efficiency, and robustness simultaneously.

To conclude, in the past years, various low-power dynamic comparators have been proposed. Here samples a few highlighted techniques:

- Pre-amplifier gain boosting techniques, such as double-tail comparators [27], [28] and cascaded input pairs [29].
- CMOS input pairs that double the pre-amplifier energy efficiency, such as bi-directional comparator [30] and FIA [34].
- Biasing techniques that boost $g_m/I_D$ of the input pairs, such as dynamic biasing pre-amplifier [33] and FIA [34].

*2) Low-Power Time-Domain Comparators:* In addition to the voltage-domain circuit optimizations, another promising direction is to perform the comparison in time-domain, which benefits from technology scaling with increased transistor speed and reduced power consumption. Time-domain comparators have been proposed and demonstrated in SAR ADCs, showing good potential in power efficiency and scalability [35]–[43]. In the time-domain comparison, an input voltage signal is first converted to a time delay, which is then digitized using a 1-bit time-to-digital converter. The voltage-to-time conversion can be implemented by amplifiers [36], voltage-controlled delay lines (VCDLs) [37], [39], [42], and voltage-controlled oscillators (VCOs) [38], [40].

To further exploit the time-domain information, Yang *et al.* [44] and Shim *et al.* [41] proposed the edge-pursuit comparator (EPC), as shown in Fig. 8. The comparison

is performed by two clock edges chasing each other over a ring oscillator, with the two path delays controlled by the differential input voltages respectively. Eventually, the oscillation collapses, and the end state indicates the comparison result. Note that it automatically scales comparison energy according to its input difference, resulting in energy saving for coarse comparisons. By comparison, the conventional comparator consumes nearly constant energy regardless of the input levels. Benefited from this architecture, it achieves a 67 times automatic energy scaling between the MSB and LSB bit decisions in a 15-bit SAR ADC. However, limited by the slow time-domain comparison, this prototype only realizes 20 kS/s conversion speed.

The time-domain comparator naturally operates under low-supply voltage, demonstrating a good fit for advanced technology. The edge-pursuit comparator [41], [44] presents automatic input and energy scaling. However, it suffers from low comparison speed and has not been widely adopted. As for the multi-bit comparators, due to the nature of non-linear voltage-to-time conversion, they usually require calibration.

### *B. Architectural-Level Comparator Power Reduction Techniques*

Besides designing an energy-efficient comparator, we can also take advantage of a SAR ADC's architectural level property to reduce the total comparator power. For an $N$-bit SAR ADC, its comparator needs to fire $N$ times, but the noise requirements for different comparisons are not the same. With a small comparator input, the comparator noise needs to be low to ensure a correct decision. However, with a large input, the comparator noise requirement can be significantly relaxed while still producing the correct decision. Notice that out of the $N$ comparisons, the comparator input is less than LSB/2 only once. For all other comparisons, the noise requirement can be loosened to save energy. Nevertheless, the challenge is that we do not know when the critical decision happens, as it depends on an unknown input. Researchers have developed several techniques to address this concern.

One solution is to identify this critical comparison cycle and reduce its noise accordingly. Harpe *et al.* [45], [46] employed a judger circuit to identify the critical comparison cycle by comparing the decision time with a pre-set timer. Once the critical cycle is identified, it repeats the decision multiple times and adopts the majority result, thus effectively reducing the comparator noise. Equivalently, it reconfigures the comparator into low-noise mode for critical decisions. Take a 12-bit SAR conversion as an example. A 5 times majority voting reduces the total input-referred noise from 0.95 LSB down to 0.66 LSB with a SAR power increase of 33%. To achieve the same performance, conventional analog-scaling requires a 300% increase of the comparator power consumption (4× power consumption for 2× noise reduction). However, just like other time-domain operations, the critical comparison judger suffers from PVT variations and requires calibration.

The other widely adopted solution is providing redundancy in the SAR search algorithm, which allows the mistakes in earlier decisions to be corrected later [47]–[51]. By leveraging the redundancy, it can tolerate various errors during the conversion, such as comparator noise and DAC settling error/noise, as long as they are within the following redundancy range. It equivalently relocates the critical comparisons to the LSB decisions.

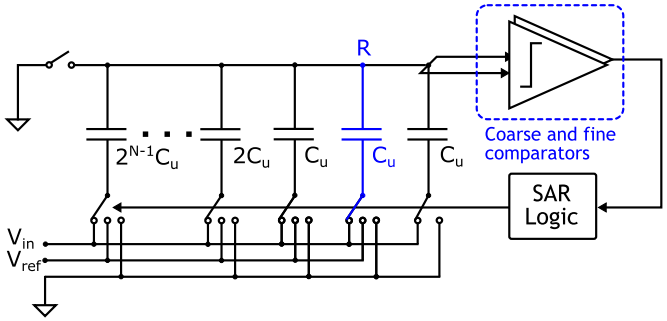


Fig. 9. The combined redundancy with two-comparator architecture [52].

Giannini *et al.* [52] combined the redundancy with a two-comparator architecture, as shown in Fig. 9. The last two bit decisions including the redundant bit adopt a low-noise comparator to ensure the conversion accuracy, while the previous $(N-1)$ conversions rely on a high-noise but low-power comparator to save energy. The input-referred noise of the fine comparator is designed to be half of that of the low-power one. A rough estimation indicates the power consumption of the low-noise comparator is 4 times that of the low-power one. Compared to the conventional design, where all $N$ decisions require the low-noise comparator, this work only needs to fire it twice, thus reducing the total comparator power by approximately 55% in a 9-bit SAR ADC. However, it suffers from the offset mismatches between two comparators, which has to be calibrated. One can also provide large redundancy to correct the offset mismatch. However, the large redundancy needs to be provided in a more significant bit, which increases the number of low-noise comparisons and leads to low energy efficiency.

To reduce the comparator offset mismatches, Harpe *et al.* [53] reported a load switching comparator, whose load capacitor could be reconfigured to switch between low-noise and low-power modes. By sharing the comparator input transistors between two modes, the offset mismatch is largely reduced. Thus, it can be corrected by a small redundancy provided at LSB and does not require offset calibration. Another variation was reported in [54], where the same comparator is reconfigured into low-noise mode for LSB conversions by majority voting.

As the comparator noise switching technique shows great energy efficiency improvement, the question then arises: what is the optimal number of comparator noise modes? To answer that, Ahmadi and Namgoong [55] explored the optimal allocation of the comparator noise power, demonstrating that optimal comparator noise monotonically decreases from MSB to LSB. Interestingly, a simple two-comparator design has already achieved a rough approximation of the ideal allocation. In a 10-bit SAR design without redundancy, the last 3 bit adopting the low-noise comparator realizes a 42% power

reduction compared to the SAR with a single comparator. The improvement would be more significant if there is redundancy allocated to the critical LSBs. Although employing more than two comparators further improves the ADC power efficiency, most of the energy reduction occurs when two comparators are employed. The use of additional comparators suffers from diminishing returns. Inspired by the majority voting technique, Ahmadi and Namgoong [56] further explored the optimal voting allocation for the SAR ADC. By changing the voting numbers for each bit decision, it configures the same comparator into different noise modes. Since it only requires one comparator, the offset mismatch issue is obviated. It is worth noting that the edge-pursuit comparator introduced in the earlier section naturally realizes the dynamic noise power scaling [41].

The adaptive tracking average technique is reported by Miki *et al.* [57] to reduce the comparator noise in the LSB decision. It fires the LSB comparison multiple times with the DAC updating. By adopting the averaged output codes, it can reduce not only the comparator noise, but also the quantization noise; in other words, the original $N$-bit SAR can realize a resolution over $N$-bit. The additional LSB DAC switching also tolerates DAC incomplete settling error, thus making it suitable for high-speed applications. In this prototype, the LSB is averaged 8 times. Compared to a conventional design with the same performance, it achieves over 60% comparator power reduction at the cost of an additional LSB DAC.

To further reduce the comparator power and noise, Verbruggen *et al.* [58] and Chen *et al.* [59] introduced the statistical estimation theory to the field of ADC design. They fire LSB comparison multiple times without DAC reconfiguration and exploit all the information embedded in the comparator output distribution. By utilizing maximum likelihood estimator (MLE) [58] and Bayes estimator (BE) [59], they not only make a binary majority decision for the LSB bit, but also estimate the magnitude of the residue comparator input voltage. This residue estimation process effectively reduces comparator noise, DAC noise, and quantization noise. The work equipped with Bayes estimator can realize a 7-dB SNR improvement with 17 times LSB firing [59], which presents over 85% comparator power reduction compared to the conventional analog scaling.

Researchers also explored to embed the time-domain comparator into the multi-comparator architecture [60]–[62]. They use a coarse voltage-domain comparator for the first few quantizations and a fine time-domain comparator for the last critical ones. With the low-power time-domain comparator, they achieve great overall energy efficiency.

To conclude, in the architecture level, researchers have developed various techniques aiming to scale the comparator power with the noise requirement dynamically. Sampled highlighted techniques include:

- Identifying the critical comparison with dynamic noise reduction [45], [46]
- Relocating the critical comparisons to LSBs with comparator reconfiguration [52], [53]
- Statistical noise reduction techniques that trade speed for accuracy [58], [59]

## V. DAC Switching Power Reduction

With the DAC capacitor size limited by sampling noise requirement, the DAC switching power contributes a significant part towards the total power consumption. The reference buffer needs to supply the switching energy and ensure fast settling during the conversion. Therefore, the DAC power reduction also eases the design requirement of the reference buffer. Although the reference buffer power itself has not been captured by ADC energy efficiency calculation (e.g., FoM), it shows increasing importance from the system perspective.

The DAC switching power is presented in the form of $\alpha \cdot C_{dac} \cdot V_{ref}^2$, where $\alpha$ is the effective DAC switching rate and $C_{dac}$ represents the total DAC capacitance. This section first reviews a few widely-adopted low-power switching techniques that lower the switching activity, which reduces the DAC switching energy. Then, the latest developments in minimizing capacitive DAC size $C_{dac}$ to approach thermal noise limit are surveyed.

### A. Low-Power Switching Techniques

This part reviews a few widely-used switching techniques. To form a fair comparison, they are evaluated in a 10-bit SAR with the same full-scale input and total DAC capacitance, which represents the fundamental thermal noise limitation.

To start, the conventional switching technique is explained. For a conventional fully-differential $N$-bit SAR DAC [1], it requires a total of $2^{N+1}$ unit capacitors (a single-ended version is shown in Fig. 3). The differential inputs are bottom-plate sampled in that prototype. After sampling, the DAC array is reconfigured to present $V_{in}$ at the comparator input, where MSB capacitor is connected to $V_{refp}$ and the others are connected to $V_{refn}$. Then, the comparator result updates the differential DAC successively and makes both DAC top plate voltages approach $V_{cm}$, thereby realizing SAR conversion. Unfortunately, the conventional switching scheme is not power efficient due to the differential DAC switching. In addition, 50% of codes need preset-(evaluate)-reset switching operations, which consume considerable energy. Although the bottom-plate sampling is adopted in [1], its top-plate counterpart has the same energy consumption. Although the top-plate switching saves MSB reconfiguration energy, it consumes reset power.

To overcome these limitations, Liu *et al.* [13] reported the monotonic switching technique. The top-plate sampling is adopted, where the DAC bottom plates are reset to $V_{refp}$. This obviates the MSB reconfiguration power and reset power. In addition, each reconfiguration only requires a single-side capacitor switching and eliminates the preset-(evaluate)-reset process. As a result, this realizes a 63% power reduction compared to the conventional one. However, all capacitors can only be switched from $V_{refp}$ to $V_{refn}$, resulting in a monotonically decreasing DAC output common-mode voltage that drops from $V_{cm}$ to ground. This limits the SAR conversion linearity [22], since it causes severe comparator performance variation (e.g., noise, offset, and speed).

To reduce the common-mode variation, Sanyal and Sun [63] presented the bi-directional single-side switching technique.

TABLE II
AVERAGE SWITCHING ENERGY OF A 10-BIT SAR ADC

| Architecture | Conversion energy ($CV^2$)* | Reset energy ($CV^2$)* | Normalized total energy | No. of unit cap** |
|---|---|---|---|---|
| Conventional | 682.65 | 0 | 1 | $2^{N+1}$ |
| Monotonic | 255.5 | 0 | 0.37 | $2^N$ |
| Bi-directional | 42.7 | 191.5 | 0.34 | $2^{N-1}$ |
| $V_{cm}$-based | 170.2 | 0 | 0.25 | $2^N$ |
| Split-cap | 170.2 | 255.5 | 0.63 | $2^{N+1}$ |
| CAS | 88.6 | 255.5 | 0.5 | $2^N$ |

* Normalized to the same $V_{FS}$ and $C_{dac}$
** Calculated for a N-bit differential SAR DAC

It maintains the single-side capacitor switching as in [13], but the DAC bottom plate reset voltages include both $V_{refp}$ and $V_{refn}$. As a result, the DAC output common-mode voltage can be switched bi-directionally to reduce the variation. Combined with the redundancy strategy, it mitigates the common-mode variation impact on the ADC performance [22], [64]. By configuring the reset voltages, it realizes different output common-mode voltage varying patterns that can be optimized for speed or noise [65], [66]. By introducing $V_{cm}$, it further reduces the switching energy consumption. Overall, it represents a 66% switching power saving compared to the conventional design. Note that, it consumes the reset power and requires a $V_{cm}$ generation circuit if there is not one already.

Zhu *et al.* [67] reported a $V_{cm}$-based switching technique. During the sampling phase, the bottom plates of the DAC are reset to $V_{cm}$, which avoids the reset power. During the SAR operation, the DAC is switched differentially to maintain a constant common-mode voltage. Overall, it realizes a 75% power reduction compared to the conventional design with the cost of an additional reference voltage $V_{cm}$ and the increased switch driving power.

To eliminate the introduction of $V_{cm}$, Ginsburg and Chandrakasan [68] split each capacitor into two equal sub-capacitors that are reset to $V_{refp}$ and $V_{refn}$, respectively. This maintains the constant output common-mode while mitigating $V_{cm}$. This switching process is equivalent to the $V_{cm}$-based switching, but it requires additional reset power. Overall, it realizes a 37% power reduction compared to the conventional design. Similar technique was reported in [69]. On top of that, Liou and Hsieh [70] reported the charge-average switching (CAS) technique. It generates the DAC output voltage shift by charge averaging between the bottom plates of the differential DACs instead of a conventional charging (or discharging) operation. It reduces the power consumption to 50% of that of the conventional design. However, it requires local boosted switches for the charge average operation, which is challenging especially in low supply designs.

Fig. 10 shows the DAC switching energy curves for a 10-bit SAR ADC, including both conversion and reset powers, versus output codes of the aforementioned techniques. Table II compares the average conversion energy, reset energy, and the total required unit capacitor elements.

Since the majority of the switching power comes from the MSB capacitors, it is highly desirable to reduce MSB switching specifically. Hsieh and Hsieh [29] presented a semi-resting switching (SR) technique. It uses the two identical sub-ADCs to convert the positive and negative inputs respectively, thus avoiding the most energy consuming MSB DAC switching. The integral non-linearity splitting switching (INLS) introduces an additional $V_{cm}$ reference voltage to further reduce the power consumption [61]. However, they double the input buffer power as well as hardware cost. The mismatches between the sub-ADCs need to be calibrated to ensure conversion linearity.

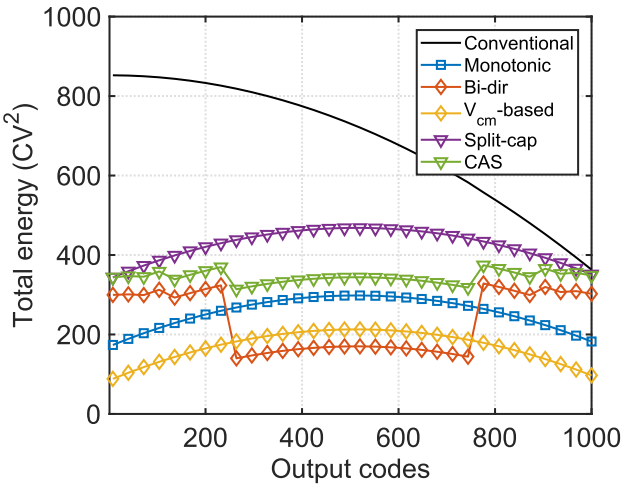


Fig. 10. DAC total energy versus output codes.

Tai *et al.* [71] reported a sub-ranging SAR ADC with a detect-and-skip (DAS) scheme, as shown in Fig. 11. A small coarse ADC is used to determine the first few MSB bits of the sampled signal, and the conversion results are applied directly to the MSB part of the fine DAC. Then, the fine ADC continues to resolve the remaining LSB bits. As a result, the unnecessary MSB capacitor switching in the fine ADC is skipped, achieving a significant reference buffer power reduction. A low-power comparator can be employed for the coarse ADC to further reduce the ADC energy consumption. With this technique, this work advanced state-of-the-art energy-efficiency ADC and realized the first sub-1 fJ/conversion-step SAR ADC. Alternatively, Lee *et al.* [72] realized a 2-bit coarse ADC through a single comparator. The comparator detects the polarity of the MSB bit. Simultaneously, the next bit is determined by checking its comparison time with a pre-calibrated delay. In this manner, the first two MSB bits are resolved right after the input sampling without any DAC switching.

Among those emerging switching techniques, $V_{cm}$-based [67] and split-capacitor-based [68] switching schemes are recent favorites due to the balance between energy efficiency, implementation simplicity, and good common-mode control. Detect-and-skip [71], as the universal switching energy reduction technique, is widely adopted in high-resolution designs with large DAC capacitance.

### *B. Custom MoM Capacitor Layout*

In addition to the switching activity reduction, the designer should also minimize the DAC capacitor size toward the

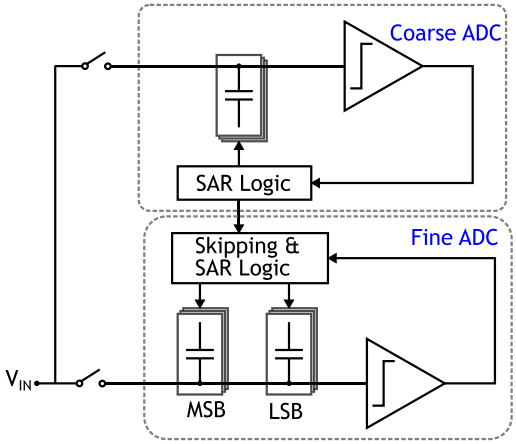


Fig. 11. Sub-ranging SAR ADC [71].

fundamental thermal noise limit to improve the power and area efficiency. Yet, this is usually hindered by the available minimum unit capacitor size and capacitor mismatch requirement. This part first surveys the emerging developments in custom-designed capacitive DACs. Then, mismatch suppression techniques that address the DAC linearity issues are introduced.

For a 12-bit ADC with 1-V signal swing, the conventional switching scheme only requires a unit capacitor size of 0.2 fF to meet $kT/C$ noise requirement. However, such a small capacitor is usually not available in the foundry's standard library. As a result, the DAC size is often overdesigned, leading to a waste of power and area. To address this issue, researchers proposed the custom-designed capacitive DACs.

In [73], Harpe *et al.* presented a metal-oxide-metal (MOM) DAC array with 0.5-fF unit capacitors. The DAC array is made with finger capacitors. It uses top metal layers with minimum width and space to reduce the unintended parasitic capacitance. The unit capacitor value can be easily adjusted by changing the finger length. Huang *et al.* [74] presented an encapsulated MOM capacitor design, where the top-plate of the capacitor is enclosed by the bottom-plate to reduce the parasitic capacitance. The capacitor design in [75] consists of multiple layers of crossing metals, increasing the capacitance density and reduces the fringe field coupling.

To further improve the area efficiency and accuracy, Harpe [76] demonstrated the unit-length capacitor design. The effective capacitance is defined by the length difference between two strips. This way, a binary-scaled DAC array can be realized by scaling the length difference rather than the element number. As a result, $N$-pair capacitors with equal length are sufficient to realize a $N$-bit DAC, in contrast to $2^N$ as required in conventional design, thus greatly simplifying the implementation and interconnection. Note it also relieves the edge effects, which are largely canceled through capacitance subtraction between two strips. A small LSB capacitance of only 125 aF is realized in this design, and the 10-bit SAR ADC occupies only $36 \times 36$ um$^2$.

With the feature size shrinking, the MOM capacitor offers increasing area efficiency. Together with the removal of extra masks required in the metal-insulator-metal (MIM) counterpart, it has been more favored in recent years. A few state-of-the-art unit capacitor implementations are surveyed to provide design references [73]–[76]. Designers should pay extra care to layout-dependent nonidealities. For instance, dummy cells of a few $\mu$ms are usually required to relieve the edge effects.

### C. Capacitor Mismatch Error Suppression Techniques

With the reduction of unit capacitor size, the capacitor mismatch may become the linearity bottleneck for a SAR ADC. Certain switching techniques can alleviate the capacitor mismatch issue by reducing the maximum switched voltage. For instance, as reported in [77], in addition to the switching energy reduction, DAS can halve the worst case INL by halving the worst case voltage error [71], [77].

However, to fully resolve such issue and target for high precision applications, more sophisticated solutions are required. One classic method is to provide analog compensation. In [15], Lee *et al.* presented a self-calibration technique. In this work, the mismatch of a single capacitor in the main DAC is converted to an error voltage by swapping the bottom plate voltages between the measured capacitor and the reference ones [78]. The voltage error is then measured and digitized with an extra sub-DAC. The digitized error codes are stored in a RAM and are used to correct the capacitor mismatch during the subsequent normal SAR conversions. To reduce the overheads for calibration, Ding *et al.* [79] proposed to make use of SAR redundancy and only detect the sign of errors through an extra trial at the end of a SAR conversion phase. The accurate analog correction is finally achieved by a stepwise feedback loop with multiple detections.

In contrast to the analog calibration discussed above, researchers also proposed the digital calibration, which adjusts the digital weight to match its actual capacitor value. A widely-used approach is to use the digital conversion results to build a cost function. Then an adaptive algorithm, e.g., least mean squares (LMS), is applied to figure out the optimal capacitor weights that minimize the cost function. The set of optimal weights will then be used in the normal conversions. The LMS engine can be implemented either off-chip [80] or on-chip [81].

Apart from calibrations, error shaping techniques may also be used to address the capacitor mismatch issue. This takes advantage of the fact that even Nyquist-rate ADCs often sample at multiples of the Nyquist frequency to relax the system's anti-aliasing requirements. The classic mismatch error shaping (MES) technique in $\Delta\Sigma$ ADCs is dynamic element matching (DEM). However, the circuit complexity of DEM grows exponentially with the DAC resolution, so it is not suitable for SAR ADCs. To resolve this, in [82], Shu *et al.* developed an error feedback (EF) MES technique well suited for high-resolution SAR ADCs, as shown in Fig. 12. The idea is to reapply the conversion result of the previous cycle during sampling. By doing so, it explicitly feeds back the mismatch errors from the previous conversion cycle and subtracts them out in the present cycle, thus creating a first-order shaping effect on the mismatch error. The hardware

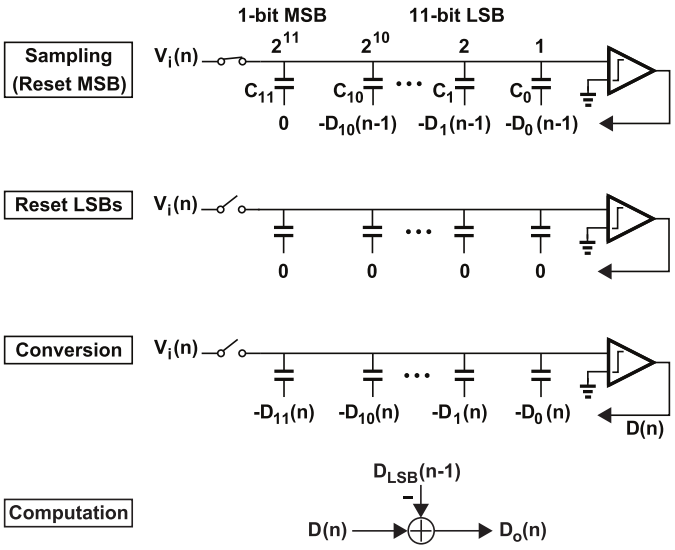


Fig. 12. The first-order EF MES [82].

cost grows linearly with the number of bits and is substantially lower than DEM. Liu *et al.* generalized the EF MES technique to second-order and more advanced forms [83], [84], enabling it to be applied to various types of low-pass, band-pass, and high-pass converters.

With the reduction of unit capacitor size, the mismatch errors usually require extra care to ensure DAC linearity. Digital calibrations have been widely adopted by the industry thanks to the increasing computation power [80]. The mismatch error shaping technique has just emerged and already demonstrated its potential in high-resolution systems [82], [83].

## VI. Digital Power Reduction

Digital circuits consume both active and leakage power. The active power is proportional to $C_{total} \cdot V_{DD}^2$, where $C_{total}$ represents the digital circuit capacitance, including both routing and transistor parasitics, and $V_{DD}$ is the digital power supply. $C_{total}$ benefits naturally from technology scaling due to the reduced feature size and the corresponding routing overhead. Thanks to the reduced transistor threshold voltages in the advanced technology, a lower power supply can be applied, which has been widely used in state-of-the-art low-power designs, e.g., 0.45 V in [71], 0.4 V in [29], and 0.3 V in [85].

In addition to the technology scaling, researchers have developed various techniques to simplify the SAR logic design and further reduce $C_{total}$. In a classic SAR ADC, a system clock is required to generate the sampling and comparator clock. For example, an $N$-bit SAR operation requires at least one clock cycle for sampling and $N$ cycles for comparison. Hence, a system clock running at $(N+1) \cdot f_s$ is required for the ADC with $f_s$ sampling rate. To generate the required clock phases, a clock counter and a decoder form the state machine, which is triggered by the system clock. A separate shift register array is required in the SAR logic to generate the data latch signal. As a result, each comparison cycle triggers 1 D-type Flip Flop (DFF) in the clock counter, 1 DFF in the sequencer, and 1 data storage DFF.

Researchers have devoted to simplify the SAR logic. An example is reported in [31]. The SAR sequencer is merged with the clock generation block, which contains only one shift register chain. In addition, a latch is used for data storage instead of the DFF. As a result, the SAR logic power is reduced by roughly 2 times; it only includes 1 DFF and 1 latch switching energy per bit. On top of that, DFFs can be implemented with dynamic logics to further reduce digital power, e.g., the true single-phase clock (TSPC) logic of [86], [87] is adopted in [31].

Besides the active power, leakage also contributes a significant proportion of the total digital power, especially in ultra-low-power SAR ADCs within nanowatt power range. To alleviate this issue, a few low-leakage circuit optimizations have been introduced in [88], including employing a low digital supply voltage, adopting high threshold and long channel transistors, and stacking transistors. With all these techniques, the leakage power still constitutes 25% of the total power, as reported in [88]. One reason is that with a low conversion speed of several kHz, the ADC often operates in the data-driven mode with long idle time. To address this issue, right after the SAR conversion, the circuit can be power-gated [89] or reset to a predefined state with minimum leakage power [90].

Given the higher frequency of the external system clock required in the synchronous SAR ADC, the clock generation and distribution also pose a large power overhead. To resolve this, Chen and Brodersen [80] presented an asynchronous timing scheme for the SAR ADC. It only requires a set of global sampling clocks, and all the clocks for SAR blocks, including comparator and DAC updating, are generated internally. Although this scheme is designed to achieve high conversion speed initially, it finds great usage in low-power SAR designs as it requires only a low frequency system clock of $f_s$ and saves substantial clock generation and distribution power.

Although digital power benefits from the technology scaling automatically, researchers still developed techniques to further reduce the active and leakage power consumption, e.g., simplified SAR logic and power gating [31], [88], [89]. Lowering supply voltage has proven to be very effective with the cost of potential speed limitation [29], [71], [85]. Clock generation and distribution power can be largely reduced by adopting asynchronous operation [80].

## VII. Benchmarking and Trend Summary

This Section summarizes the SAR energy efficiency evolution and gains insights. The results from recent publications (till June 2021) are plotted in Fig. 13. In observing the past developments, we draw several conclusions:

- Prior to 2015, SAR energy efficiency improves dramatically. It is close to 2× per year, faster than feature size shrinking speed. It is made possible by both technology advancement and engineering ingenuity.
- Since 2016, the SAR energy efficiency has not improved much. Researchers started to focus more on

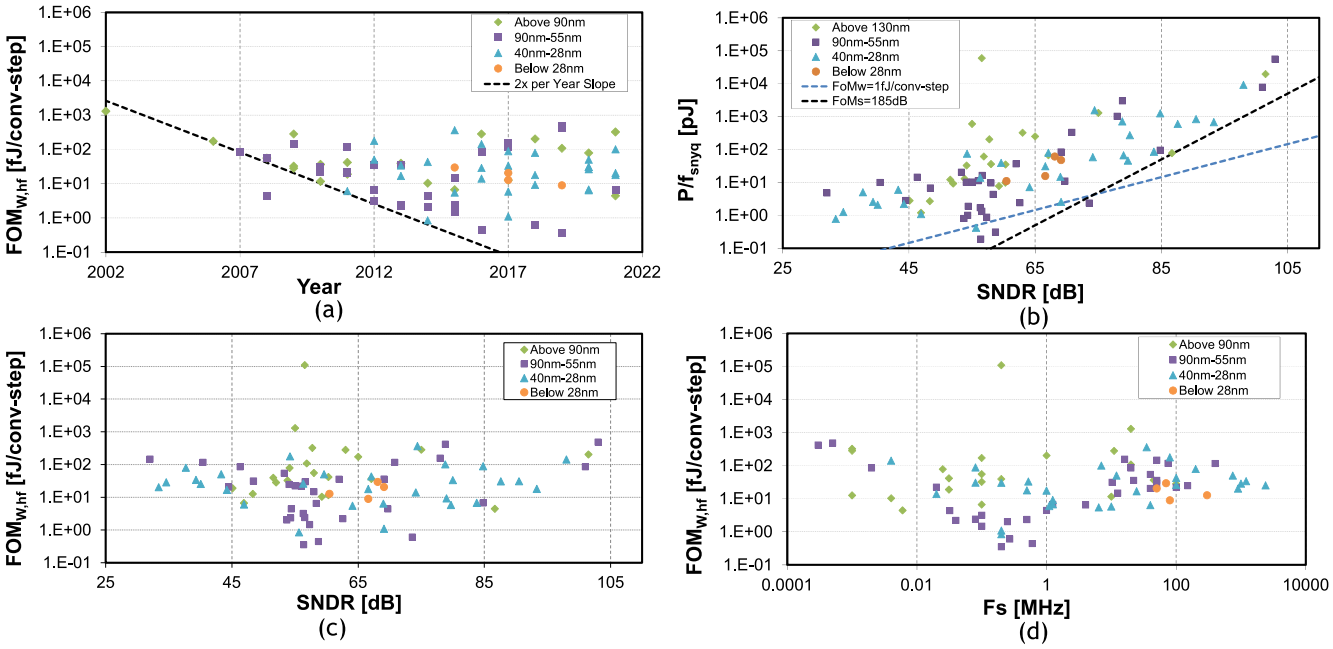


Fig. 13. (a) The survey of FoMw over year, the surveys of (b) conversion energy and FoMw over SNDR, and (d) the survey of FoMw over conversion speed [2].

performance-driven designs, such as high-precision ($\geq$ 14b) and high-speed ($\geq$ 200MS/s) converters.

- With the technology evolving from 180nm to 55nm, the SAR energy efficiency keeps improving. For low-to-medium speed SAR converters, the technology sweet spot is presented between 90nm and 55nm, where the digital power has been reduced substantially.
- The introduction of more advanced technologies, e.g., FinFET below 28nm, mainly contributes to the conversion frequency. Since the SAR power is limited by thermal noise, which does not scale with technology, the advanced technology does not help energy efficiency much.
- For SAR converters below 10-b, the energy efficiency is mainly limited by digital circuits, i.e., technology nodes. Thus, their energy efficiency follows by 2×-per-bit trend, as indicated by FoMw in Fig. 13(b).
- For converters over 13-b, their power consumption is dominated by the analog components such as comparators, and thus, they follow the 4×-per-bit trend (FoMs).

## VIII. Emerging Developments and Conclusion

Benefiting from technology scaling, SAR becomes one of the most popular implementations for analog-to-digital interfaces in system-on-chip designs. It achieves leading energy efficiency and opens up numerous opportunities for emerging applications. This paper provided a comprehensive understanding of the SAR energy efficiency limiters. Various emerging techniques were introduced to improve the energy efficiency of the comparator, input/reference buffers, and digital logic at both circuit and architectural levels. Those innovations have enabled SAR architecture to advance state-of-the-art performance for the past decade.

With the core SAR ADC performance approaching the limit, noise, mismatch, and other physical constraints pose stringent challenges for further improvements. There are a few future trends that are currently explored by researchers.

### A. Search Algorithm Optimization

In addition to circuit design innovations, researchers started to optimize the search algorithm to reduce the conversion power. For instance, Liu *et al.* [91] and Huang *et al.* [92] reported the bypass window technique, allowing SAR to skip several conversion steps when the signal is within a small predefined window. Similar techniques were reported in [43], [93], [94]. Researchers also investigated solutions to reduce the SAR switching activity by leveraging the input signal's prior knowledge. For instance, targeting sparse input signal, Yaul and Chandrakasan [95] make use of the signal activity pattern and propose LSB-first successive approximation. It saves both DAC switching and comparison energy. With the emerging of application-specific designs, researchers should optimize SAR ADCs accordingly for the best energy efficiency.

### B. System-Level Co-Optimization

The rapidly growing chip integration level indicates the urgency to improve the energy efficiency from system perspective. Researchers are actively exploring system-level co-optimization techniques to tackle the overheads brought by the peripheral components, e.g., input and reference buffers.

For example, researchers have explored techniques to optimize the input buffer design by the range pre-selection sampling technique [96], [97]. Buffer-in-the-loop architectures are proposed to shield the sampling capacitance from the external driver [98]–[100]. Researchers also proposed techniques to

break sampling $kT/C$ noise limitation [18], thus enabling a smaller DAC capacitance to reduce both input and reference driving costs. Early demonstrations include correlated double sampling-based $kT/C$ noise cancellation [101] and noise bandwidth switching technique [102].

### C. Hybrid SAR Converters

By combining the merits of SAR and other types of ADCs, hybrid SAR converters show promising features and receive wide attention recently. For instance, emerged since 2010s, pipelined SAR adopts high-speed pipeline operations while still maintaining energy efficient nature of SAR converters [103]. SAR-assisted zoom ADC utilizes SAR to perform low-power coarse searching for accurate zoom-in conversion [104]. The noise-shaping (NS) SAR ADC inherits the energy efficiency from SAR and the high resolution from $\Delta\Sigma$ ADC [105], and becomes extremely popular in recent years. Those efforts continuously push SAR-based converters realizing unprecedented performance improvements.

### D. SAR Design Automation

In addition to performance improvements, researchers also endeavor to boost SAR's design efficiency by combining design knowledge with state-of-the-art electric design automation (EDA) techniques. For instance, a synthesizable SAR is proposed in [106], aiming to boost SAR design efficiency with synthesizable digital circuits. Design automation in device sizing [107] and layout generation [108] are being actively explored. However, current approaches still require manual efforts in designing custom libraries or layout templates, and are short in precision and flexibility.

### E. Conclusion

As a concluding remark, SAR architecture has already achieved huge successes in many industry applications. Noting the emerging techniques and innovations in recent years, we can expect SAR-based data converters to continue pushing state-of-the-art energy efficiency. We hope that these citations help the designers find the proper low-power techniques for the specific design targets, and can be a good starting point for new SAR-related research.

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