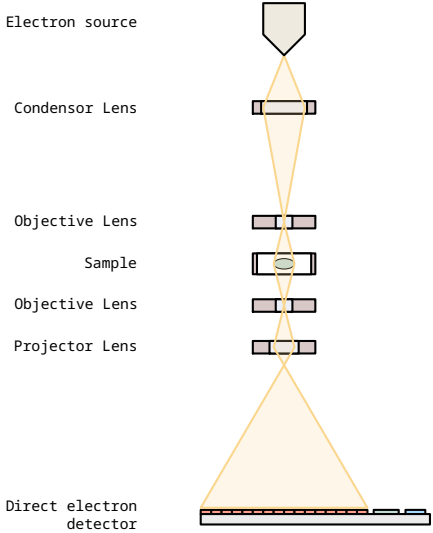
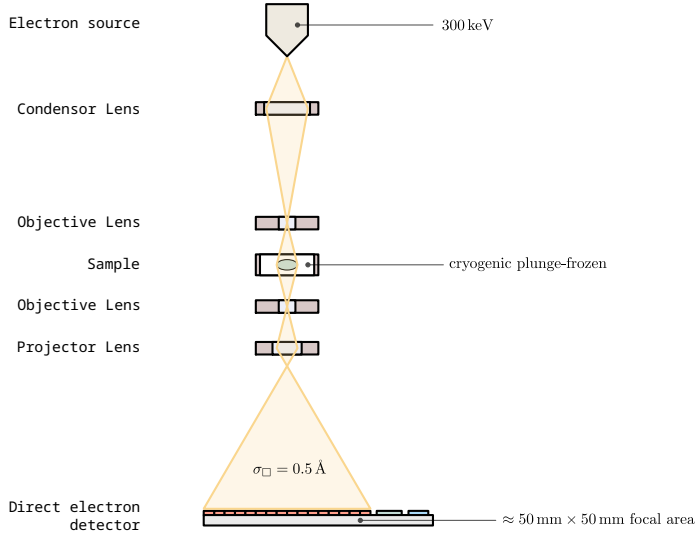
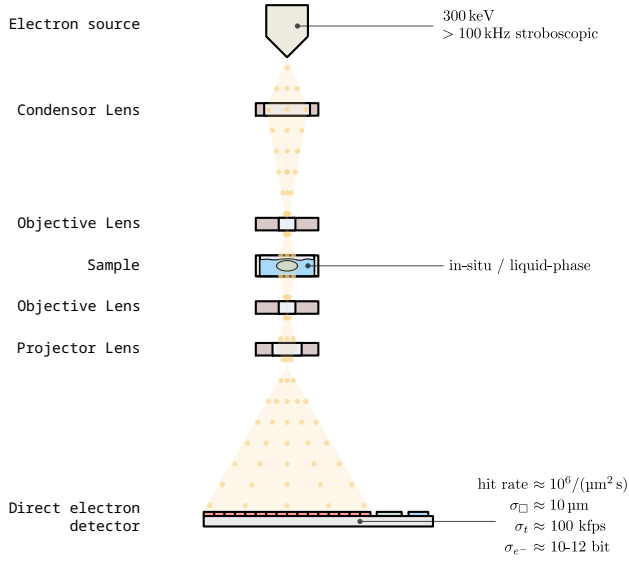
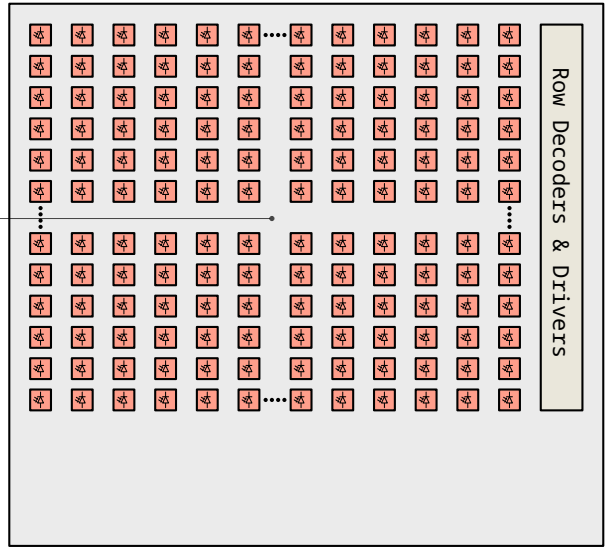
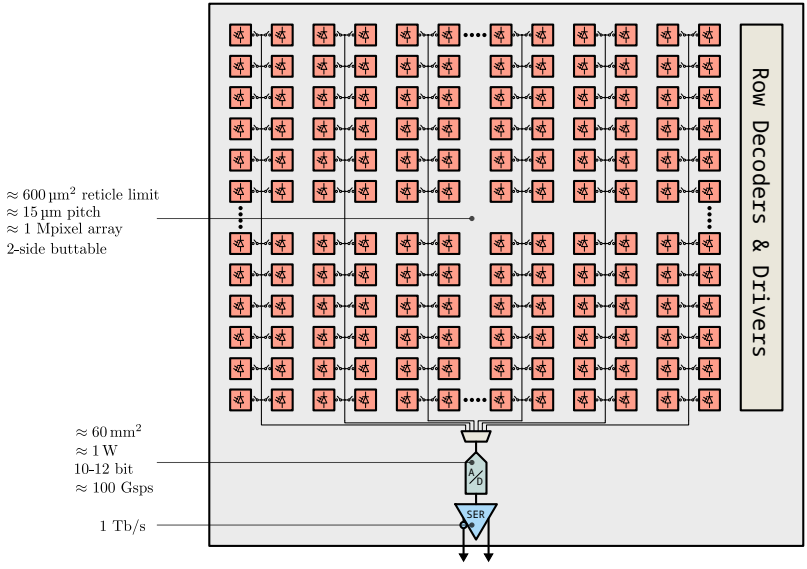
Modeling data converters for high frame rate imaging detectors

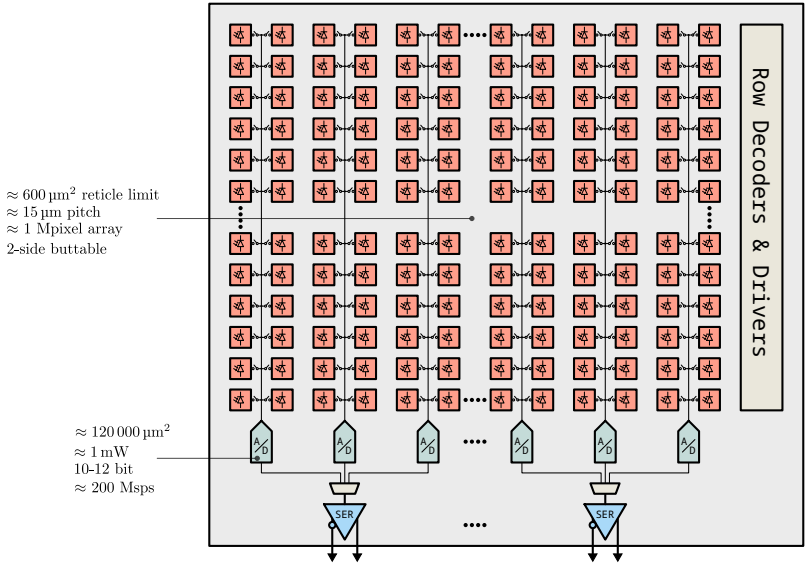

Electron source
Condensor Lens
Objective Lens
Sample
Objective Lens
Projector Lens
Direct electron
detector

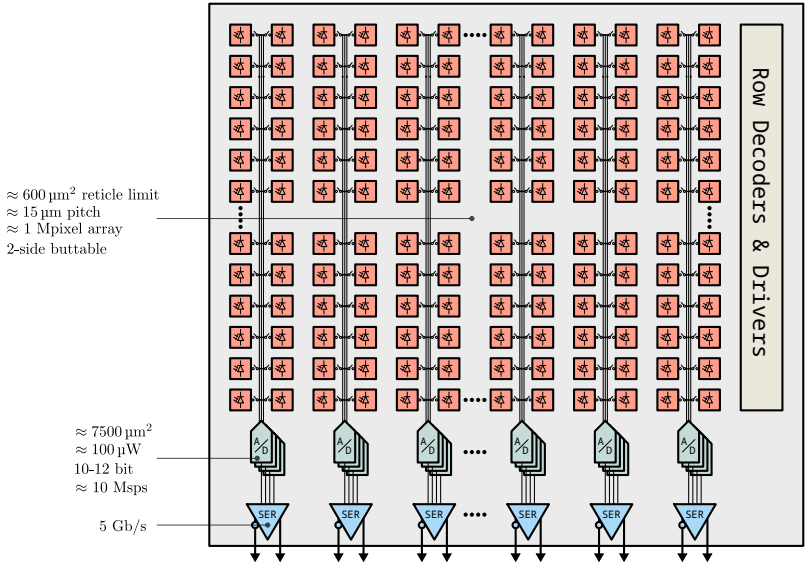

Electron source
300 keV
Condensor Lens
Objective Lens
Sample
cryogenic plunge-frozen
Objective Lens
Projector Lens
$\sigma_{\square} = 0.5\,\text{Å}$
Direct electron detector
$\approx 50\,\text{mm} \times 50\,\text{mm}$ focal area

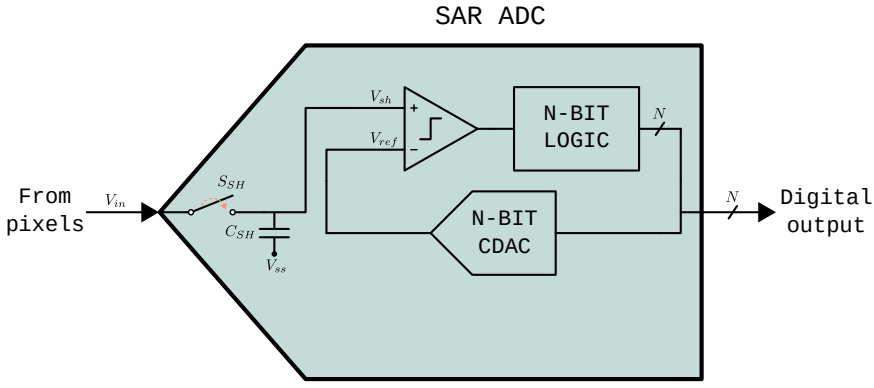

Electron source
300 keV
> 100 kHz stroboscopic
Condensor Lens
Objective Lens
Sample
in-situ / liquid-phase
Objective Lens
Projector Lens
Direct electron detector
hit rate ≈ 10^6/(µm^2 s)
σ□ ≈ 10 µm
σt ≈ 100 kfps
σe− ≈ 10-12 bit

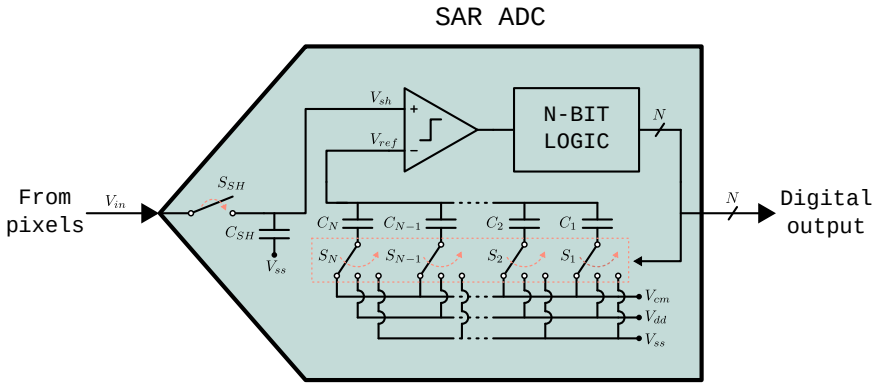

Row Decoders & Drivers
≈ 600 µm² reticle limit
≈ 15 µm pitch
≈ 1 Mpixel array
2-side buttable

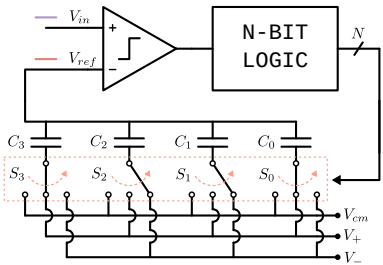

≈ 600 µm² reticle limit
≈ 15 µm pitch
≈ 1 Mpixel array
2-side buttable
≈ 60 mm²
≈ 1 W
10-12 bit
≈ 100 Gsps
1 Tb/s
Row Decoders & Drivers
A/D
SER

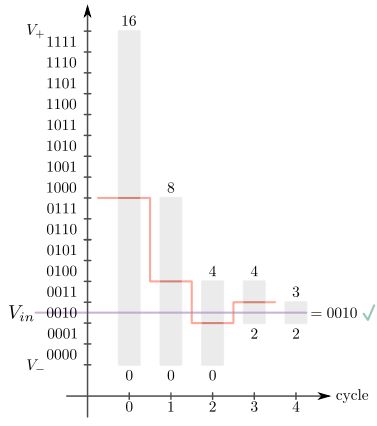

≈ 600 µm² reticle limit
≈ 15 µm pitch
≈ 1 Mpixel array
2-side buttable
≈ 120 000 µm²
≈ 1 mW
10-12 bit
≈ 200 Msps
Row Decoders & Drivers
A/D
SER

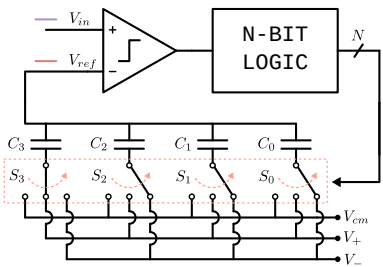

≈ 600 µm² reticle limit
≈ 15 µm pitch
≈ 1 Mpixel array
2-side buttable
≈ 7500 µm²
≈ 100 µW
10-12 bit
≈ 10 Msps
5 Gb/s
Row Decoders & Drivers
A/D
SER

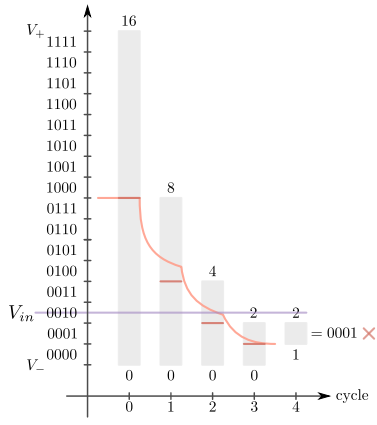

SAR ADC
From pixels
V_{in}
S_{SH}
C_{SH}
V_{ss}
V_{sh}
V_{ref}
+
−
N-BIT LOGIC
N-BIT CDAC
N
N
Digital output

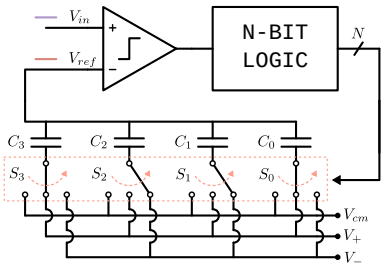

SAR ADC
From pixels
V_{in}
S_{SH}
C_{SH}
V_{ss}
V_{sh}
V_{ref}
+
−
N-BIT LOGIC
N
N
Digital output
C_N
C_{N-1}
C_2
C_1
S_N
S_{N-1}
S_2
S_1
V_{cm}
V_{dd}
V_{ss}

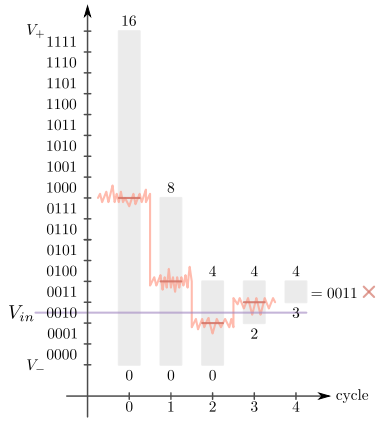

V_{in}
V_{ref}
+
−
N-BIT
LOGIC
N
C_3
C_2
C_1
C_0
S_3
S_2
S_1
S_0
V_{cm}
V_+
V_-

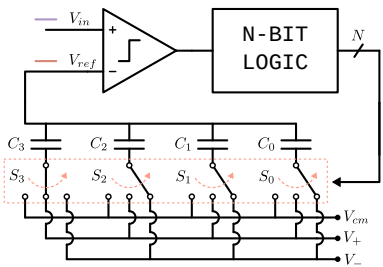

V_+
1111
1110
1101
1100
1011
1010
1001
1000
0111
0110
0101
0100
0011
V_{in}
0010
0001
0000
V_-
16
8
4
4
3
2
2
0
0
0
cycle
0
1
2
3
4
= 0010 ✓

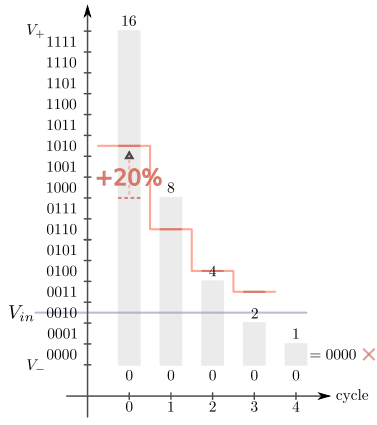

V_{in}
V_{ref}
+
−
N-BIT
LOGIC
N
C_3
C_2
C_1
C_0
S_3
S_2
S_1
S_0
V_{cm}
V_+
V_-

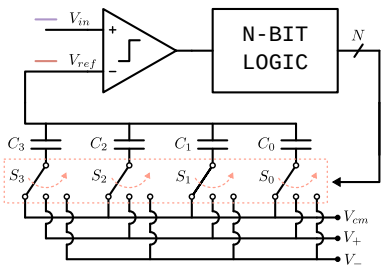

V_+
1111
1110
1101
1100
1011
1010
1001
1000
0111
0110
0101
0100
0011
V_{in}
0010
0001
V_-
0000
16
8
4
2
2
1
= 0001
0
0
0
0
cycle
0
1
2
3
4


V_{in}
V_{ref}
+
−
N-BIT
LOGIC
N
C_3
C_2
C_1
C_0
S_3
S_2
S_1
S_0
V_{cm}
V_+
V_-


V_+
1111
1110
1101
1100
1011
1010
1001
1000
0111
0110
0101
0100
0011
V_{in}
0010
0001
0000
V_-
16
8
4
4
4
= 0011
3
2
0
0
0
cycle
0
1
2
3
4


V_{in}
V_{ref}
+
−
N-BIT
LOGIC
N
C_3
C_2
C_1
C_0
S_3
S_2
S_1
S_0
V_{cm}
V_+
V_-


V_+
1111
1110
1101
1100
1011
1010
1001
1000
0111
0110
0101
0100
0011
V_{in}
0010
0001
V_-
0000
16
+20%
8
4
2
1
= 0000
0 0 0 0 0
cycle
0 1 2 3 4



$\downarrow$ C_{total} $\uparrow$

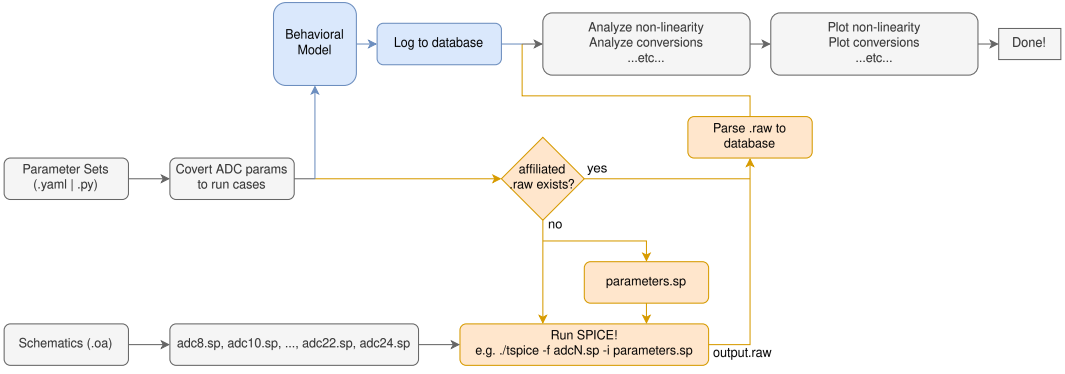
MOM cap density $\approx 0.5\,\mathrm{fF}/\mu\mathrm{m}^2$

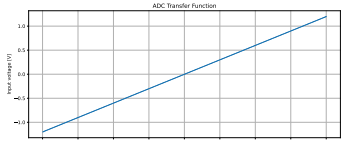
$E_{CDAC} \approx CV^2$

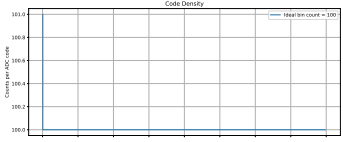
$\tau_{CDAC} \approx R_{switch} \times C_{total}$

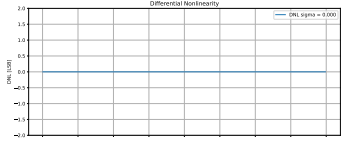
$C_\sigma \approx \frac{1}{\sqrt{C_{total}}}$

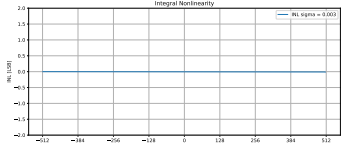
$V_{rms} = \sqrt{\frac{k_B T}{C}}$

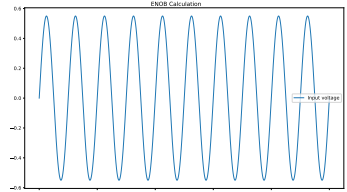

Behavioral Model
Log to database
Analyze non-linearity
Analyze conversions
...etc...
Plot non-linearity
Plot conversions
...etc...
Done!
Parse .raw to database
Parameter Sets (.yaml | .py)
Covert ADC params to run cases
affiliated .raw exists?
yes
no
parameters.sp
Schematics (.oa)
adc8.sp, adc10.sp, ..., adc22.sp, adc24.sp
Run SPICE!
e.g. ./tspice -f adcN.sp -i parameters.sp
output.raw

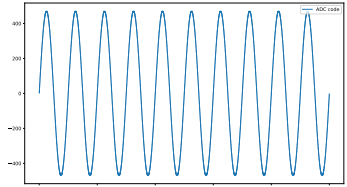


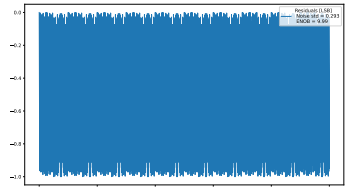




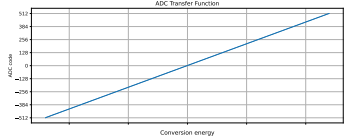


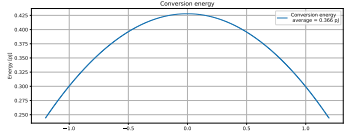


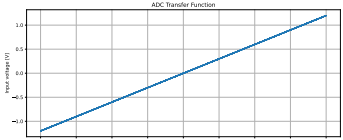


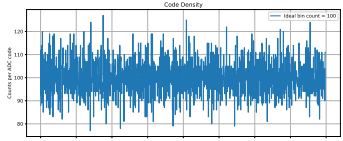


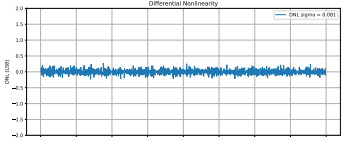
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	Msps
LSB size	2.344	mV
DAC weights array	[256 128 64 32 16 8 4 2 1]	
DAC weights sum	511	
DAC capacitor array size	9	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	0.000	mV
Comparator offset	0.000	mV
Reference voltage noise	0.000	mV
DNL	0.00	LSB
INL	0.00	LSB
ENOB	9.99	bits
FOM (energy/conversion)	0.04	pJ

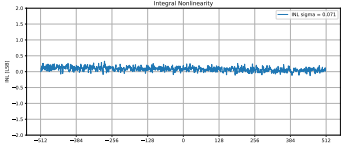


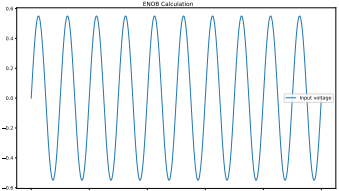


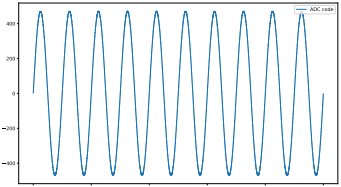


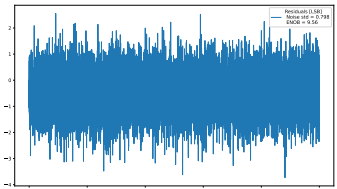












Parameter	Value	Unit
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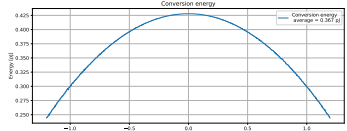
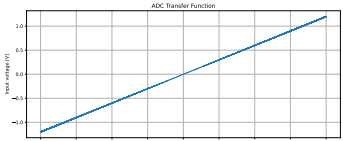
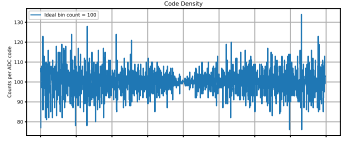
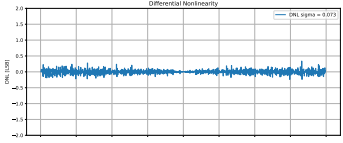
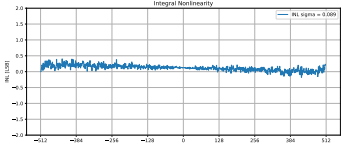
DAC weights sum	511	
DAC capacitor array size	9	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	0.000	mV
DNL	0.08	LSB
INL	0.07	LSB
ENOB	9.56	bits
FOM (energy/conversion)	0.04	pJ

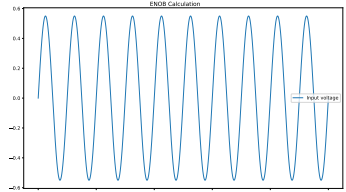


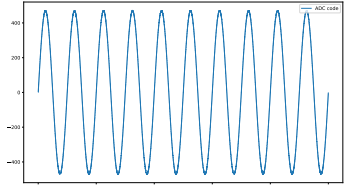


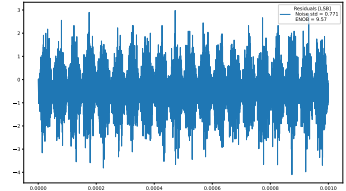




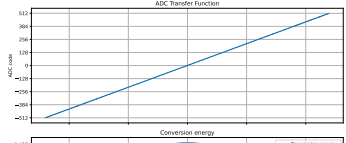


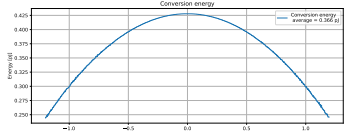


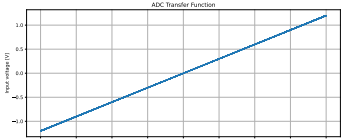


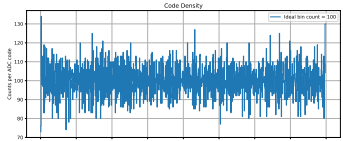


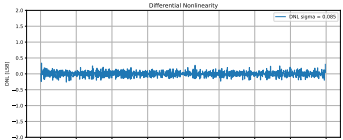
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	Msps
LSB size	2.344	mV
DAC weights array	[256 128 64 32 16 8 4 2 1]	
DAC weights sum	511	
DAC capacitor array size	9	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	0.000	mV
Comparator offset	0.000	mV
Reference voltage noise	3.000	mV
DNL	0.07	LSB
INL	0.09	LSB
ENOB	9.57	bits
FOM (energy/conversion)	0.04	pJ

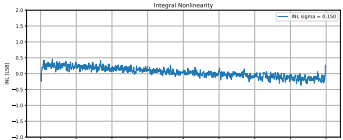


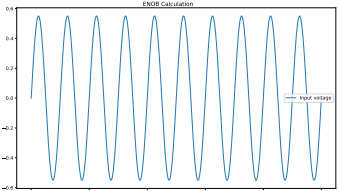


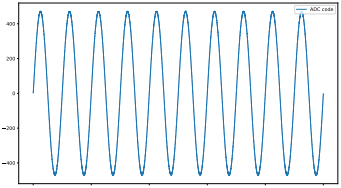


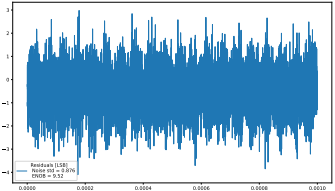












Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	Msps
LSB size	2.344	mV
DAC weights array	[192 128 64 56 32 16 8 7 4 2 1 1]	
DAC weights sum	511	
DAC capacitor array size	12	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	3.000	mV
DNL	0.08	LSB
INL	0.15	LSB
ENOB	9.52	bits
FOM (energy/conversion)	0.04	pJ