A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS

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***Abstract*—A 1.2 V 10-bit 100 MS/s Successive Approximation (SA) ADC is presented. The scheme achieves high-speed and low-power operation thanks to the reference-free technique that avoids the static power dissipation of an on-chip reference generator. Moreover, the use of a common-mode based charge recovery switching method reduces the switching energy and improves the conversion linearity. A variable self-timed loop optimizes the reset time of the preamplifier to improve the conversion speed. Measurement results on a 90 nm CMOS prototype operated at 1.2 V supply show 3 mW total power consumption with a peak SNDR of 56.6 dB and a FOM of 77 fJ/conv-step.**

***Index Terms*—Charge-recovery, reference-free, switched technique.**

I. Introduction

LOW POWER is the most relevant design concern for battery-powered mobile applications, such as DVB-T, DVB-H and TDMB [1]. Since the ADCs operate at tens of MS/s with 10 b to 12 b, the pipeline ADC is the commonly used architecture because of its power efficiency [2]–[4]. However, recently, the successive approximation register (SAR) architecture has re-emerged as a valuable alternative to the pipelined solution.

The conventional pipeline topology uses op-amps and switched capacitor structures to generate the residual. Moreover, the internal flash uses $2^n - 1$ comparators (n is the number of bits of the stage). All these blocks burn up power. Moreover, the reduction of supply voltage, as requested by sub-100 nm technologies, increases the consumed power because the reduced quantization step amplitude imposes an equivalent increase of the transconductance. Recent works [5]–[9] optimize the power design of pipeline ADCs but the figure of merit (FoM) remains in the hundred of fJ/conv-step range.

The pipeline architecture does not benefit from the technology scaling because the use of low voltage supplies gives rise to an augmented consumption of power. In contrast, the scaling of technology does not penalize much the SAR ADC architecture because its analog part is simply made by a comparator and a capacitive DAC array. Indeed, the FoM values of state-of-art SAR ADCs [10]–[12] are well lower than those of pipelines and the best FoM in record is an SAR ADC [13]. The FoM of a SAR converter that improves with thinner line-widths is now in the range of tens of fJ/conv-step. However, for 65 and 90 nm technologies, the conversion rate is still low, not more than 50 MS/s.

The speed of a SAR ADC is determined by the time required by the DAC to settle within 1/2-LSB. With large number of bits and capacitive arrays, the main cause of power consumption is the reference generator that must provide very low output resistance. A second important source of consumed power is the dynamic power of the DAC. Previous works [12]–[14] improve the conversion efficiency by saving part of the switching energy during each bit cycling. However, the spared energy is a small fraction of the total power dissipated by the reference voltage generator, especially at high conversion speed [15]. Therefore, the power efficiency improves if the power needed by the reference generator is not accounted for [9], [16], [17]. When this power is included the FoM drops significantly.

This design obtains remarkable power effectiveness for medium resolution and high conversion speed by using two strategies: the first avoids the reference generator by directly using the supply voltages; the second saves the switching energy during the SA conversion. The use of the supply voltage as the reference of the ADC would lead to a signal swing of the converter that is wider than the typical signal range; this would reduce the effective SNR. This drawback is removed with the proposed technique that grants a passive gain by 2 of the input. A doubling of the LSB, that relaxes the limits of noise and offset, also lowers the power consumption of the comparator. In addition, it is worth to notice that a multiplication by 2 enables an input signal that is half the rail-to-rail and not the full rail-to-rail as is presented in [12], [13], [18], [19]. Having an input range of the converter well within the supply limit is suitable for signals generated on-chip. This is very common because the input of an ADC is the result of on-chip

Manuscript received December 14, 2009; revised February 28, 2010; accepted March 24, 2010. Current version published June 09, 2010. This paper was approved by Associate Editor Lucien Breems. This work was supported by Research Grants from University of Macau and Macao Science and Technology Development Fund (FDCT).

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Digital Object Identifier 10.1109/JSSC.2010.2048498

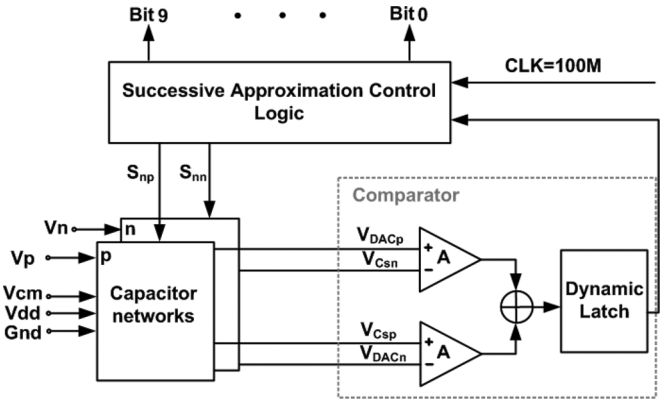

Fig. 1. Overall schematic diagram of the ADC architecture.

pre-conditioning, like amplification or filtering, obtained with op-amps whose signal swing represents headroom from the supply limits.

The switching energy saving technique, described in detail below, avoids the mismatch error at the conventional most significant bit (MSB) transition and enables a reduction by 2 of the overall capacitance used in the SAR. The charge recovery, implemented during each bit cycling, cuts by 1/3 the switching energy with respect to the one achieved in [12]. In addition, the used switching approach improves the conversion linearity that typically affects a conventional SAR ADC.

Instead of using the asynchronous processing [16] this paper avoids the fast clock by implementing a variable self-timed loop that adjusts the plus width of the preamplifier to reduce the ideal time for the LSBs conversions.

II. ADC Architecture

Fig. 1 shows the architecture of the proposed 10-bit SAR ADC. It comprises differential capacitor networks, a dynamic comparator and the SA control logic. The differential capacitor networks are composed by 10-bit split schemes with the additional sampling capacitors $\mathrm{C_s}$ necessary for the passive multiplication by 2. The SA logic controls $\mathrm{V_{out,DAC}} = \mathrm{V_{DACp}} - \mathrm{V_{DACn}}$ for bringing it toward $\mathrm{V_{out,Cs}} = \mathrm{V_{Csn}} - \mathrm{V_{Csp}}$. In the comparator, the 4 inputs preamplifier and the dynamic latch determine the value of each bit. The SA control logic includes shift registers, bit registers and a switching logic block, which control the DAC operation to perform the binary-scaled feedback during the successive approximation cycle. The frequency of the clock used by the SA block is the ADC sampling frequency. No fast clock at the input is needed because the SA uses the self-timed technique. All the SA control signals result from a proper use of internal delay lines and their logic combination.

As mentioned in the introduction, the scheme presented in the next sub-section obtains as a great benefit the equivalent multiplication by two of the input. This permits the reference free operation and enhances the profit of charge recovery, thus reducing power consumption.

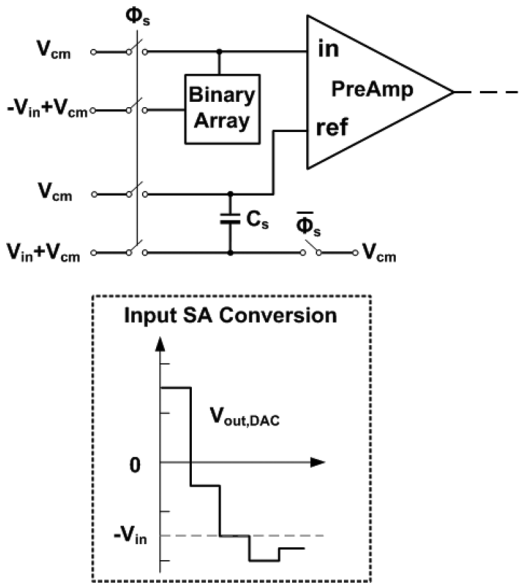

Fig. 2. Conceptual scheme that obtains a passive gain by 2.

A. Passive Multiplication by 2

A well-known feature of many SAR architectures is their insensitivity to parasitic capacitances. With conventional approaches the input of the comparator is at the reference voltage in the beginning of the conversion cycle and draws near the reference at the end of the conversion. As a result, the charge of the parasitic capacitance is almost the same at the beginning and the end of the conversion cycle. The schemes that are sensitive to parasitic experience a gain error and a linearity error. Obviously, the gain error due to the top-plate parasitic of DAC is not very important as it corresponds to an error of the voltage reference. More relevant is the non-linearity of the preamplifier input parasitic: the variation of the gate voltage may degrade the integral nonlinearity (INL). However, this parasitic nonlinearity effect is irrelevant: the parasitic of the preamplifier input is quite small when compared with the total capacitance of the DAC array. Therefore, the SAR ADC is, in practice, insensitive to the parasitic effects of both the DAC array and preamplifier. Consequently, for medium resolutions, parasitic insensitivity can be traded with other more valuable features. This design trades the parasitic insensitivity with the passive amplification by 2.

The conceptual scheme of Fig. 2 illustrates the method. During the sampling phase the binary-weighted capacitive DAC samples the input, like in a conventional scheme, while $\mathrm{C_s}$ samples the complementary input. During the conversion phase $\mathrm{C_s}$ shifts the voltage of the reference node to $-V_{\mathrm{in}}$, making equal to $2V_{\mathrm{in}}$ the signal that the SAR algorithm must compensate for.

The conventional SAR algorithm drives the DAC to finally converge to the common mode voltage (V_{cm}) at the end of the bit-cycling, according to

$$V_{\mathrm{in}} - \frac{\sum_n S_n C_n V_{\mathrm{ref,con}}}{C_{\mathrm{DAC,Sum}}} \rightarrow 0; \qquad (1)$$

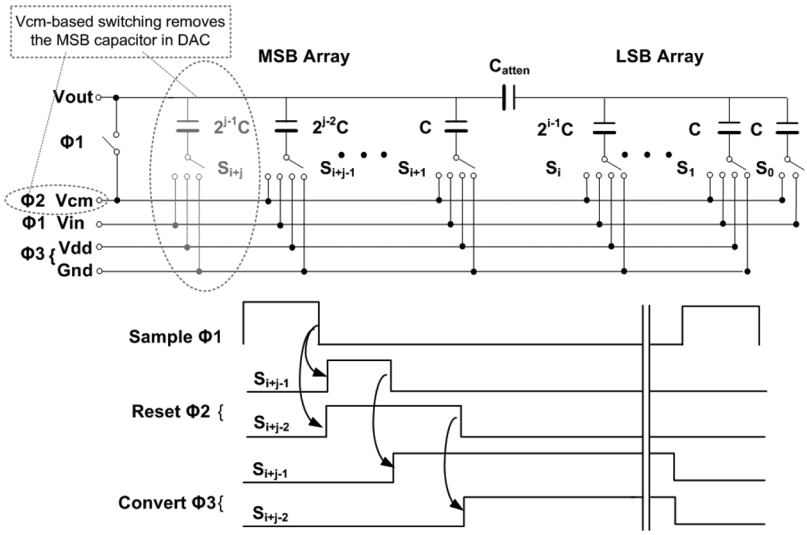

Fig. 3. The $\mathrm{V_{CM}}$-based switching timing diagram with its n-bit split capacitive DAC array $(\mathrm{n} = \mathrm{i} + \mathrm{j})$.

on the contrary, the proposed method drives the DAC to converge toward $-V_{\rm in}$ instead of $V_{\rm cm}$

$$V_{\rm in} - \frac{\sum_n S_n C_n V_{\rm ref,pro}}{C_{\rm DAC,Sum}} \rightarrow -V_{\rm in} \tag{2}$$

$$2V_{\rm in} - \frac{\sum_n S_n C_n V_{\rm ref,pro}}{C_{\rm DAC,Sum}} \rightarrow 0 \Rightarrow V_{\rm ref,pro} = 2V_{\rm ref,con}. \tag{3}$$

In the above equations S_n (1 or 0) is the ADC decision for bit n and C_n, $C_{\rm DAC,Sum}$ represents the capacitors connected to the reference voltage $V_{\rm ref,con}$ and the total array capacitance. Moreover, (3) certifies that the proposed operation corresponds to a passive amplification by 2 of the input. Furthermore, the proposed technique uses a reference voltage, $V_{\rm ref,pro}$, that is twice $V_{\rm ref,con}$, as used in the conventional counterpart. This is a key feature for the use of the supply voltage as reference. With $V_{\rm ref,pro} = 1.2\,\mathrm{V}$ identical to the supply voltage, the signal swing is 0.3–0.9 V with $V_{\rm cm} = 0.6$ V, a value that allows the ADC to use signals generated by on-system stages biased by the supply voltage.

The sampling capacitor $\mathrm{C_s}$ serves to hold the input signal for the SA conversion, consequently no specific matching condition is required between $\mathrm{C_s}$ and the DAC array. However, $\mathrm{C_s}$ must be large enough to comply with the kT/C noise constraint.

In addition to the supply voltages this architecture uses the common mode voltage to pre-charge the capacitors. However, since the processing is fully-differential, no charge flows through the common mode terminal, unless there is a mismatch between the used common mode and the one of the input signal. Assuming that the mismatch is less than 10%, the common mode generator must provide a limited charge: 10 times smaller than what is required to references used in conventional SAR converters. Therefore, the output resistance of the common mode generator and its power needs are significantly relaxed.

B. $V_{\rm cm}$-Based Switching Method

Switching the capacitive array consumes significant power. In order to reduce this term the value of the unit capacitance must be brought down to the limit allowed by the technology and the kT/C noise. Moreover, the use of the split capacitive array, that substitutes the full binary-weighted array, helps in the power reduction because the method reduces the total capacitance of the arrays. Further energy saving is obtained with effective switching approaches [12]–[14], [20], [21]. One of them, the set-and-down method recently proposed [12], saves significant switching energy thanks to its halving of the overall capacitance. The method used here, named $\mathrm{V_{CM}}$-based switching approach, also obtains a half-capacitance reduction. In addition, as shown below, the switching sequence reduces the energy by an additional 1/3 with respect to the set-and-down technique.

The $\mathrm{V_{CM}}$-based switching approach determines the sign of the differential input (MSB) by connecting the differential arrays to $V_{\rm cm}$. The power dissipation is just derived from what is needed to drive the bottom-plate parasitic of the capacitive arrays, while in the conventional charge-redistribution [13], [22] and the charge-recycling [14] methods the necessary MSB "up" transition costs significant switching energy and settling time. Moreover, the MSB capacitor, being not required anymore, can be removed from the n-bit DAC array. Therefore, the next $\mathrm{n}-1$ bits estimation is done with an $(\mathrm{n}-1)$ bit array instead of its n-bit counterpart, leading to half capacitance with respect to the conventional and charge-recycling methods.

Fig. 3 details the $\mathrm{V_{CM}}$-based switching algorithm. In the global sampling phase Φ_1, $V_{\rm in}$ is stored in the capacitor array. During the resting phase Φ_2, all the capacitors' bottom-plates are switched to the common-mode voltage, resulting in the equivalent output voltage $-V_{\rm in}$ at the output. The value of $V_{\rm out}$ determines the MSB during Φ_3 as the logic properly controls S_{i+j-1}. If $-V_{\rm in} > 0$, S_{i+j-1} goes to $\mathrm{G_{nd}}$ while the other switches $S_{i+j-2,\ldots}S_0$ remain connected to $V_{\rm cm}$. The result is that the voltage at $V_{\rm out}$ [2] becomes $-V_{\rm in} - V_{\rm ref}/2$.

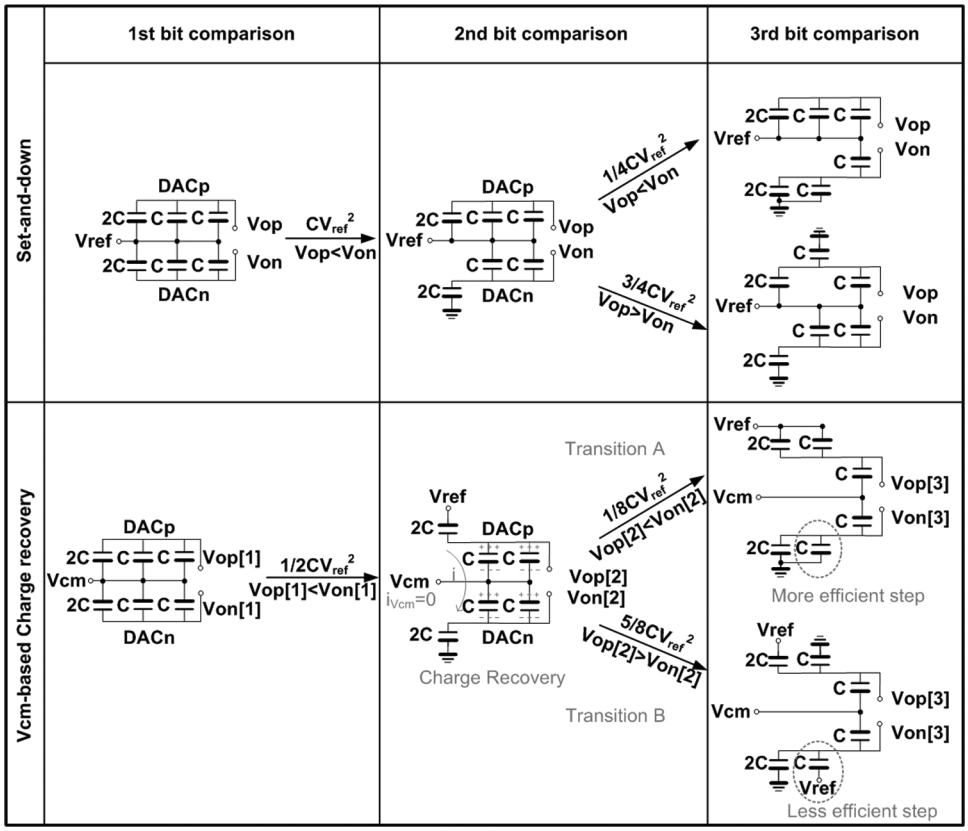

Fig. 4. A 3-bit example of set-and-down and proposed $\mathrm{V_{CM}}$-based switching procedures.

If $-V_{\mathrm{in}} < 0$, S_{i+j-1} is switched to $\mathrm{V_{dd}}$, raising the voltage at V_{out} [2] to $-V_{\mathrm{in}}+V_{\mathrm{ref}}/2$. The cycle is repeated for $\mathrm{n}-2$ times.

The scheme of Fig. 3 and the above description are for a single ended operation. In reality, the fully differential operation makes the algorithm insensitive to the input common mode, $V_{\mathrm{cm,in}}$. The difference between the common mode input and V_{cm} determines equal shifts $(V_{\mathrm{cm}} - V_{\mathrm{cm,in}})$ of the output of the array of Fig. 3. These shifts, assumed within the limits of the comparator common mode range, are rejected being a common mode component. Moreover, the $\mathrm{V_{CM}}$-based switching method foresees "up" or "down" transitions after the comparator determines the bit and not before. This does not require pre-charging of capacitors and, possibly, their discharging after the bit decision. Therefore, the performed charge-redistribution is just what is required without wasting power. The only additional cost of this method is that it uses n more switches to initially reset all the capacitors to a common-mode voltage.

C. Charge-Recovery

The $\mathrm{V_{CM}}$-based switching method operates in a similar way as the set-and-down [12] technique. Both reduce the capacitive array and simplify the MSB transition. However, for the determinations of the remaining $\mathrm{n}-1$ bits there is a different switching sequence.

To outline the difference between the two methods Fig. 4 shows the operational steps of a 3-bit differential capacitive array performing the $\mathrm{V_{CM}}$-based charge recovery and the set-and-down methods. From [12] when the supply is directly used as the reference voltage, a rail-to-rail input signal is required. Fig. 4 illustrates the case where the input signal of the two methods is in both rail-to-rail. Accordingly, the reference voltage $\mathrm{V_{ref}}$ and the common-mode voltage $\mathrm{V_{CM}}$ in the two approaches are equal to $\mathrm{V_{dd}}$ and $1/2\mathrm{V_{dd}}$, respectively. The switching energy needed for the first bit comparison is just what is necessary for driving the bottom-plate parasitics of the DAC arrays. Since the $\mathrm{V_{CM}}$-based method charges the parasitic to half of the reference voltage, while the set-and-down uses the full reference, the consumed energy for the first bit comparison of the $\mathrm{V_{CM}}$-based method is half of the set-and-down. The parasitic capacitance depends on technology and layout. Its value can be large because for medium and high-resolutions it is necessary to use electronic shielding on the top and the bottom which prevents couplings and noise injections.

The value of the MSB sets the arrays for second bit estimation. The SA logic controls the 2C of the $\mathrm{DAC_p}$ and $\mathrm{DAC_n}$ for "up" or "down" transition, respectively, as indicated also in Fig. 4, and the DACs' outputs finally settle to the following values:

$$\begin{aligned} V_{\mathrm{op}}[1] &= -V_{\mathrm{in}} + V_{\mathrm{cm}} \\ V_{\mathrm{on}}[1] &= V_{\mathrm{in}} + V_{\mathrm{cm}} \\ V_{\mathrm{op}}[2] &= -V_{\mathrm{in}} + 3/4V_{\mathrm{ref}} \\ V_{\mathrm{on}}[2] &= V_{\mathrm{in}} + 1/4V_{\mathrm{ref}}. \end{aligned} \tag{4}$$

The energy needed for the "up" transition in the $\mathrm{DAC_p}$ is E_{up} from 2C charged up from V_{cm} to V_{ref} and $E_{\mathrm{Vcm,p}}$ from the other capacitors connected to V_{cm}. They are

$$\begin{aligned} E_{\mathrm{up}} &= -2CV_{\mathrm{ref}}\left[(V_{\mathrm{op}}[2]-V_{\mathrm{op}}[1])-(V_{\mathrm{ref}}-V_{\mathrm{vcm}})\right] \\ &= 1/2CV_{\mathrm{ref}}^2 \end{aligned} \tag{5}$$

$$\begin{aligned} E_{\mathrm{Vcm,p}} &= -2CV_{\mathrm{cm}}\left(V_{\mathrm{op}}[2]-V_{\mathrm{op}}[1]\right) \\ &= -1/4CV_{\mathrm{ref}}^2. \end{aligned} \tag{6}$$

For the "down" transition in $\mathrm{DAC_n}$, the switching energy is only $E_{\mathrm{Vcm,n}}$ coming from the capacitors connected to V_{cm} and the value is

$$E_{\mathrm{Vcm,n}} = -2CV_{\mathrm{cm}}\left(V_{\mathrm{on}}[2]-V_{\mathrm{on}}[1]\right) = 1/4CV_{\mathrm{ref}}^2. \tag{7}$$

From (6) and (7) it is deducted that the energy used by the differential DACs is complementary. Therefore, $\mathrm{DAC_p}$ compensates the energy drawn from V_{cm} by $\mathrm{DAC_n}$. Qualitatively, the charge-recovery effect corresponds to a compensation of the charge transferred to $\mathrm{DAC_n}$ with charge coming from $\mathrm{DAC_p}$, as illustrated also in Fig. 4. Accordingly, we don't need energy from V_{cm} in each bit-cycling. Due to the charge-recovery implementation, the "down" transition of $\mathrm{DAC_n}$ does not consume switching energy; the second bit comparison just needs the energy E_{up} for $\mathrm{DAC_p}$ where the capacitor 2C is charged from V_{cm} to V_{ref}. The switching energy of the second bit transition is output code independent, and it always obtains 50% less energy than the set-and-down which requires CV_{ref}^2 to discharge the same capacitor in one of the differential DAC arrays.

The estimation of the energy required for the 3rd bit estimation is code dependent and gives rise to the values indicated in Fig. 4. For the transition A the $\mathrm{V_{CM}}$-based switching method is more advantageous; for the transition B the energy is almost the same.

For the conventional charge-redistribution method the switching energy also depends on the code. The consumed energy is much higher because of unnecessary charging and discharging actions. Fig. 5 compares the switching energy of the charge-recycling, the set-and-down and the $\mathrm{V_{CM}}$-based approaches. The given figures assume equal unit capacitor for the 10 b capacitor arrays. For all the methods the peak of the consumed power occurs at half scale. The set-and-down method is more effective than the charge-recycling technique by almost a factor of 3. The $\mathrm{V_{CM}}$-based switching method grants an additional 33% average benefit.

D. Linearity

As known the SAR algorithm does not ensure intrinsic monotonicity. The most critical transition for the conventional SAR ADC is at the middle range where half of the array switches-on and the other half (minus one) switches-off. The random variation ε_{C} of the value of the unity capacitance with variance σ_{C} renders rise to a differential nonlinearity (DNL) at the critical transistion equal to $\sqrt{2}\varepsilon_C \cdot 2^{N/2}$ [20], [23]. Since the $\mathrm{V_{CM}}$-based switching approach determines the MSB mismatch-independently, the worst case DNL occurs at $1/4\mathrm{V_{FS}}$ and $3/4\mathrm{V_{FS}}$. The feature relaxes the request of matching between unit capacitor by a factor $\sqrt{2}$. Therefore

$$\sqrt{2}\varepsilon_C \cdot 2^{(N-1)/2} < \frac{1}{2} \tag{8}$$

that, for the used technology and 3σ design, gives $C_U > 12$ fF. However, this project employs a larger unity value: $C_U = 50$ fF. The choice serves to make negligible the effect of parasitic associated to the interconnection metal lines.

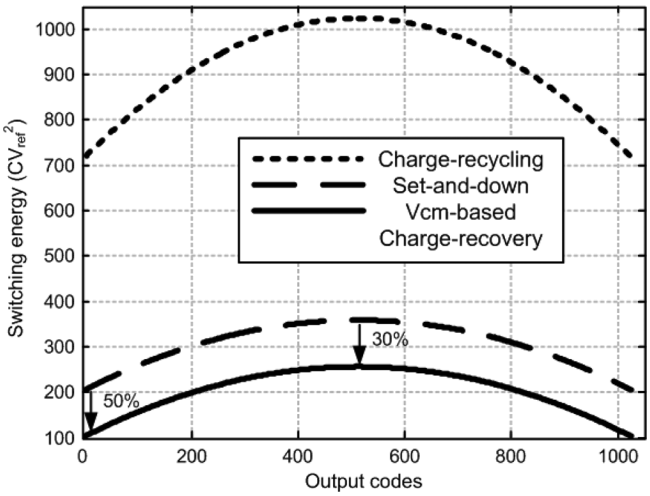

Fig. 5. Switching energy versus output code for three different techniques.

III. Circuit Design

A. Comparator Design

Fig. 6 shows the circuit schematic of the comparator with resistive loaded preamplifier and latch [24]. The comparator preamplifier has two differential pairs M1, M2 and M3, M4 connected to the outputs of the differential capacitive DAC and the additional sampling capacitor $\mathrm{C_s}$. The currents at the output of the two pairs are summed up and injected on the resistive loads, $\mathrm{R_d}$. The bias current and the load resistance yield a preamplifier gain of 27 dB.

The comparison cycling is divided into a reset phase and a regeneration phase. During the reset phase $(\mathrm{STROBE} = 0)$, the preamplifier output is shorted to avoid memory effect of the comparison. Moreover, M11–M14 reset the regenerative loop and set the outputs $\mathrm{V_{op}}$ and $\mathrm{V_{on}}$ to $\mathrm{V_{dd}}$. Since the current source transistor M15 is switched off no current flows from the supply to ground. When the regeneration phase starts $(\mathrm{STROBE} = 1)$ M15 switches on and the input transistors M5–M6 force currents flowing through the back-to-back inverters M7–M8 and M9–M10 to amplify the voltage difference to a full swing.

The devices mismatch in the comparator bias does not affect the linearity of the conversion. Since the non constant common mode voltage is rejected by the CMRR of the preamplifier, the component mismatch gives rise to an equivalent input offset, as it is the case in conventional solutions.

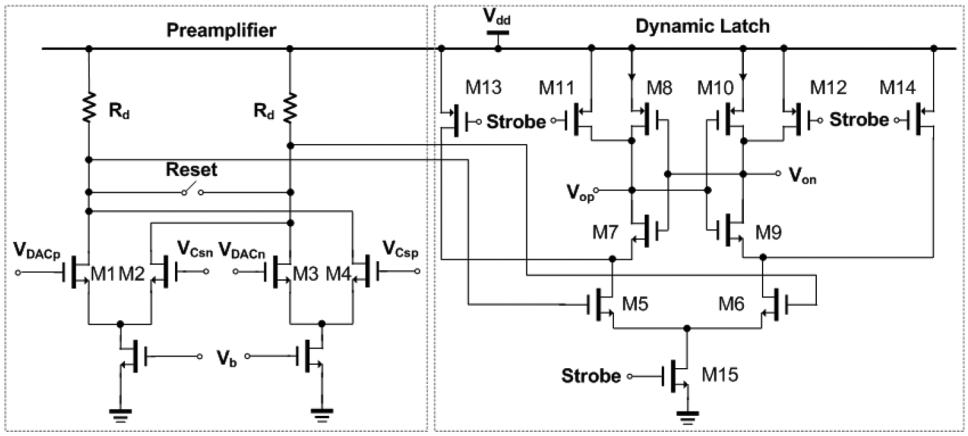

Fig. 6. Circuit schematic of the dynamic comparator.

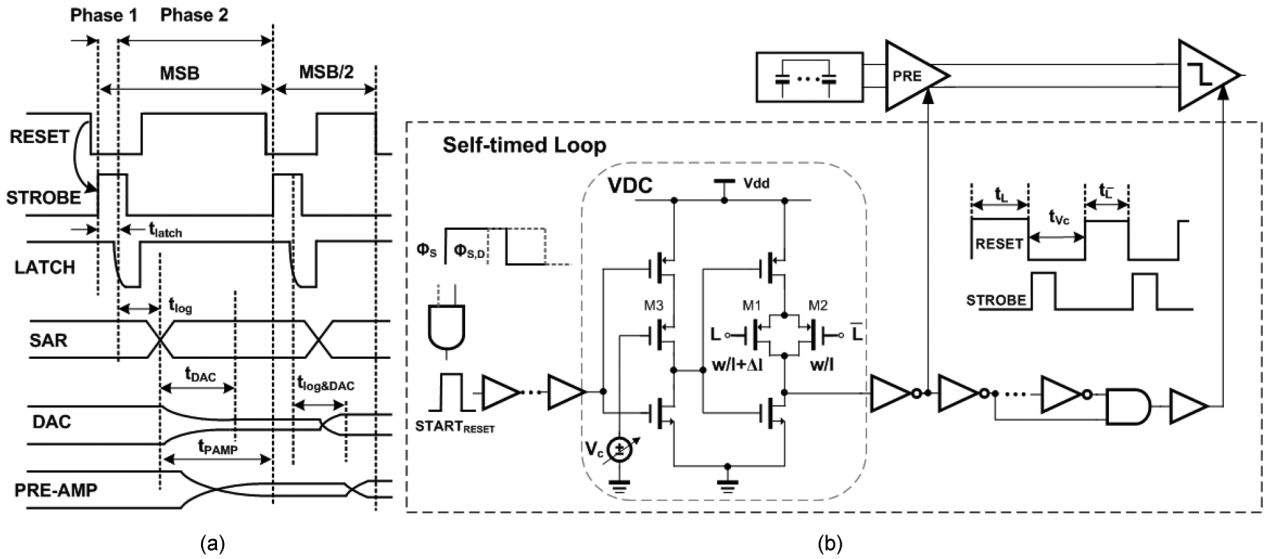

Fig. 7. (a) Timing diagram of bit-cycling. (b) Self-timed loop diagram and circuit schematic of VDC used to generate the preamplifier reset signal.

B. Variable Self-Timed Loop

The bit-cycling can be divided into two phases as shown in Fig. 7(a): phase 1 for regeneration of the latch that depends on the topology of the comparator; phase 2 for the SAR logic delay and settling for the DAC and preamplifier, which mainly depends on the DAC's structure and complexity of the logic. The asynchronous processing [16] can improve the conversion speed by synchronizing the bit-cycling with the latch's resolving time, which contributes with time saving between two adjacent strobes only when the time required by the phase 1 is significant. Furthermore, its implementation depends on the time required for phase 2 being identical and fast enough. Indeed, the ladder structure of the capacitive DAC [16] allows the bit switching of equivalent smaller capacitance instead of binary weighted capacitor array, thus insuring that the next comparison signal triggered by the previous output of the latch should start after the DAC and preamplifier are settled. However, in this design, the SA logic and DAC settling in phase 2 dominate the bit-cycling (i.e., the latch delay in phase 1 is much smaller). Since the MSBs are switched in the early bit comparisons the conversion cycle is successively reduced according to the binary-weighted capacitor array. When the asynchronous processing is applied the comparison period will be always limited by the worst case DAC settling (the MSB/2 transition in this work), which loses the advantage of asynchronous operation. Instead, the scheme uses a variable delay controller (VDC) that optimizes the pre-amplifier reset signal according to the switching sequence. As shown in Fig. 7(b), the beginning of the reset signal is synchronous with the sampling clock Φ_S and its delayed $\Phi_{S,D}$ version, and it is triggered periodically by an inverter chain in series with the VDC. The pulsewidth of the reset signal is controlled by the different sized PMOS transistors M1 and M2, which are enabled or disabled according to the gate logic. The gate voltage of M3 is controlled by an external V_c to determine the tradeoffs between the extended settling time and ADC's performance.

C. SAR Logic

For high-speed operation the SAR logic must be minimized to achieve more spare time allocation for the DAC and preampli-

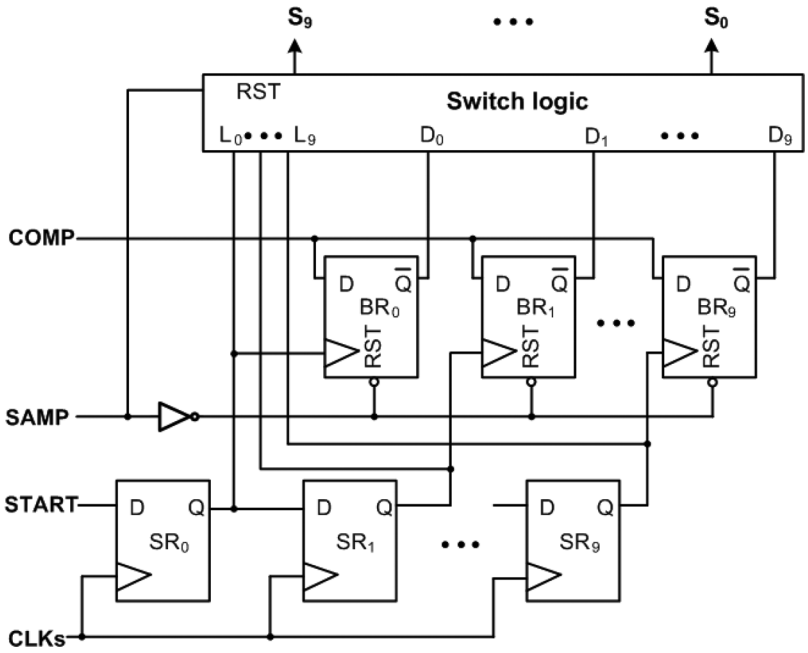

Fig. 8. Block diagram of the SAR logic.

fier settling. The SAR logic, shown in Fig. 8, consists of a set of shift registers [25] ($\mathrm{SR}_0-\mathrm{SR}_9$), bit registers [26] ($\mathrm{BR}_0-\mathrm{BR}_9$) and a switching logic block. The CLKs used to control the shift registers are synchronous with the reset of the comparator. The bit register detects each bit decision from the comparator and locks it for next stage processing. Since the circuit uses the $\mathrm{V_{cm}}$-based switching the designed switching logic block obtains the outputs S_n according to the switching sequence of Fig. 3. Both the shift registers and bit registers are implemented in full custom dynamic logic, which provides a faster and lower power consumption SAR implementation.

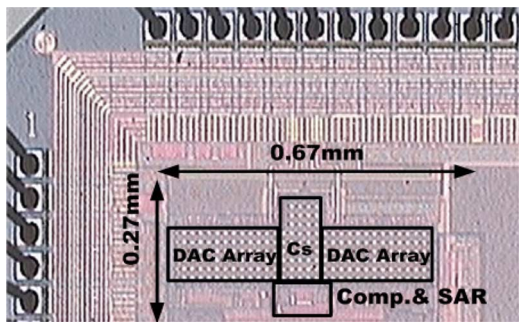

Fig. 9. Die microphotograph of the SAR ADC.

D. Technology and Layout Considerations

The 10-bit SAR implementing the $\mathrm{V_{cm}}$-based switching approach has been designed using a one-poly-nine-metal (1P9M) CMOS process with metal–insulator–metal (MIM) capacitor. The supply voltage is 1.2 V with a target conversion speed of 100 MS/s. The digital part of the SAR ADC obtains low power and fast conversion speed. Moreover, special care on the design of the layout prevents the capacitor mismatch and parasitic nonlinearity effect [23].

Since the scheme uses the supply as reference, the switching speed of the capacitor array improves because the MOS transistors that realize the switches are controlled with a maximum overdrive. The split structure of the capacitive DAC requires a low parasitic in the array's LSB internal node [23]; furthermore, it is necessary to reduce the spur interference. The layout satisfies these two requests by using of MIM capacitors and a carefully layout routing. The result limits the top-plate parasitic to about 3%. As mentioned above, there is no requirement of matching between the capacitive DAC array and the sampling capacitor $\mathrm{C_s}$. The only limitation is the kT/C limit that is very relaxed. The design uses $\mathrm{C_s} = 8\mathrm{C_U}$, where $\mathrm{C_U}$ is the unit capacitor equal to 50 fF. The split DAC leads to an architecture with 5 b MSB array and 4 b LSB array, being the total capacitance 2.75 pF.

IV. Measurement Results

The prototype ADC was fabricated and tested. Fig. 9 shows the die photograph whose total active area is 0.18 mm^2. The ADC has a full-scale input range of $1.2V_{\mathrm{pp}}$ differential, or $0.6V_{\mathrm{pp}}$ single-ended. Fig. 10 shows the dynamic performance of the ADC with input frequency swept from 1.8 MHz to Nyquist. At a sampling rate of 100 MS/s the ADC can achieve 9.1 ENOB@1.8 MHz and 8.6 ENOB@Nyquist. Fig. 11 shows the ADC output spectrum with the input frequency at 1.8 MHz and 47 MHz. The second-harmonic distortion dominates the Spurious Free Dynamic Range (SFDR): 71 dB at low frequency and near Nyquist frequency 65 dB. The mismatch between two differential paths of the ADC is likely the cause. The third-harmonic becomes significant at Nyquist and the SNDR drops by 3 dB with a loss of 0.5 b. The distortion at high

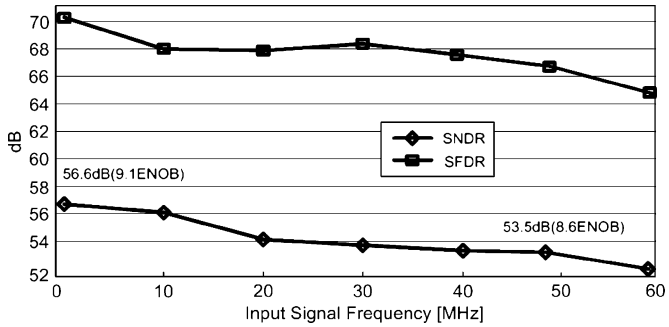

Fig. 10. Dynamic performance versus input frequency.

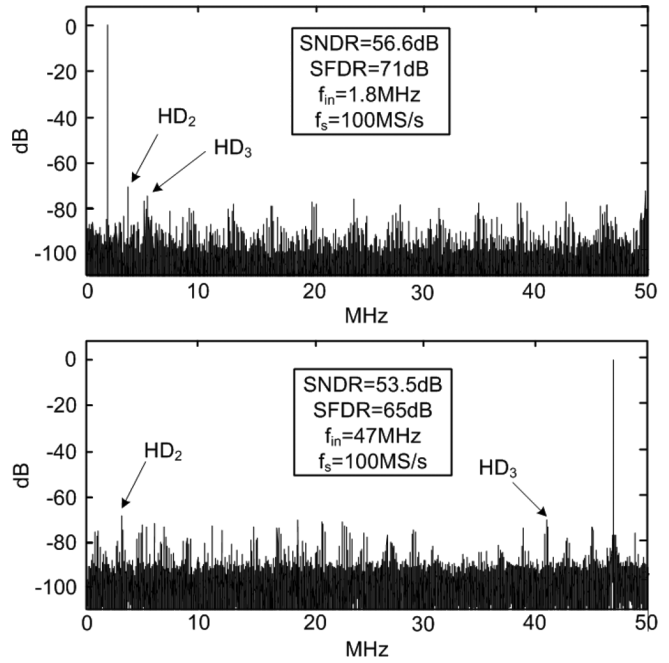

Fig. 11. FFT of the digital output. The input is either a 1.8 MHz or a 47 MHz sine wave (full-scale) sampled at 100 MS/s.

frequency increases because of a relatively high nonlinearity of the on-resistance of the sampling switches.

The DNL and INL are illustrated in Fig. 12. At 100 MS/s, the DNL and INL are $+0.79/-0.27$ LSB and $+0.86/-0.78$ LSB, respectively. Usually, the worst case DNL and INL happens in the middle (the MSB transition) in the conventional SAR ADC. The experimental measurements verify the benefit of the V_{cm}-based switching approach that imposes a lower DNL at the MSB transition. The INL is s-like and is minimized in the middle. The advantage is due to the MSB decision's independence of the capacitor mismatch as discussed in Section II-D. The worst cases DNL occur at points where the parasitic effect of the split DAC structure is more significant. The power consumption is 3 mW at 1.2 V. The analog power, including the capacitive DAC array, the comparator and the sampling network, is 1.3 mW and the digital power is 1.7 mW. Since the conventional tradeoff between conversion speed and power of the reference generator does not affect this design the digital power is a significant fraction of the total power dissipation. It is mainly drawn from the switches buffers and self-timed loop.

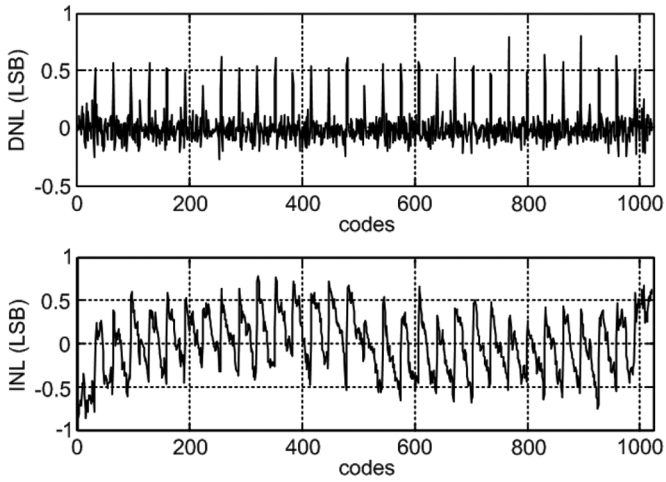

Fig. 12. Measured INL and DNL.

TABLE I
SUMMARY OF PERFORMANCE

Technology	90-nm CMOS
Resolution	10-bit
Sampling Rate	100-MS/s
Supply Voltage	1.2-V
Full Scale Analog Input	1.2-V_{PP} differential
SNDR	56.6dB
SFDR	71dB
ENOB	9.1-bit
FOM=Power/2^{ENOB}*f_s	55 fJ/conv-step
FOM=Power/2^{ENOB}*2*ERBW	77 fJ/conv-step
DNL	+0.79/-0.27LSB
INL	+0.86/-0.78LSB
Power Consumption	
Analog	1.3mW
Digital	1.7mW
Total	3mW

The measured performance of the prototype ADC is summarized in Table I. Table II compares this work with the state-of-the-art ADCs. The designs with a slightly better FoM [11], [12] are for lower speed and ENOB.

V. CONCLUSION

A 1.2 V 10-bit 100 MS/s SAR ADC has been presented. The reference-free and the power efficient V_{cm}-based switching technique enable high speed and low power SAR ADC's operation. The V_{cm}-based switching approach ensures a mismatch free MSB determination and, at the same time, saves capacitor area. The charge-recovery in each bit cycling leads to switching energy lower than both charge-recycling and set-and-down methods. The reference-free implementation and the passive multiplication by 2 avoid the use of the power-hungry resistive ladder/reference buffer without imposing a rail-to-rail input. The result is a fast *RC* settling and low power dissipation during SA conversion in the capacitive DAC array. The utilization

TABLE II
COMPARISON TO STATE-OF-THE-ART WORKS

	[9] ISSCC' 09	[27] VLSI' 08	[28] ISSCC' 08	[11] ISSCC' 08	[12] VLSI' 09	This work
Architecture	Pipelined	Pipelined	Pipelined	SAR	SAR	SAR
Technology	0.18-μm	90-nm	65-nm(with low V_t)	90-nm	0.13-μm	90-nm
Resolution	10-bit	9.4-bit	10-bit	9-bit	10-bit	10-bit
Sampling Rate	50-MS/s	50-MS/s	100-MS/s	40-MS/s	50-MS/s	100-MS/s
Supply Voltage	1.8-V	1.2-V	1.2-V	1-V	1.2-V	1.2-V
SNDR	58.2dB	49.4dB	59dB	53.3dB	52.8dB	56.6dB
ENOB	9.4-bit	7.91-bit	9.5-bit	8.6-bit	8.5-bit	9.1-bit
DNL	N/A	+0.37/-0.38LSB	+0.1/-0.1LSB	+0.7/-0.45LSB	+0.88/-1LSB	+0.79/-0.27LSB
INL	+0.7/-0.8LSB	+1.29/-0.88LSB	+0.2/-0.2LSB	+0.56/-0.65LSB	+2.2/-2.09LSB	+0.86/-0.78LSB
Power	9.9mW (P_{ref} not included)	1.44mW	4.5mW	820μW	920μW	3mW
FOM=Power/2^{ENOB}*f_s	300 fJ/step.	119 fJ/step.	62 fJ/step.	54 fJ/step.	52 fJ/step.	55 fJ/step.
FOM=Power/2^{ENOB}*2*f_{in}	337 fJ/step.	148 fJ/step.	62 fJ/step.	68 fJ/step.	64 fJ/step.	77 fJ/step.

of a variable self-timed loop minimizes the waste of time during each bit cycling and improves the conversion speed. The prototype ADC draws only 3 mW power from the 1.2 V supply and has a FoM of 77 fJ/step.

ACKNOWLEDGMENT

The authors would like to thank the Associate Editor and the anonymous reviewers for their insightful comments and suggestions.

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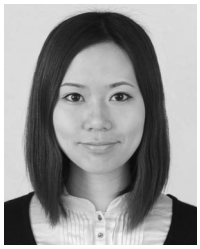

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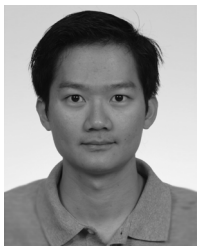

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