EDET Chipset Upgrades

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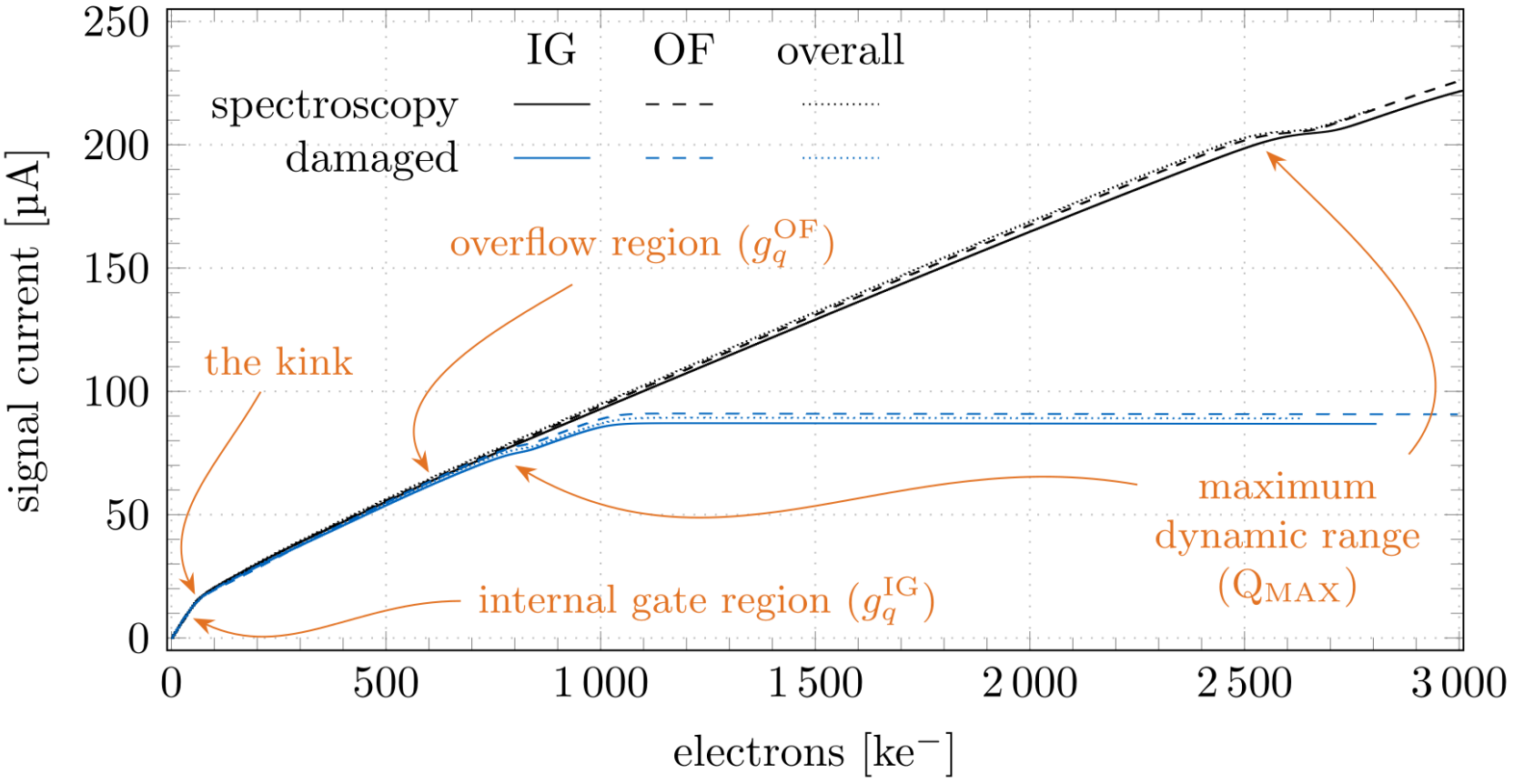
Application Basics [Epp 2016 VERTEX]

- Time resolution 10^{-3} - 10^{-6}, i.e. structural changes in biology
- $60\mu m$ pitch, $50\mu m$ thickness, signal mostly in-pixel
- 300 kEV e^- source $\rightarrow \approx$8000 e-h pairs in $50\mu m$ Si
- 100+ primaries in most pixels ($> 1000ke^-$ signal); only a couple under target

Detector Characteristics [Predikaka 2022 Thesis/NIMA]



- Transfer Gains: $g_q^{IG} = 300pA/e^-$; $g_q^{OF} = 70pA/e^-$?
- $\approx 14e^-$ ENC? [Chap 5.3] $\rightarrow$ 5 nA RMS noise @ drain?

Column Parallel ADC Specs

- P power consumption (μW)
- T_c conversion time (ns), $T_c = \frac{1}{f_s}$
- A silicon area (μm^2)
- DR dynamic range: ratio of max signal to noise floor

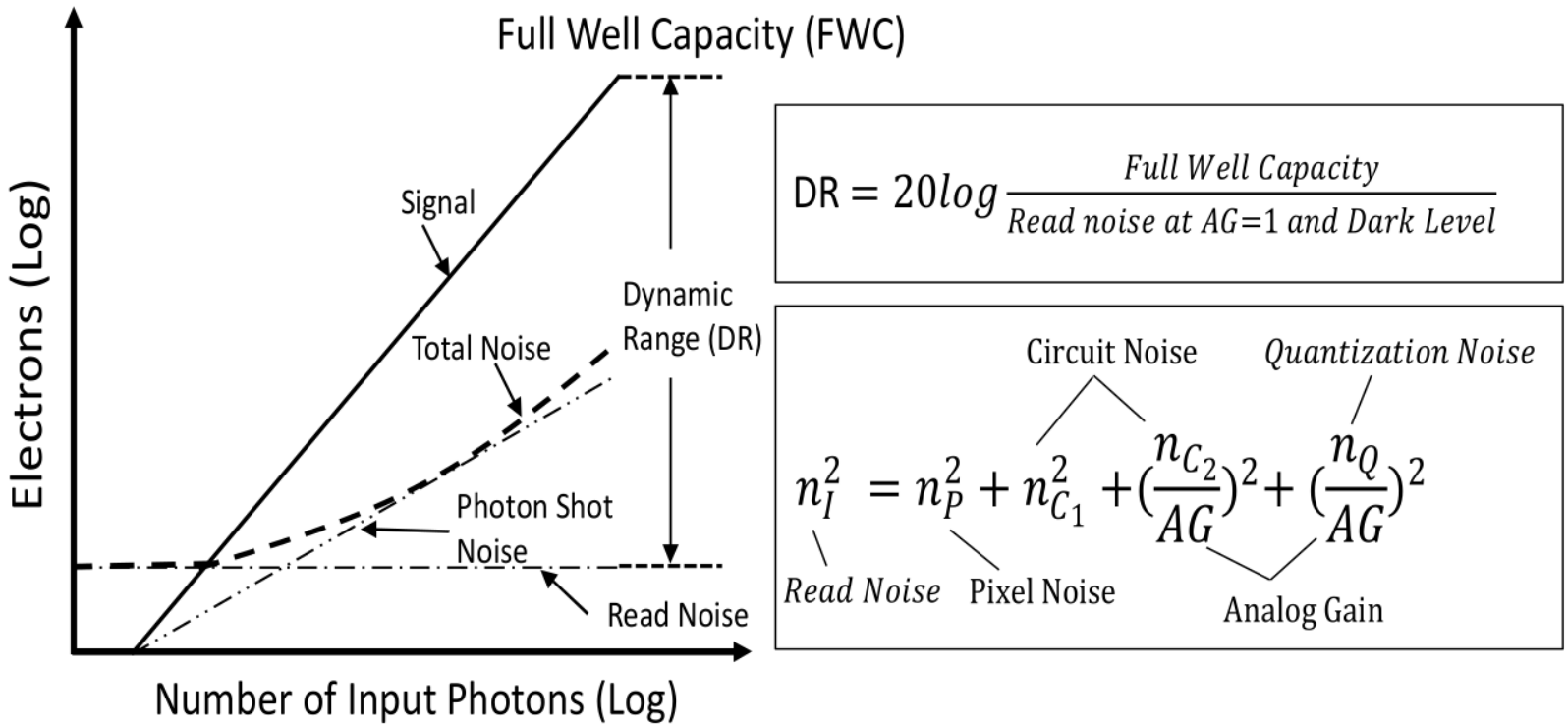


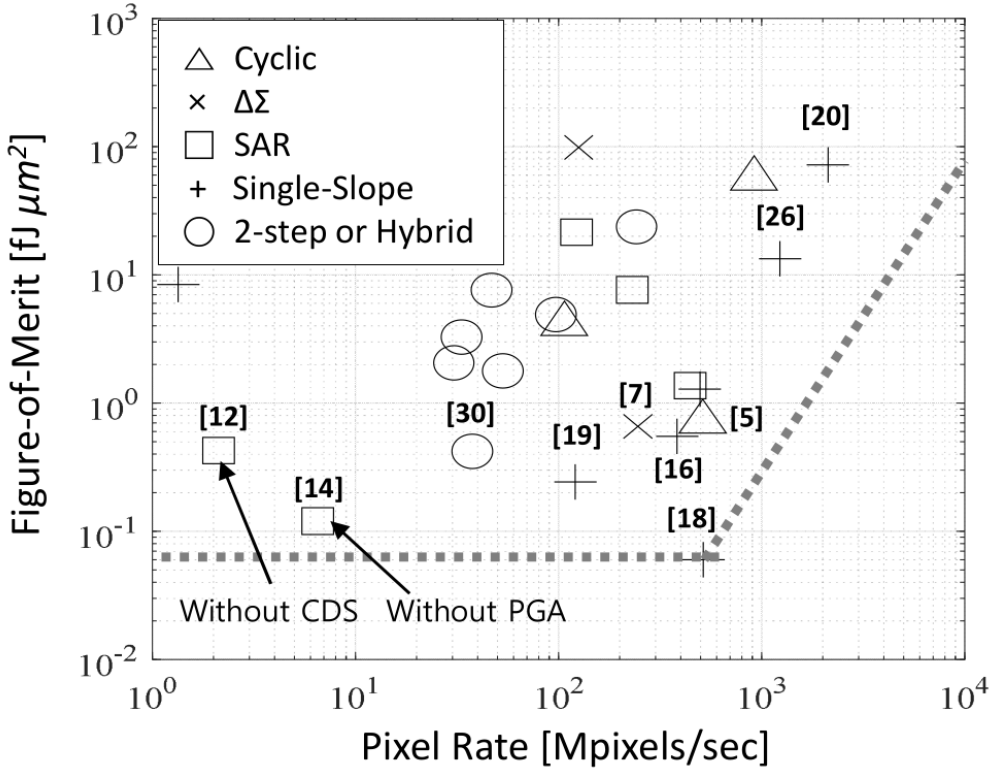
Figure: Kwon 2018 ISCAS

DCD Specs [Peric 2017]

- $P \approx 5000\mu W$ consumption per channel
- $T_c \approx 100ns$, no CDS, not fully reserved for ADC
- $A = 180\mu m \times 200\mu m = 36000\mu m^2$ silicon area
- $1000ke^-$ signal $\rightarrow \Delta 90\mu A$ [Prinker 2022 Chap 6]
- 8-bit across DR $\approx 40LSB$ for first $100ke^-$ signal, $LSB = 2500e^-$
- $\frac{LSB}{\sqrt{12}} \approx 720e^-$ quantization error (QE)
- $DR = 20\log(\frac{1000ke^-}{2500e^-}) \approx 48dB$ best case
- ADC non-linearity/skipped codes degrade this even further
- Dispersion, leakage, etc not suffciently corrected by 2-bit pedestal DAC

Column Parallel ADC Specs [Kwon 2018 ISCAS]

- $FOM = \frac{P \times T_c \times A}{10^{(\frac{DR-1.76}{10})}} \left[\frac{fJ \cdot \mu m^2}{conv.step}\right]$
- $FOM_{DCD} \approx 40000 fJ \cdot \mu m^2$
- $Rate_{DCD} = 10 Mpixels/sec$



Data Conversion Summary

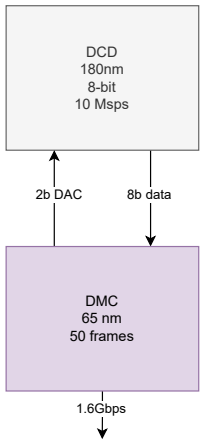
- Pixel Rate ($10 Mpixels/sec$) and Area ($36000 \mu m^2$) are typical, and sufficient for application
- Nominal resolution (8-bit) nowhere near noise limit (QE limited), but acceptable for application ($LSB = 2500 e^-$)
- Nonlinearity + offset significantly degrade beyond nominal resolution
- Power consumption of $\approx 5 mW$ seems to offer room for improvement
- Need equivalent circuit for drain current signal dynamics

Memory Buffer, PLL, Wireline PHY

- PLL frequency upgrade to 3+ Gbps
- SRAM 65nm $0.680\mu m^2$ $\rightarrow$ 28nm $0.127\mu m^2$
- SP/DP SRAM vs FIFO?
- What speeds are supported by MGT in FPGA?

Potential architectures

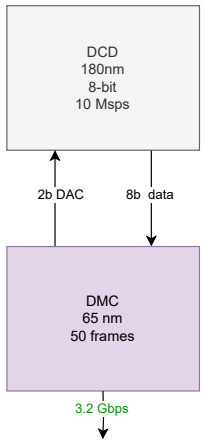
Current Architecture:



Potential Improvements?

increase frames per burst
increase measurement resolution
increase bursts per second

Config A:



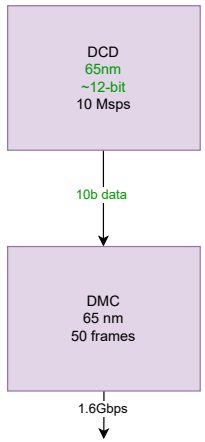
Changes:

no DCD change

no increase in frame memory

improve PLL speed
2x bursts per second
(2x less dead time)

Config B:



Changes:

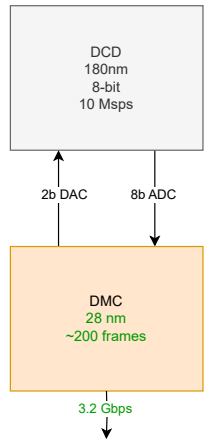
port DCD to 65nm

redesign ADC as ~12-bit
built-in pedestal DAC,
frees full 10-wide bus
10-bit ENOB measurments resolutions

potentially higher DCD power

no change in DMC

Config C:



Changes:

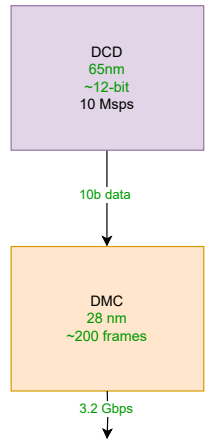
no DCD change

port DMC to 28nm

increase frame memory
4x frames per burst (200)

2x improved PLL speed, but
bursts/second will likely 0.5x
(2x longer dead time)

Config D:



Changes:

Essentially Plan B + Plan C

port DCD to 65nm

redesign ADC as ~12-bit

built-in pedestal DAC,
frees full 10-wide bus
10-bit ENOB resolutions

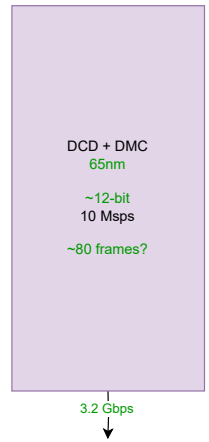
port DMC to 28nm

increase frame memory
4x frames per burst (200)

2x improved PLL speed, but
bursts/second will likely 0.5x
(2x longer dead time)

potentially increased power

Config E:



Changes:

monolithic DCD + DMC in 65nm
requires ASM balcony redesign
more total silicon area

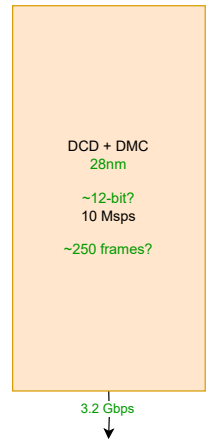
redesign ADC as ~12-bit,
similar to plan B
10-12 bit measurement resolution?

minor increase to frame memory
1.5x frames per burst (80) ?

2x improved PLL speed, but
0.5x bursts/second likely 0.5x
(2x longer dead time)

power difference?

Config F:



Changes:

monolithic DCD + DMC in 28nm
requires ASM balcony redesign
more total silicon area

redesign ADC as ~12-bit
supply may limit ADC resolution?

increase frame memory
5x frames per burst (250) ?

2x improved PLL speed, but
bursts/second likely 0.5x
(2.5x longer dead time)

power difference?