DESIGN OF HIGH-SPEED, HIGH-RESOLUTION SAR A/D CONVERTERS IN NANO-SCALE CMOS PROCESSES

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DOCTOR OF PHILOSOPHY

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Abstract

Successive approximation register (SAR) analog-to-digital converters (ADCs) are known for their outstanding power efficiency as well as good technology scaling characteristics. However, since SAR ADCs use a serial conversion algorithm, their low power advantage significantly deteriorates at high sampling frequencies (> 100 MS/s).

This research investigates the design of high-speed SAR ADCs to identify circuit techniques that improve their conversion speed while maintaining low energy operation. In addition, it explores the limitations of pipelined-SAR ADCs, which recently have demonstrated high power efficiency at conversion rates of several tens of MS/s and SNDR > 65 dB. A modified pipelined-SAR architecture is proposed, which uses two switched-capacitor digital-to-analog converters (DACs) at the ADC frontend. This technique separates the high-speed SAR operation from the low noise residue computation and improves the conversion speed to over 150 MS/s while maintaining an SNDR > 65 dB with good power efficiency.

Three prototype ICs were designed during this work. First, a test structure to extract mismatch information of small (~1fF) on-chip single-metal MOM capacitors was designed in the IBM 32 nm SOI CMOS process. Measurement results show very good matching characteristics with a matching coefficient of approximately $0.85\% \times 1fF$.

Next, an 8-bit SAR ADC was designed in a 65 nm CMOS process. This design uses 0.75 fF unit capacitors in the DAC, top-plate sampling with symmetric DAC switching, SAR loop delay optimization, and a fast comparator optimized for regeneration and reset. Measured results show an SNDR of 47.3 dB (Nyquist input)

at 450 MS/s with 6.1 mW power dissipation, which corresponds to a Walden FOM of 72 fJ/conv-step. To the best of our knowledge, this is the fastest SAR ADC using a single comparator.

Lastly, to evaluate the proposed pipelined-SAR architecture, a prototype ADC was implemented in a 65 nm CMOS process. Measured results show an SNDR of 68.3/66 dB at low frequency/Nyquist inputs, respectively with a sampling frequency of 160 MS/s, which corresponds to a Schreier FOM of 167/164.7 dB respectively. These results validate the concept of the proposed two switched-capacitor DAC pipelined-SAR architecture, and the achieved performance compares favorably with the state of the art.

Acknowledgement

Ambition, expectations or securing a good job were not the key drivers of my decision to enter graduate school. I just wanted to continue the wonderful experience I had during my undergraduate years with a little more direction and purpose. Looking back at this juncture, when I am close to graduation, I can finally say, "What a good decision that was".

The PhD journey has been very nourishing with enriching life experiences. In the past 5 years, some of the most amazing and wonderful people have touched my life in a positive fashion for which, I feel blessed and will always be indebted. Below, I sincerely acknowledge the individuals who have been instrumental during my research. Despite my best efforts, I know the list will be invariably incomplete so I offer my heart-felt gratitude to all. I have called Stanford University home for a long period and I leave it with a great sense of loss to embark upon my next journey.

My PhD advisor, Prof. Boris Murmann, has been a source of constant inspiration and his motivation, guidance and support made my progress possible. He is a visionary, a brilliant independent thinker, a caring mentor and is one of the most hardworking and dedicated person I know. I thank him for his continuous commitment towards my growth and hope to emulate the same sincerity in my character as well. As an individual, I have been most inspired by his work ethic and his love towards his subject. I express my deepest, heartfelt gratitude to Prof. Murmann for the things I have learnt and wish him well for the future.

The Murmann research group as a whole has contributed significantly towards this thesis. The healthy environment and an inclination to help each other helped me in more ways than I could have imagined. I learned much from the interactions with senior students and hopefully have passed on some of that knowledge to the younger students, who taught me loads well. Friendly discussions with peers regularly brought a fresh perspective. This played a major role in streamlining my thought process and helped develop new ideas. Members of the Murmann group have been coworkers, friends, and companions and I have always been proud to be a part of this research group.

I want to give special thanks to Alex Guo, my colleague and office mate, for the numerous invaluable discussions (both technical and otherwise) we had together. It was a comforting feeling that I can run any crazy idea with him and expect a patient, measured and intelligent response. We joined Murmann group practically at the same time, and now, when we coincidentally graduate almost together, I wish him luck in all his future endeavors.

My parents have encouraged and supported me throughout my life, especially during graduate education. They have always taken great pains to ensure that I get the best in life and I thank them for their unconditional love and continuous selfless commitment towards my welfare.

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I thank the faculty and staff of Stanford University for their role in my education and research. Ann Guerra, the ‘Angel’ of Murmann group deserves a special mention for her amazing support over the years. She went out of her way many times to help me. Thank you, Ann.

I thank all of my friends; whose contributions towards this thesis cannot be described using words and neither do I have enough pages in this dissertation to

mention all of them. In my time away from home at Stanford, they were my bedrock and helped me have a wonderful life outside research, which allowed me to relax and return fresh, especially when I was pressured by heavy work load. Although, many friends may have grown apart either due to distance or different career goals, they infused a sense of meaning to life and provided the much needed work-life balance.

I thank Mother Nature for letting me discover my love for the outdoors during the course of my PhD. The experiences I had while hiking in the hills behind Stanford, or in Yosemite National Park or in the wildernesses of Sierra Nevada have shaped my thoughts like no other. I was really lucky to be admitted to Stanford as a graduate student because in addition to the excellent academic environment and diversity, its proximity to some of the world's finest mountains and coasts has augmented my graduate life experience in ways, which I will slowly comprehend only in years to come.

Finally, I bow my head in front of the Almighty, who gave me this blessed life and has always been so kind to me. In HIS words from the 'Bhagvad Geeta', the path of education and knowledge leads to salvation and may I remain sincere and truthful in my steps during the journey forward. I will conclude with a Sanskrit hymn (below) from the 'Brhadaranyaka Upanisad'. Its English translation is, "from the unreal lead me to the real, from the darkness lead me to the light, from the dead lead me to the immortal".

“asato mā sad gamaya

tamaso mā jyotir gamaya

mṛtyor mā amṛtaṁ gamaya”

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List of Abbreviations

A/D – Analog Digital

ADC – Analog-to-Digital Converter

BW – Bandwidth

f_s – Sampling Frequency

ENOB – Effective Number of Bits

DAC – Digital-to-Analog Converter

CDAC – Capacitive DAC

SAR – Successive Approximation Register

SNDR – Signal-to-Noise + Distortion Ratio

SNR – Signal-to-Noise Ratio

THD – Total Harmonic Distortion

FOM_W – Walden Figure-of-Merit

FOM_S – Schreier Figure-of-Merit

I/O – Input-Output

FFT – Fast Fourier Transform

MOS – Metal-Oxide-Semiconductor

CMOS – Complementary MOS

SoC – System-on-Chip

MOM – Metal-Oxide-Metal

Chapter 1

Introduction

1.1. Motivation

Modern communication systems employ complex systems-on-chip (SoCs) to perform a multitude of operations. Analog-to-digital (A/D) converters are an integral part of such a communication signal chain. Integration of the ADC with the digital backend is usually desirable, since then a single digital CMOS die can be used to implement the entire signal processing chain. This puts the onus on circuit designers to realize the required A/D converters in advanced CMOS processes, making them suitable for SoC integration.

Recently, SAR ADCs have attracted substantial research interest, thanks to their good power efficiency and technology scaling properties. However, the power efficiency of a SAR ADC, which uses a serial conversion algorithm, deteriorates at high conversion speeds (> 100 MS/s) as the constituent blocks are pushed against the process technology limit. This work investigates the design of high-speed SAR ADCs to identify circuit techniques that improve their conversion speed while maintaining low power dissipation. Moreover, it proposes a modified pipelined-SAR architecture, which uses two switched-capacitor DACs in the frontend. This allows SAR ADCs to penetrate into the design space that is more commonly occupied by conventional multi-stage pipeline ADCs (~12-bit resolution, sampling frequency >100 MS/s) with significantly better power efficiency.

1.2. Successive Approximation Register A/D Converter

A. Basic Operation

As the name suggests, SAR ADCs convert an analog input to its digital equivalent by a series of successive approximation steps, usually using a binary search algorithm. A simple block diagram representing this process is shown in Fig. 1.1. The DAC output voltage is compared to the input signal and the result of this comparison is fed back to the DAC, thereby closing the successive approximation loop. The control logic is designed to perform a feedback subtraction and brings the DAC voltage closer to the analog input with every comparison (see Fig. 1.1). As a result, the converter's resolution depends on the number of successive approximation cycles (serial operation). In addition, the resolution is primarily limited by the sensitivity of the comparison block and the accuracy of the D/A converter.

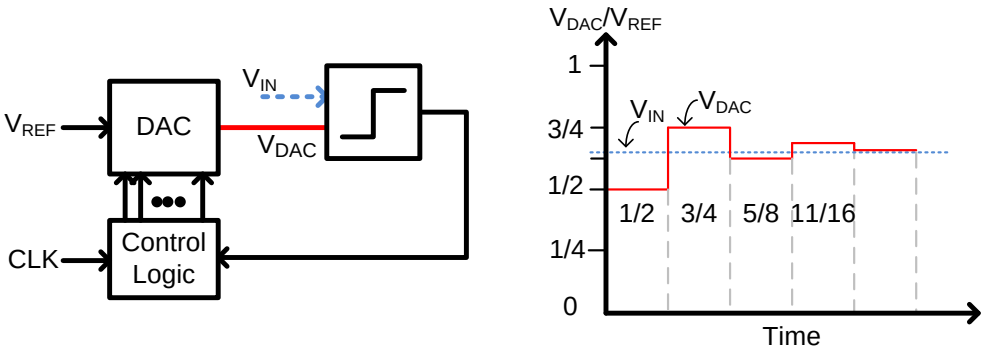


Fig. 1.1 Basic SAR ADC block diagram and operation.

B. Historical Perspective

The first commercial ADC design is described in the work of [1], which was an 11-bit, 20 kS/s vacuum tube based SAR ADC designed at EPSCO (now Analogic corporation [2]). This ADC weighed 150 lbs, consumed 500 W of power and sold for approximately $ 8000. The same author also explained the details of logic block required to implement the successive approximation algorithm in [3].Conceptually,

the idea of a successive-approximation based A/D converter was independently proposed a few years earlier to [1], in the works of [4], [5], [6] and [7].

C. MOS Implementation

Fig. 1.2 shows the circuit schematic of the first MOS implementation of a SAR ADC [8]. It employs a binary weighted, switched-capacitor D/A converter (CDAC) to perform the feedback subtraction. The ADC operation is described in Fig. 1.3 and 1.4 (3-bit single ended example for simplicity). During the sampling phase (Fig. 1.3), one end of all the capacitors in the CDAC is tied to analog input V_{in}, and the comparator's input are tied to a common mode voltage (V_{CM}). At the end of sampling, the input and common mode are disconnected and the sampled input is held on the CDAC. This is followed by a bit-test operation: the MSB capacitance is connected to reference voltage V_{REF}, while the other capacitors are tied to ground (or V_{REFN} in a fully differential implementation). In case the subsequent comparator decision is logic high (MSB = 1), the next largest capacitance is connected to V_{REF} and the above operation is repeated. Instead, if the comparator decision was logic low (MSB = 0), first the MSB capacitor is switched from V_{REF} to ground, then the next largest capacitor is tied to V_{REF}. This process continues until all the bits are resolved. These bits are usually stored in a flip-flop and read out during the next sampling phase.

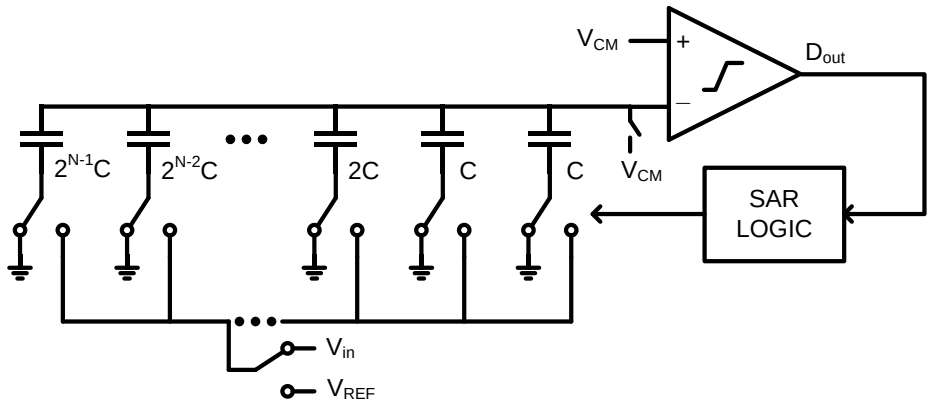


Fig. 1.2 Block diagram of a SAR ADC using a binary weighted switched-capacitor DAC.

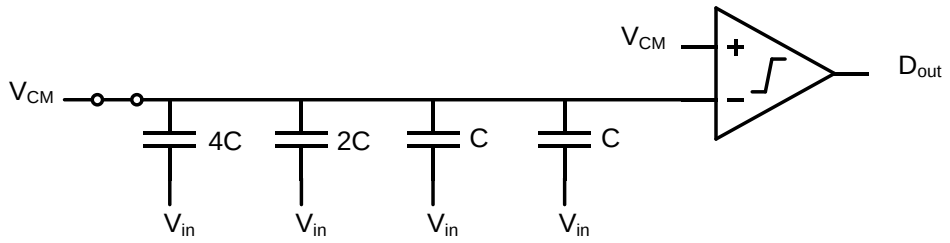


Fig. 1.3 SAR ADC during sampling.

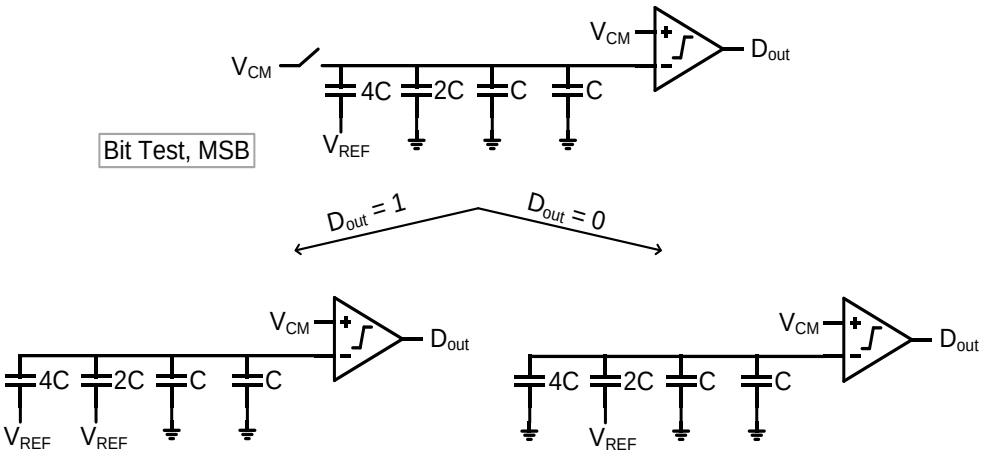


Fig. 1.4 SAR ADC conversion phase showing bit test operation.

D. Why SAR ADCs?

After the first published MOS implementation [8], commercial single-channel SAR ADCs typically were slow, accurate (16-bit) converters (e.g. [9]). Research interest in SAR A/D converters was initiated once again by the work of [10], which interleaved eight, 6-bit SAR ADCs to demonstrate a 10 mW, 600 MS/s A/D converter. Since then, the number of publications on SAR ADCs at the International Solid-State Circuits Conference (ISSCC) and the VLSI Circuit Symposium have steadily grown (see Fig. 1.5). This increase in research activity has led to significant improvements in SAR ADC performance, which is depicted by ploting the trend in their conversion speed (single-channel) over the last 7 years (see Fig. 1.6). This observed boost in performance stems from the inherent digital-like architecture of a SAR ADC, which scales well with process and achieves very good energy efficiency. Specifically, a conventional SAR ADC (Fig. 1.4) comprises of a comparator, MOS switches, digital logic and capacitors, all of which benefit from process

scaling. For example, smaller channel length result in improved MOS switches as well as comparator speed. It also reduces the digital gate delay, thereby speeding up the SAR logic. Moreover, improvements in lithography with every CMOS generation have made it possible to realize small on-chip capacitors with good matching characteristics, which are used to implement the CDAC in a SAR ADC (see Chapter 2). A brief summary of recent circuit innovations in SAR ADCs is presented in the next section.

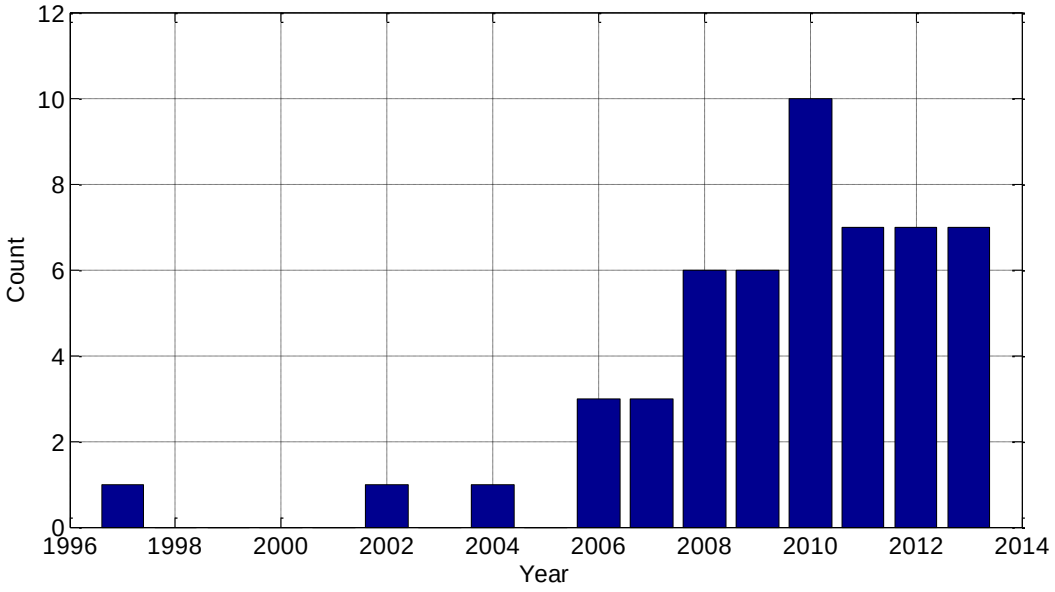


Fig. 1.5 Recent publication trend of SAR ADCs in ISSCC and VLSI Symposium.

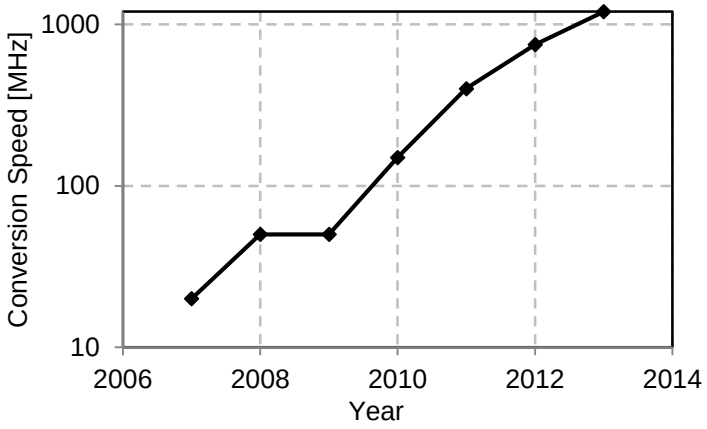


Fig. 1.6 SAR ADC conversion speed trend (only single-channel ADCs).

1.3. Recent Advancements in SAR ADCs

Fig. 1.7 shows a plot of Walden figure-of-merit ($FOM_W = P/(2^{ENOB} \times f_s)$) vs. conversion speed for SAR ADCs using the data collected in [11]. It is evident that recent designs cover a wide performance spectrum (conversion speeds from sub-MS/s to several GS/s) and achieve very good power-efficiency at low to moderate conversion speeds (< 100 MS/s). This can be attributed to the recent advancements in SAR ADCs, which are described below.

First, the improvement in photolithography has resulted in fine line CMOS processes with 8-10 metal layers. The width and spacing of these metal layers is accurately controlled (lateral dimension), which is exploited to realize small lateral-field metal-oxide-metal (MOM) capacitors[1]. The capacitive DAC in a SAR ADC uses these capacitors as unit elements to scale down the total capacitance, thereby improving both speed and power dissipation (see e.g. [12]).

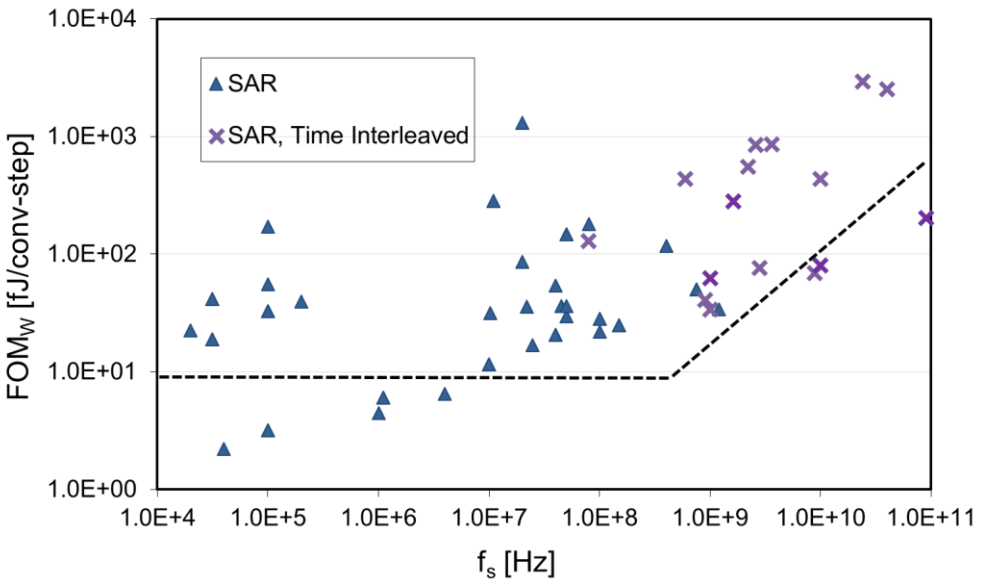


Fig. 1.7 FOM_W vs. conversion speed showing SAR ADC performance space.

Second, there has been a significant amount of research on reducing the CDAC's switching energy. Capacitance splitting [13], monotonic switching [14],

[1] A detailed discussion on matching properties of such capacitors is presented in Chapter 2.

merged capacitor switching [15] and aligned switching [16] are some of the energy-efficient switching schemes proposed in recent years. In these techniques, switching energy is saved by either making the switching symmetric across the DAC transition codes (37 % savings) [13], eliminating the MSB capacitance switching (81 % savings) [14], using a common-mode voltage halfway between the DAC references (87.5 % savings) [15], or using a separate coarse-ADC to calculate the MSBs [16]. Use of energy efficient switching together with small unit DAC capacitance significantly reduce the DAC switching energy, which reduces the overall ADC power dissipation and improves its power efficiency. For example, the work of [16] achieves a state-of-the-art FOM_W of 0.85 fJ/conv-step.

Third, the use of asynchronous SAR logic [17] as well as incomplete DAC settling together with redundancy [18] significantly improve ADC conversion speed[2]. Time-interleaved SAR ADCs, which combine several SAR ADC slices have demonstrated very high conversion speeds with good power efficiency [19]. Furthermore, massive time interleaving using hierarchical track-hold circuits was proposed in the work of [20], which achieved a Nyquist SNDR of 48.5 dB at 2.6 GS/s.

Lastly, a two-stage pipelined-SAR architecture employing two moderate resolution SAR ADCs was proposed to achieve 12-bits at 50 MS/s [21]. The key idea is to use a relatively high-resolution frontend (~6 bits), which simplifies the design of the residue amplifier (see Chapter 3 for a detailed discussion). More recent work on pipelined-SAR A/D conversion has demonstrated high power efficiency at conversion rates of several tens of MS/s and SNDR > 65 dB [22]. Moving forward, it is desirable to extend the speed of this architecture so that it can compete with traditional multi-stage pipelined ADCs, which still dominate the application space requiring f_s > 150 MHz and similar SNDR. The works of [23] and [24] take steps in this direction by time-interleaving two 125/205 MS/s pipelined SAR ADCs. However, in both of these designs, the SNDR at Nyquist input frequency is limited to 56 dB.

[2] A detailed discussion on high-speed SAR ADC design techniques is presented in Chapter 3.

The final goal of this research was to explore circuit techniques that extend the performance of SAR based A/D converters to conversion speed of > 150 MS/s with an SNDR of over 65 dB, while maintaining a small full-scale range and power dissipation to make it suitable for SoC deployment. Fig. 1.8 shows our targeted ADC design space.

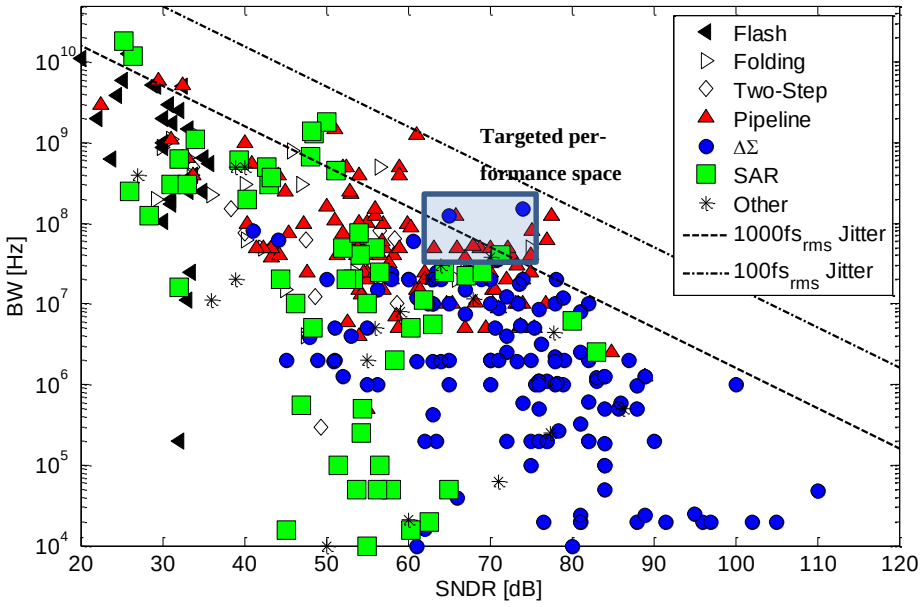


Fig. 1.8 Plot of ADC bandwidth vs. SNDR [11] showing targeted design space in this research.

1.4. Organization

The remainder of this thesis is organized as follows. Chapter 2 presents a mismatch study of small, on-chip MOM capacitors realized using a single metal layer. Chapter 3 explains various high-speed SAR ADC design techniques and introduces the pipelined-SAR architecture along with its drawbacks. It also presents a modified pipelined-SAR architecture that uses two switched-capacitor DACs in the ADC frontend. Chapter 4 demonstrates an 8-bit, 450 MS/s, single-channel, 1-bit/cycle SAR ADC prototype in 65 nm CMOS including a description of important circuit blocks and measurement results. Chapter 5 describes the design and measurements of a 160 MS/s, 68.3 dB SNDR prototype ADC in a 65 nm CMOS process

that serves as a proof-of-concept of the two-CDAC pipelined-SAR architecture. Finally, Chapter 6 summarizes this work.

Chapter 2

Mismatch Characterization of Small MOM capacitors

2.1. Introduction

The effect of process scaling on SAR A/D converters, considered in Chapter 1, underlines the importance of small unit capacitors. In a modern CMOS process with aggressively scaled feature sizes, it is possible to realize very small, yet well-matched metal-oxide-metal (MOM) fringe capacitors using the interconnect layers. One of the main applications for such capacitors is in the capacitive D/A sub-converter of SAR ADCs [8]. In order to minimize the switching energy, unit capacitors as small as 0.5 fF are now being used routinely [12], [25] while the most aggressive designs employ values as small as 50 aF [26]. In addition to SAR ADCs, small MOM capacitors (~10 aF) find their use in the capacitor bank of digitally controlled oscillators (DCO) [27].

This chapter presents a systematic study of the mismatch characteristics of small on-chip capacitors, realized using a single metal layer [28], [29] and is structured as follows. Section 2.2 discusses the properties of the single-layer MOM capacitors considered in this work. Next, we review prior-art methods for capacitor mismatch measurements using custom test structures in Section 2.3. Sections 2.4

and 2.5 describe the proposed characterization technique along with its circuit realization and a discussion of error sources. This is followed by measurement results in Section 2.6, and conclusions are drawn in Section 2.7.

2.2. Single layer MOM capacitors

A. Basic Structure

Single layer MOM capacitors take advantage of the sophisticated lithography of a modern CMOS process: their capacitance is mostly defined by lateral fields, and the matching is primarily dependent on lithography, rather than oxide film thickness. Designers, therefore tend to favor this topology over its alternatives that involve vertical fields between multiple metal layers. Fig. 2.1 shows such a structure that is sized and laid out as in today's typical SAR ADC designs [12], [25]. The area penalty due to the relatively low capacitance density is usually acceptable in moderate resolution A/D converters, which tend to require a total capacitance on the order of only 100 fF. Table 2.1 presents the dimensions of 0.45 fF and 1.2 fF capacitors implemented via the structure of Fig. 2.1.

Since, the fringe capacitance between the metal fingers sets the capacitance of the structures in Fig. 2.1, it scales with the dimension perpendicular to the lateral field. Consequently, when the length L of such a capacitance is scaled by λ (while keeping all other dimensions the same), its capacitance also scales approximately by λ. In this research, the effect of changing the finger spacing, S was not considered.

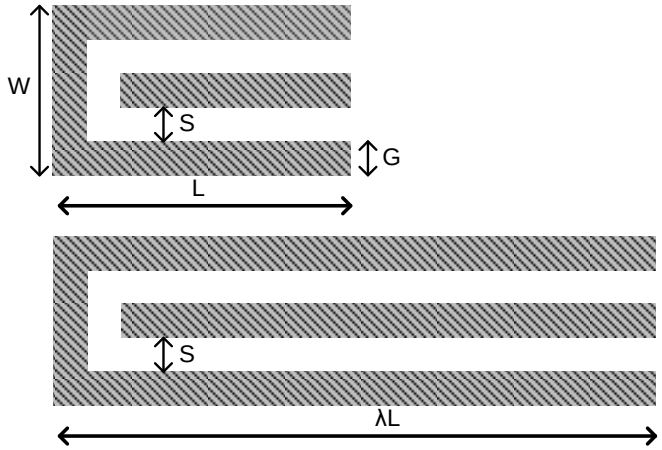


Fig. 2.1 Single-layer lateral field capacitors considered in this research.

Table 2.1: Unit capacitor dimensions

Dimensions	0.45 fF	1.2 fF
W (μm)	0.65	0.65
L (μm)	3.6	9.5
S (μm)	0.13	0.13
G (μm)	0.13	0.13

B. Modeling

Consider a unary array of N single-layer, lateral field capacitors tiled adjacent to each other as shown in Fig. 2.2. We model each of the unit capacitors in this array as a Gaussian random variable with mean C_u and standard deviation σ_u. Due to the very small dimensions and proximity of the unit elements (see Table 2.1), we also consider correlation through a nearest neighbor model. Each unit element is assumed to have finite correlation (depicted by covariance σ_{ab}^2) with its nearest neighbors and is independent of the rest. As a result, the assumed covariance matrix (Σ) is tri-diagonal and given by

$$\Sigma = \begin{bmatrix} \sigma_u^2 & \sigma_{ab}^2 & 0 & 0 & \cdots \\ \sigma_{ab}^2 & \sigma_u^2 & \sigma_{ab}^2 & 0 & \cdots \\ 0 & \sigma_{ab}^2 & \sigma_u^2 & \sigma_{ab}^2 & \ddots \\ 0 & 0 & \sigma_{ab}^2 & \sigma_u^2 & \ddots \\ \vdots & \vdots & \ddots & \ddots & \ddots \end{bmatrix} \tag{2.1}$$

The quantity of interest here is the relative unit element mismatch $c_v = {\sigma_u}/{C_u}$ (also referred to as the coefficient of variation), which enumerates the matching accuracy between two unit capacitors.

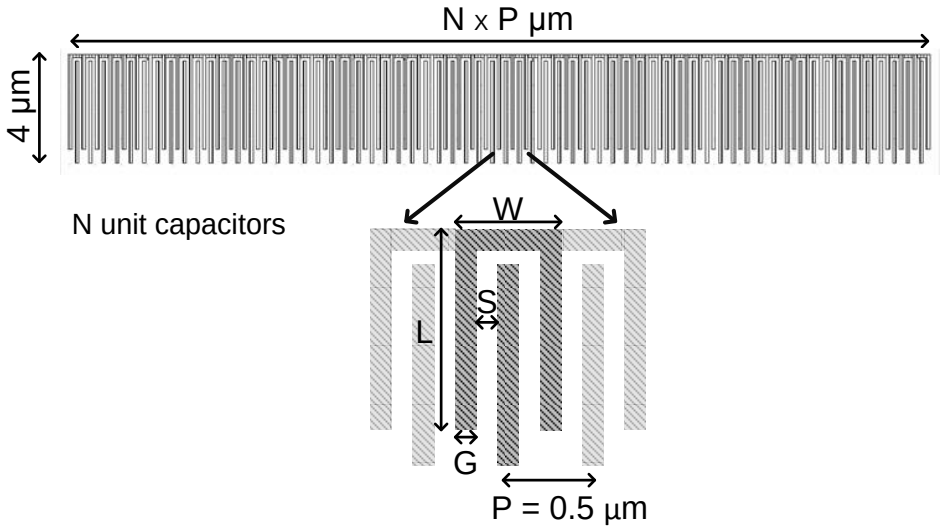


Fig. 2.2 Layout of the unary capacitive array.

2.3. Prior Art Mismatch Measurement Techniques

While the matching properties of integrated capacitors have been studied previously, most of the available measurement data is for relative large capacitors on the order of 1 pF [30], [31], [32], [33] and designers tend to estimate the mismatch of smaller capacitors indirectly, from the measurements of larger circuit blocks. For example, the work of [34] uses even order harmonics in a DCO's tuning characteristic to infer the mismatch among small MOS tuning bank varactors. Similarly, the work of [35] uses static linearity measurements of a 10-bit SAR ADC to estimate the capacitance mismatch for MOM capacitors as small as 2 fF. Such indirect methods have several disadvantages. First, the circuits tend to be large, which makes it

difficult to obtain sufficient statistics with a limited number of parts or chip area. Second, extracting the desired information needs relatively sophisticated measurement setups. Consequently, there has been some prior work to devise dedicated test structures in order to extract capacitance mismatch information.

Most of the published works on dedicated test structures translate the capacitance mismatch information into another domain where it is easier to measure. This is because the presence of pad capacitances and the limited resolution of bench top measurement equipment make the direct probe-based measurement of small capacitances impractical. Prior art techniques can be broadly divided into two categories: (a) voltage-based measurements and (b) frequency-based measurements.

A. Voltage-Based Measurement

Fig. 2.3 shows an example of a voltage-based technique. A voltage ramp is applied at node A when B is grounded (and vice-versa), so that the mismatch information is contained in the difference of the output slopes for the two cases (S_1 and S_2) [36], [37]. This technique is plagued by the analog nature of the measurement, and the experimental data will typically be impaired by a variety of noise sources and noise coupling mechanisms.

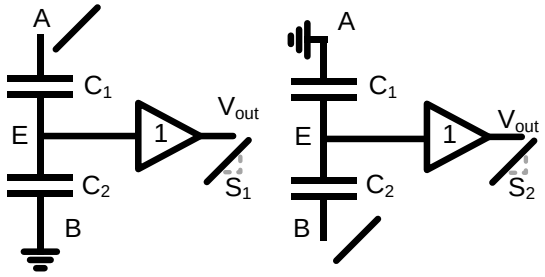


Fig. 2.3 Voltage-based mismatch measurement.

B. Frequency-Based Measurement

Reference [38] identified the shortcomings of voltage-based measurements and proposed a mismatch characterization method based on frequency. The key idea is to translate the relative mismatch between two capacitors to a relative change in frequency of oscillation. Fig. 2.4 shows the circuit that was used to characterize mismatch of capacitance values down to 8 fF. While this approach is substantially more robust and provides a "quasi-digital" readout, it requires undesired de-embedding of circuit parameters that lead to measurement uncertainty. First, it needs reliable simulation data to account for the loading effects of large resistances that are added to the amplifiers in the ring oscillator (Fig. 2.4) to suppress switch mismatch. Second, this simulation data must be combined with measurements from an unloaded replica of the structure to scale the observed values.

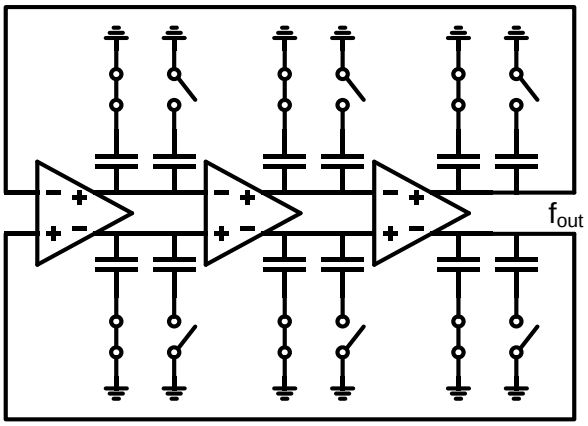


Fig. 2.4 Ring oscillator for frequency-based mismatch measurement.

2.4. Proposed Mismatch Measurement Technique

A. Capacitance Switching Scheme

We use a switching scheme to distinguish random mismatch from variations that are common to neighboring unit elements. The capacitors in the unary capacitive array (see Fig. 2.2) are switched to generate a mismatch-proportional error voltage as shown in Fig. 2.5. First, the top plate (node T) is connected to V_{REF} while

the bottom plates are connected to V_{REF} or GND alternately, in groups of two (pre-charge). Then, the top plate switch is turned off and the bottom plate connections are reversed (redistribution). In presence of capacitive mismatch, this generates an error voltage V_Δ, which is

$$V_\Delta = V_{REF}\frac{\sum_{i=1,2,5,6\ldots} C_i - \sum_{j=3,4,7,8,\ldots} C_j}{\sum_{k=1}^{N} C_k} = V_{REF}\frac{X}{Y} \tag{2.2}$$

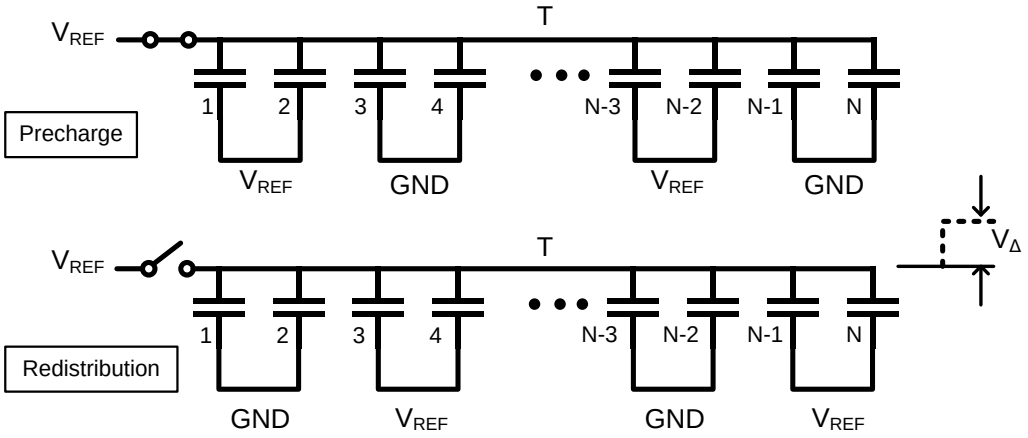


Fig. 2.5 Capacitance switching scheme.

For N unit elements in the unary array, with the above-assumed covariance matrix, the mean and variance of V_Δ (see Appendix A.1) are

$$E(V_\Delta) = -\frac{V_{REF}}{[E(Y)]^2}Cov(X,Y) \tag{2.3}$$

$$Var(V_\Delta) = \frac{V_{REF}^2}{N}\left[\left(\frac{\sigma_u}{C_u}\right)^2 + \frac{2}{N}\left(\frac{\sigma_{ab}}{C_u}\right)^2\right] \tag{2.4}$$

From (2.3), we can see that the mean of the error voltage will be negative in presence of finite neighbor correlations (confirmed later by measurement results in Section 2.6). More importantly, it is clear from (2.4) that for large N, the described

switching scheme suppresses the effect of finite nearest neighbor correlation and allows us to infer the coefficient of variation (σ_u/C_u) from the variance of V_Δ[3].

B. Error Voltage Measurement

The preceding section describes a means of deducing the coefficient of variation from the variance of the error voltage V_Δ. This leads to two logical questions:

1) How to accurately measure V_Δ?
2) What value of N (the number of capacitors in the unary array) will suffice to suppress the effect of nearest neighbor correlations?

We address the first question by opting for a digitized readout of the error voltage, which alleviates the issues associated with analog voltage measurements (see Section 2.3). This is accomplished by A/D converting the error voltage with sufficient resolution to replace $V_\Delta$by its digital approximation in (2.4). The coefficient of variation is now given by

$$c_v = \frac{\sigma_u}{C_u} \approx \sqrt{N}\frac{V_\Delta}{V_{REF}} Stdev(\mathrm{D}\{V_\Delta\}) \tag{2.5}$$

To answer the second question, we perform Monte Carlo simulations in MATLAB. These simulations assume the capacitance model given in (2.1), with a mean capacitor value of 1 fF and a relative mismatch standard deviation of 1%. The nearest neighbor covariance is assumed to be one fourth of the variance. The error voltage was generated (in MATLAB) as per the switching scheme described above with V_{REF} set to 1 V (see (2.2)) and the variance of the error voltage V_Δ was calculated from 100,000 Monte Carlo runs. Fig. 2.6 shows the simulated variance versus the dual log of the number of elements in the unary capacitive array. This is compared with a variance estimate of V_Δ calculated assuming an i.i.d. model for the capacitors (no correlation). It is evident that for more than 2^5 = 32 unit capacitors

[3] Appendix A.2 describes a switching scheme that can be used to also infer the nearest neighbor correlation once σ_u/C_u is known.

in the array (Fig. 2.2), the error due to the covariance term in (2.4) becomes negligible. This simulation result also verifies the efficacy of the switching sequence described above.

The next step is to perform a sweep over the resolution of the A/D conversion and compare the simulated variance with the variance of the digital representation of V_Δ. This is shown in Fig. 2.7, which indicates that 6-bit resolution suffices for our purpose.

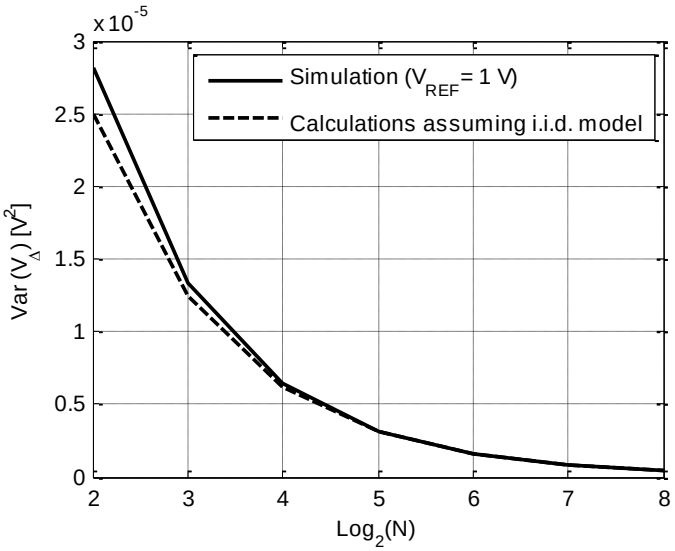


Fig. 2.6 Variance of error voltage (V_Δ) vs. $\log_2 N$, where N is number of unit elements in the unary capacitive array.

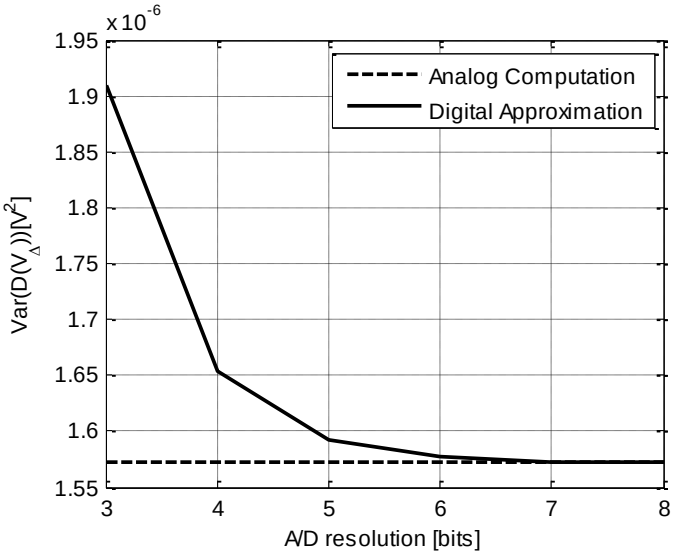


Fig. 2.7 Variance of the digital representation of V_Δ vs. feedback DAC resolution (solid line). The computed variance of V_Δ (dashed line) is also shown for comparison.

C. Test Structure

As mentioned previously, the proposed test structure is designed to realize a fully digital readout of mismatch data without requiring extensive (manual) measurement calibration. This is accomplished by using a SAR ADC-like test structure that utilizes the switching scheme presented in Section 2.4 (A) to generate an error voltage proportional to capacitance mismatch and then translates it into a digital bit stream.

Fig. 2.8 shows a schematic of the test structure. The structure resembles a SAR ADC, except that the converter takes no input and the capacitor array is unary and comprises of 64 same-size capacitors. This capacitor array is identical to that of Fig. 2.2 with the addition of 32 dummy elements on either side to reduce potential systematic errors due to metal density fluctuations[4]. Moreover, with the exception of V_{REF} and $V_{ref,dac}$, all I/Os of the circuit are digital.

The clock signal ϕ_1 is exercised only in the positive-half circuit generating an error voltage (as explained further below), which is then digitized via DAC2A, B, forming a successive approximation loop around the comparator. The SAR A/D conversion is differential for robustness and this is realized by using a replica unary array of 64 unit capacitors in the negative-half circuit, as shown in Fig. 2.8. The array size and the 6-bit resolution of DAC2A, B were chosen as per the MATLAB simulation results of Section 2.4 (B).

DAC1 and DAC2A, B are implemented as thermometer coded resistive DACs, which are inherently monotonic and have good differential nonlinearity [39]. The circuit operates at a relatively low speed (f_{CLK} ~5 MHz), which makes the design of the comparator, clock generation and SAR logic non-critical and fairly straightforward. Yet, this operating speed ensures short enough clock cycles to alleviate any issue due to leakage currents.

[4] This large number of dummies was conservatively chosen to ensure that density effects would not affect our measurements. Determining the minimum number of required dummies was beyond the scope of this work.

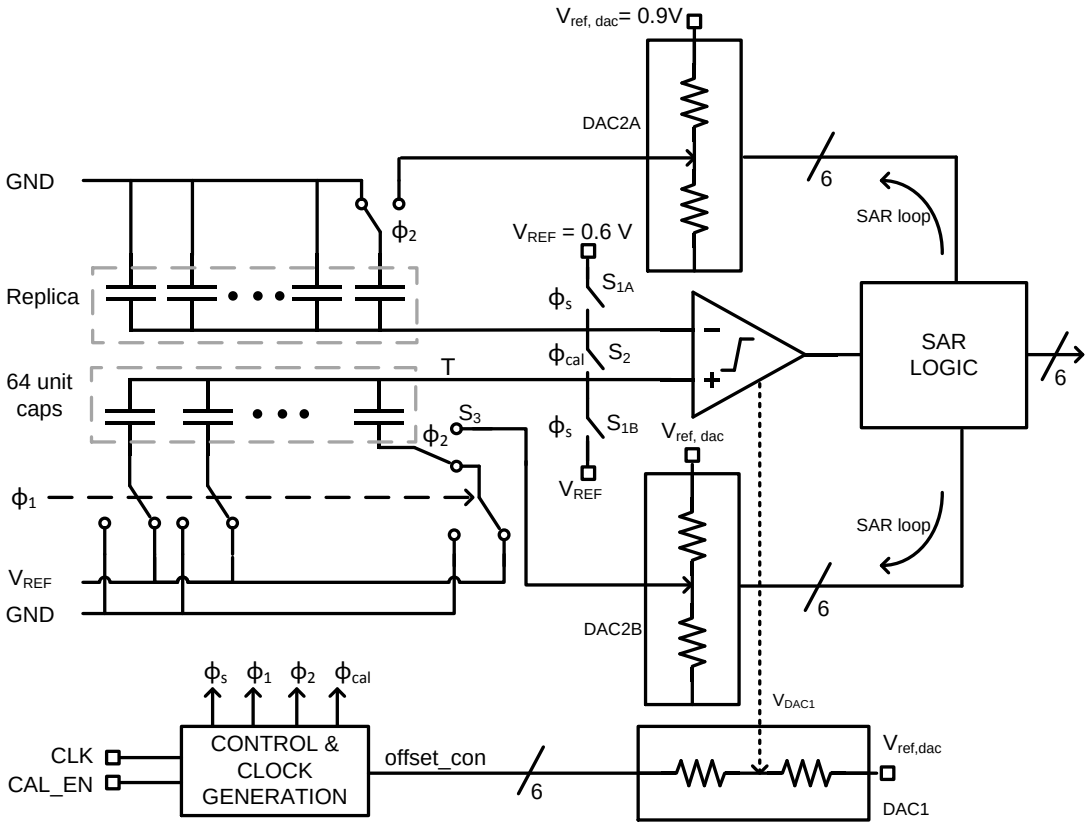


Fig. 2.8 Proposed test structure for capacitance mismatch measurement.

D. Comparator Implementation

Fig. 2.9 shows the comparator schematic. It comprises of a resistively loaded differential pair (preamplifier) followed by a regenerative latch. The regenerative latch design is similar to that in [40] and together with the preamplifier, it reduces the comparator kickback to insignificant levels. The comparator offset calibration setup is also depicted in Fig. 2.9 (similar to [41]). An additional differential pair driven by DAC1 is employed to tilt currents in the appropriate direction to minimize the comparator offset. The DAC1 resolution as well as its reference voltage ($V_{ref,\,dac}$) is chosen so that about 50 mV of input offset (approximately 3σ) can be reduced to within a few LSBs of the SAR loop (see Fig. 2.8).

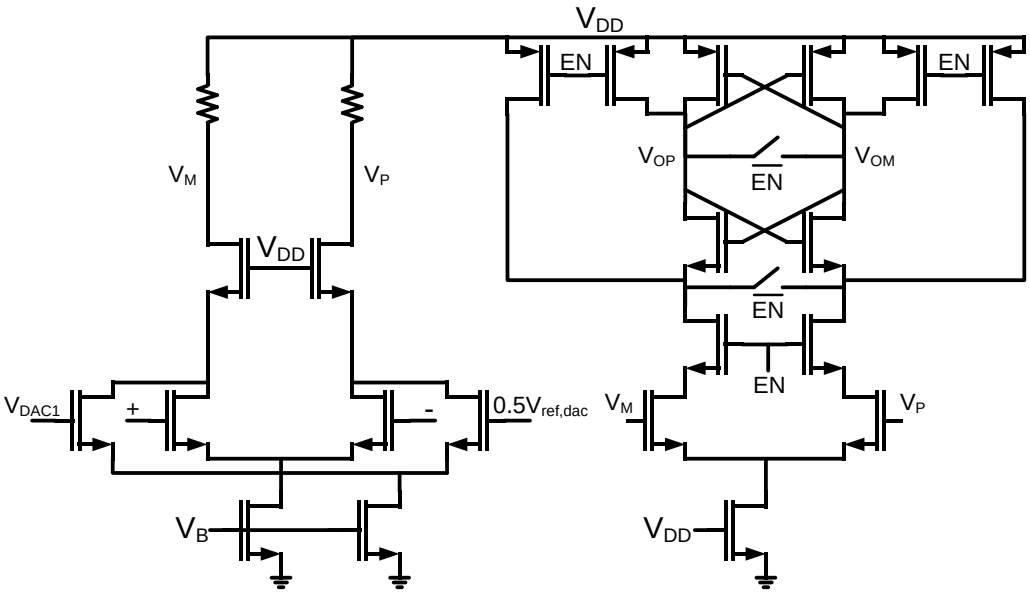


Fig. 2.9 Comparator schematic.

2.5. Circuit Operation

Fig. 2.10 presents a timing diagram of the circuit operation of the test structure circuit shown in Fig. 2.8. As illustrated (in Fig. 2.10), this can be divided into two phases: calibration phase and measurement phase, which are described next.

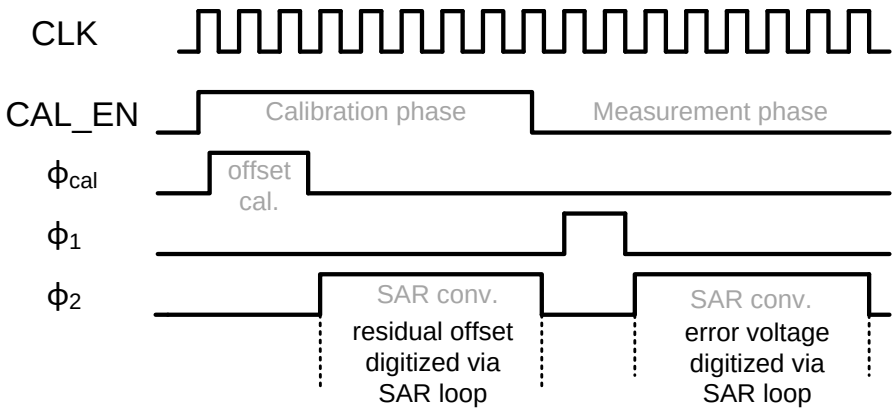


Fig. 2.10 Timing diagram.

A. Calibration Phase

During the calibration phase, the external signal CAL_EN is set to logic high and the circuit operation begins with a coarse offset calibration cycle (ϕ_{cal}), where the comparator input is shorted and its offset is minimized via DAC1 (Fig. 2.11). Next, the residual offset is measured through SAR conversions via DAC2A, B. S_3 is turned on and the feedback DAC is coupled to the comparator via one unit capacitor (as shown in Fig. 2.12), which gives an attenuation and LSB size reduction of approximately 64.

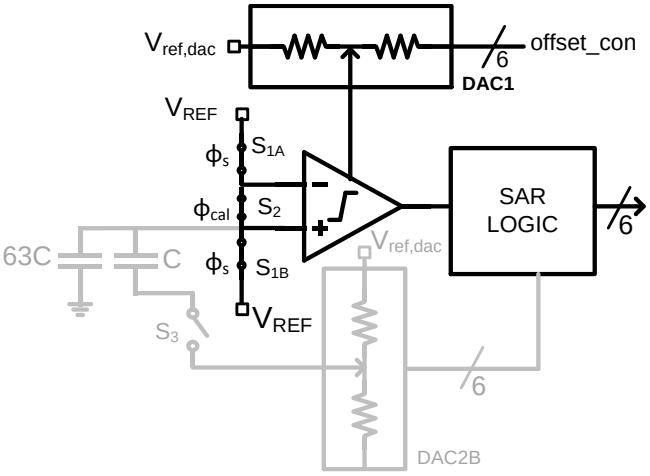


Fig. 2.11 Coarse calibration of comparator offset (half-circuit of the SAR loop is shown for simplicity).

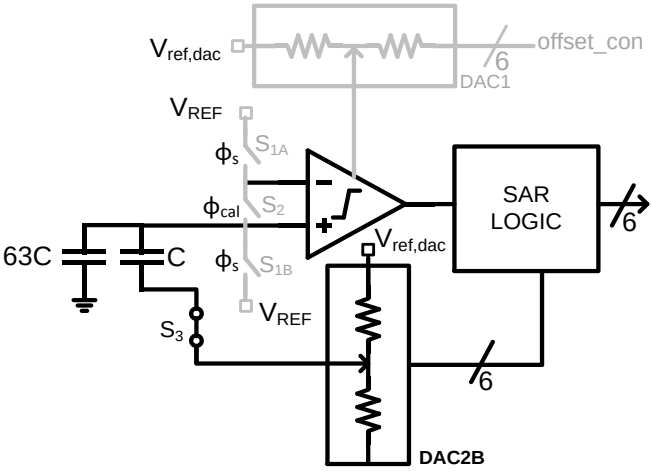


Fig. 2.12 Residual offset measurement using SAR conversion via DAC2B (half circuit is shown for simplicity).

B. Measurement Phase

In this phase, the the CAL_EN signal is set to logic low and the unit capacitors are switched via ϕ_1 to generate the error voltage (V_Δ), which is then quantized via the same SAR loop (as in the calibration phase). The earlier digitized residual offset is subtracted from this measurement. Unlike the capacitance switching via ϕ_1 (which is done only in one half circuit), the feedback DAC signal is fully differential for robust SAR A/D conversion (see Fig. 2.8). With 6 bits of resolution in DAC2A, B, and 64 unit elements in the capacitive DAC, the LSB size of the measurement corresponds to that of a 12-bit ADC. The measurements are repeated and averaged to reduce the kT/C noise to within an LSB at the 12-bit level.

The above-described characterization procedure is summarized in Fig. 2.13. Even though it combines several measurements and includes a calibration step, it avoids the key shortcomings of [38], where the characterization routine relies on simulation data and measurement results from a separate reference structure.

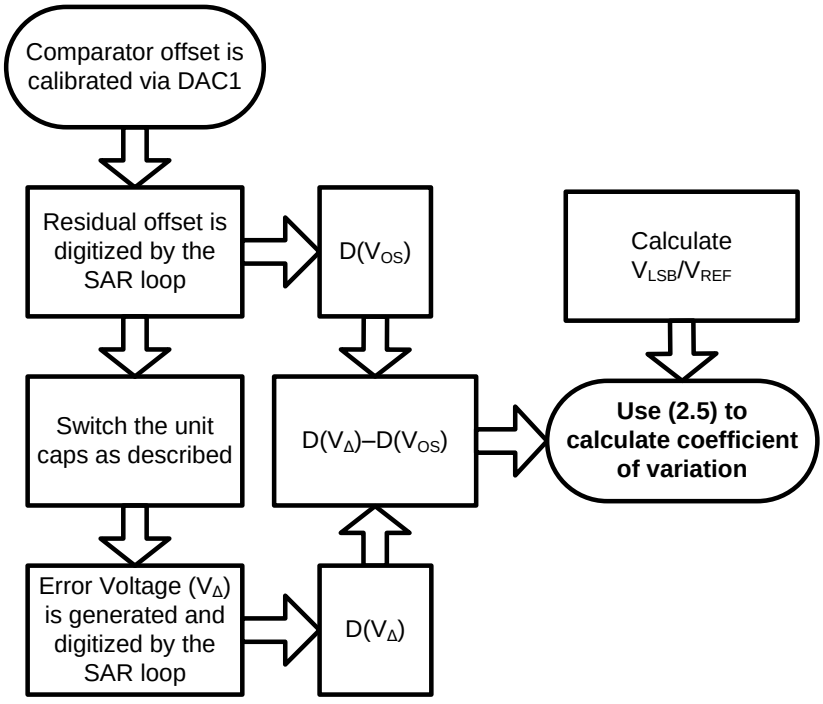


Fig. 2.13 Characterization procedure.

C. Error Sources

It is important to consider error sources that may affect the accuracy of the mismatch characterization. One imperfection to consider in our circuit is the mismatch in the coupling capacitance that injects the feedback DAC signal as depicted in Fig. 2.14 (a). Analysis shows (see Appendix A.4) that this error merely scales the measurement by the mismatch factor; i.e., the percent uncertainty in the measurement is equal to the mismatch percentage, which is on the order of one percent and thus negligible.

Another imperfection to consider is the effect of parasitic capacitance at the comparator input. C_P in Fig. 2.14 (a) models the comparator's input capacitance, stray capacitance of wires and the capacitive array, as well as any junction capacitance of $S_{1A,B}$ (if a bulk process is used). This capacitance attenuates the comparator input signal (equivalent to a comparator gain reduction) and does not affect the linearity of the SAR A/D conversion. It also reduces the signal to noise ratio (SNR), which is inconsequential, thanks to the extensive averaging used in measurements. Furthermore, owing to the fact that the error voltage signal (V_Δ) and the feedback DAC signal go through the same attenuation, C_P does not alter the full scale range of the SAR ADC (similar to a bottom plate sampling circuit). Consequently, the test structure of Fig. 2.8 is insensitive to parasitics, which also means that using a metal layer closer to the substrate (for example, metal 3 or metal 5 instead of metal 7) for the capacitances will be acceptable.

Finally, the proposed test structure relies upon the accuracy of DAC2A, B for the SAR A/D conversion and the minimum mismatch that can be measured is limited by the integral nonlinearity (INL) of the feedback DAC (see Fig. 2.14 (b)). Detailed analysis shows (see Appendix A.5) that the INL of DAC2A, B must be less than its LSB (at the 6-bit level). The expected INL from process data lies within one fifth of this requirement.

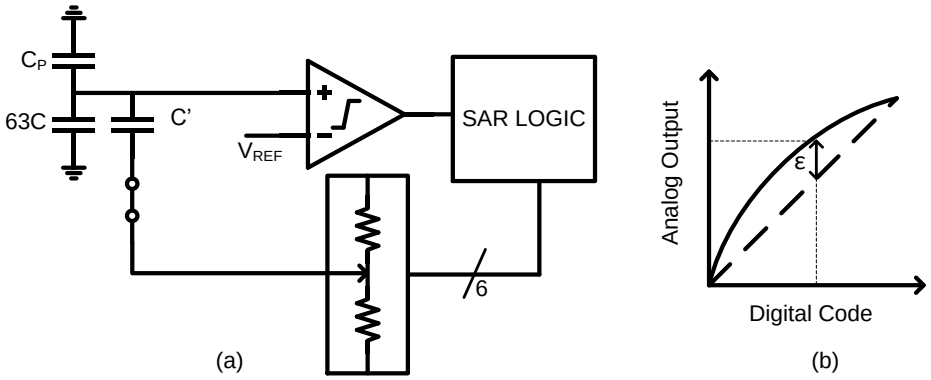


Fig. 2.14 Error sources in the test structure: (a) Parasitic capacitance (C_P) and mismatch in the DAC coupling capacitance C' and (b) INL of the feedback DAC.

2.6. Prototype IC and Measurement Results

The designed chip was fabricated in IBM's 32nm CMOS SOI process and contains 72 of the test structures shown in Fig. 2.8. Half of the test structures are built with capacitances of 0.45 fF in the unary array, while the other half uses 1.2 fF. The dimensions of one structure are 90 μm × 55 μm (0.005 mm^2). Fig. 2.15 shows the die photo along with the chip layout.

A 7-bit decoder (on chip) is used to enable the test structures one at a time and a PC controls the measurement and data collection as shown in Fig. 2.16. Thermal (kT/C) noise is suppressed by averaging 131,072 measurements for each test structure.

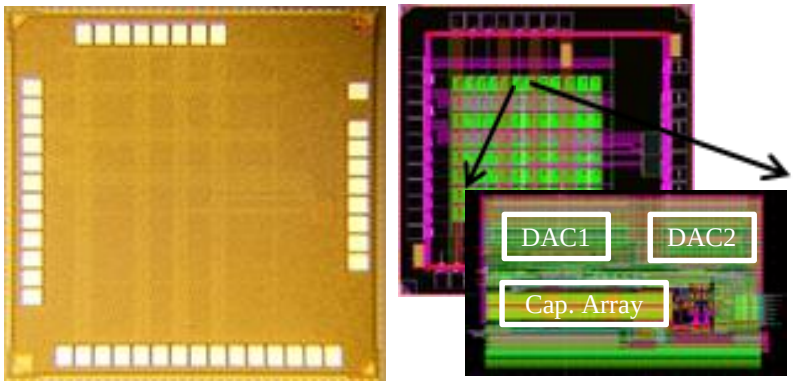


Fig. 2.15 Die photo and layout.

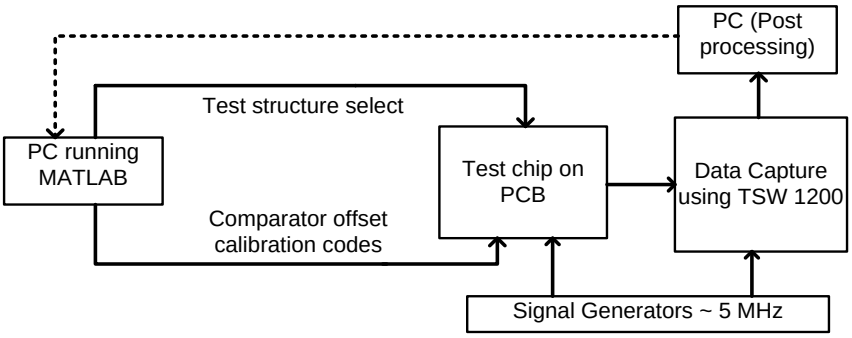


Fig. 2.16 Measurement setup using a TSW 1200 data capture card (Texas Instruments).

A. Measurement Results

Fig. 2.17 shows mismatch histograms for all test structures on a single die. From the histogram, it can be seen that the measured mean is negative. This is confirmed by (2.3), which predicts a negative mean for (2.2) in presence of finite neighbor correlation among the unit elements. Fig. 2.18 shows our measurement results across 8 dies. The calculated sample coefficient of variation is 1.2% for 0.45 fF, and 0.8% for 1.2 fF unit capacitors, respectively. The sample variance is $1/\sqrt{N}$ = 0.167 or 16.7% (N = 36), which is in line with the variations seen from chip-to chip in Fig. 2.18.

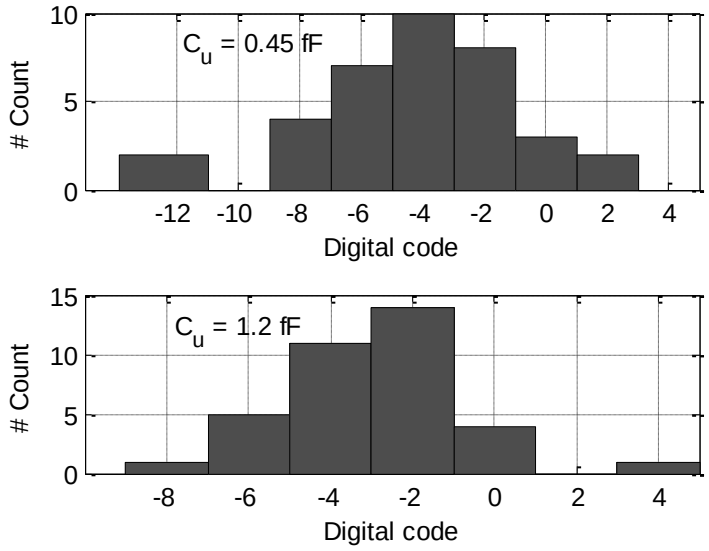


Fig. 2.17 Measured mismatch histogram on a single die.

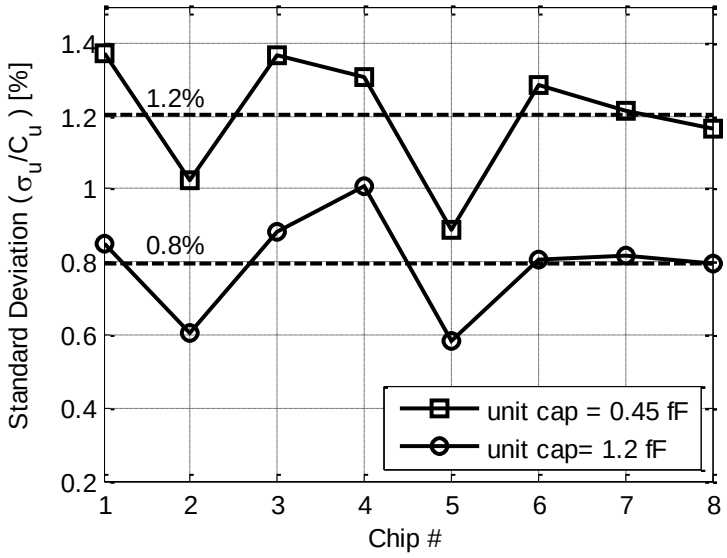


Fig. 2.18 Mismatch measurement across 8 dies.

B. Mismatch Coefficients

The above measurement results can be used to compute the mismatch coefficients for the considered single-layer MOM capacitors as per the Pelgrom's mismatch model (Variance ~ 1/Area) [42]. The relative unit element mismatch (c_v) can be expressed as

$$c_v^2 = \frac{A_{f1}^2}{C} \tag{2.6}$$

Since the capacitance C is proportional to area, the above equation becomes

$$c_v^2 = \frac{A_{f2}^2}{WL} \tag{2.7}$$

where W and L are dimensions of the realized capacitance (see Fig. 2.1), and $A_{f1}$and A_{f2} are the mismatch coefficients. It is important to note here that (2.6) and (2.7) are equivalent, as the capacitance C scales with length L (as described in Section 2.2) and doubling L doubles the capacitance (as well as the capacitor's area). A_{f1} is estimated by fitting (2.6) with our measured data, (as shown in Fig. 2.19) and is calculated to be approximately 0.85% × 1 fF. Using this computed value of A_{f1} along with the capacitor dimensions from Table 2.1, A_{f2} is 1.9 % × 1 μm.

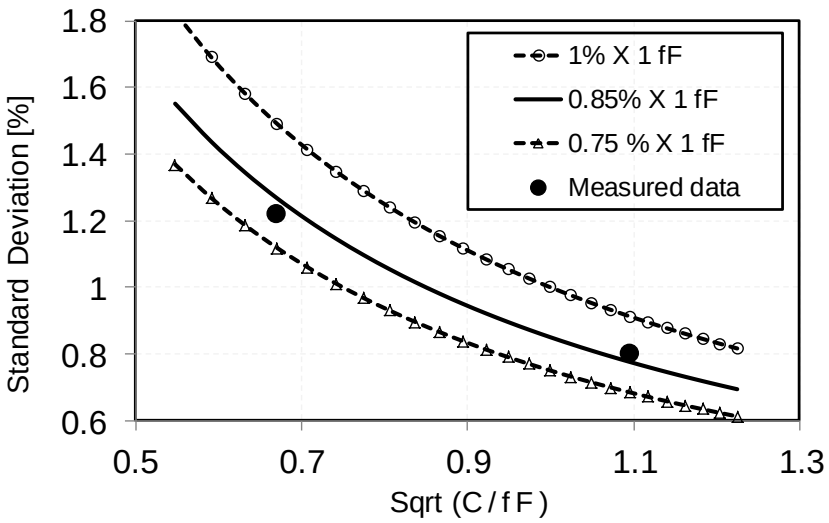


Fig. 2.19 Standard deviation (relative unit element mismatch) vs. unit capacitor size. Each curve corresponds to a different Pelgrom's mismatch coefficient and our measured data fits well with the one corresponding to 0.85% × 1 fF (solid line).

These mismatch coefficients (A_{f1} and A_{f2}) enable a designer to choose minimum possible unit capacitors, especially for mismatch-limited designs. For example, the variance of mid-code DNL of an M-bit binary weighted capacitive DAC is[5]

$$\sigma_{DNL}^2 = c_v^2(2^M - 1) \tag{2.8}$$

Using (2.8) and Fig. 2.19, we can pick a unit capacitor size for a specific DAC resolution and a certain DNL. This is illustrated in Table 2.2 for a target σ_{DNL} of 0.1 LSB.

Table 2.2 Unit capacitor size for various DAC resolutions

DAC Resolution (bits)	Unit Capacitor Size (fF)
6	0.4
8	0.65
10	2

[5] This assumes that the unit capacitors as independent random variables. Appendix A.3 presents a more general equation for σ_{DNL} in presence of nearest neighbor correlations.

2.7. Summary

This chapter presented a systematic study of mismatch characteristics of small (sub-femto Farad), single layer, lateral field capacitors. A unary capacitive array was used as a means to infer the relative mismatch between two unit capacitors. The capacitors in this array were assumed to be Gaussian random Variables with finite correlation among nearest neighbors. A capacitor-switching scheme was devised to suppress the effect of this correlation and translate the mismatch information (coefficient of variation) into an error voltage. A test structure to enable digital readout of this error voltage was then presented. The salient features of the proposed test structure include: (1) no analog inputs (except for DC reference voltages) and (2) a purely digital output bit-stream that contains the mismatch information, thus eliminating sources of error like instrumentation inaccuracy and noise. For each chip, 72 test structures were measured (36 each for 0.45 fF and 1.2 fF unit capacitance) and the obtained results confirm good matching despite small geometries. Moreover, the matching improvement was found to be in accordance with Pelgrom's area scaling formula ($\sigma^2 \sim 1/\text{Area}$).

Chapter 3

Design Techniques for High-Speed SAR A/D Converters

3.1. Introduction

The SAR A/D conversion method, which was briefly discussed in Chapter 1, achieves outstanding power efficiency, especially at low to moderate conversion rates [18], [43]. The use of small unit capacitors (~0.5 fF) within the capacitive D/A converter improves this advantage further by reducing the switching energy [12]. Chapter 2 discussed the mismatch characteristics of such small capacitors realized using a single-metal layer in a modern CMOS process. In addition, the use of small capacitors also reduces DAC settling time, thereby improving the conversion rate of a SAR ADC.

This chapter presents a study of various circuit design techniques that were explored during the course of this research, with the main goal of increasing the conversion speed of single-channel SAR A/D converters. Asynchronous timing, top-plate sampling, SAR loop delay optimization and comparator design are discussed in Section 3.3. Section 3.4 introduces the pipelined-SAR A/D converter along with its speed bottlenecks followed by the proposed two CDAC pipelined SAR architecture in Section 3.5. A time constant matching technique is discussed in Section 3.6.

3.2. High Speed SAR A/D Converters

The power efficiency of an A/D converter deteriorates when operating at high conversion speed as the constituent blocks are pushed against the speed limits of the process technology. This is an effect that is particularly pronounced in SAR ADCs due to the sequential nature of the conversion. At this point, one may ask, what is high speed for a SAR ADC? The answer to this question depends on multiple factors such as process technology, ADC resolution etc. A reasonable number may be inferred by plotting the Walden FOM[6] (FOM_W) vs. ADC conversion speed for SAR ADCs published at the ISCCC and the VLSI Symposium as shown in Fig. 3.1 [11]. It is evident that there are multiple SAR ADC designs that achieve an FOM_W < 100 fJ/conv-step at conversion speeds of < 100 MS/s. However, only three single-channel SAR ADCs [44], [45], [46] achieve similar power efficiency at conversion rates above 200 MS/s (see Fig. 3.1). Hence, for the purpose of discussion in this chapter, we designate SAR ADCs operating at > 200 MS/s as high speed and present design techniques that enable such conversion frequencies in the next section.

3.3. High-Speed SAR ADC Design Techniques

A. Asynchronous Timing

During a SAR conversion process, the comparator makes its critical decision when the input is less than an LSB as shown in Fig. 3.2. As a result, the comparator resolves significantly faster for other non-critical decisions (compared to the critical one). The asynchronous timing in a SAR ADC takes advantage of this particular fact and allocates more time for the critical decision by allowing the comparator to trigger itself using on-chip delay lines [17]. Since now the other decisions (non-critical) take much less time together, this results in substantial improvement in the

[6] $FOM_W = P/(f_s \times 2^{ENOB})$, $ENOB = (SNDR - 1.76)/6.02$

ADC conversion speed compared to a synchronous SAR ADC, which allocates equal time for all the comparator decisions by using a fast external clock [17].

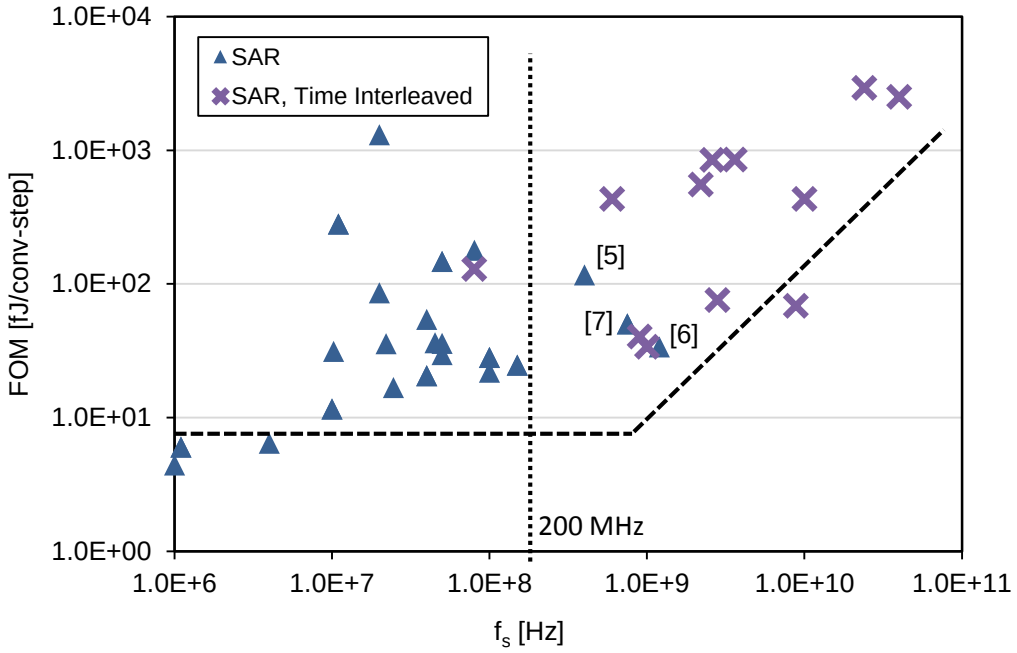


Fig. 3.1 Walden FOM vs. ADC conversion speed.

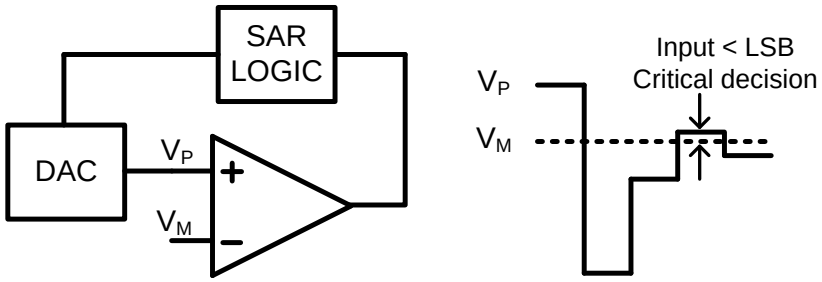


Fig. 3.2 Comparator inputs ($V_{P,M}$) during SAR operation (single ended for simplicity).

Fig. 3.3 shows the asynchronous SAR operation in more detail. It begins at the end of the sampling phase, when the falling edge of sampling clock enables the first comparison (MSB). A simple NAND (or XOR) operation on the comparator's outputs indicates the end of a comparator decision and this, together with an on-chip delay line, generate a comparator control signal ('LATCH' in Fig. 3.5) that enables subsequent comparisons during the SAR operation [14]. Another approach for generating this control signal is to use combinatorial logic together with an external

control voltage to set the delay duration [47]. This delay essentially guarantees sufficient comparator reset time to erase the previous state and avoid SNR degradation due to hysteresis. The delay can also be made input dependent to further optimize the SAR conversion time [48]. Essentially, the LATCH signal replaces the external high-speed SAR clock of a synchronous SAR ADC, except that it is generated on-chip and its logic high phase duration varies with the comparator input.

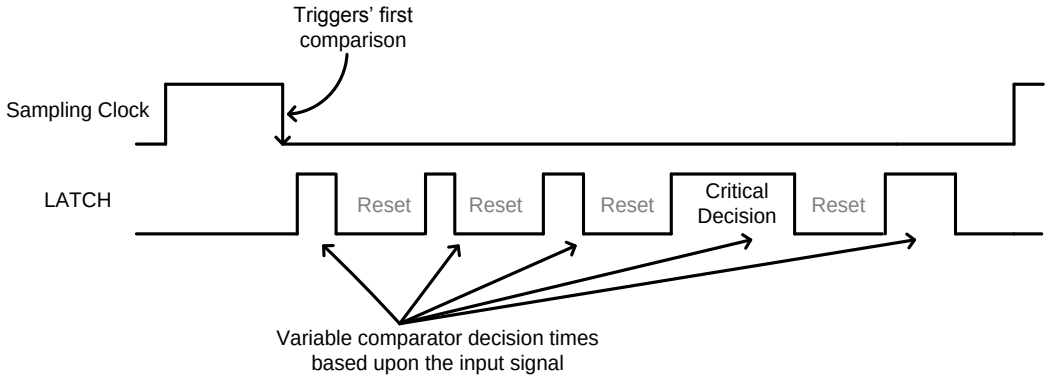


Fig. 3.3 Sampling clock and comparator control signal in an asynchronous SAR ADC.

B. Top Plate Sampling

Fig. 3.4 shows the top plate sampling scheme [49] for a 3-bit SAR ADC (as an example). During sampling, the input signal is tracked on the common top plate of the capacitive DAC. At the end of sampling phase, the MSB is directly resolved by simply enabling the comparator, as no charge redistribution is needed in this case (in contrast to bottom plate sampling technique [50]). This results in 50% savings in total DAC capacitance and eliminates the MSB capacitor transition, which translates to an 81% savings in DAC switching energy [49]. However, the top plate sampling method, as originally proposed in work of [49], results in monotonic DAC switching. Consequently, the comparator has a variable input common mode, which is undesirable. Chapter 4, Section 4.3 A presents a modified top plate sampling scheme with symmetric DAC switching, which solves this particular problem.

It is important to note here that with good bootstrapping of the sampling switches, top plate sampling can be used in ADC designs up to 10 bits of resolution

(SNDR of 60 dB). Beyond this value, its usefulness is limited by signal dependent charge injection [51]. In the design space of ADCs targeting more than 10 bits of resolution, bottom plate sampling is almost exclusively employed (see e.g. [52], [53] with a very recent exception [54]).

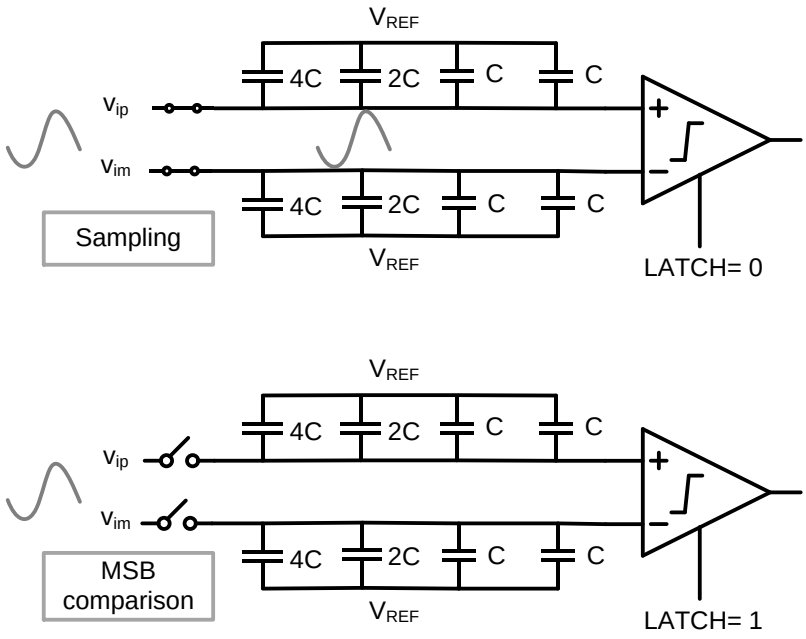


Fig. 3.4 Top plate sampling and MSB comparison.

C. SAR Loop Delay Optimization

A SAR ADC comprises of three main circuit blocks: a comparator, a capacitive DAC and SAR logic as shown in Fig. 3.5. As a result, the speed of a SAR ADC is limited by the sum of the delays through these blocks (see Fig. 3.5): DAC settling (T_{DAC}), comparator decision time (T_C) and SAR logic delay (T_L). Maximizing the speed therefore boils down to a joint minimization of all three components. To illustrate the associated tradeoffs, consider a DAC MSB circuit slice shown in Fig. 3.6. The DAC uses an inverter circuit to drive the bottom plates of the capacitors (connected to V_{REF} during sampling) and the size of the PMOS device is defined by the required on-resistance during sampling. The optimum size for the NMOS follows from a more complex consideration that includes the loading of the SAR

logic. Widening the NMOS improves the DAC settling time (T_{DAC}) during redistribution, but increases the logic delay (T_L). Consequently, there exists an optimum sizing that minimizes $T_L + T_{DAC}$ as shown. The optimum is shallow, but the reward for proper optimization is high, since the time savings multiply with the number of conversion cycles.

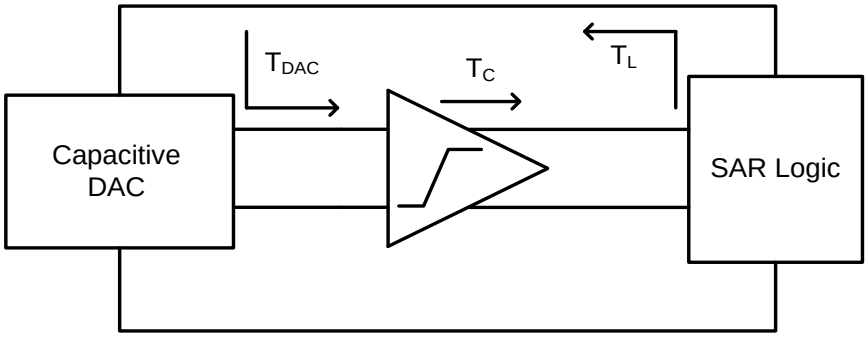


Fig. 3.5 Delays in a SAR loop.

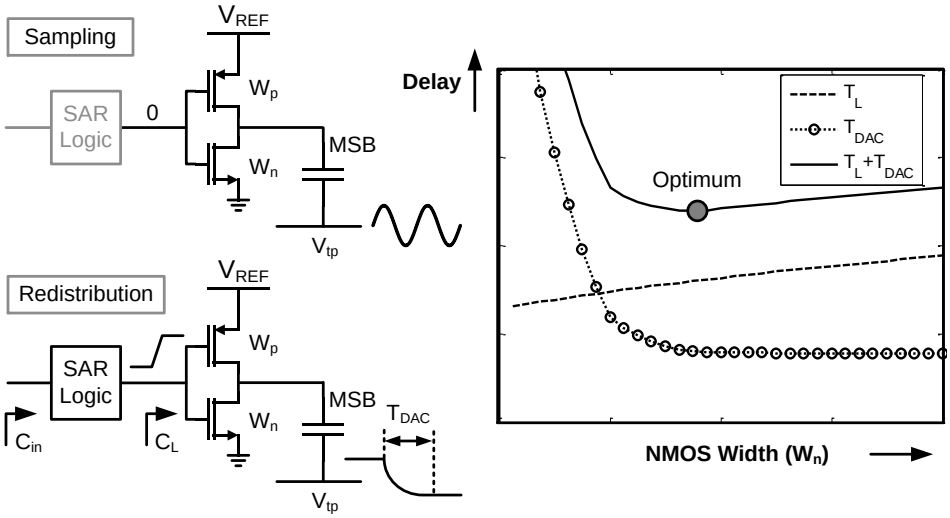


Fig. 3.6 Optimization of logic and DAC delay ($T_L + T_{DAC}$).

D. Comparator Design

A fast comparator with accurate reset is critical for high-speed SAR A/D conversion. This is even more important in an asynchronous design because it relies upon the comparator decisions to generate the internal SAR clock. Fig. 3.7 depicts a generic comparator block diagram, which consists a pre-amplifier followed by a

cross-coupled latch (positive feedback). In addition to attenuating the comparator kickback and reducing the input referred offset, the preamplifier can also be used to optimize regeneration and reset [55]. This is discussed in more detail in Chapter 4, Section 4.3 B.

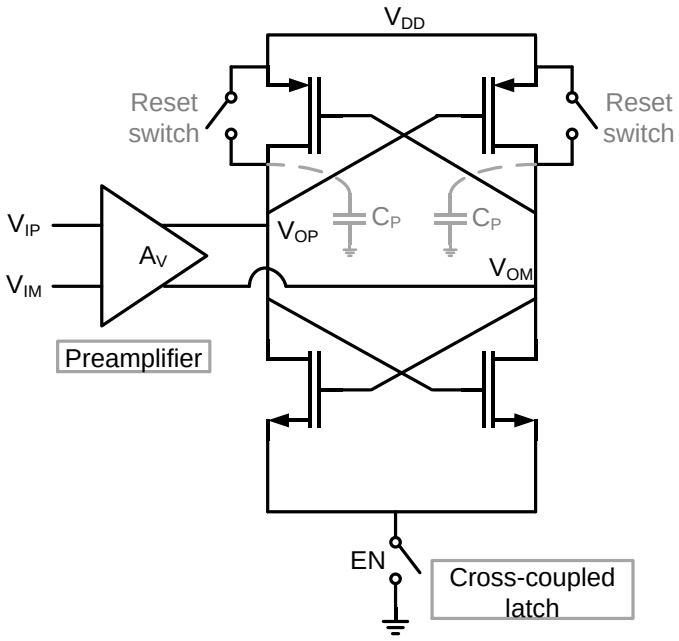


Fig. 3.7 A generic comparator schematic.

Designing a fast comparator usually boils down to minimizing its regeneration time constant (τ_{reg}), which results in smaller comparator decision time (T_C) as well as lower metastability probability [51]. The key to achieving this is to make the latch more self-loaded or in other words minimize the extra parasitic capacitance at the regenerative nodes (C_P in Fig. 3.7). Large gate-drain fringe capacitance in a modern CMOS process (almost comparable to the intrinsic gate capacitance) tend to increase the parasitic load on the cross-coupled latch. This is particularly important when large reset switches (which add extra fringe capacitance during regeneration) are needed to clear hysteresis in a relatively short reset time. This may become a bottleneck in a high-speed SAR design and the work of [45] proposes the use of alternating comparators to relax the reset time constraints.

One way to reduce the fringe capacitance is by increasing the drain-contact to poly spacing (e.g., 2 to 3 times the minimum spacing) in the transistor layout as

shown in Fig. 3.8. Another interesting approach is to isolate the regenerative nodes in the latch by employing either poly-resistors [56] or on-chip low-Q inductors [57]. Fig. 3.9 shows the latter technique in more detail. When the latch is fired (EN= 1), the critical nodes N_1 and N_2 do not directly see the load capacitance C_L, which results in smaller τ_{reg}(faster regeneration), thereby improving speed as well as the metastability probability ($P_{meta} \propto e^{-\tau_{reg}}$). In the reset phase (EN= 0), the weak bleed current sources $I_{1,2}$ help erase the stored-state in the inductors.

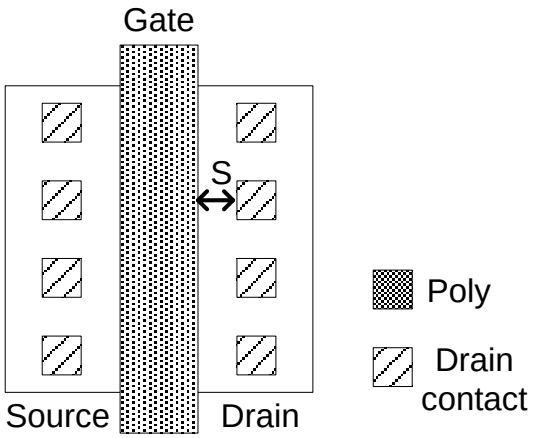


Fig. 3.8 Transistor layout showing the drain contact-poly spacing (S).

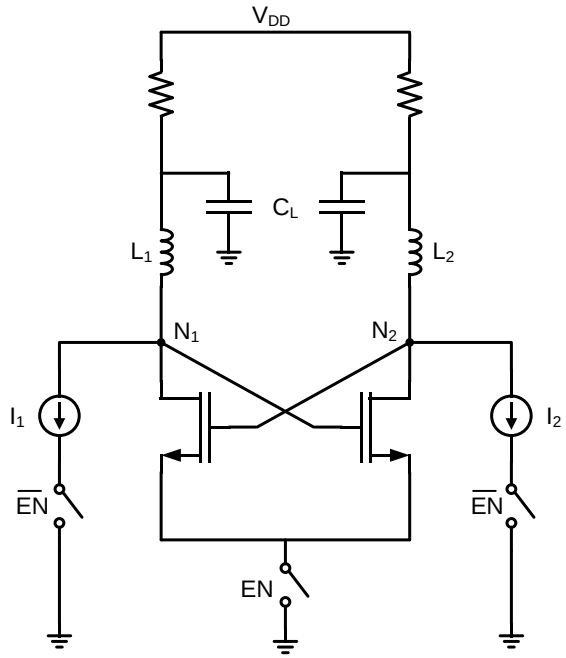


Fig. 3.9 Isolation inductors in a cross-coupled latch.

3.4. Going Beyond 10 bits

Fig. 3.10 shows a plot of conversion frequency (f_s) vs. SNDR for SAR ADCs published at ISSCC and the VLSI Symposium [11]. From this plot, it is evident that most single-channel SAR designs with > 100 MS/s conversion speed are limited to moderate resolution (~50 dB SNDR). This is because the sequential nature of conversion in a SAR ADC means that every extra bit adds an additional SAR loop delay (Section 1), and this reduces the A/D conversion speed. Moreover, increasing resolution, usually increases the total DAC capacitance because the capacitance mismatch limits the minimum unit capacitor size (see Chapter 2) and driving this large input capacitance becomes increasingly challenging at high speeds.

One way to circumvent this problem is to use sub-ranging SAR architectures [58]. These designs essentially use a high-speed flash ADC to resolve the first few bits, which are then loaded in the capacitive DAC of a conventional SAR ADC that completes the A/D conversion. Another promising approach is to pipeline SAR ADCs, which leads to SAR-assisted pipeline or simply pipelined SAR A/D converters (described next).

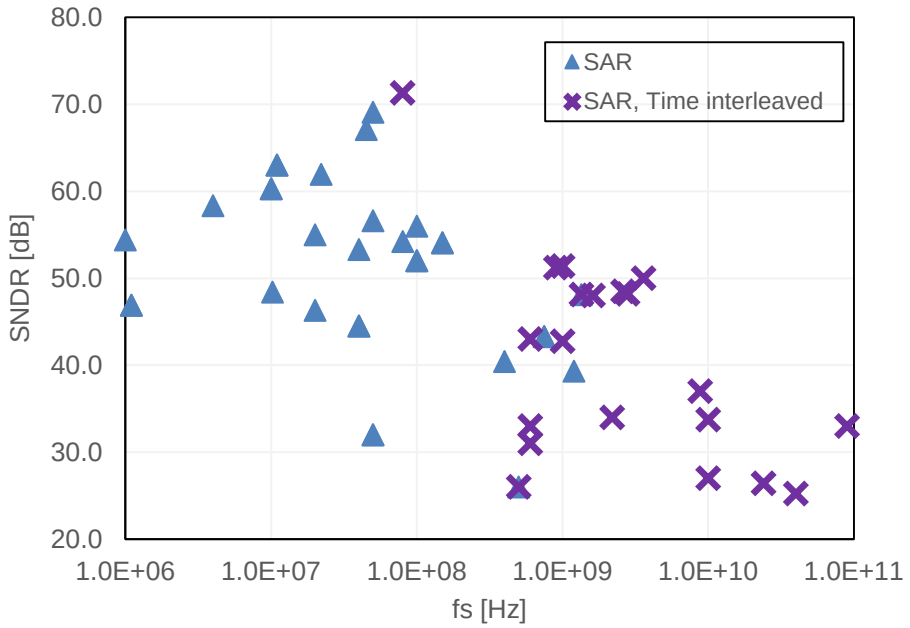


Fig. 3.10 Plot of SNDR vs. SAR ADC conversion frequency.

Fig. 3.11 shows a top-level block diagram of a pipelined SAR ADC along with its timing diagram. This architecture was proposed independently in the works of [21], [59], [60]. It comprises of two moderate resolution (6-8 bits) SAR ADCs pipelined using one inter-stage gain element (residue amplifier). This results in good power efficiency, especially when compared to conventional multi-stage pipeline ADCs that employ several residue amplifiers. A recent work reports outstanding power efficiency by using a dynamic residue amplifier [22]. In general, large resolution (~6 bits) in the first stage significantly relaxes the design of the inter-stage amplifier because of the resulting small input signal swing [21].

Fig. 3.12 shows the implementation details of the 12 bit, 50 MS/s pipelined SAR ADC reported in [21]. The total capacitance of the (capacitive DAC) CDAC in the frontend (stage 1) is defined by kT/C noise, e.g., 1.8 pF in this case. The input signal is sampled on this DAC, which also performs the SAR operation along with residue computation. Consequently, the large DAC capacitance switches at the internal high-speed SAR clock frequency resulting in increased DAC switching power dissipation. Moreover, since stage-1 can allocate only a small A/D conversion time, as it shares the clock period with tracking and residue amplification, switching the large DAC capacitance at the internal SAR speed becomes a major speed limitation of this ADC architecture targeting high SNDR (> 65 dB).

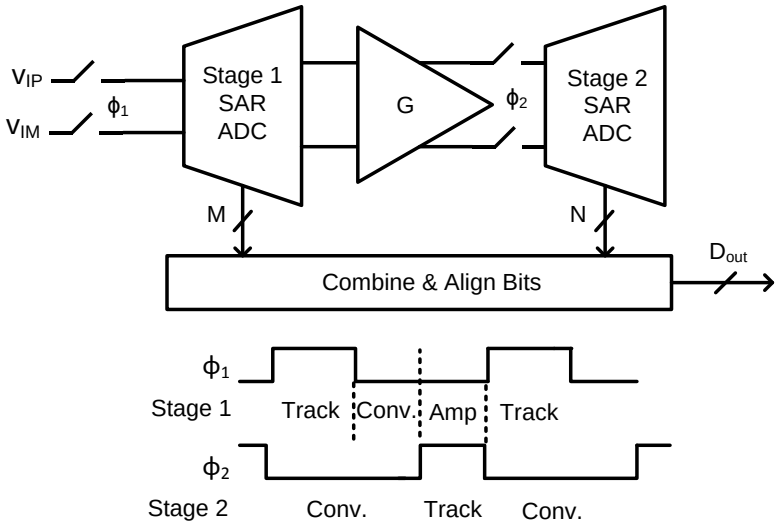


Fig. 3.11 Block diagram of a Pipelined SAR ADC.

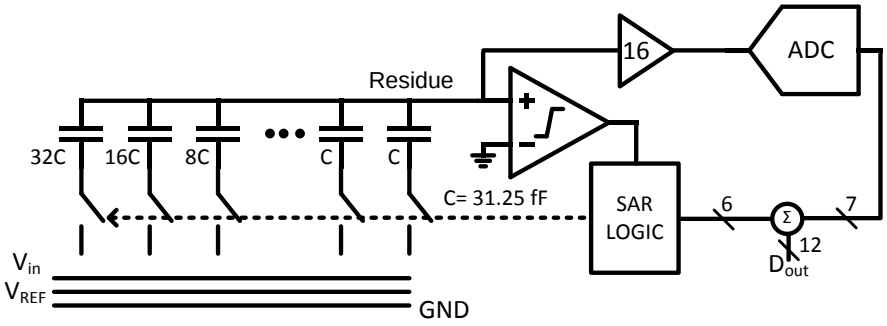


Fig. 3.12 Implementation details of the pipelined SAR ADC showing the large DAC capacitance in the frontend.

3.5. Two-CDAC Pipelined-SAR ADC Architecture

The previous section highlighted a major drawback of the pipelined SAR architecture, i.e. it uses one CDAC for both SAR conversion and residue computation, which becomes a bottleneck in improving the conversion speed. The proposed two-CDAC architecture solves this issue by leveraging a key concept of ADC pipelining: only the residue needs to be accurate to the overall ADC precision, while the decision errors in stage 1 are absorbed by redundancy. Fig. 3.13 illustrates this notion in more detail: The DAC errors (ε in Fig. 3.13 (a)) are directly referred to the input and as a result, the DAC needs to be accurate to the overall ADC precision, which also ensures sufficient accuracy in the residue voltage V_{res}. Errors in the stage 1 decisions, modeled by comparator threshold variation (depicted by grey lines in Fig. 3.13 (b)), are absorbed in the redundancy, provided that these do not over range the backend ADC (see Fig. 3.13 (b)). Intuitively, this is a function of the inter-stage gain (G) because it also amplifies the errors in stage 1. Therefore, the true resolution for a pipelined-SAR ADC is N + $\log_2$G, when both stage 1 and stage 2 have equal full-scale range (FSR) [51]. In case of unequal full-scale range, G is replaced by $G' = \alpha \times G$, where alpha equals FSR_1/FSR_2 (the ratio of stage 1 FSR to stage 2 FSR).

A. Proposed Two-CDAC Architecture

Fig. 3.14 presents a top-level block diagram of the proposed two CDAC pipelined SAR A/D converter, which employs two capacitive DACs in stage 1 (6-b example). DAC1 has a small total capacitance of 160 fF (6 bit accuracy) and forms a high-speed SAR loop (highlighted in red in Fig. 3.14), which computes the digital bits. The total capacitance of DAC2, which computes the low noise residue voltage, is 1.6 pF, set by kT/C noise constraints. Use of an extra DAC addresses the issue of fast switching of noise limited DAC capacitance (Section 3.4) by separating the noise-limited path from the high-speed path. The next section explains this in more detail.

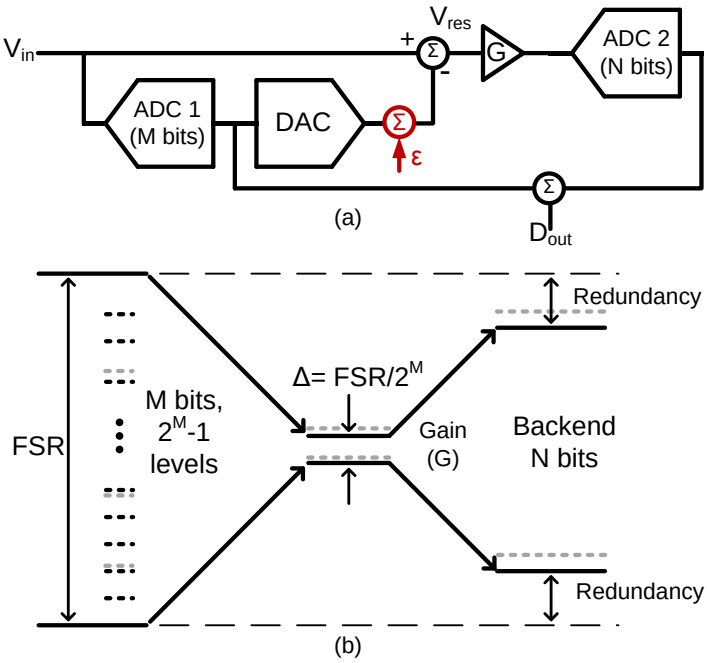


Fig. 3.13 A generic two-stage pipeline ADC showing the input referred DAC errors (top) and stage 1 error absorption via redundancy (bottom).

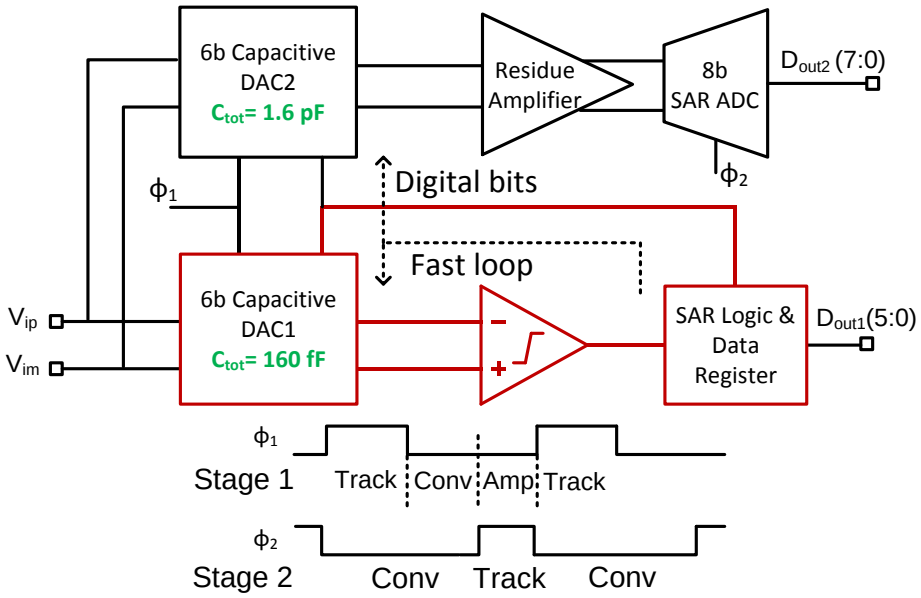


Fig. 3.14 Top-level block diagram of the proposed two CDAC architecture.

B. Stage 1 Operation in the Two-CDAC Pipelined-SAR ADC

The timing diagram of the proposed two-CDAC pipelined SAR ADC is shown in Fig. 3.14. For simplicity, let us assume that the both DAC1 and DAC2 are binary weighted DACs (similar to the one shown in Fig. 3.12) with different unit capacitor values. During ϕ_1, the input is simultaneously tracked on both of these CDACs and acquired via bottom plate sampling (assumption: ADC resolution > 10 bits). At the end of the sampling phase, DAC2 capacitors are left floating and the A/D conversion begins by connecting the MSB capacitance in DAC1 to a known reference voltage, V_{refp} (bit test operation). This is followed by a comparator decision that computes the MSB. If MSB is '1', the bit test operation moves to the MSB-1 capacitance, continuing the SAR operation. Instead, if MSB is '0', the MSB capacitance is switched from V_{refp} to V_{refn} ($V_{refp} > V_{refn}$), followed by the bit test operation on MSB-1 capacitance. This procedure is repeated until all the bits in stage 1 are computed. The resolved bits are subsequently loaded into DAC2, which generates the low-noise residue that is passed to the second stage via the residue amplifier.

Fig. 3.15 shows the stage 1 operation and DAC transient waveforms for the digital code of 010101 (as an example). These waveforms highlight the advantages

of using two CDACs in stage 1. The energy inefficient bit test operations (capacitance charge/discharge) are performed on DAC1, which has a small total capacitance. This results in small wasted charge that reduces DAC switching power compared to a conventional pipelined-SAR architecture [21]. Moreover, since the large noise-limited capacitors of DAC2 are not switched at the internal SAR clock frequency, a relatively long time is available for the residue voltage to settle to the required precision (see Fig. 3.15), thereby not limiting the ADC conversion speed. This essentially solves the speed bottleneck problem of a conventional pipelined-SAR architecture that was described in Section 3.4, while maintaining low energy A/D conversion.

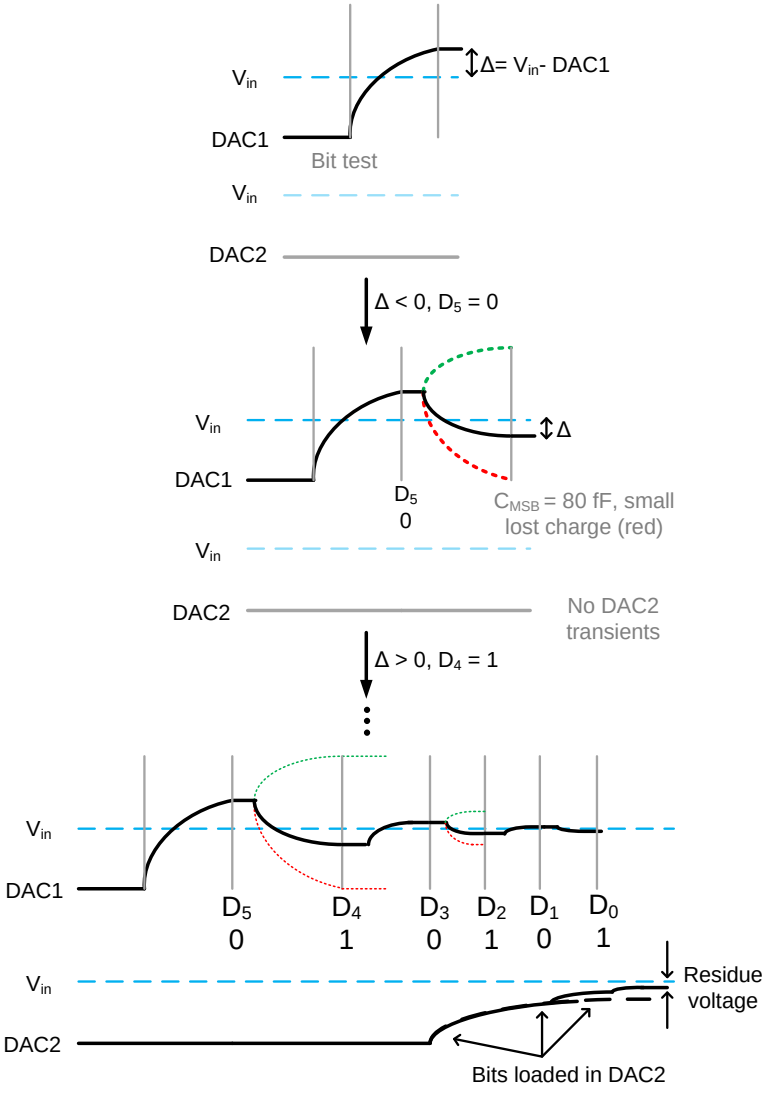


Fig. 3.15 Stage 1 operation and DAC transients.

3.6. Time Constant Matching

Section 1 discussed the various components of the SAR loop delay, which limits the conversion speed of SAR A/D converters. The DAC settling time is a significant fraction of this loop delay, especially in case of low power, low voltage designs (e.g. $V_{DD} < 0.8$ V). This is because a lower V_{DD} results in a smaller gate-drain overdrive voltage for MOS transistors, which translates to a high switch on-resistance (R_{ON}), thereby increasing the DAC settling time constant ($\tau \sim R_{ON}C$). Increasing the switch size reduces R_{ON} but increases the logic delay in the SAR loop, which may in turn increase the overall SAR loop delay (see Fig. 3.6). Non-binary scaling of capacitances [61] and bit overlap in the DAC array [18] has been proposed to take care of settling errors due to incomplete DAC settling. Both of these techniques use redundancy in the capacitor array with extra digital logic in the backend to correct for these errors. Instead, the time constant matching technique takes advantage of pole-zero cancellation to speed up DAC settling. It is similar to the time constant matching method used widely in oscilloscope probes.

A. Basic Concept

Fig. 3.16 shows a 5-bit capacitive DAC (part of a 6-b SAR ADC) in the sampling phase, during which the bottom plates are connected to a reference voltage (V_{ref}). The switch resistances of Fig. 3.16 are sized to keep equal time constants in each branch. For an 'n' bit converter, this means

$$R_{n-1} = R_{ref}$$
$$R_{n-1} = \frac{R_{n-2}}{2} = \frac{R_{n-3}}{4} \ldots = \frac{R_1}{2^{n-2}} \tag{3.1}$$

We assume now as an example that after the sampling phase, the first comparison has resulted in MSB=1. This is thus followed by switching of the MSB capacitance in the positive DAC half circuit from V_{ref} to ground (V_{gnd}) as shown in Fig. 3.17. The ground switch resistances are also scaled as per (3.1) with the minimum resistance being R_{gnd} for the switch, which connects the MSB capacitor to V_{gnd}

(Switch S_5' in Fig. 3.18). The equivalent simplified circuit schematic is shown in Fig. 3.18 with the switching being modeled as a step input at V_{in}.

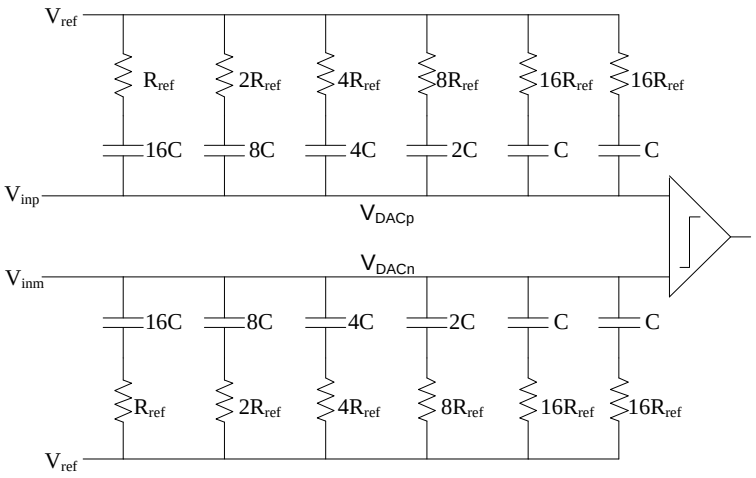


Fig. 3.16 DAC during sampling phase.

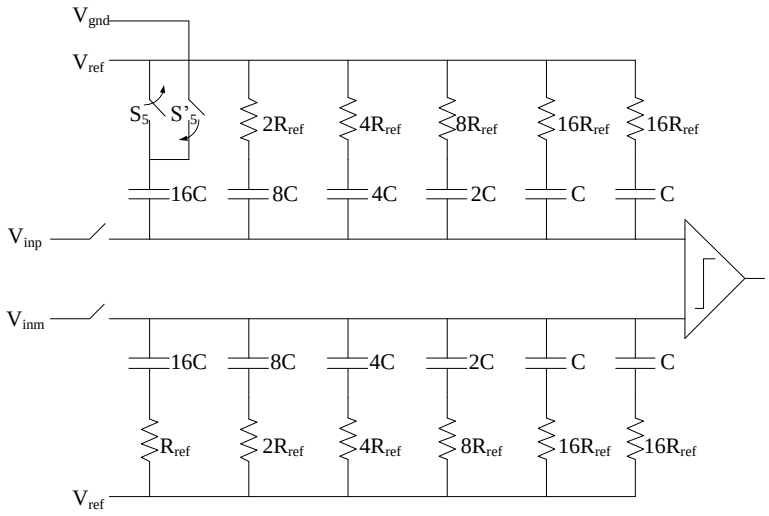


Fig. 3.17 MSB capacitance switching from V_{ref} to V_{gnd}.

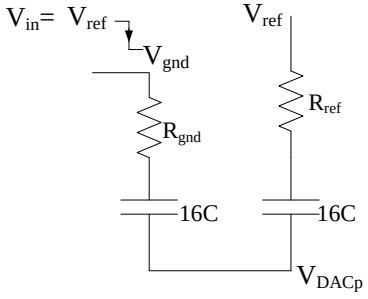


Fig. 3.18 Simplified circuit schematic of the DAC array after the MSB capacitor is switched from V_{ref} to V_{gnd}.

If R_{ref} is made equal to R_{gnd} (in Fig. 3.18), the time constants in the two paths are equal leading to pole-zero cancellation and the input step is directly transferred to the output leading to very fast settling of the DAC output voltage. This holds true for other DAC transitions as well and therefore improves the overall speed of operation. Fig. 3.19 shows the plot of settling time (for 0.5 LSB settling accuracy) vs. the ratio of R_{ref} to R_{gnd} for this ideal model. We see that a 10% mismatch in resistances causes substantial loss in settling time improvement due to a pole-zero doublet in the transfer function. This means that a relatively good matching between pull-up and pull-down resistance is needed to avail the benefits of time-constant matching (also see Fig. 3.21).

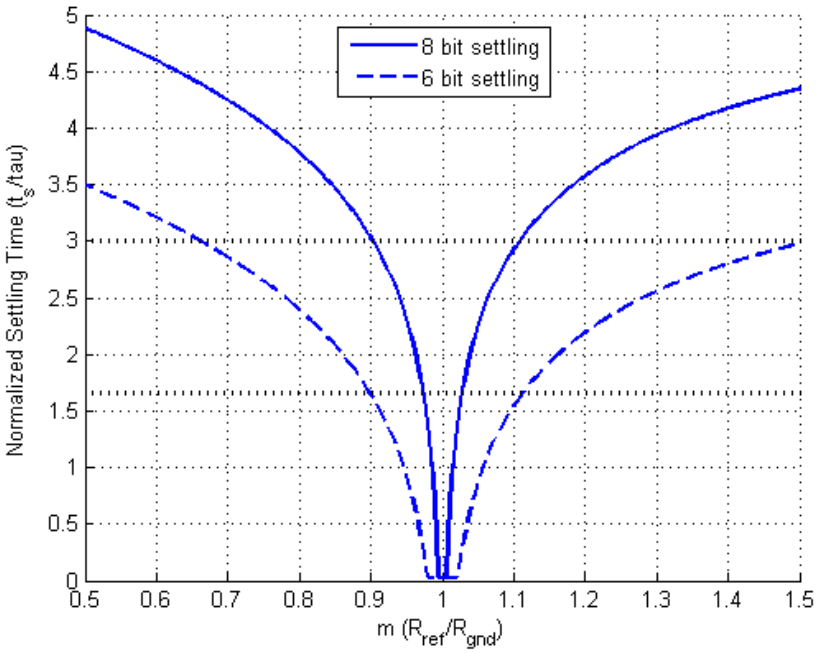


Fig. 3.19 Normalized[7] settling time vs. resistance ratio for the ideal model. When the time constants are matched, pulse transfer occurs resulting in close to zero settling time.

B. Detailed Analysis

Unfortunately, implementing the switches using MOS transistors results in variable resistance during the DAC switching transient. This section presents the effect of this nonideality on DAC output voltage settling in detail. The switches to V_{ref} (in

[7] Settling time normalized to time constant (tau) given by $tau = (R_{ref} + R_{gnd}) \times C_{DAC}/2$, C_{DAC}= 32C (in this example).

Fig. 3.16) are implemented using PMOS transistors and we assume that their resistance remains constant (to first order) during the DAC switching. Fig. 3.20 shows the simplified circuit schematic used for analysis in which R_{gnd} (in Fig. 3.18) is replaced by an NMOS transistor.

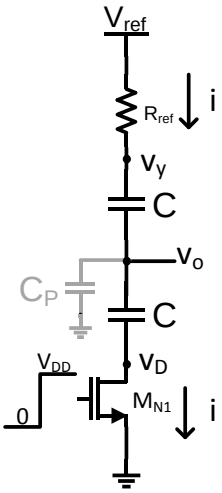


Fig. 3.20 Simplified circuit for analysis.

Assuming square law behavior for M_{N1} in Fig. 3.20, and neglecting parasitic capacitance C_P, v_D and v_O are related as (see Appendix B)

$$v_D^{\left(\frac{R_{ref}}{R_{gnd}}+1\right)}(2V_{OV}-v_D)^{\left(\frac{R_{ref}}{R_{gnd}}-1\right)} = \left\{V_{ref}^{\left(\frac{R_{ref}}{R_{gnd}}+1\right)}(2V_{OV}-V_{ref})^{\left(\frac{R_{ref}}{R_{gnd}}-1\right)}\right\}\exp\left(-\frac{2t}{R_{gnd}C}\right) \tag{3.2}$$

where $V_{OV} = V_{DD} - V_t$ and V_t is the threshold voltage of M_{N1} in Fig. 3.20.

For $\frac{R_{ref}}{R_{gnd}} = 1$, v_D has a closed form solution given by

$$v_D = V_{ref}\exp\left(-\frac{t}{R_{gnd}C}\right) \tag{3.3}$$

and therefore the output voltage v_O can be written as

$$v_O = v_i - \frac{1}{2}V_{ref} + \frac{v_D}{2}\left(1-\frac{R_{ref}}{R_{gnd}}\right) + \frac{R_{ref}}{R_{gnd}}\frac{v_D^2}{4V_{OV}} \tag{3.4}$$

From (3.4), we see that using an NMOS transistor for ground switches results in a decaying exponential settling response of the DAC output voltage (instead of an instantaneous step). Equations (3.2) and (3.4) can be numerically solved to calculate the settling times of the DAC output voltage as a function of R_{ref}/R_{gnd}, as shown in the next section.

C. MATLAB Simulations

For solving (3.2) numerically using MATLAB, the following values were assumed: $V_{DD} = V_{ref} = 1$ V, C = 128 fF (Total capacitance in the DAC array = 256 fF), V_{th}= 0.36V. The ratio of R_{ref}/R_{gnd} (variable m) was varied from 0.75 to 1.3. Fig. 3.21 shows the comparison of normalized settling times for 6, 8 and 10 bit settling of the DAC output voltage assuming 0.5 LSB accuracy. The settling times are normalized to the case when m=1 ($R_{ref}=R_{gnd}$). It can be seen that settling time reduces beyond the case of matched time constants (m=1). This is because the zero in the transfer function provides an overshoot, which further improves settling time if the overshoot magnitude is contained within the settling error bound. For 10 bit accuracy in settling, this extra improvement is much less compared to a 6 bit settling, as expected.

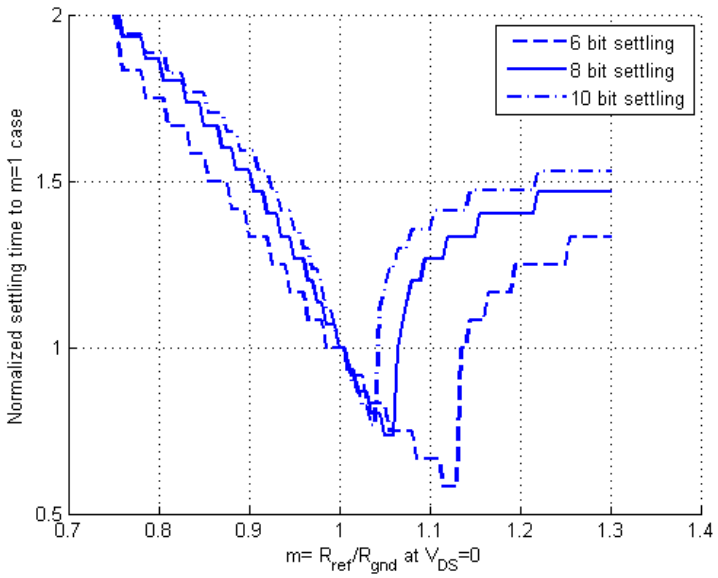


Fig. 3.21 Comparison of normalized settling times (MATLAB simulation) for DAC output voltage settling.

D. Limitations and Practical Applications

It is evident from the MATLAB simulations presented above that even with non-ideal switches, designing the switch resistances around $R_{ref}/R_{gnd} = 1$ help reduce the DAC settling time (Fig. 3.21). However, this result is based upon the analysis of Section 3.6 B, which neglects parasitic capacitance at the DAC output $v_O(t)$ (common top plate). Fig. 3.22 shows a Cadence simulation plot of the normalized settling time (8 bit settling) for the circuit of Fig. 3.20 with a parasitic capacitance $C_P = C/4$ at the output node. It is apparent that in the presence this parasitic capacitance the output settling time reduces almost monotonously with the increase in pull-down resistance (R_{gnd}). This is because the parasitic pole diminishes the effect of the zero in the transfer function, thereby resulting in smaller overshoots. Therefore, in the presence of a large parasitic capacitance at the DAC output, time constant matching technique does not provide the striking reductions in DAC settling time observed in Fig. 3.21. This prevented us from using time constant matching in our proof-of-concept prototypes A/D converters, which are discussed in detail Chapters 4 and 5. Chapter 6 will describe few ideas on how this technique can be potentially employed in practical SAR ADC designs to improve their performance.

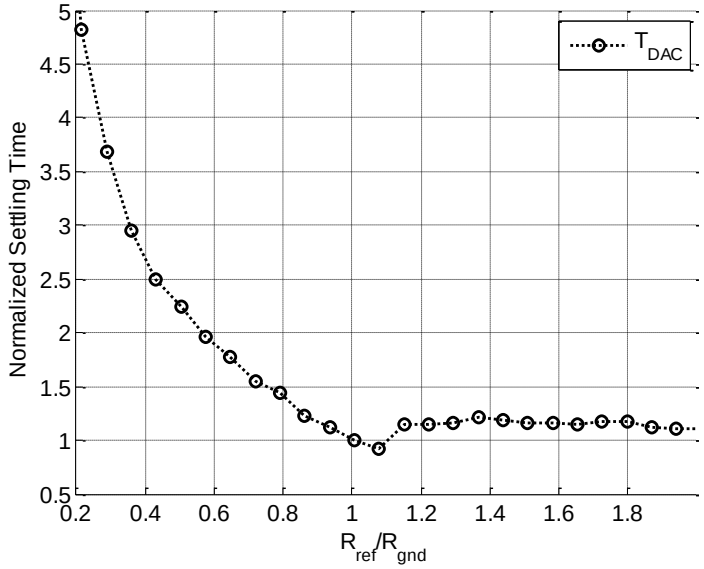


Fig. 3.22 Cadence simulation showing normalized DAC output settling time (to $R_{ref}/R_{gnd} = 1$ case) in presence of output parasitic capacitance ($C_P = C/4$) for the circuit of Fig. 3.20.

3.7. Summary

This chapter presented circuit design techniques to improve the conversion speed of SAR A/D converters. Asynchronous timing allocates more time for the critical decision during SAR conversion (comparator input < LSB) by using a self-triggered comparator. This also reduces the total time required for other non-critical decisions, which results in significant improvement in the overall conversion speed (compared to a synchronous SAR ADC). Moreover, use of asynchronous timing also obviates the need of an external fast SAR clock as the comparator control signal together with individual SAR sequencing clocks are generated on-chip using delay lines. Top plate sampling eliminates the MSB transition, thereby reducing the DAC capacitance by 50 %, 81% reduction in switching energy and an overall improvement in ADC conversion speed. SAR loop delay that comprises of comparator decision time, SAR logic delay and DAC settling time limits the speed of a SAR ADC. A joint optimization approach for the total SAR loop delay along with reducing each of these individual delays help further speed up the A/D conversion. Small reductions in SAR loop delay also result in significant total savings as it is multiplied by the number of SAR conversion cycles. A small comparator regeneration time constant reduces the comparator decision time, which results in a smaller total SAR loop delay. In addition, fast, accurate reset is also critical in the comparator, especially to avoid SNR degradation due to hysteresis. Lastly, we discussed time constant matching in the capacitive DAC. The key idea is to take advantage of pole-zero cancellation during DAC switching to speed up DAC settling time.

Chapter 4

Prototype Implementation— 8-bit, 450 MS/S SAR ADC

4.1. Introduction

The previous two chapters presented important design techniques and aspects for high-speed SAR A/D converters. Specifically, Chapter 2 discussed the mismatch characteristics of small single layer MOM capacitors, which are used to implement the unit elements in the capacitive DAC [12]. Small capacitors also help reduce the switching energy and DAC settling time, thereby improving ADC performance. Chapter 3 focused on circuit design techniques and circuits that enable high-speed SAR operation such as top-plate sampling [49], asynchronous processing [17], SAR loop delay optimization [55] and fast comparators. In this chapter, we present an 8-bit, single-channel, single-bit/cycle SAR ADC [55] that serves as a proof-of-concept for the evaluation of these techniques. The ADC uses 0.75 fF unit capacitors in the CDAC and was designed to advance the attainable throughput of the conventional SAR architecture while maintaining attractive power efficiency.

The chapter's organization is as follows. Section 4.2 describes the overall ADC architecture followed by detailed circuit implementations in Section 4.3. Measurements results are presented in Section 4.4 with a short summary in Section 4.5.

4.2. ADC Architecture

Fig. 4.1 shows the ADC block diagram along with its 7-bit binary weighted capacitive DAC, which acquires the input via top plate sampling [49]. This allows us to resolve the first bit without redistributing any charge, which saves energy and improves speed (see Chapter 3). The capacitor C_{DIV} attenuates the DAC signal and sets the converter's full-scale range to 0.7 V peak-differential. This choice is preferred over a rail-to-rail input range to maintain linear input sampling up to high frequencies. The DAC reference voltage V_{REF} is generated off-chip and is decoupled with an internal 500 pF gate oxide capacitor. The decoupling capacitance is sized such that it supplies the dynamic currents with a maximum transient glitch of 1/3 LSB. As a result, the external voltage supplies only the relatively small average reference current. The input tracking begins with the positive edge of the incoming clock and its length is set to approximately 0.3 ns (13.5% duty cycle) via an on-chip delay line. The delay line is sized such that its jitter does not deteriorate the overall performance. Once the input is acquired, the SAR loop runs asynchronously (see Chapter 3) until all bits are resolved. We also employ SAR loop delay optimization (minimize $T_{SAR}= T_C + T_L + T_{DAC}$), which was described in Chapter 3 to speed up the A/D conversion.

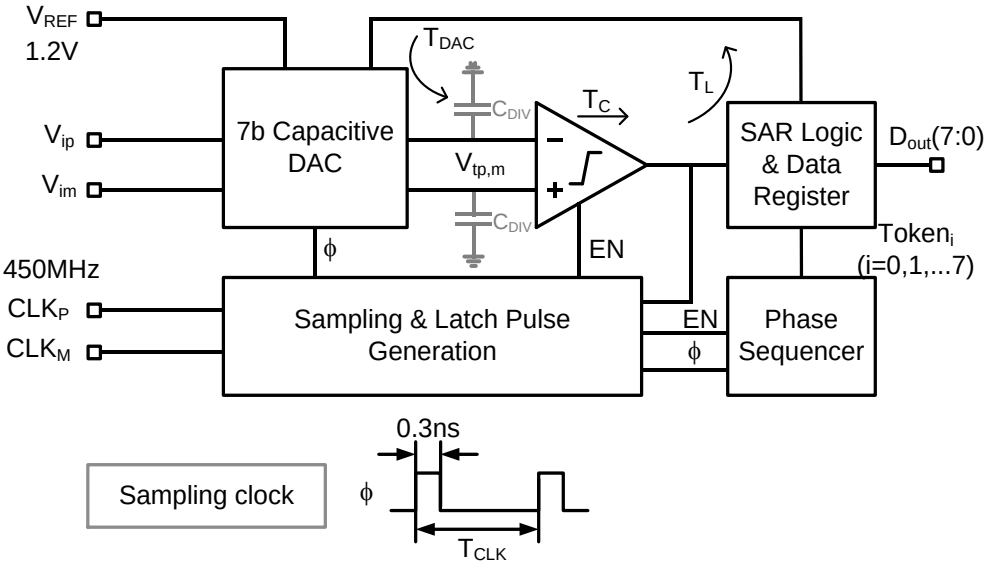


Fig. 4.1 ADC block diagram.

4.3. Circuit Implementation and Operation

A. Capacitive DAC

Using the original top plate sampling scheme of [49] requires a comparator with good common-mode (CM) rejection, since large CM jumps occur during charge redistribution. Capacitor splitting can be used to alleviate this issue [43]. The improved splitting used here achieves (nearly) symmetric switching and constant common mode. The MSB capacitance, which is usually formed by 64 unit elements, is split into 2x32 units that see opposite bottom plate voltages in the track phase (one set is charged against V_{REF}, the other against GND; see Fig. 4.2). This split is applied to all capacitances in the DAC, except for the LSB, which is minimum-size. As shown in Fig. 4.3 (using the MSB as an example), for every capacitance switching on the positive half of the circuit, there is an equal capacitance switching on the opposite side making the DAC transitions symmetric. The only exception occurs for the LSB transition, which is asymmetric but has almost no effect on the input common mode due to the inherently small step size.

Fig. 4.4 shows the layout of the capacitive DAC[8]. Single-layer MOM capacitor structure (discussed in Chapter 2) is used to implement the unit capacitor value of 0.75 fF. The capacitors are designed using metal 7 (M7), largely to facilitate easy layout. The parasitic capacitance from M7 to substrate is absorbed in C_{DIV} and the total input capacitance is approximately 160 fF.

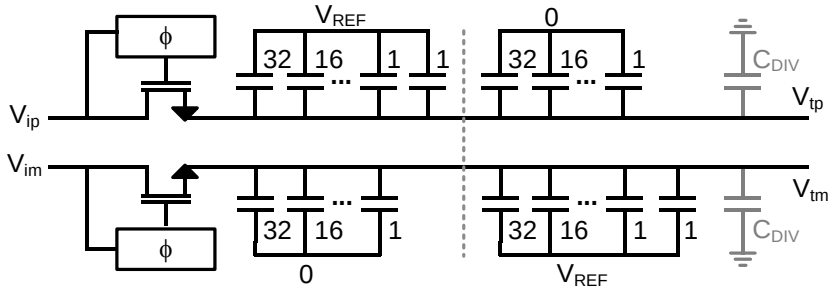


Fig. 4.2 DAC during sampling.

[8] Dummies (not shown in Fig. 4.4) were used on both sides to reduce the impact of process gradients (copper dishing).

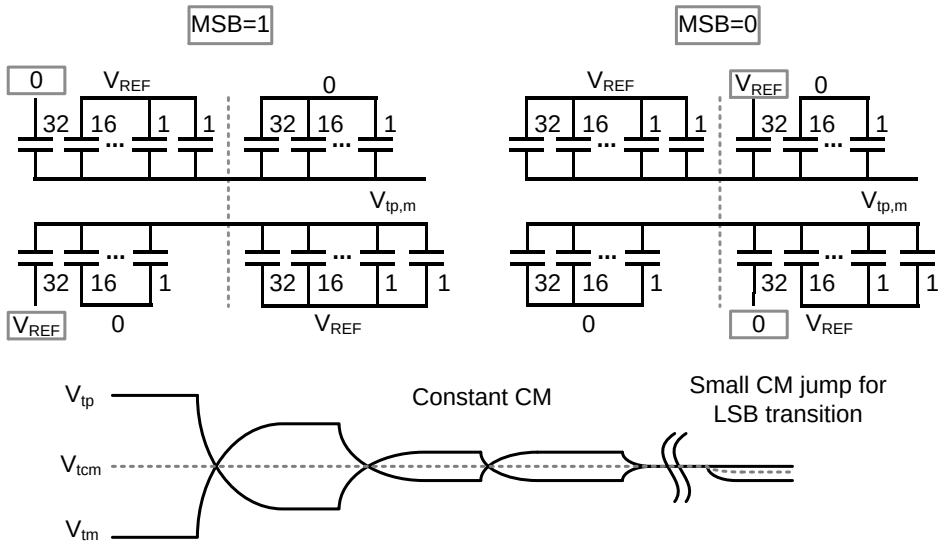


Fig. 4.3 DAC switching.

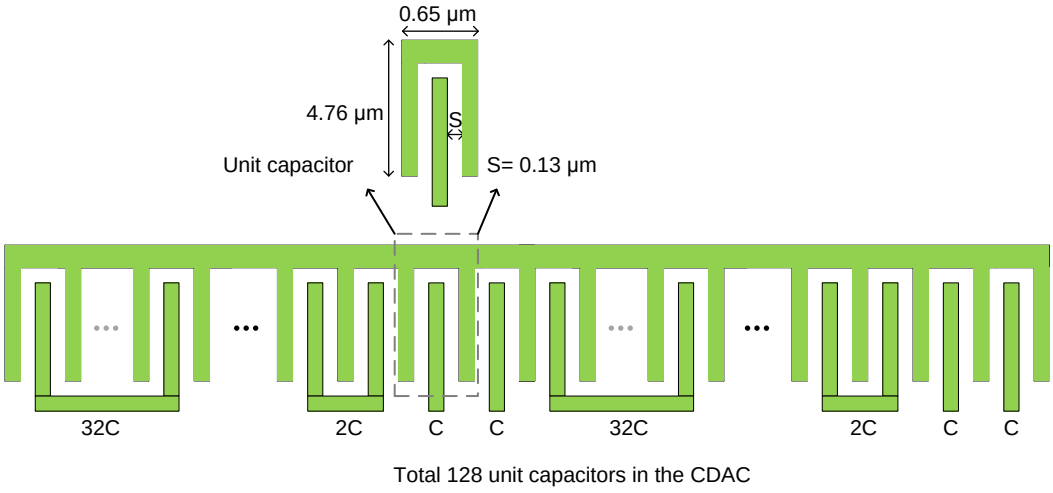


Fig. 4.4 Layout of the capacitive DAC with a unit capacitance of 0.75 fF (single ended structure shown for simplicity).

B. Comparator

Fig. 4.5 shows the comparator. It employs two pre-amplifiers to attenuate kick-back to the input and to optimize reset and regeneration speed. The first stage provides a voltage gain of 8 dB while the second acts as a near unity gain buffer (when EN = 0). The loads of this buffer perform the reset of the latch and obviate the need for explicit reset switches, which would add capacitance that slows the regeneration. On the other hand, accurate and fast reset is needed due to the high effective

clock rate of the loop (~4 GHz). Increasing the size of the PMOS load (W_P in Fig. 5) reduces the comparator reset time (T_R). However, it this also reduces the gain of the second preamp and increases the parasitic load at the latch's regenerative nodes. As a result, the comparator's regeneration time steadily increases with W_P and there exists an optimum that minimizes $T_C + T_R$ as shown in Fig. 4.6. With the described optimizations, the comparator achieves a regeneration time constant of approximately 6 ps (measured through post-layout simulations).

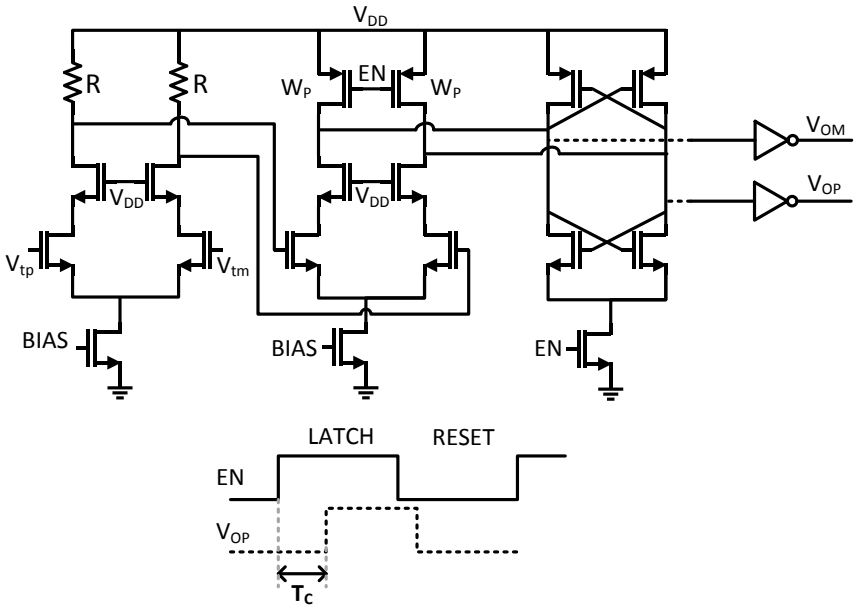


Fig. 4.5 Comparator schematic and timing.

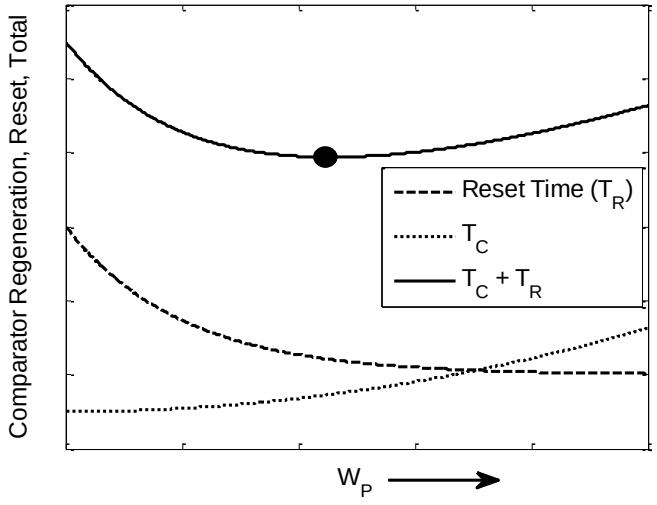


Fig. 4.6 Comparator optimization.

C. Asynchronous Pulse Generation

The comparator clock (EN) is generated asynchronously using a programmable delay line as shown in Fig. 4.7. The delay line is similar to the design of [62] and uses alternate inverters loaded with MOS capacitors to add programmability, which in the example of Fig. 4.7 is controlled by digital bits D_0 and D_1. The alternate unloaded inverters restore fast rise/fall times of the signal moving through the delay line. This is important to prevent low-pass filtering of a narrow input pulse while it propagates through the delay line.

The pulse generation circuit of Fig. 4.7 uses domino logic to speed up the operation. Its circuit operation begins with the sampling clock (ϕ) going high (sampling phase), which discharges the internal node X, thereby setting EN= 0 (comparator reset). This also pre-charges the domino node Y to V_{DD}, which in turn sets VALID= 0, thereby setting the domino logic for evaluation.

At the end of sampling phase (ϕ= 0), node X is charged to V_{DD} via transistor M_{P1}. This in turn switches the EN signal to logic high that starts comparator regeneration (see Fig. 4.5). At the end of the comparator's decision, one of its outputs (V_{OP} or V_{OM}) is at logic high (e.g. V_{OP}= 1 in Fig. 4.7). This ultimately discharges node Y and sets VALID= 1. A logic high VALID signal again discharges node X, which as before sets EN= 0, thereby initiating comparator's reset as well as pre-charging node Y to V_{DD}. At this point, the circuit's internal nodes are back to their original state that was present at the end of sampling phase (except that ϕ= 0).

The VALID signal is inverted and delayed using the delay line (VALID' in Fig. 4.7) and this signal controls the pull-up switch M_{P2}. When VALID'= 0, node X is charged to V_{DD}, which in turn sets EN= 1, thereby enabling the comparator to regenerate once more. This process continues until the onset of next sampling phase (ϕ= 1) and a detailed timing diagram depicting the above is presented in Fig. 4.7. Moreover, this EN signal is used to generate individual SAR clock phases (Tokens in Fig. 4.1), which is described next.

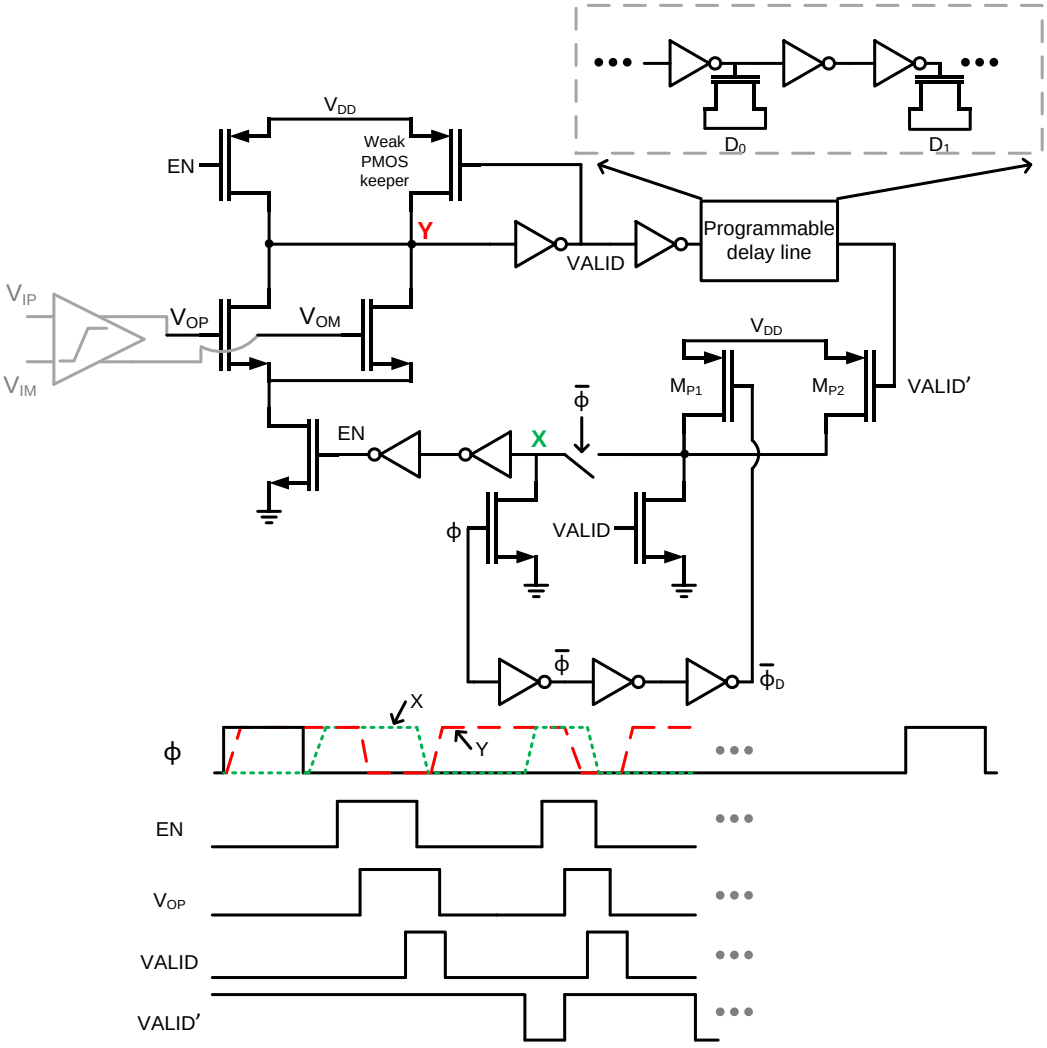


Fig. 4.7 Circuit schematic of asynchronous pulse generation and timing diagram.

D. SAR Clock Generation

The required eight clock edges are generated asynchronously during the SAR operation in order to capture the output bits and also to time the feedback to the DAC. Domino logic is used with its evaluation triggered by the comparator enable signal EN (see Fig. 4.8), so that the clock generation path stays out of the critical SAR loop delay (and does not limit the conversion speed). Fig. 4.9 shows a timing diagram depicting all the SAR phases (Tokens) along with the comparator control signal (EN).

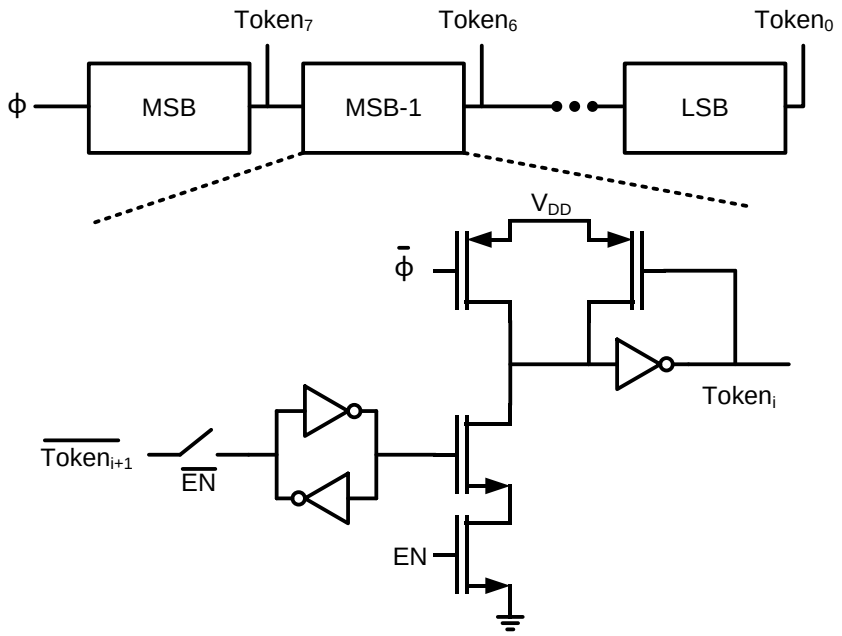


Fig. 4.8 SAR clock generation.

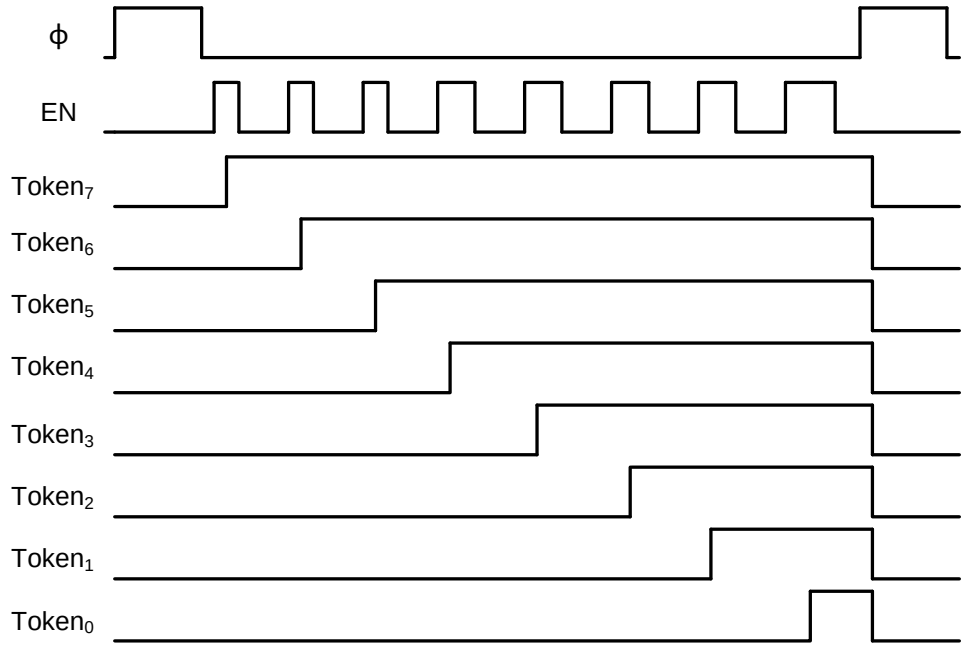


Fig. 4.9 Timing diagram showing the sampling clock (ϕ), comparator control signal (EN) and different SAR phases ($Token_7$…$Token_0$).

E. Data Capture Latch

During the conversion phase, the outputs of the comparator are captured by the data capture latch, which must perform the following two tasks: (1) Store the comparator decision (digital output) until the latch is reset for the next conversion cycle. (2) Feed back the comparator decision as quickly as possible to the capacitive DAC. This delay is part of the SAR loop delay (see Chapter 3) and minimizing it is critical to achieve high conversion speed. In our design, we employ a custom designed latch (modified from [48]) for each of the 8 output bits (see Fig. 4.10). Transistors $M_{1A,B}$ are added and a delay is incorporated between the start of the sampling phase ($\phi \rightarrow 1$) and the latch reset phase ($\overline{RST} \rightarrow 0$) shown as 'Bit Out' time in Fig. 7. This allows us to store the latch state (D) and buffer it off-chip during sampling (without eating into the SAR conversion time) together with resetting both feedback nodes (FBP, FBM) to ground.

At the end of the sampling and latch reset ($\overline{RST} \rightarrow 1$) phase, the output nodes D/D' are pre-charged to V_{DD}, the comparator outputs $V_{OP,M}$ are reset to ground and the latch is ready for evaluation. This phase begins with the rising edge of $Token_i$, which enables the PMOS cross-coupled pair to resolve and store the corresponding comparator decision at nodes D/D'. This result is also fed back to the DAC via FBP and FBM. The PMOS cross-coupled devices are sized just large enough to latch nodes D/D' in the available time. This allows lower power dissipation and fast latch reset, but also results in smaller gain, which may cause incorrect DAC feedback if $Token_i$ is asserted during the comparator decision time. In this design, we added an NMOS cross-coupled pair ($M_{2A,B}$) across FBP/FBM to provide additional gain, thereby ensuring fast and correct feedback to the DAC. The clock to feedback delay ($Token_i$ to FBP/FBM) of the latch is 22 ps (measured through post layout simulation).

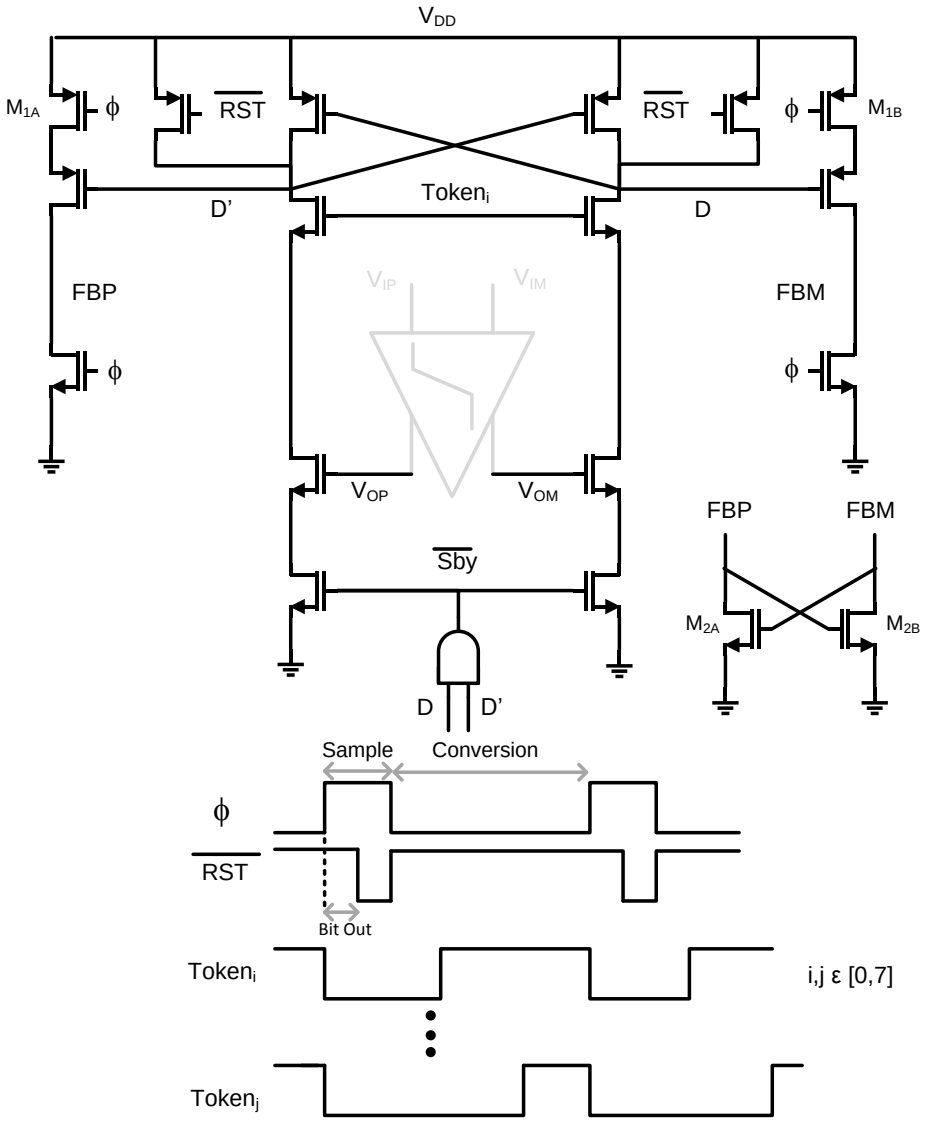


Fig. 4.10 Data capture latch.

F. ADC Front End

Fig. 4.11 shows a simplified schematic of the ADC frontend. During sampling, the input is sampled directly on the capacitive DAC (represented here by C_S) with a tracking duration of 300 ps, which is essential to allow sufficient time for A/D conversion. The presence of input bond wires (see Fig. 4.9) makes sampling especially challenging because of the required relaxation time for the bond wire inductance. This issue is partly alleviated by using an explicit on-chip MOM capacitor (C_F in Fig. 4.11), which basically forms an LC lowpass filter with the bond wire

inductor and supplies the initial transient charge to the sampling capacitor at the onset of sampling phase. The value of C_F is chosen such that it does not attenuate the input signal amplitude in the frequencies of interest, but is large enough to provide sufficient transient current (depending on the size of C_S and target SFDR) at the beginning of sampling phase.

The sampling switches $S_{A, B}$ are bootstrapped to ensure small on-resistance and signal independent charge injection (to first order). The bootstrapping circuit is shown in Fig. 4.12, which is based upon the design of [63]. The additional pull up switch (M_P) is activated by a short pulse (~100 ps), which helps fast charging of the gate capacitance, thereby improving the speed of the overall T/H circuit [20]. Post layout simulations show an SFDR of over 65 dB at 200 MHz input frequency for the passive T/H circuit of Fig. 4.12, which is sufficient for our target 8 bit ADC.

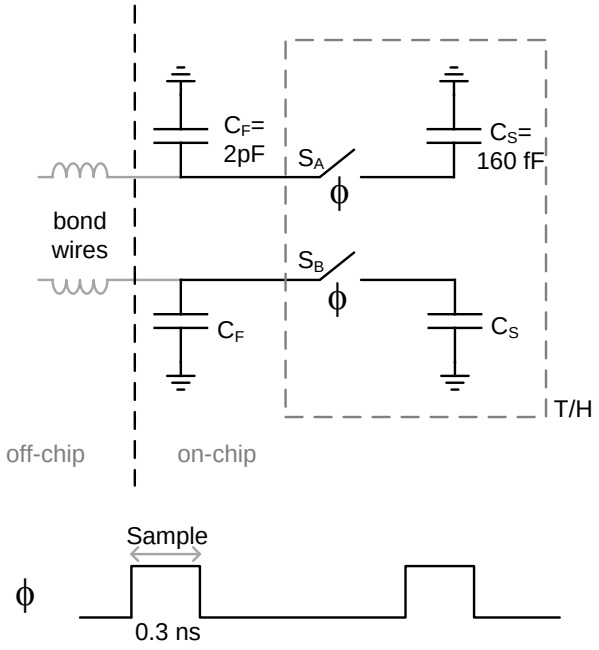


Fig. 4.11 Simplified schematic of the ADC frontend.

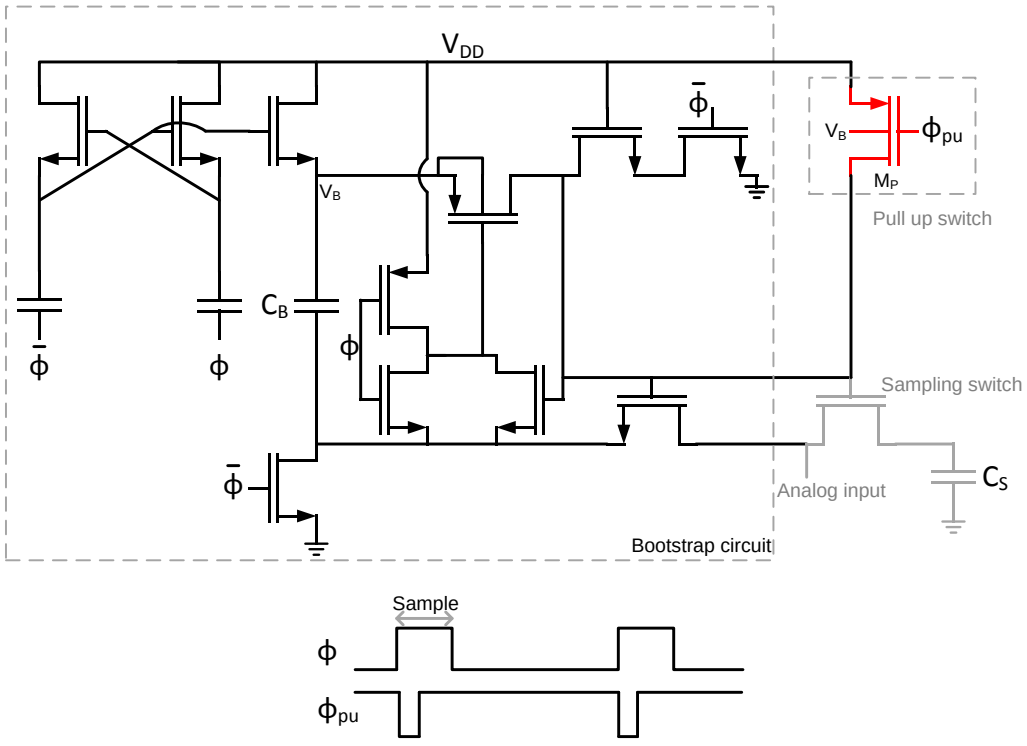


Fig. 4.12 Bootstrap circuit with pull up switch M_P.

4.4. Experimental Results

A. Measurement Setup

The prototype ADC is fabricated in the TSMC 1P9M 65-nm GP CMOS process with a core chip area of 0.035mm^2. The die micrograph with the layout of the ADC core is shown in Fig. 4.13. The fabricated chip is packaged in a 48 pin QFN and is mounted on a custom designed PCB board. This PCB board interfaces with a TSW 1200, an ADC data capture card from Texas Instruments [64] as shown in Fig. 4.14. Using this measurement setup, the output data is captured at full speed and fed to a PC for performance evaluation.

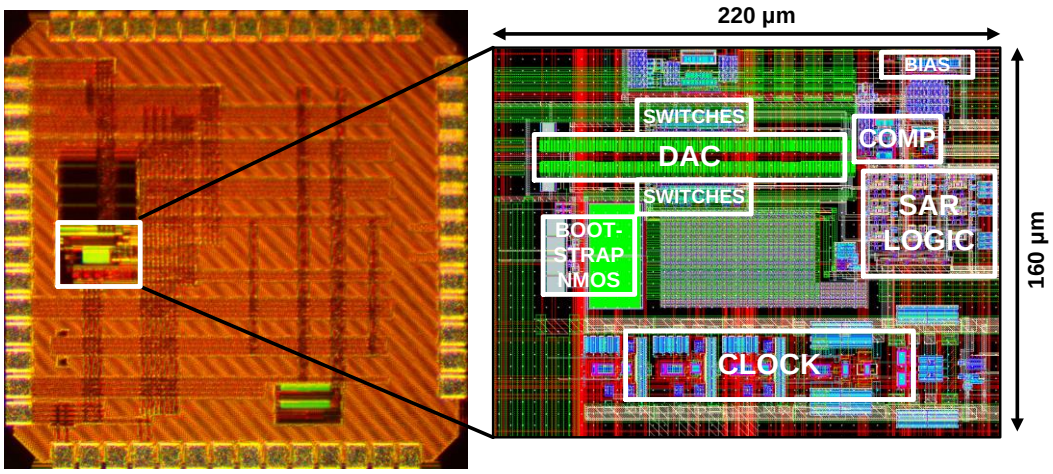


Fig. 4.13 Die photo and layout of the ADC core.

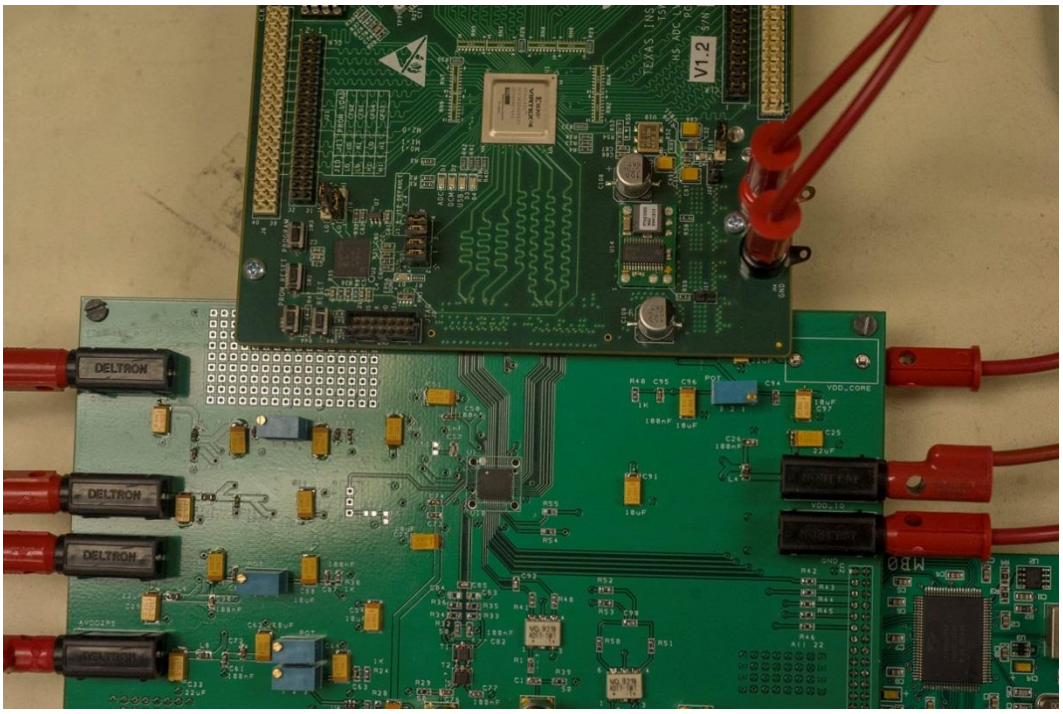


Fig. 4.14 ADC test setup showing the custom designed PCB board (bottom) and TSW 1200, a capture board from Texas Instruments (top).

B. ADC Measurements

Fig. 4.15, Fig. 4.16, and Fig. 4.17 summarize the measurement results obtained at f_s = 450 MHz. The DNL and INL are within ±1 LSB, which indicates good matching of the small unit capacitors. The measured SNDR is nearly flat with input frequency (f_{in}) and the ADC achieves SNDR = 47.3 dB at Nyquist. It consumes 5.4 mA (including bias generation and external reference current but excluding I/O) from a supply voltage of 1.2 V, with a dynamic contribution of approximately 57%. This translates into a Walden FOM ($P/(f_s 2^{ENOB})$) of 76.1 fJ/conversion-step (at Nyquist). To our knowledge, this is the fastest non-interleaved SAR ADC containing a single comparator reported to date. It achieves approximately the same ratio of sampling rate to process f_T as [45], without the need for a second comparator and offset-calibration. Fig. 4.18 shows a comparison of input bandwidth vs. SNDR among SAR ADCs designed in 90 nm, 65 nm and 40 nm processes, which highlights the high input bandwidth (and conversion speed) of our SAR ADC. Table 4.1 compares our prototype ADC to the current state-of-the-art and an FOM_W comparison is shown in Fig. 4.1 [11].

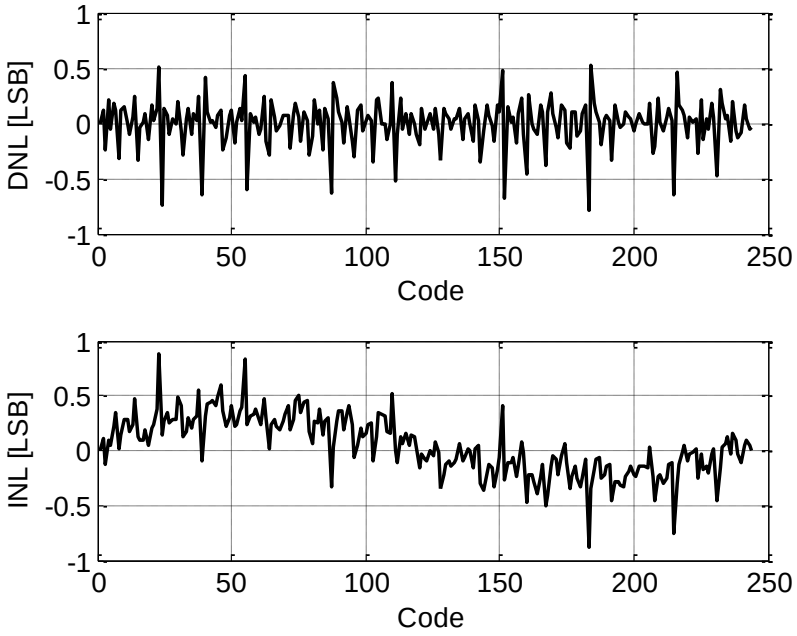


Fig. 4.15 Measured DNL and INL.

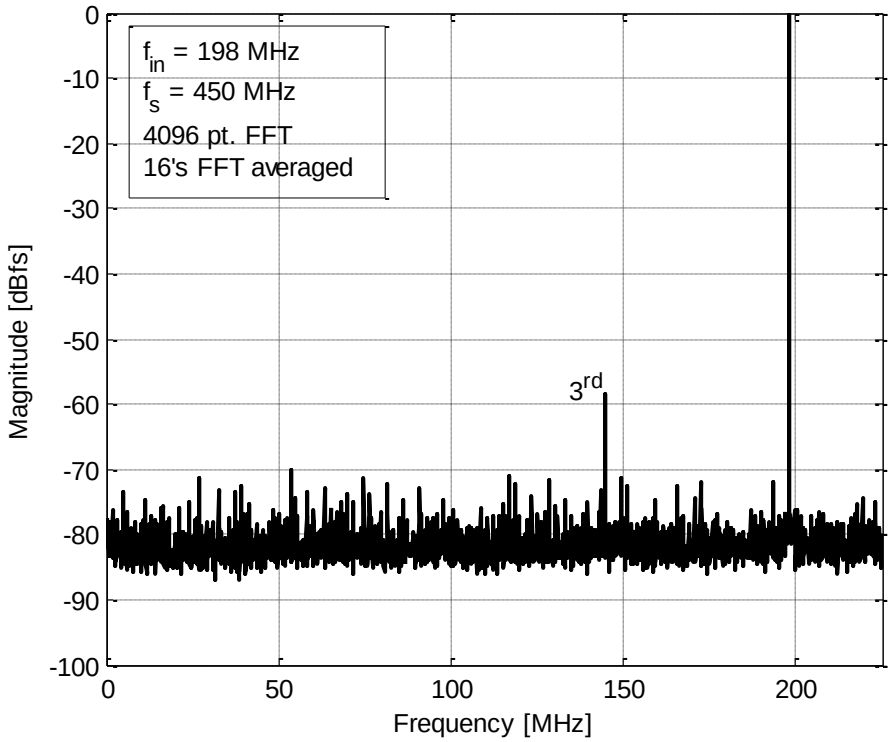


Fig. 4.16 Measured ADC output spectrum.

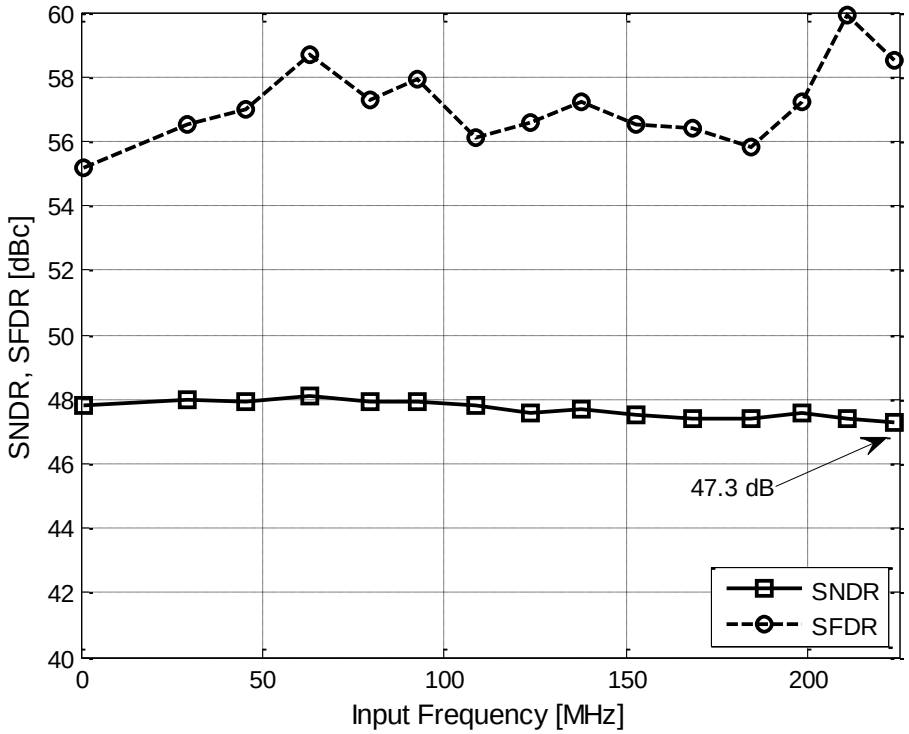


Fig. 4.17 SNDR and SFDR vs. input frequency.

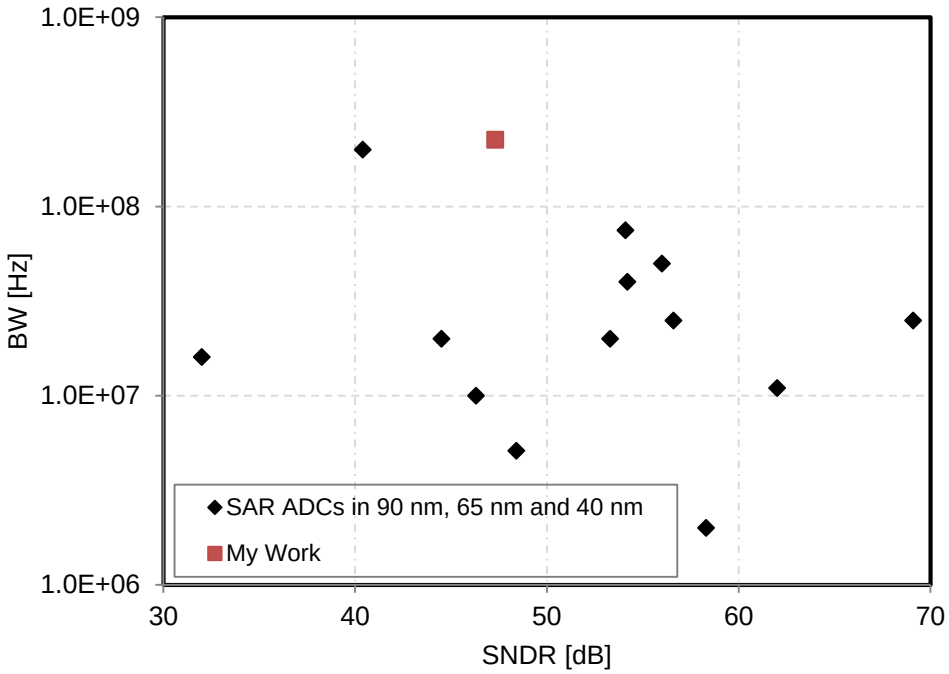


Fig. 4.18 Plot of ADC bandwidth vs. SNDR.

Table 4.1 ADC performance summary and comparison

	[44]	[18]	[46]	[45]	This Work	
Architecture	2b/cycle	1b/cycle	2b/cycle	1b/cycle (2 cmp)	1b/cycle (1 cmp)	
Technology [nm]	65	65	28	32	65	
Supply voltage [V]	1.2	1.2	1	1	1	1.2
Resolution [bits]	8	10	8	8	8	8
fs [MS/s]	400	100	750	1000	400	450
SNDR (@Nyq.) [dB]	40.4	56	43.3	37.8	47.4	47.3
FOM_W [fJ/conv-step]	116.9	21.9	50.2	32.9	57	76

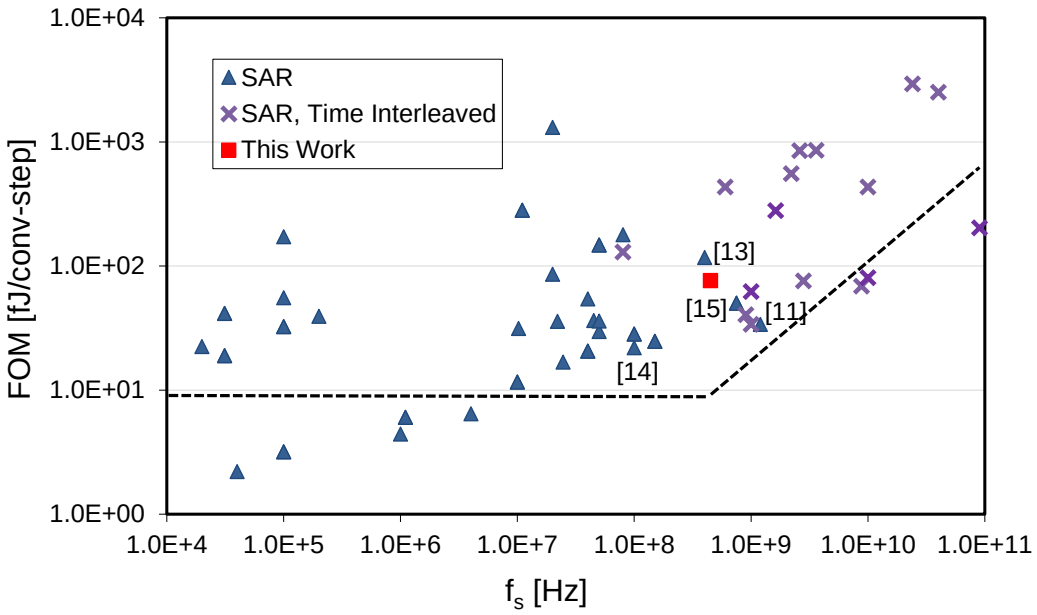


Fig. 4.19 Plot of Walden FOM vs. ADC conversion frequency.

4.5. Summary

The design and measurement of an 8 bit, 450 MS/s, single-channel, single-bit/cycle SAR ADC in 65 nm CMOS was presented in this chapter. The A/D converter combines a variety of design techniques: (1) judicious optimization of DAC settling and logic delay with asynchronous timing, (2) a comparator designed for the optimum tradeoff between its regeneration and reset delays, and (3) a symmetrically switched DAC using top-plate sampling and small unit capacitors (0.75 fF). Measurement results show good performance across the entire first Nyquist zone with an SNDR of 47 .3 dB at Nyquist input frequency (225 MHz). A potential application for this converter is within a time-interleaved array, where the combination of high-speed (leading to low channel count), low complexity (minimum number of offset-prone comparators) and small input capacitance (~160 fF) is highly valued.

Chapter 5

Prototype Implementation— 68.3 dB SNDR, 160 MS/s Pipelined-SAR ADC

5.1. Introduction

Chapter 4 presented a proof-of-concept prototype of an 8-bit, 450 MS/s SAR ADC that employs sub-femto Farad unit capacitors in the CDAC. Merits and drawbacks of pipelined-SAR A/D converters [21] were described in Chapter 3 and a two-stage pipelined-SAR A/D converter with two switched capacitor D/A converters (CDACs) in the frontend was proposed [65]. In this ADC architecture, one uses minimum size capacitors to enable fast and low-energy SAR iterations, and the second DAC is sized for low-noise residue generation. In this chapter, we present a 68.3 dB SNDR, 160 MS/s pipelined-SAR ADC that serves as a proof of concept of the two-CDAC architecture [65]. The ADC employs a custom-designed dynamic latch to speed up the SAR logic for the specific case of bottom plate sampling. Moreover, residue amplification is performed using an open-loop gain stage with incomplete settling, which reduces power dissipation and also helps improve the conversion speed.

This chapter is organized as follows. Section 5.2 discusses the ADC architecture followed by the implementation details in Section 5.3. ADC measurement results are presented in Section 5.4, which is followed by a brief summary in Section 5.5.

5.2. ADC Architecture

The ADC's two-stage architecture, which resembles a two-CDAC pipelined-SAR structure (described in Chapter 3), is shown in Fig. 5.1. The first stage employs two 6-bit switched-capacitor DACs (DAC1 and DAC2). An open-loop residue amplifier with a gain of approximately 16 is used between the first and second stage, which is an 8-bit SAR ADC similar to [55] and with half the full-scale range of the first stage. This configuration results in 13-bit quantization[9] with 1 bit of redundancy that helps absorb certain errors in the first stage (e.g., the noise of DAC1 and Comp1). Both the frontend and backend SAR ADCs employ asynchronous timing and their sampling clocks ($\phi_{1,2}$), as well as the internal SAR phases ($Token_i$ in Fig. 5.1), are generated using on-chip delay lines (similar to Chapter 4, Section 4.4 C).

The design uses three external reference voltages V_{refp}, V_{refn} and V_{ref2}, which are set to 0.65 V, 0 V and 0.65 V, respectively. The resulting ADC full-scale range is 1.3 Vpp-diff, which is suitable for SoC deployment with on-chip, low-voltage driver circuits [22]. This is in contrast to [21] and [66], which use rail-to-rail inputs. In order to ease the requirements on the external references, we employ on-chip decoupling with thick gate oxide capacitors (2 nF for the frontend and 250 pF for the backend). These decoupling capacitances supply the dynamic currents, so as to maintain a maximum transient glitch of less than 0.5 LSB. As a result, the external reference voltages supply only the relatively small average reference current.

[9] See Chapter 3, Section 3.5

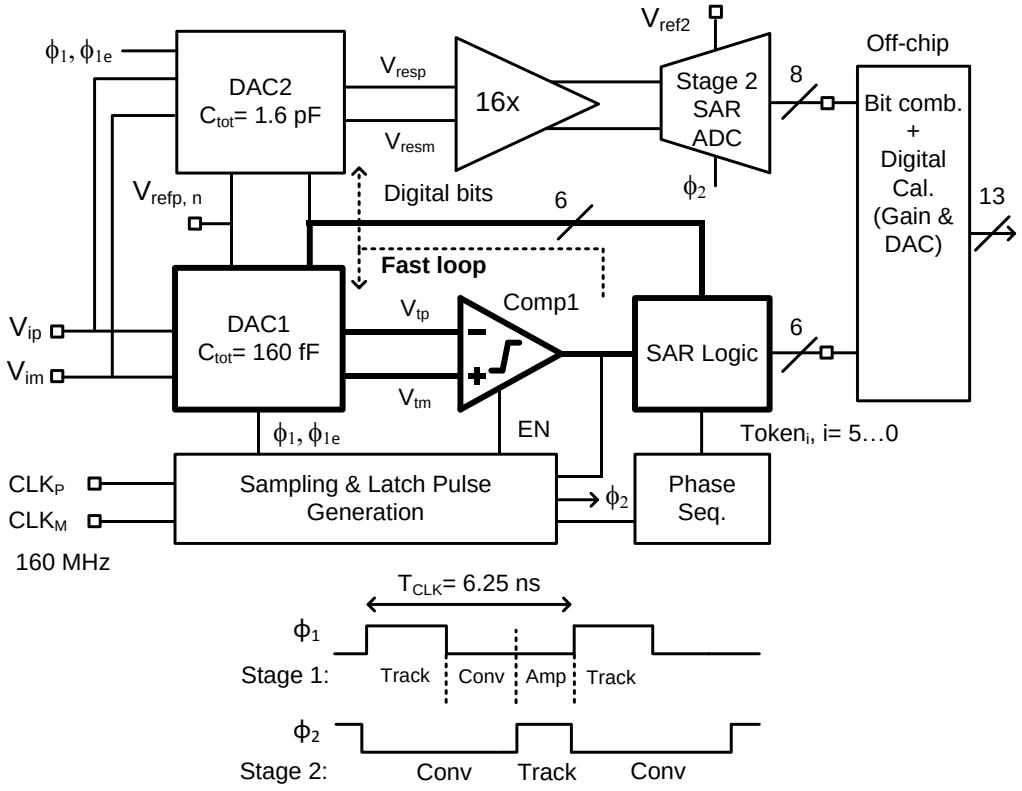


Fig. 5.1 ADC block diagram.

5.3. Circuit Implementation and Operation

A. ADC Frontend

The key advantage of a two-CDAC pipelined SAR architecture is that it decouples the noise-limited residue generation path from the high-speed SAR operation, thereby improving the conversion speed (see Chapter 3, Section 3.5).

Fig. 5.2 shows the ADC frontend in the sampling phase (actual implementation is fully differential). During ϕ_1, the input is simultaneously tracked on both DAC1 and DAC2 and acquired via bottom-plate sampling. The unit capacitors and switch sizes in the two DACs are scaled by the same factor to minimize tracking errors, which may eat into the redundancy budget. The residual errors are absorbed by the redundancy similar to others errors in the stage-1 ADC (e.g., offset and noise). Af-

ter sampling, the six front-end bits are determined within 2 ns using a fast asynchronous SAR loop around DAC1, with a total capacitance of only 160 fF. Due to the small capacitances being switched, the required energy is also low. The resolved bits are subsequently loaded into DAC2, which generates the low-noise residue that is passed to the second stage via the residue amplifier. The total DAC2 capacitance is set to 1.64 pF per kT/C sampling noise requirements. Since DAC2 is not switched at the SAR speed, a relatively long time is available for settling to the required precision, and the bandwidth requirements on $V_{refp,n}$ are also reduced. Furthermore, no energy is wasted on bit trials with large, noise-limited capacitances.

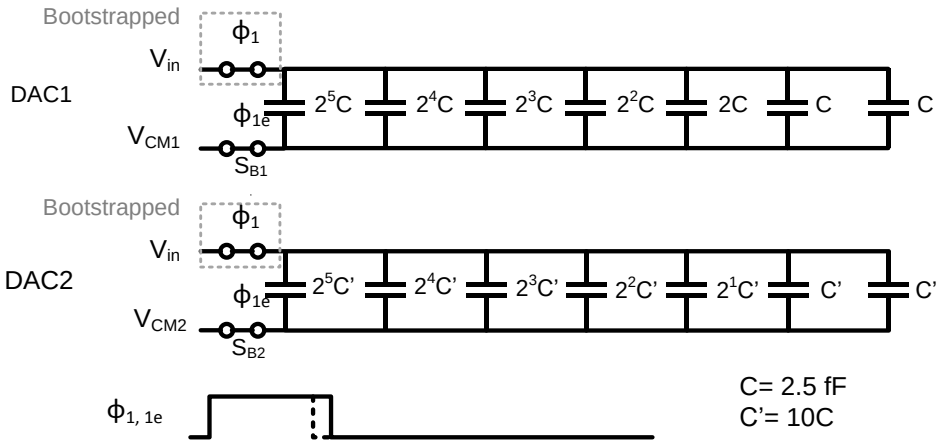


Fig. 5.2 DAC1 and DAC2 during sampling.

B. Design and Layout of CDACs

DAC1 and DAC2 (see Fig. 5.2) are implemented using single-metal MOM capacitors (Chapter 2) as unit elements. Fig. 5.3 shows the layout of DAC1. 64 unit capacitors (2.5 fF each) are tiled next to each other and connected in a particular fashion to implement a 6-bit binary weighted capacitive DAC.

The design of DAC2 is identical to that of DAC1 except that the unit capacitance of 25.4 fF (10 times that of DAC1) is implemented using a parallel combination of two 12.7 fF capacitors (see Fig. 5.4). This reduces the total series resistance

associated with the capacitance, which otherwise may slow down its charging/discharging characteristics. Both of the CDACs use metal 7 (M7) to implement the single-metal MOM capacitors for ease of layout and routing.

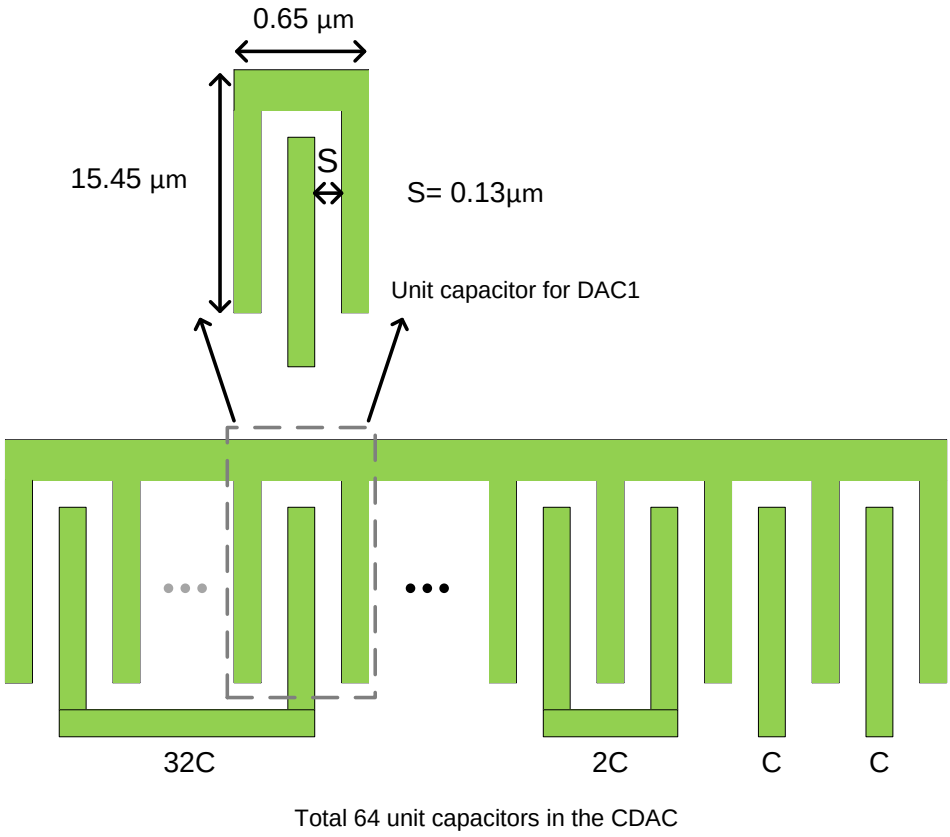


Fig. 5.3 Layout of DAC1.

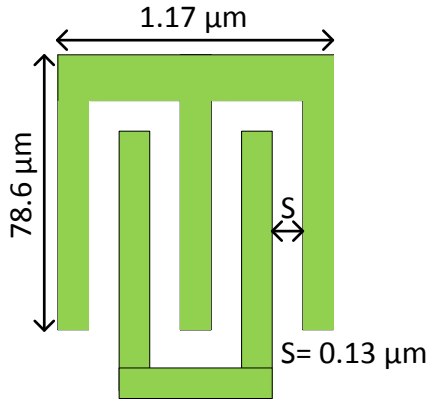


Fig. 5.4 Unit capacitor used in DAC2

C. Stage-1 Comparator

Fig. 5.5 shows the comparator schematic. Its design is based upon the optimizations presented in Chapter 4, Section 4.3 B, except that the input is a PMOS device, which allows us to choose a comparator input common mode of 0.4 V. This facilitates the realization of bottom plate sampling switches ($S_{B1,2}$ in Fig. 5.2) via NMOS devices, without the need for bootstrapping. This is an essential requirement for achieving a small fall time for the ϕ_{1e} clock signal (see Fig. 5.2), which ensures low jitter in the sampling instant. Moreover, the cascode devices $M_{N1,2}$ can now be controlled by the $\overline{EN}$ signal (instead of V_{DD}) as shown in Fig. 5.5. This shuts off the second stage during comparator regeneration, thereby improving the output signal swing as well as reducing power dissipation.

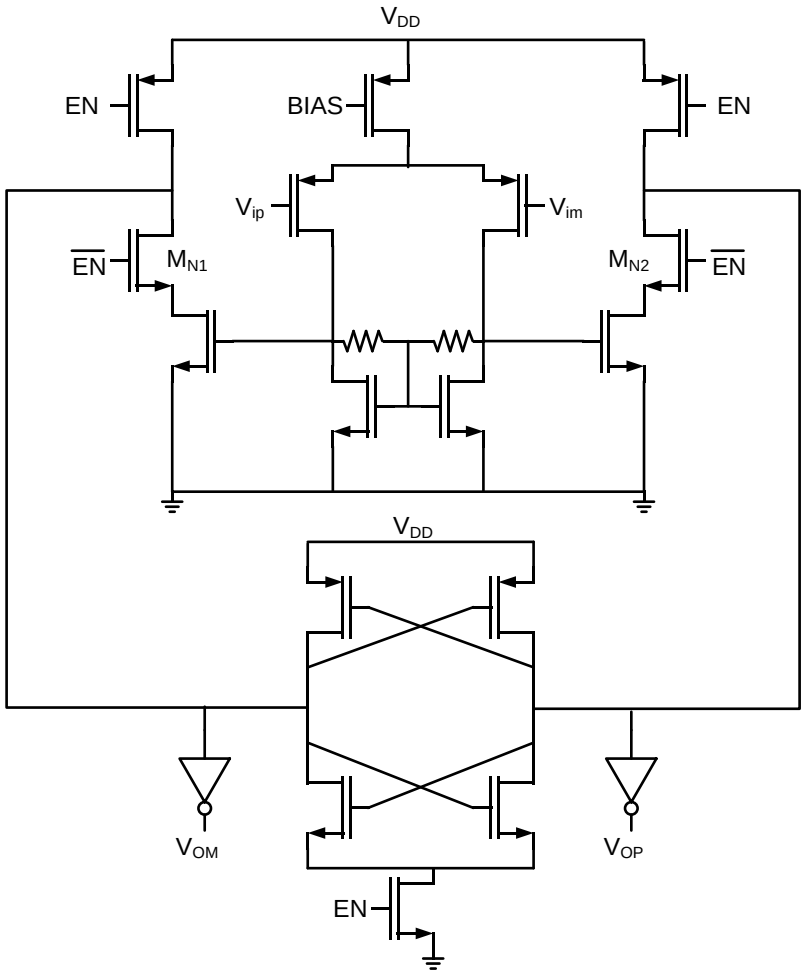


Fig. 5.5 Comparator schematic.

D. Stage 1 SAR Loop

Fig. 5.6 shows the stage 1 SAR loop with DAC1 in more detail (the actual implementation is fully differential). The SAR cycle for the i^{th} bit begins by charging the corresponding capacitor to V_{refp}. If the subsequent comparator decision is high (D_i= 1), the SAR operation moves on to the next bit. If the comparator decision is logic low (D_i= 0), the capacitor's reference connection must be flipped to V_{refn}. In this event, the SAR logic must ensure that the capacitor is first disconnected from V_{refp} (break) before it is connected to V_{refn} (make) in order to avoid a reference crowbar current. To achieve this timing reliably at high speed (~4 GHz), we designed a custom data capture latch, as described next.

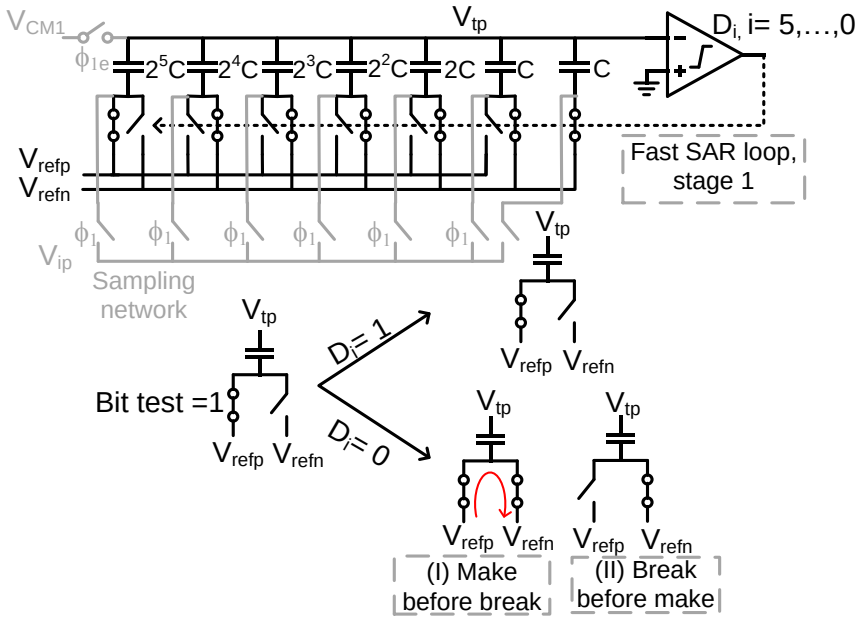


Fig. 5.6 Stage 1 SAR loop operation using DAC1 (sampling network is shown in grey).

E. Dynamic Latch

The employed latch is based on the work of [48], and modified for bottom plate sampling, while maintaining its key advantages (high speed, low power). Six of the latches shown in Fig. 5.7 are used in stage 1 and individually activated by their respective tokens ($Token_5$ for the MSB and $Token_0$ for the LSB). The circuit operation can be divided into three phases: reset, precharge (bit test) and latch.

During ϕ_1 (reset), D_i and $\overline{D_i}$ are both connected to V_{DD}, which erases the previous state of the latch. In addition, nodes FBP and FBM (control signals for DAC1 switches) are connected to ground as required per DAC switching logic. This is depicted in Fig. 5.8.

In the precharge phase, nodes FBP and FBM are set to '1' and '0', respectively, for the bit test. This is done by generating a precharge signal using a XOR gate that operates on $Token_{i+1}$ and $Token_i$ for the i^{th} latch as shown in Fig. 5.9. The subsequent comparator decision is latched via the cross coupled PMOS devices when $Token_i$ is asserted (storing ADC output bit). This is the latch phase of the dynamic data capture latch, which is depicted in Fig. 5.10. In case the comparator decides low, the 'break before make' timing described above is ensured through the highlighted feed-forward path in Fig. 5.10. Transistors M_{1A} and M_{1B} pull down the control signal FBP (thus breaking the connection) before the control signal FBM is charged to V_{DD}. Post layout simulations of the dynamic latch indicate a $Token_i$ to FBP/FBM delay of 25 ps (for comparison, the FO4 inverter delay in our process is about 21 ps).

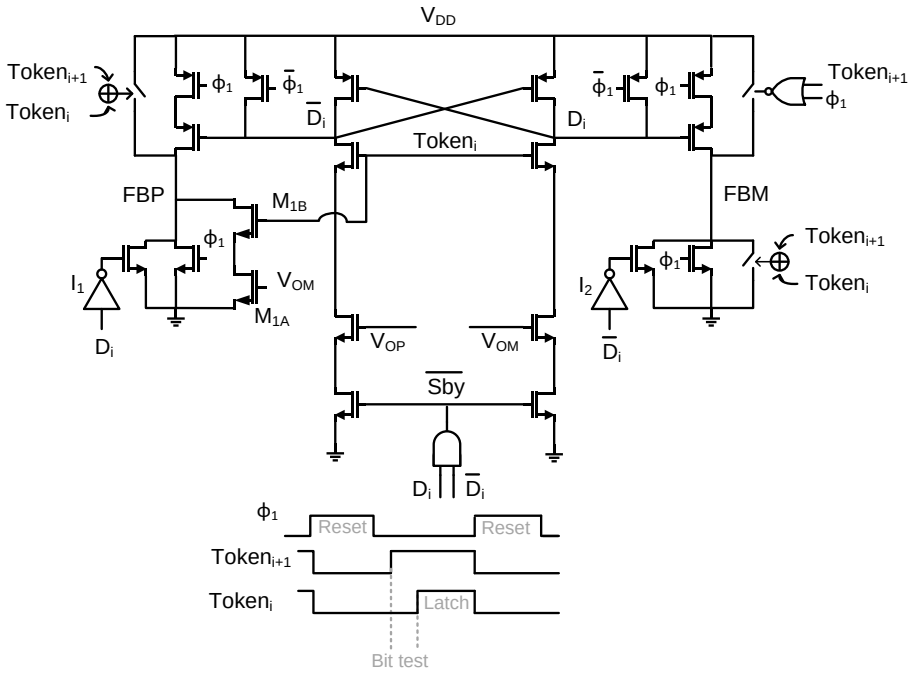
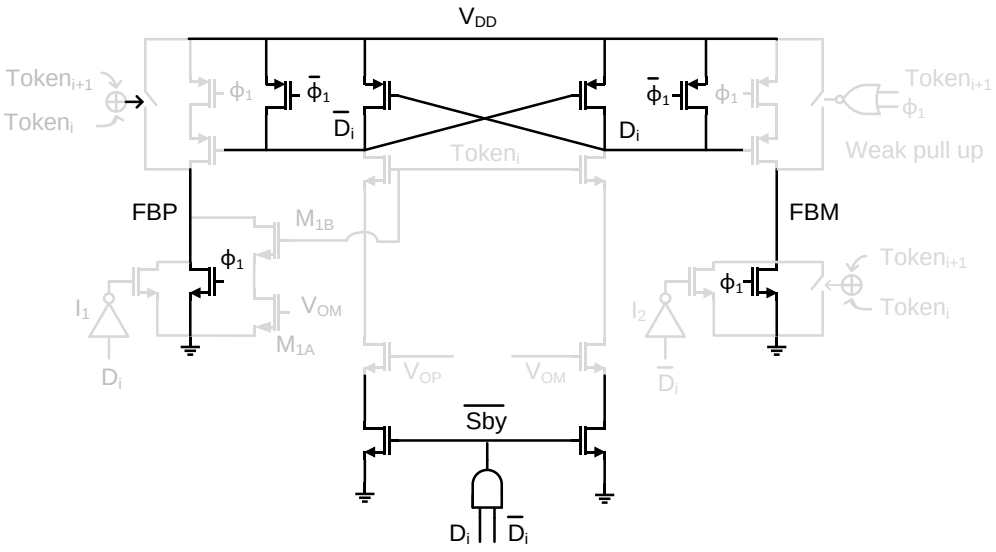
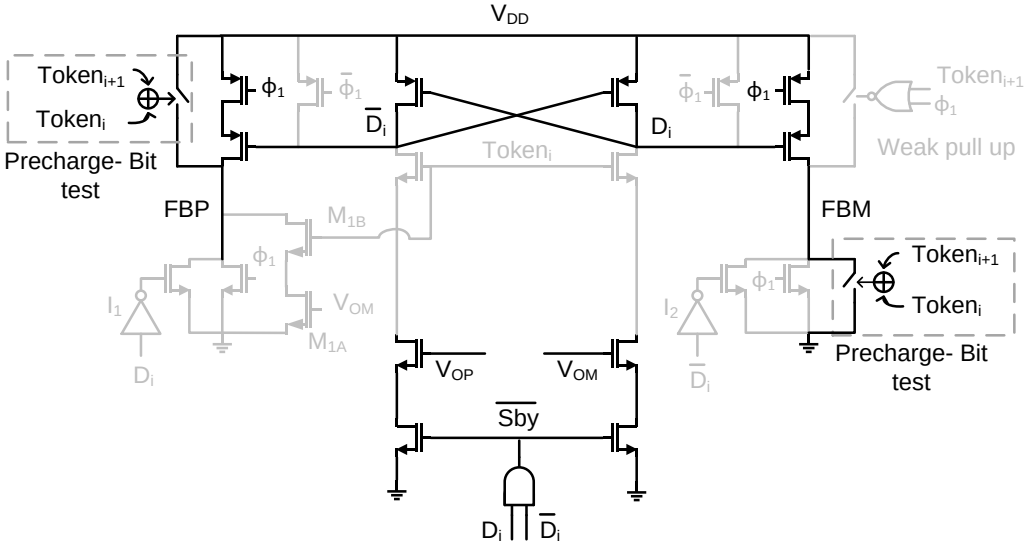


Fig. 5.7 Complete circuit schematic of the dynamic data capture latch.



Reset phase: $\phi_1 = V_{DD}$, $Token_{i+1} = 0$, $Token_i = 0$

Fig. 5.8 Dynamic data capture latch during reset.



Precharge (bit test): $\phi_1 = 0$, $Token_{i+1} = V_{DD}$, $Token_i = 0$

Fig. 5.9 Dynamic data capture latch during bit-test operation.

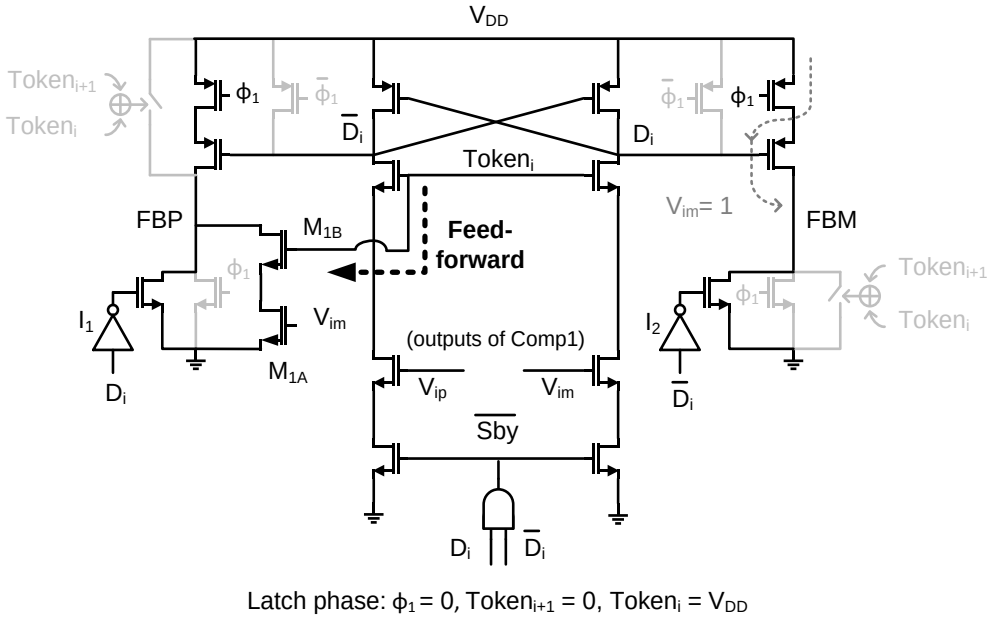


Fig. 5.10 Dynamic data capture latch during latch phase.

F. Residue Generation

Fig. 5.11 provides details on the residue voltage generation (the actual circuit is fully differential), which involves the bits generated by the stage 1 SAR loop. At the beginning of the stage 1 SAR conversion, the capacitors in DAC2 are left floating. At the end of the third conversion cycle ($Token_3$ goes high), the two MSBs (D_5 and D_4) are loaded together into DAC2. Similarly, the two ISBs (D_3 and D_2) are loaded at the end of the fifth conversion cycle ($Token_1$ goes high), while the LSBs D_1 and D_0 are loaded immediately after they become available. This staggered approach of loading the bits into DAC2 lengthens the available settling time for the large MSB capacitors and allows us to connect the residue amplifier to stage 2 early, which relaxes its settling time requirement and thus saves power. As shown at the bottom of Fig. 5.11, the MSBs of DAC2 and the residue amplifier can settle over multiple cycles of DAC1, which again highlights the advantage of the proposed architecture.

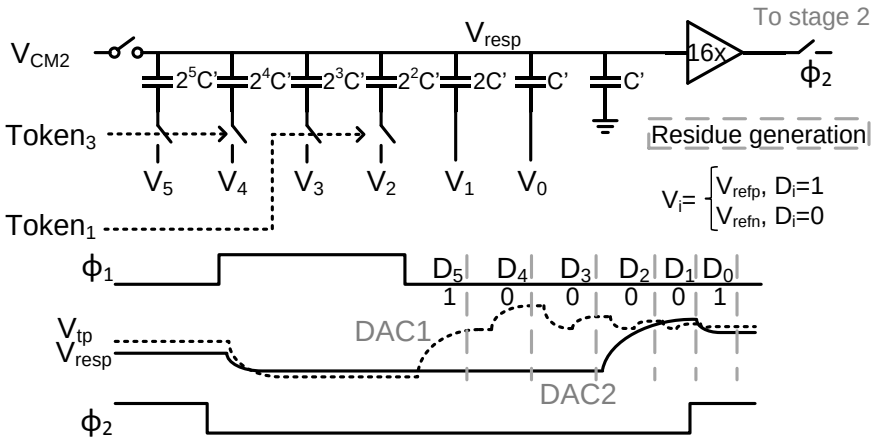


Fig. 5.11 Residue generation using DAC2.

G. Residue Amplifier

We employ an open-loop gain stage for residue amplification (see e.g. [67]) as shown in Fig. 5.12. The interstage gain is an important parameter in the ADC design as it affects both the redundancy and thermal noise [51]. Here, we analyze the latter aspect in more detail. For the two-stage pipeline SAR ADC of Fig. 5.1, the total input-referred thermal noise is the sum of kT/C noise associated with sampling, amplifier noise and noise from stage-2 ADC. This is depicted in (5.1).

$$N_{tot,in} = \frac{2kT}{C_s} + \frac{N_{amp}}{G^2} + \frac{N_{Stage2}}{G^2} \tag{5.1}$$

It is evident from (5.1) that the amplifier gain (G) is an important parameter in thermal noise optimization [68] and it trades off directly with amplifier power dissipation. Fig. 5.13 presents an example showing the various thermal noise components of the ADC. The solid lines depict the targeted ADC thermal noise (blue) and the frontend sampling noise (red, circle markers). Stage-2 noise is scaled by the inter-stage gain represented by dashed black lines in Fig. 5.13 (corresponding to different gain values). The difference between the total ADC noise (blue, square markers) and the sum of sampling noise with the scaled stage-2 noise represents the thermal noise budget available for the amplifier. Clearly, a small inter-stage gain will result in very tight amplifier noise requirement, thereby increasing amplifier power dissipation. In addition, a very large amplifier gain will also result in

extra amplifier power dissipation for a minimum required bandwidth for settling. Intuitively, the optimum power will lie somewhere in between these two extremes. Using small-signal circuit analysis, it can be shown that the input referred thermal noise for amplifier shown in Fig. 5.12 is given by

$$N_{amp,input} = \frac{2kT}{C_L G_1 G_2}\left[\frac{G_1 g_{m3}\left(1 + {g_{m2}}/{g_{m1}}\right)}{g_{m1}\left(1 + {\omega_2}/{\omega_1}\right)} + \frac{1 + \frac{\omega_c}{\omega_2}\frac{g_{m4}}{g_{m3}}}{G_1}\right] \tag{5.2}$$

where G_1 and G_2 are the voltage gains of stage 1 and stage 2 with an overall amplifier gain of $G = G_1 \times G_2$. C_L is the amplifier's output load capacitance, g_{m1}, g_{m2}, g_{m3} and g_{m4} are the transconductances of transistors M_1, M_2, M_3 and M_4, ω_1, ω_2 are output pole frequencies of stage 1 and stage 2, respectively, and ω_c is the cascode pole frequency. The transistor excess thermal noise factor (γ) is assumed to be unity.

Rearranging (5.2) gives

$$g_{m1} = \left(\frac{{G}/{R_L}\,(1 + 0.6)}{G N_{amp,input} C_L / 2kT - {1.3}/{G_1}}\right)\frac{1}{\left(1 + {\omega_2}/{\omega_1}\right)} \tag{5.3}$$

In this expression, for a first cut design, we assumed g_{m2}/g_{m1} to be 0.6, which reduces[10] the thermal noise contribution of the NMOS transistor M_2. We further assumed that second stage cascodes are supposed to contribute no more than 30% of the noise with $g_{m4}/g_{m3} = 1$. Since the load capacitance, C_L is fixed by the input capacitance of the backend ADC, the output load resistance R_L is set by the amplifier's settling time requirement ($\tau = R_L C_L$). Moreover, for a specific SNDR requirement and certain thermal noise from the backend ADC, the amplifier noise can be calculated using (5.1). Now the remaining parameters in (5.3) are swept in MATLAB to calculate the input transconductance g_{m1}, following which, the current consumption in amplifier's stage 1 and stage 2 can be computed. The resulting optimum is shown in Fig. 5.14. For this particular plot, noise numbers presented in

[10] This also reduces output voltage swing of the first stage, which is in consequential due to its small voltage gain.

Fig. 5.13 were used. In addition, a g_m/I_D of 10 S/A and 6 S/A was assumed for M_1 and M_3[11], respectively. The ratio of ω_2/ω_1 was 0.2, which along with other assumptions can be revisited after a better estimate of device and junction capacitance following a first cut design.

The final design of the residue amplifier circuit uses two stages with voltage gains of 3.2 and 5, respectively, to realize the desired voltage gain of approximately 16. The amplifier drives the 8-bit SAR ADC backend during ϕ_2, which acts as a capacitive load that sets the amplifier's output resistance and power dissipation. A small unit capacitance (0.75 fF) along with top plate sampling reduces the total DAC capacitance in stage 2 to approximately 160 fF [55]. The ratio of ω_2/ω_1 was 0.2, which can be later changed depending on the design.

Due to the large number of bits resolved in stage 1, the residue amplifier sees only a small voltage at its input. The 1.3 $V_{pp\text{-}diff}$ full-scale range of our design translates to an input signal of 1.3/64= 20.3 $mV_{pp\text{-}diff}$. This helps in several ways. First, the amplifier maintains sufficient DC linearity (see Fig. 5.15) across this range and does not require digital linearization (this was confirmed through measurements). Secondly, the amplifier does not slew and can therefore be operated with incomplete settling [40], which only leads to a linear gain error that can be absorbed through a simple radix calibration [69]. The simulated power consumption of the residue amplifier is 4.3 mW (V_{DD} = 1.2 V).

[11] For first cut analysis, largely set by amplifier's linearity requirement.

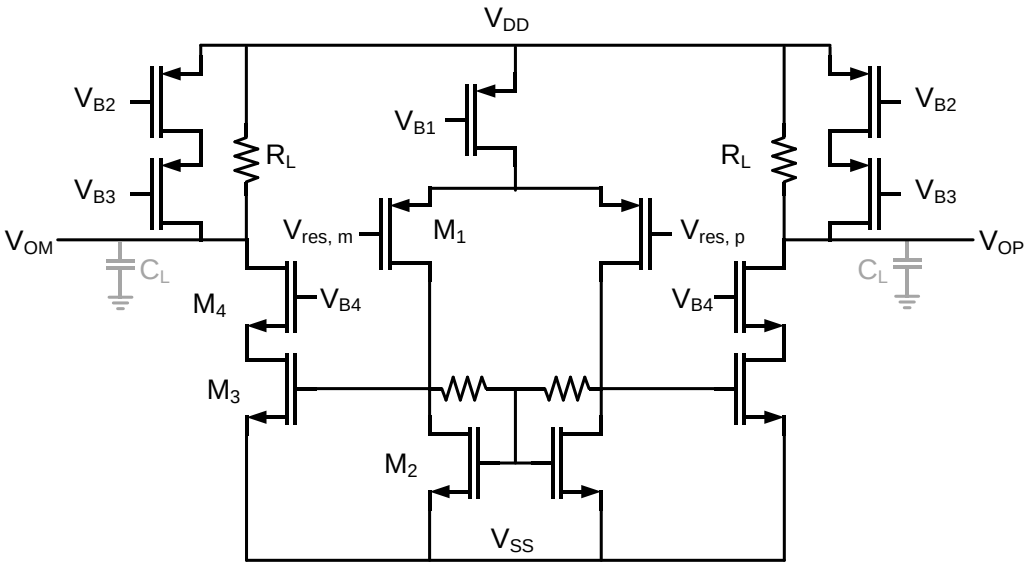


Fig. 5.12 Residue amplifier.

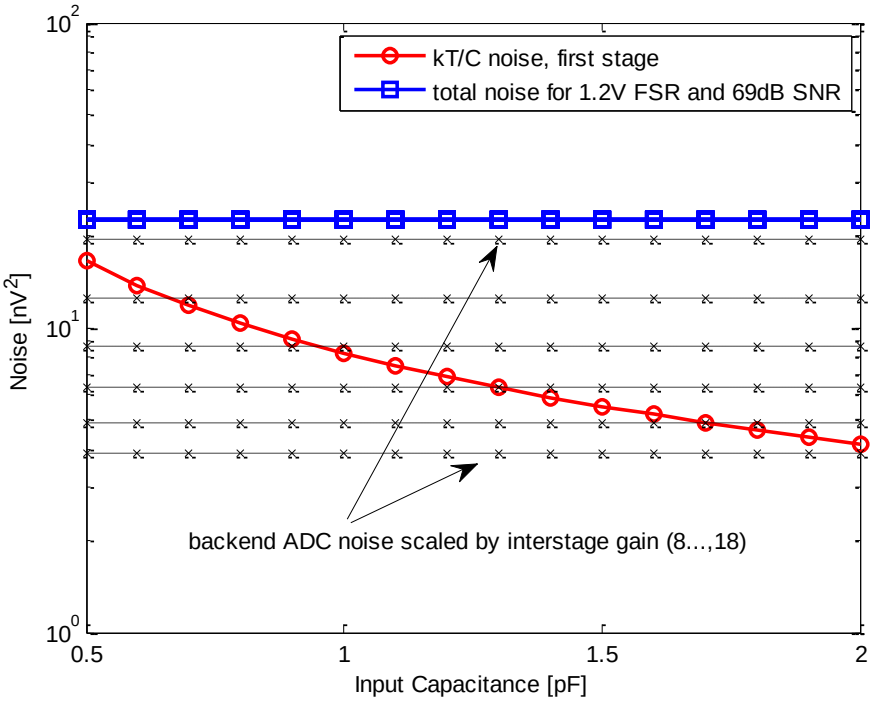


Fig. 5.13 Plot of thermal noise versus input capacitance showing various ADC noise components.

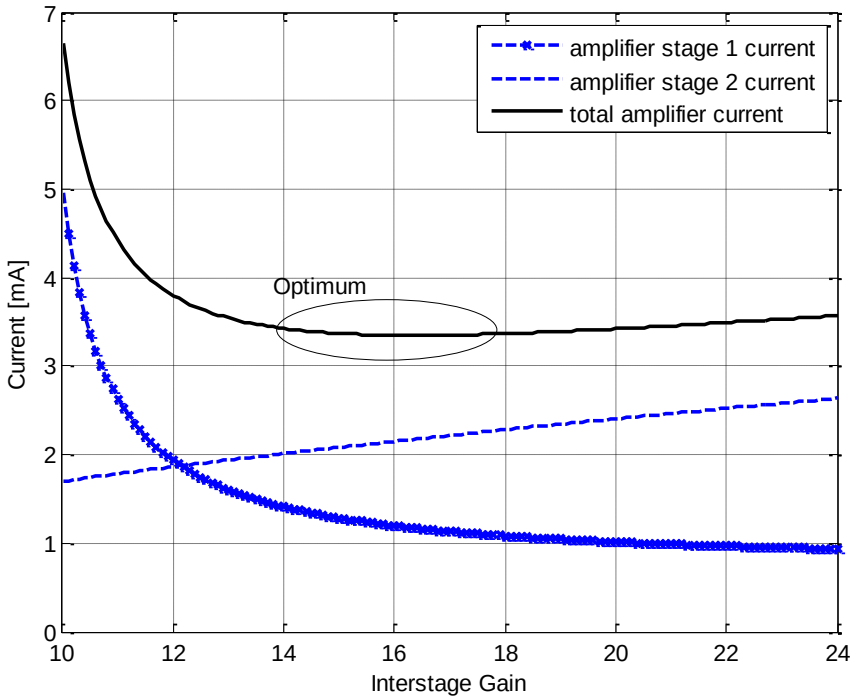


Fig. 5.14 Plot of amplifier current consumption vs. gain depicting the design optimum.

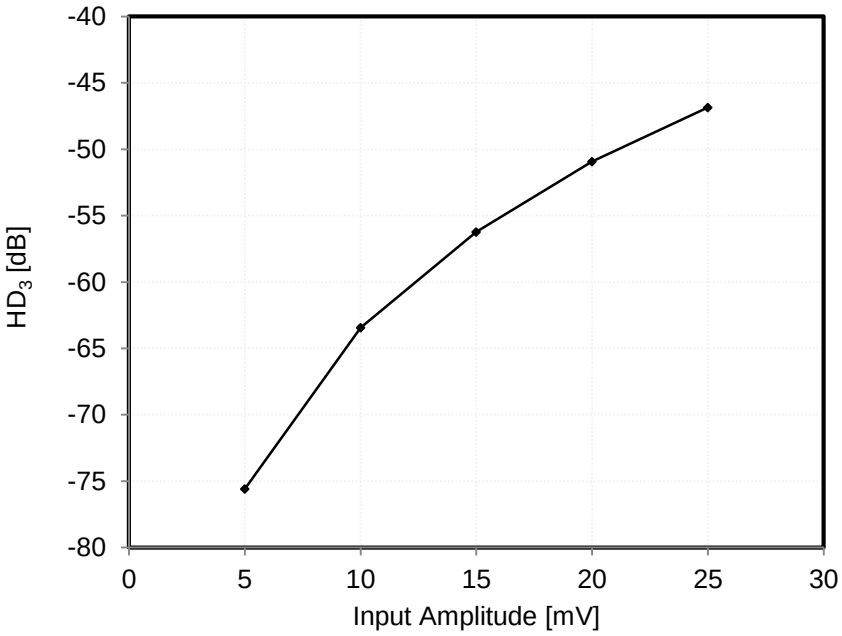


Fig. 5.15 Post layout simulation of the residue amplifier showing the plot of HD_3 vs. input amplitude.

H. Sampling Clock Generation

A low jitter sampling clock (ϕ_{1e} in Fig. 5.2) with less than 50 % duty cycle is essential for our ADC. We generate this clock using on-chip delay lines [62] and digital gates as shown in Fig. 5.16. The 'CML to CMOS buffer' is supplied from clean power lines (CLK_VDD and CLK_GND), which are not shared with any other on-chip circuit blocks. It is evident from Fig. 5.16 that the low-jitter falling edge controls the sampling instant of the ADC. As a result, the achieved SNDR is not limited by clock jitter at Nyquist input frequency, which is confirmed by measurement results showing a relatively flat SNR (see Fig. 5.23).

I. Common Mode and Bias Generation

The input common mode voltages of the stage-1 comparator and residue amplifier (V_{CM1} and V_{CM2} in Fig. 5.2) are generated on-chip using diode connected devices as shown in Fig. 5.17. Bypass capacitances implemented using standard multi-layer MOM capacitors are used to couple the common mode voltage to its respective supply voltage. The total current consumption for common mode generation is approximately 0.5 mA. This current level was chosen to yield sufficiently fast transient recovery in post-layout simulations.

All required bias currents (and voltages) are generated on-chip using a constant-g_m bias circuit [70], which consumes approximately 150 μA current in steady state from its 1.2 V supply voltage. Trim options are employed to change the bias currents by $\pm$20%.

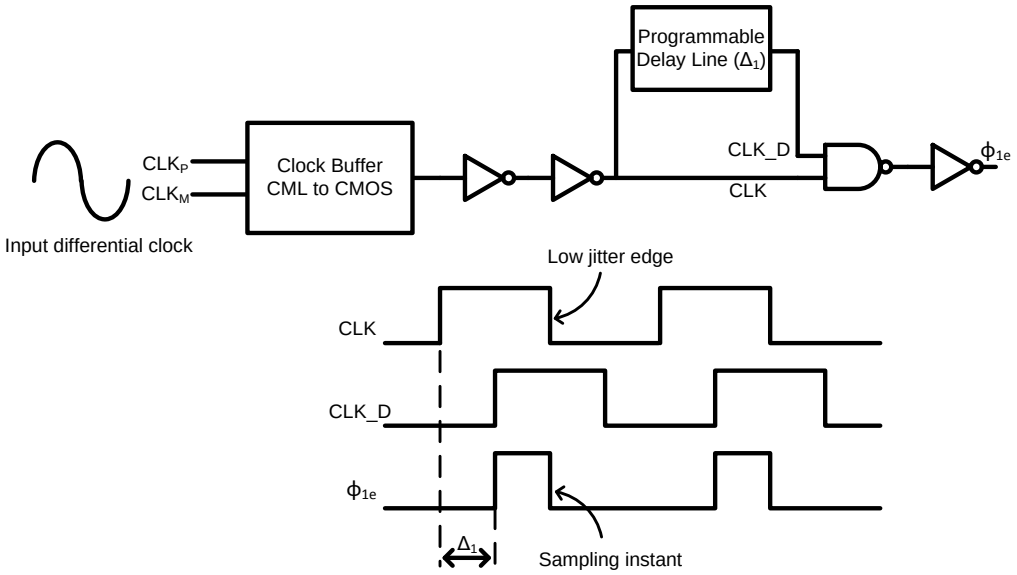


Fig. 5.16 Sampling clock generation.

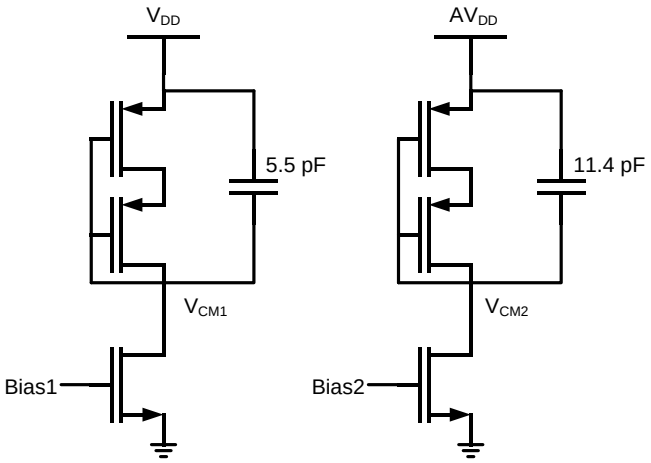


Fig. 5.17 On-chip common mode generation circuit. AV_{DD} is the clean supply voltage (1.2 V) used in the residue amplifier and constant-g_m bias circuit.

J. Stage-2 SAR A/D Converter

Fig. 5.18 shows the top-level block diagram of the SAR ADC employed in stage 2 of the design (see Fig. 5.1). The design is similar to [55] and was discussed in detail in Chapter 4. One notable change is the use of CMOS sampling switches in the frontend, as opposed to the bootstrapped NMOS switches used in [55]. Since the stage-2 ADC shares its tracking duration with residue amplification (see Fig. 5.1), it has much longer time for A/D conversion (compared to stage-1 ADC) and

is therefore not a speed bottleneck in a pipelined-SAR architecture. We can therefore require a switch with higher on resistance.

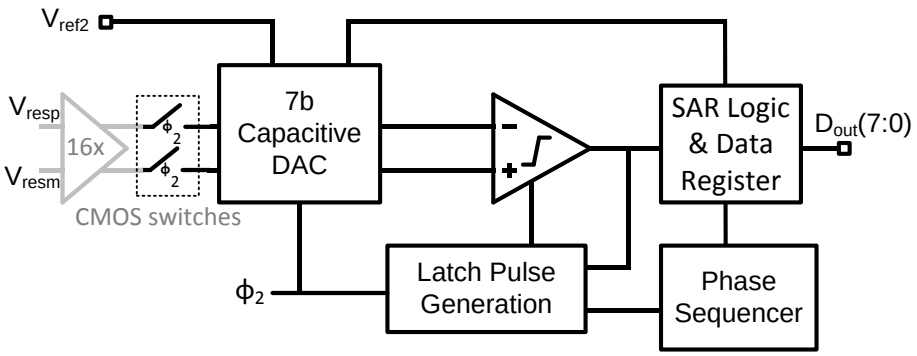


Fig. 5.18 Stage-2 SAR A/D converter block diagram.

5.4. Experimental Results

A. Measurement Setup

The prototype ADC was fabricated in a 1P9M 65-nm CMOS process and occupies a core chip area of 0.09 mm^2 (excluding decoupling capacitances). Fig. 5.19 shows the top-level chip layout. Its dimensions are 2 mm × 2 mm (pad limited) and the area occupied by the decoupling capacitors[12] is 1.2 mm^2. The die micrograph with the layout of the ADC core is shown in Fig. 5.20. The fabricated chip is packaged in a 64 pin QFN and is mounted on a custom designed PCB board. This PCB board interfaces with a TSW 1200, an ADC data capture card from Texas Instruments [64] (identical setup as the one shown in Chapter 4, Fig. 4.14). Using this measurement setup, the output data is captured at full speed and fed to a PC for performance evaluation.

[12] Since the chip is pad limited, we did not attempt to minimize the decap area. Assuming a typical capacitance density of 8 fF/μm^2, the area can be reduced to 0.3 mm^2.

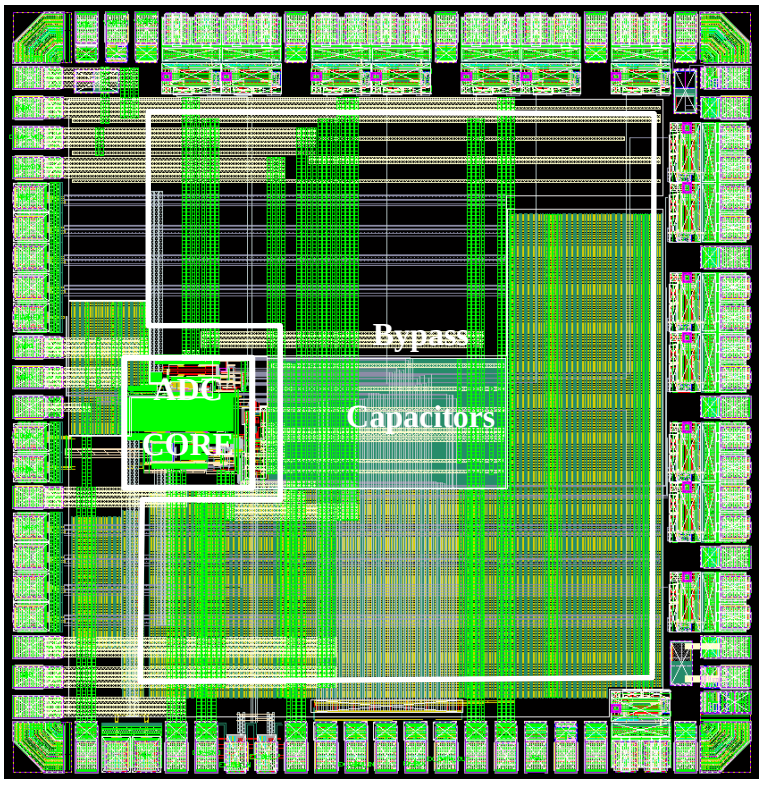


Fig. 5.19 Chip layout.

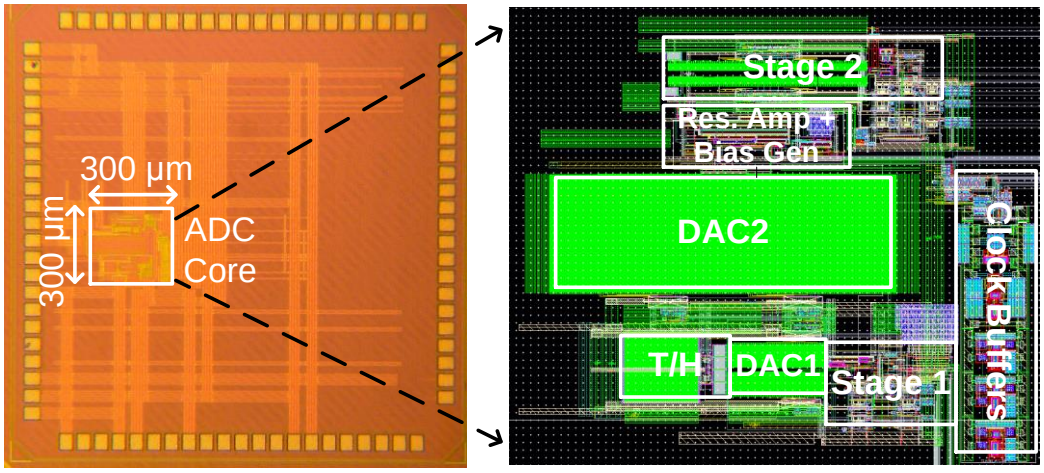


Fig. 5.20 Die photo and layout of ADC core.

B. Measurement Results

The stage 1 radix (residue amplifier gain) and DAC2 capacitor mismatch were measured using foreground calibration at start-up, and a single set of coefficients was used to post-process all measurements (MATLAB code in Appendix C). Alternatively, any standard calibration technique could be used to determine these parameters on chip (see e.g., [67], [69], [71] and [72]).

Fig. 5.21 shows the measured output spectrum of the stage-1 SAR ADC, which confirms a 6-bit SAR A/D conversion in the ADC frontend. The measured output spectrum of the ADC (after combining the bits) running at 160 MS/s with an input frequency of approximately 52 MHz is shown in Fig. 5.22. Fig. 5.23 plots the measured SNDR, SNR, SFDR and THD across the first Nyquist zone (at f_s= 160 MS/s). The measured SNDR at an input frequency of 1 MHz is 68.3 dB. At Nyquist, the measured SNDR drops to 66.2 dB. From Fig. 5.23, we observe that the SNR remains relatively flat around 68.5 dB, which means that the drop in SNDR is largely due to an increase in harmonic distortion with input frequency (attributed to the sampling network). This also confirms sufficiently low jitter in the sampling clock for our target ADC specifications. The ADC consumes 5.8 mW from its digital supply voltage (1 V), 5.16 mW from the analog supply voltage (1.2 V) and 0.16 mW from the reference pins. The total power consumption is thus 11.1 mW, including bias generation and references, but excluding I/O. The corresponding Schreier FOM (SNDR[dB] + $10\cdot\log_{10}$(P/BW)) is 167 dB at 1 MHz and 164.7 dB at Nyquist. A performance summary of the ADC and a comparison with the state-of-the-art is given in Table 5.1. Fig. 5.24 compares the FOM_S at Nyquist ($FOM_{S,hf}$) with other published ADC designs [11].

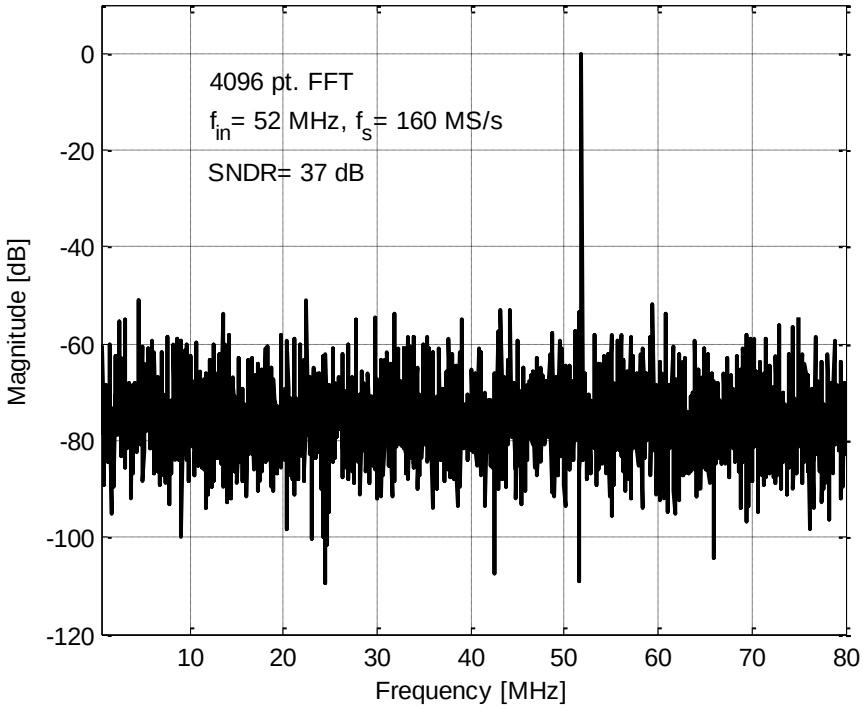


Fig. 5.21 Stage-1 ADC output spectrum showing 6-bit SAR A/D conversion.

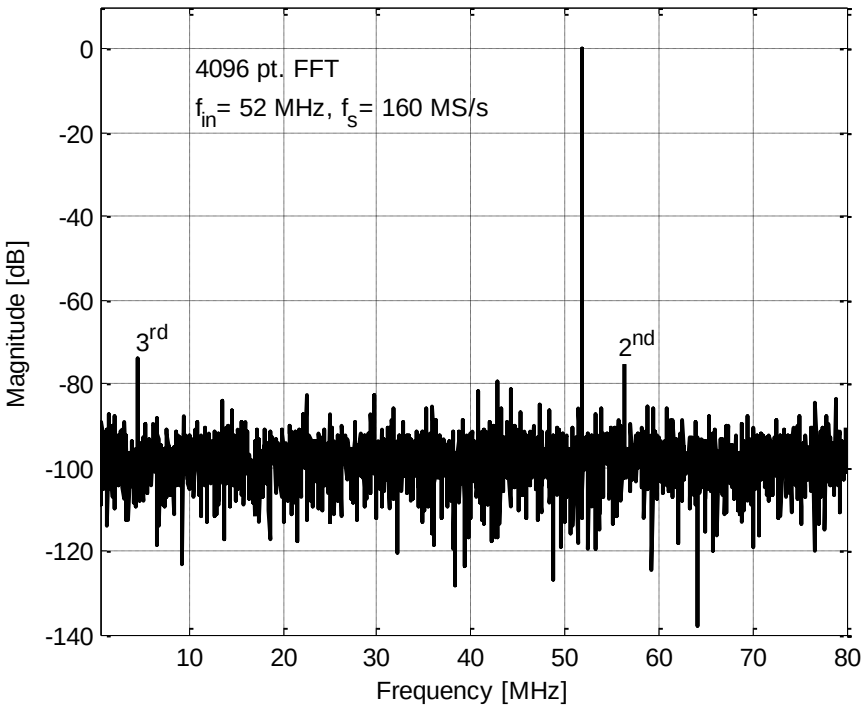


Fig. 5.22 ADC output spectrum after bit combination and calibration.

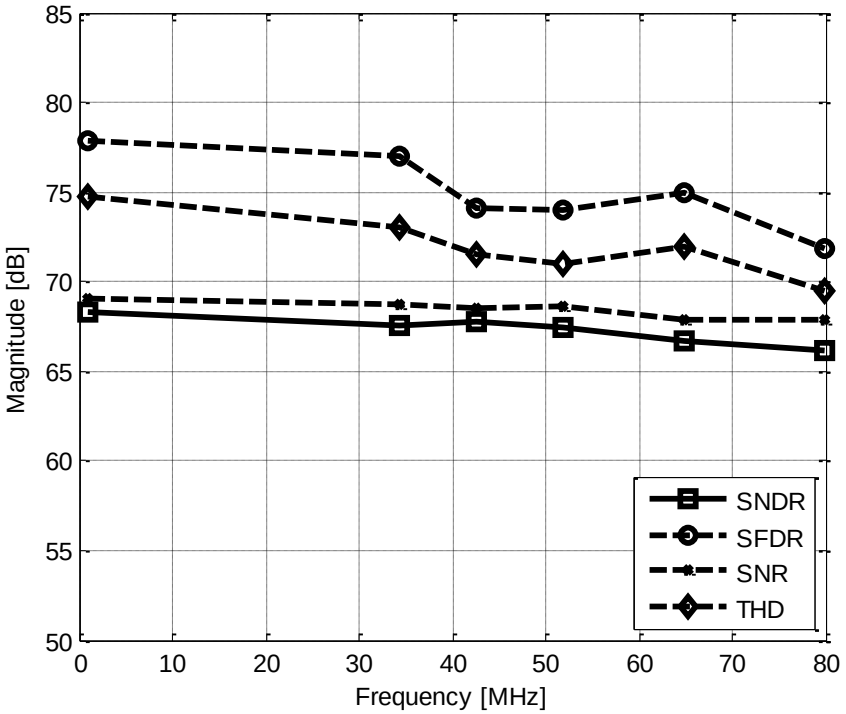


Fig. 5.23 Measured SNDR, SNR, SFDR and THD across the first Nyquist zone.

Table 5.1 Performance Comparison

	This work	[21]	[23]
Technology [nm]	**65**	65	40
Architecture	**Pipelined SAR, two CDACs in stage-1**	Pipelined SAR	Pipelined SAR
Time Interleaved	**No**	No	2x
Supply [V]	**1.0 (Digital)** **1.2 (Analog)**	1.3	1.1
Full Scale Range [V]	**1.3**	2	-
f_s [MS/s]	**160**	50	250
SNDR (LF) [dB]	**68.3**	66	58.7
SNDR (Nyq.) [dB]	**66.2**	64.4	56
Total Power [mW]	**11.1**	3.5	1.7
FOM_S (LF) [dB]	**167**	164.5	167.4
FOM_S (Nyq.) [dB]	**164.7**	162.9	164.7
FOM_W (LF) [fJ/conv-step]	**32.6**	42.9	9.1
FOM_W (Nyq.) [fJ/conv-step]	**41.6**	51.8	13.2

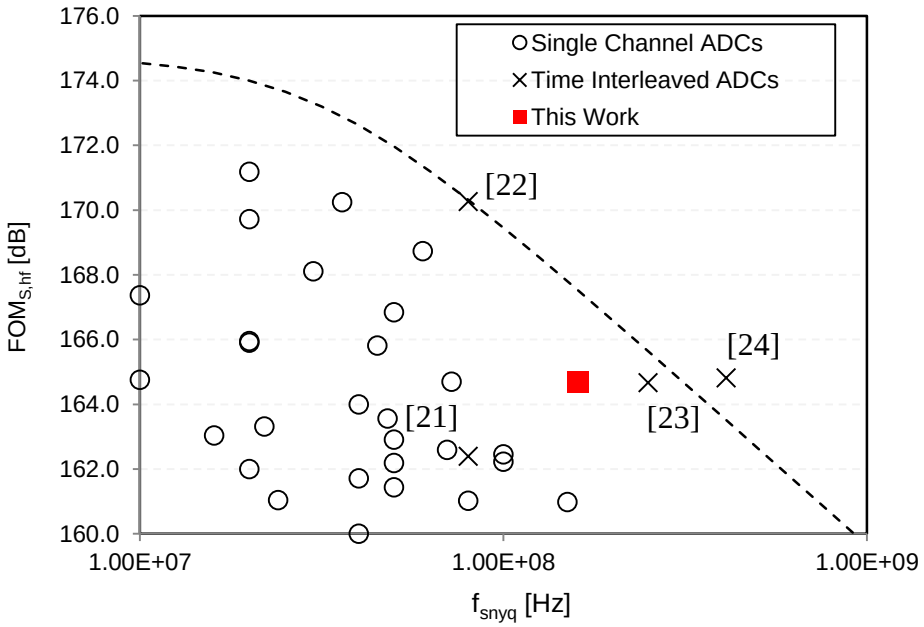


Fig. 5.24 Schreier FOM vs. Nyquist sampling frequency.

5.5. Summary

This chapter presented a proof-of-concept pipelined SAR ADC in 65-nm CMOS, featuring two capacitive DACs in its frontend. The proposed architecture separates the first stage's high-speed SAR operation from the noise limited residue generation, resulting in significant improvements in conversion speed and DAC switching energy. The two CDACs are designed using single-metal MOM capacitors and the ADC input is sampled on both simultaneously via bottom plate sampling. A fast comparator with asynchronous SAR logic speeds up the stage-1 operation. Furthermore, the design employs a custom-designed dynamic latch that implements SAR logic for bottom plate sampling in the stage-1 SAR ADC, as well as an open-loop residue amplifier with incomplete settling. The ADC was designed and fabricated in the TSMC 65-nm GP CMOS process. It runs at 160 MS/s and achieves a peak SNDR of 68.3 dB with a Schreier FOM of 164.7 dB at Nyquist, which compares favorably with the state-of-the-art.

Chapter 6

Conclusions and Future Work

6.1. Summary

This research focused on high-speed SAR A/D converters designed in advanced CMOS processes and started out with a mismatch study of small on-chip single-metal MOM capacitors. The use of small capacitors in the CDAC reduces its switching power dissipation as well as settling time and is a key factor in improved SAR ADC performance. Prior to this work, however, there was little published data on matching characteristics of such capacitors and to address that, we designed a test-structure to extract the capacitance mismatch information.

Next, we explored high-speed SAR ADC design techniques that improve the conversion speed while maintaining low enough power dissipation. Asynchronous timing, top-plate sampling with symmetric DAC switching, SAR loop delay optimization, regeneration-reset optimized comparator and a dynamic data capture latch were investigated for this purpose. A prototype 8-bit SAR ADC was designed and fabricated as a proof of concept for these design techniques.

Finally, we investigated the concept of SAR-pipelining as a viable option to realize moderate to high resolution (> 65 dB SNDR), high-speed (> 150 MS/s), low energy A/D converters. A modified pipelined-SAR architecture that uses two-CDACs in the ADC frontend was proposed. The prototype ADC used this architecture along with the learnings from previous two designs (capacitance mismatch

measurements and 8-bit SAR ADC). The final implementation had its own challenges including small sampling duration, high-speed bottom plate sampling SAR logic and power efficient residue amplification (to list a few).

This thesis presented the key aspects of the mismatch study of small on-chip single-metal capacitors in Chapter 2 including description of capacitance layout, mathematical modeling, a switching scheme to suppress nearest neighbor correlations and implementation details of the test structure used to extract mismatch information. Measurement results (also in Chapter 2) for the prototype IC show good matching characteristics for the investigated single-metal capacitors, with matching coefficients of approximately $0.85\ \% \times 1\ fF\ or\ 1.9\ \% \times 1\ \mu m$. A circuit designer can use this information to choose the smallest possible unit capacitance for designs limited by capacitance mismatch. Chapter 3 discussed various high-speed SAR ADC design techniques in detail including SAR pipelining and the proposed two-CDAC architecture. Chapter 4 presented the implementation details and measurement results of an 8-bit, 450 MS/s, single-bit/cycle SAR ADC. To our knowledge, this is the fastest published SAR ADC using a single comparator to date. Next, Chapter 5 described the implementation details of the two-stage pipelined-SAR ADC employing two-CDACs in the ADC frontend. It also presented the measurement results and compared the achieved performance to the state-of-the-art. Though our ADC was designed using a relatively old 65 nm CMOS process, it compares very well with the state-of-the-art, thus validating the effectiveness of the proposed two-CDAC pipelined SAR architecture.

6.2. Future Work

A. Further Improvements

The measurement results presented in Chapter 5 correspond to state-of-the-art performance. However, the design achieves a relatively low SFDR of 72 dB at Nyquist, which limits the overall SNDR. There is an opportunity to improve this

by redesigning the frontend sample-hold circuit along with sampling clock generation. In addition, an integrated input buffer to drive the ADC may be considered to further improve harmonic distortion.

As a next step, it will be interesting to reduce the power consumed by the residue amplifier. As stated in Chapter 5, the open loop amplifier consumes about 40 % of the total power. Alternatively, using a dynamic amplifier [22], [23] or a ring amplifier [73], [74] for residue amplification will significantly reduce the ADC power dissipation. Both of these amplifier topologies have already been demonstrated for this resolution and sampling frequency.

Currently the ADC uses external references with on-chip decoupling capacitors. A future design may implement on-chip reference buffers along with redundancy in the CDAC as proposed in [22].

This ADC architecture has a reduced full-scale range and relatively low complexity, making it attractive for deployment in a commercial SoC. A background calibration engine to correct for DAC mismatch and amplifier gain error [67] can be employed to realize a more robust design.

B. Time Constant Matching with Redundancy

The time constant matching technique that was described in Chapter 3 uses an pole-zero cancellation in the CDAC of a SAR ADC to reduce the DAC settling time and enhance ADC conversion speed. However, parasitic capacitance at the comparator input (C_P in Fig. 6.1) reduces its benefits significantly. It is not uncommon to intentionally add additional capacitance at this node to reduce the ADC full-scale range [55], [22], which may be set by the targeted SoC application. This is because, in order to minimize the PMOS switch resistances in the capacitive DAC (for fast DAC settling), one choses a reference voltage (V_{ref}) close to the supply (V_{DD}) that results in an extended ADC full scale range ($\pm V_{DD}$). The parasitic capacitance at comparator input acts as a capacitive divider and reduces the ADC full-scale range to a desired value.

SAR A/D converters targeting bio-medical and sensor applications provide an interesting area of application for the time constant matching technique. These ADCs often use reduced supply voltage (~0.6 V) to achieve lower power dissipation [75]. In such a design, V_{ref} can be chosen equal to V_{DD} without having (since V_{DD} is now lower), which obviates the need of additional divider capacitance (see above). However, use of lower supply voltage (and V_{ref}) results in smaller gate over-drive voltage, which increases the DAC switch resistance ($M_{N,\,P}$ in Fig. 6.1). This makes the DAC settling time a significant fraction of SAR loop delay and an increased loop delay reduces ADC conversion speed. To speed up DAC settling, a designer can first minimize C_P and then employ time constant matching together with sufficient redundancy [18] in the capacitive DAC. Coarse pole-zero cancellations during DAC settling (key idea of time constant matching) now rapidly bring the DAC output transient within the redundancy window, which then essentially absorbs the long settling tails (due to pole-zero doublet), thereby reducing the DAC settling time and improving the ADC conversion speed.

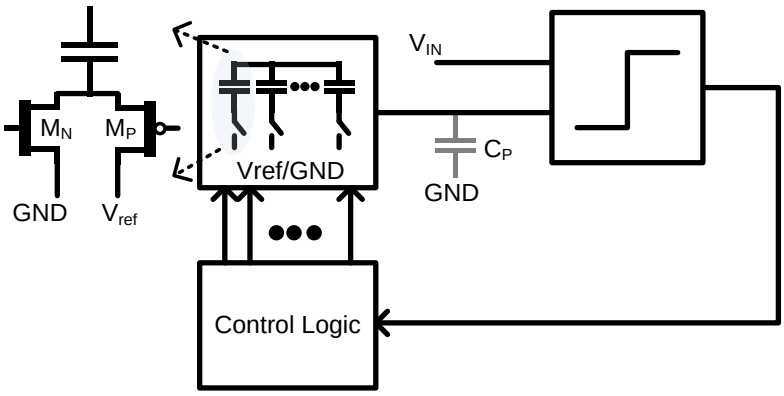


Fig. 6.1 SAR ADC block diagram showing parasitic capacitance C_P and DAC control switches $M_{N,\,P}$.

APPENDIX A

A.1. Mean and Variance of V_Δ

The error voltage V_Δ is given by

$$\mathrm{V}_\Delta = V_{REF}\frac{\sum_{i=1,2,5,6\ldots} C_i - \sum_{j=3,4,7,8,\ldots} C_j}{\sum_{k=1}^{N} C_k} = V_{REF}\frac{X}{Y}$$

Its variance, can be found using the statistics of the sums in the numerator (X) and denominator (Y)

$$Var(\mathrm{V}_\Delta) \approx V_{REF}^2\left(\frac{\mu_X}{\mu_Y}\right)^2\left[\left(\frac{\sigma_X}{\mu_X}\right)^2 + \left(\frac{\sigma_Y}{\mu_Y}\right)^2 - \frac{2C_{OV}(X,Y)}{\mu_X\mu_Y}\right] \quad \text{(A.1)}$$

where

$$\mu_X = 0 \quad and \quad \mu_Y = NC_u$$

$$\therefore Var(V_\Delta) \approx \frac{V_{REF}^2}{N^2C_u^2}\sigma_X^2 \quad \text{(A.2)}$$

The remaining unknown σ_X^2 in (A.2) is calculated as follows:

$$\text{Let } \sigma_X^2 = \sigma^2(A-B) = \sigma^2(A) + \sigma^2(B) - 2C_{OV}(A,B)$$

where,

$$A = \sum_{i=1,2,5,6\ldots} C_i \text{ and } B = \sum_{j=3,4,7,8,\ldots} C_j$$

Now,

$$\sigma^2(A) = \sigma^2\left(\sum_i C_i\right)$$

$$= \sum_i \sigma^2(C_i) + \sum_i \sum_{k,i\neq k} C_{OV}(C_i, C_k)$$

$$= \frac{N}{2}\sigma_u^2 + \frac{N}{2}\sigma_{ab}^2 \text{ , (using (2.1) from Section 2.2)}$$

Similarly,

$$\sigma^2(B) = \sigma^2\left(\sum\nolimits_j C_j\right)$$

$$= \sum_j \sigma^2(C_j) + \sum_j \sum_{k,j\neq k} C_{OV}(C_j, C_k)$$

$$= \frac{N}{2}\sigma_u^2 + \frac{N}{2}\sigma_{ab}^2$$

$$C_{OV}(A,B) = E(AB) - E(A)E(B)$$

$$= E\left[\left(\sum\nolimits_i C_i\right)\left(\sum\nolimits_j C_j\right)\right] - E\left(\sum\nolimits_i C_i\right)E\left(\sum\nolimits_j C_j\right)$$

$$= E\left(\sum_i \sum_j C_i C_j\right) - E\left(\sum\nolimits_i C_i\right)E\left(\sum\nolimits_j C_j\right)$$

$$= \sum_i \sum_j E(C_i C_j) - E\left(\sum\nolimits_i C_i\right)E\left(\sum\nolimits_j C_j\right)$$

$$= \sum_i \sum_j \{E(C_i)E(C_j) + C_{OV}(C_i, C_j)\} - E\left(\sum\nolimits_i C_i\right)E\left(\sum\nolimits_j C_j\right)$$

$$= \sum_i \sum_j C_{OV}(C_i, C_j)$$

$$= \left(\frac{N}{2} - 1\right)\sigma_{ab}^2 \text{ (again using (2.1) from Chapter 2, Section 2.2)}$$

Substituting the value $\sigma^2(A), \sigma^2(B)$ and $C_{OV}(A,B)$ in (A.2) gives,

$$\sigma_X^2 = N\sigma_u^2 + N\sigma_{ab}^2 - 2\left(\frac{N}{2} - 1\right)\sigma_{ab}^2$$

$$= N\sigma_u^2 + 2\sigma_{ab}^2$$

Using this, we obtain

$$Var(V_\Delta) = \frac{V_{REF}^2}{N}\left[\left(\frac{\sigma_u}{C_u}\right)^2 + \frac{2}{N}\left(\frac{\sigma_{ab}}{C_u}\right)^2\right] \quad \text{(A.3)}$$

A.2 Switching Sequence to Extract Nearest Neighbor Covariance

The capacitor switching sequence described in Chapter 2, Section 2.4 A, helps to infer relative mismatch coefficient (σ_u/C_u) in presence of nearest neighbor correlations. Instead, if the capacitors are switched as shown in Fig. A.1, the resulting error voltage V_Σ is

$$V_\Sigma = V_{REF}\frac{\sum_{i=1,2,\ldots,N/2} C_i - \sum_{j=N/2,\ldots,N} C_j}{\sum_{k=1}^{N} C_k} = V_{REF}\frac{P}{Q}$$

Using the analysis presented in Appendix A.1, the variance of V_Σ is

$$Var(V_\Sigma) \approx \frac{V_{REF}^2}{N^2 C_u^2}\sigma_P^2 \quad \text{(A.4)}$$

By following the steps of Appendix A.1, the quantity σ_P^2 is

$$\sigma_P^2 = N\sigma_u^2 + 2N\sigma_{ab}^2 - 6\sigma_{ab}^2$$

Substituting this in (A.4), and assuming large N, we get

$$Var(V_\Sigma) = \frac{V_{REF}^2}{N}\left[\left(\frac{\sigma_u}{C_u}\right)^2 + 2\left(\frac{\sigma_{ab}}{C_u}\right)^2\right] \quad \text{(A.5)}$$

It is clear from (A.5) that once the quantity σ_u/C_u is inferred from the variance of V_Δ, the nearest neighbor correlation can be extracted from the variance of V_Σ.

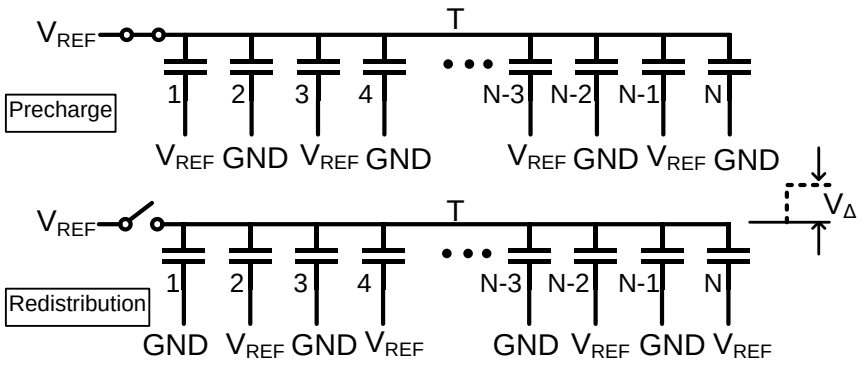


Fig. A.1 Capacitance switching scheme to extract the nearest neighbor correlation.

A.3 DNL in Presence of Nearest Neighbor Correlations

Suppose the unary capacitive array with N unit elements (Fig. 2.2) that follow the nearest neighbor correlation model of (2.1) is used to design a binary weighted DAC ($\log_2$N bits). At the mid-code transition, the DNL is given by,

$$DNL_{mid-code} = \frac{V_\Sigma + \epsilon - \text{LSB}}{LSB}$$

where, V_Σ is defined in (A.4) and

$$\epsilon = V_{REF}\frac{C_N}{\sum_{k=1}^{N} C_k} \; and \; LSB = \frac{V_{REF}}{N}$$

For large N, the variance of mid-code DNL can be approximated as

$$Var(DNL_{mid-code}) = \sigma_{DNL}^2 \approx Var\left(\frac{V_\Sigma}{LSB}\right) = N\left[\left(\frac{\sigma_u}{C_u}\right)^2 + 2\left(\frac{\sigma_{ab}}{C_u}\right)^2\right] \qquad \text{(A.6)}$$

As expected, the finite nearest neighbor correlations deteriorate the mid-code DNL variance in a binary weighted DAC. In addition, (A.6) simplifies to the well-known result of $\sigma_{DNL}^2 = N\left({\sigma_u}/{C_u}\right)^2$, when $\sigma_{ab} = 0$.

A.4. Error due to Coupling Capacitance Mismatch

Let the small capacitance used for coupling the resistive DAC to the comparator deviates from its nominal value as shown in Fig. 2.14 (C' = C(1+γ)). For a digital input code (D), the output of a 6-bit DAC (Fig. 2.14) is

$$V_{DAC} = \frac{V_{ref,dac}}{2^6} D$$

For the circuit of Fig. 2.14, the comparator input is

$$V_{comp,i+1} = V_{comp,i} - V_{DAC} \frac{C'}{C' + (2^6 - 1)C}$$

Substituting C' and V_{DAC} in the above equation, we get

$$V_{comp,i+1} = V_{comp,i} - \frac{V_{ref,dac}}{2^{12}} (1 + \gamma) D$$

$$Error = \gamma \times \frac{V_{ref,dac}}{2^{12}} D$$

A.5. Error due to Feedback DAC INL

For a digital input code (D), the output of the 6 bit DAC of Fig. 2.14 is

$$V_{DAC} = \frac{V_{ref,dac}}{2^6} D + \varepsilon$$

With 64 identical unit elements in the capacitive array, the input to the comparator is

$$V_{comp,i+1} = V_{comp,i} - \frac{V_{ref,dac}}{2^6 \times 2^6} D - \frac{\varepsilon}{2^6}$$

Therefore, the overall error due to DAC non-linearity is

$$\varepsilon_{DAC} = \frac{\varepsilon}{2^6}$$

For this error to be less than 1 LSB,

$$\frac{\varepsilon}{2^6} < \frac{V_{ref,dac}}{2^{12}}$$

$$\Rightarrow \varepsilon < \frac{V_{ref,dac}}{2^6}$$

APPENDIX B

Time Domain Analysis of DAC Switching

Consider the circuit shown in Chapter 3, Fig. 3.20 with $C_P = 0$. Assuming square law transistor behavior, the current 'i' in Fig. 3.20 is

$$i = K\left[(V_{DD} - V_t)v_D - \frac{(v_D)^2}{2}\right] \tag{A.7}$$

$$i = C\frac{d(v_o - v_D)}{dt} = -C\frac{d(v_o - v_y)}{dt} \tag{A.8}$$

The node voltage v_y and the final resistance to ground (after the voltages have settled) are given by the following equations, respectively

$$v_y = V_{ref} - iR_{ref} \tag{A.9}$$

$$R_{gnd} = \frac{1}{K(V_{DD} - V_t)} = \frac{1}{KV_{OV}} \tag{A.10}$$

Using charge conservation at node v_O,

$$\begin{aligned} C(v_o - v_D) + C(v_o - v_y) &= 2C(v_i - V_{ref}) \\ \Rightarrow v_o &= (v_i - V_{ref}) + \frac{1}{2}(v_y - v_D) \\ v_o &= (v_i - V_{ref}) + \frac{1}{2}(V_{ref} - iR_{ref} - v_D) \end{aligned} \tag{A.11}$$

Now, using (A.8), we find

$$\begin{aligned} \frac{dv_o}{dt} &= \frac{1}{2}\left(\frac{dv_D}{dt} + \frac{dv_y}{dt}\right) \\ \frac{i}{C} = \frac{dv_o}{dt} - \frac{dv_D}{dt} &= \frac{1}{2}\left(\frac{dv_D}{dt} + \frac{dv_y}{dt}\right) - \frac{dv_D}{dt} = \frac{-1}{2}\left(\frac{dv_D}{dt} - \frac{dv_y}{dt}\right) \end{aligned} \tag{A.12}$$

Next, substituting (A.9) into (A.12) gives

$$-\frac{2i}{C} = \frac{dv_D}{dt} + R_{ref}\frac{di}{dt} \tag{A.13}$$

Using the equation for current in a MOS transistor biased in the triode region in (A.13), we get

$$\frac{dv_D}{dt} + R_{ref}K(V_{OV} - v_D)\frac{dv_D}{dt} = -\frac{1}{C}Kv_D(2V_{OV} - v_D)$$

$$\therefore -\frac{t}{C} = \int_{V_{ref}}^{v_D} \frac{dv_D}{Kv_D(2V_{OV} - v_D)} + \int_{V_{ref}}^{v_D} \frac{R_{ref}(V_{OV} - v_D)}{v_D(2V_{OV} - v_D)}dv_D$$

After integrating and solving for v_D, this becomes

$$v_D^{\left(\frac{R_{ref}}{R_{gnd}}+1\right)}(2V_{OV} - v_D)^{\left(\frac{R_{ref}}{R_{gnd}}-1\right)} = \left\{V_{ref}^{\left(\frac{R_{ref}}{R_{gnd}}+1\right)}(2V_{OV} - V_{ref})^{\left(\frac{R_{ref}}{R_{gnd}}-1\right)}\right\}\exp\left(-\frac{2t}{R_{gnd}C}\right) \tag{A.14}$$

APPENDIX C

MATLAB code for ADC Calibration

```
clear all;
close all;
load Dout1_52M; % load measured ADC data
load Dout2_52M;

D1 = bi2de(Dout1, 'left-msb');
D2 = bi2de(Dout2, 'left-msb');
D1 = D1(1:end-1);
D2 = D2(2:end);   % ADC has a latency of 1
N = length(D1);
n = 1:N;
o = ones(N, 1);

% Look at stage 1 spectrum and find number of sine wave cycles
spec = abs(fft(D1));
spec = spec(1:end/2);
[m idx] = max(spec(2:end));
figure(1)
plot(0:N/2-1, 20*log10(spec/m));
cycles = idx;

% Fit a sinusoid to the stage 1 output to find input phase
```

```
A = [sin(2*pi*cycles/N*n)' cos(2*pi*cycles/N*n)' o];
coeffs = pinv(A)*D1;
fit_sin = A*coeffs;
err = fit_sin-D1 - mean(fit_sin-D1);
sndr_D1 = 20*log10(norm(fit_sin)/norm(err))
figure(3)
plot(n, D1, n, fit_sin);

% Now fit both outputs to sine wave
% Using individual bits from stage 1 in B matrix calibrates the DAC. If Dout1 is
replaced by its decimal equivalent D1, then only radix calibration is performed.

B = [Dout1(1:end-1,:) D2 o];
coeffs = pinv(B)*fit_sin;
D = B*coeffs;
residue_gain = coeffs(1)/coeffs(2)
figure(4)
plot(n, D, n, fit_sin);
err = fit_sin-D - mean(fit_sin-D);
sndr_D = 20*log10(norm(fit_sin)/norm(err))
spec = abs(fft(D));
spec = spec(1:end/2);
m = max(spec(2:end));
figure(5)
plot(0:N/2-1, 20*log10(spec/m));
```

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