# Dual Time-Interleaved Successive Approximation Register ADCs for an Ultra-Wideband Receiver

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***Abstract*—Ultra-wideband radio requires Nyquist sampling rates of at least 500 MS/s with low resolutions. While flash is the traditional choice for these specifications, a comparative energy model is used to show the potential energy savings of the time-interleaved successive approximation register architecture, which requires only a linear number of comparisons versus exponential for flash. A dual 500-MS/s, 5-bit ADC chip is implemented in a 0.18-$\mu$m CMOS process, with both ADCs synchronized for use in an I/Q UWB receiver. Each ADC uses a 6-way time-interleaved SAR topology with full custom logic, self-timed bit-cycling, and duty cycling of the comparator preamplifiers to enable 500-MS/s operation with 7.8 mW power consumption. The output resolution is adjustable down to the 1-bit level for additional power savings.**

***Index Terms*—ADC, analog-to-digital conversion, CMOS, scaleable, successive approximation register, ultra-wideband communication.**

## I. Introduction

ULTRA-WIDEBAND (UWB) communication has emerged as a technology for high speed wireless communication after recently being approved by the Federal Communications Commission (FCC). Digital communications are allowed in the 3.1–10.6-GHz band with signal bandwidths in excess of 500 MHz and average equivalent isotropic radiated power density of less than $-41.3$ dBm/MHz. Both orthogonal frequency division multiplexing (OFDM) [1] and pulse-based [2] solutions have been proposed to support high data rates at short range, even in the presence of multipath channels.

For the FCC-specified minimum bandwidth RF signal (e.g., the pulse used in [3]), direct downconversion produces a signal between 0–250 MHz, which can be sampled using a 500 MS/s Nyquist analog-to-digital converter (ADC). It has previously been shown that only a minimal performance degradation occurs when using 4-bits versus infinite resolution for reception in both noise- and interference-limited regimes [4], [5]. Furthermore, [4] showed that under favorable channel conditions (high SNR), acceptable bit-error rate (BER) performance can be obtained with even lower resolutions. The ADC should be able to lower its resolution and thereby save power when these favorable conditions arise (e.g., direct line-of-sight communication over short distances).

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An energy model has been developed to compare the flash architecture with a time-interleaved successive approximation register (SAR) topology to determine which achieves the best energy efficiency for these specifications. The model's results lead to the choice of a 6-way time-interleaved SAR to implement dual 500-MS/s, 5-bit ADCs suitable for digitizing I/Q demodulated UWB signals, fabricated in a 0.18-$\mu$m CMOS process [6]. Full custom digital logic and self-timing are used to overcome some of the power and performance penalties of the SAR topology. Each ADC consumes 7.8 mW, excluding I/O power, at the maximum sampling rate and resolution. A simple bit scaling capability reduces the resolution in each parallel channel and also reduces the total number of parallel channels in response to changing channel conditions as part of a full UWB receiver.

## II. Architecture Selection

The flash topology is the typical choice for high-speed, low-resolution converters [7], [8]. Flash ADCs achieve the highest sampling rates by comparing, in parallel, the analog input to every transition voltage, producing the output in one period with no feedback required between conversions; however, exploiting parallelism to increase speed in this manner requires the number of comparators to grow as $2^b$, where $b$ is the resolution of the converter in bits. Interpolating [9] and folding [10], [11] flash ADCs can reduce the number of preamplifiers and latches, respectively, that are needed, but the general exponential growth of comparators remains a fundamental problem with this topology.

The SAR ADC is generally used for high-resolution, low-frequency operation. By determining the digital output one bit at a time, SAR ADCs only make $b$ comparisons for a $b$-bit converter but require at least $b + 1$ clock periods to produce the output, much slower than the flash topology. By time-interleaving SAR ADCs [12], [13], high speed can be achieved without sacrificing the SAR's inherent low power. To compare SAR and flash topologies in terms of total energy efficiency, a simple theoretical model of their energy consumption has been developed. An earlier comparison emphasized the reduced comparator complexity of the time-interleaved SAR topology in higher resolution applications [12]. The model presented below expands on the comparator requirements and further includes the digital logic and capacitor array energy, which must be taken into account at low resolutions. The process-dependent constants in the model were all extracted from simulations of the basic comparator and logic block. For reference, a list of all of the symbols used is included in the Appendix.

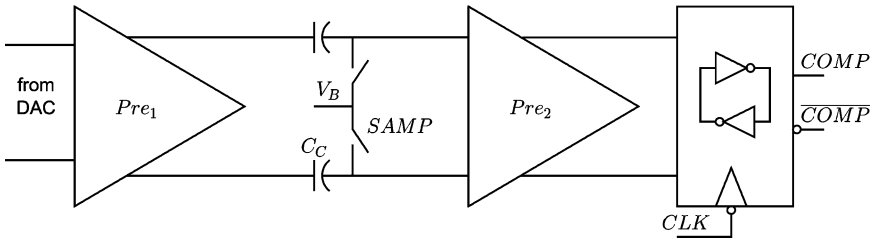


Fig. 1. Comparator with a two-stage preamplifier and regenerative latch. Autozeroing of the first preamplifier occurs while the input is being sampled on the capacitor array (*SAMP* high).

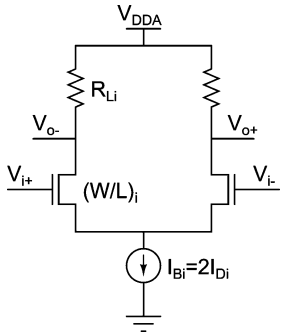


Fig. 2. Basic preamplifier schematic.

### A. SAR Energy Model

The SAR converters are time-interleaved to equal the flash converter's throughput. The number of parallel SAR converters, $M$, is constrained to be $M = b + U$, where $U$ is the number of clock periods used to sample the input and autozero the comparators. This constraint simplifies implementation and clock distribution as discussed in Section III. In particular, with this constraint, only one clock at the sampling frequency is required; thus, the clock generation requirements are the same for both a flash and a SAR ADC.

The basic SAR ADC includes a digital-to-analog converter (DAC) capacitor array, comparator, and a control block, as seen in the channel block diagram of Fig. 7. A DAC capacitor array samples the input and generates estimates of the input based on the computed digital value. The comparator includes a preamplifier and a latch to determine whether the DAC output is positive or negative, serially producing the digital output bits. The control logic performs the successive approximation algorithm and drives the switches in the capacitor array. The energy usage of each of these blocks will be examined below.

*1) Comparator:* The comparator is composed of a set of linear preamplifiers and a regenerative latch. The preamplifiers provide both sufficient gain to compensate for the relatively high input refererred offset voltage of the latch and isolation from latch kickback noise. To reduce the preamplifiers' contribution to the comparator offset, low gain preamplifiers with output offset storage (OOS) are used. A two stage preamplifier, as shown in Fig. 1, has been chosen in order to provide sufficient gain (9-25) for the full scale input voltage, $V_{FS}$, and latch input referred offset voltage, $V_{OL}$, under consideration.

Each of the preamplifiers has a differential nMOS input pair with resistive loads, as shown in Fig. 2, assumed to be loaded only by the input capacitance of the following stage. Using an approach similar to [14], both preamplifiers are biased at the same current density assumed fixed in this model.[1] Thus, there is a linear relationship between transconductance, input capacitance, and bias current ($\alpha g_m = I_D = 1/2 I_B$, $C_{\rm in} = \beta I_D$), set by process and current density dependent parameters $\alpha$ and $\beta$.

The preamplifier biases are chosen to satisfy four specifications: offset, noise, gain, and speed. The offset and flicker noise of the first preamplifier are eliminated by OOS, and it is assumed that the first preamplifier provides sufficient gain to compensate for the offset of the second preamplifier. For the high speeds and low resolution required for this ADC, the currents required to meet the gain and settling time specifications are sufficient to meet the thermal noise requirements, and therefore only gain and speed are considered. The preamplifiers are conservatively assumed to settle as a first order system, and must settle from the largest to smallest input in one half the clock period, with the latch using the other half. Thus, the two requirements for the preamplifiers are

$$A_V = A_{V1}A_{V2}\frac{C_C}{C_C + C_{in2}} = \frac{2^{b+1}V_{OL}}{V_{FS}} \tag{1}$$

$$\tau = \tau_1 + \tau_2 = R_{L1}C_{L1} + R_{L2}C_{L2} = \frac{1}{(b+1)f_s \cdot 2\ln 2}. \tag{2}$$

Here, $C_C$ is the OOS capacitor and $C_{in2}$ is the input capacitance of the second preamplifier.

Using $A_{Vi} = g_{mi}R_{Li}$, each preamplifier's bias current is

$$I_{Bi} = 2I_{Di} = 2\alpha g_{mi} = 2\alpha\frac{A_{Vi}C_{Li}}{\tau_i}, \quad i = 1, 2. \tag{3}$$

The load capacitances for the two preamplifiers are $C_{L1} = C_{in2}C_C/(C_{in2} + C_C) = \nu C_{in2}$ and $C_{L2} = C_{ilatch}$. Thus, the total preamplifier current is

$$I_{pre} = 2\alpha\frac{A_{V2}C_{ilatch}}{\tau_2}\left(1 + \alpha\beta\nu\frac{A_{V1}}{\tau_1}\right). \tag{4}$$

Note that $\alpha\beta = C_{ini}/g_{mi} \approx 1/(2\pi f_T)$, where $f_T$ is the cutoff frequency of the transistor. Thus, the second addend above represents how close the circuit is operating to the $f_T$ of the device. Assuming the device $f_T$ is well above the circuit operating frequency ($\alpha\beta\nu A_{V1} \ll \tau_1$), (4) simplifies to

$$I_{pre} \approx 2\alpha\frac{A_{V2}C_{ilatch}}{\tau_2}. \tag{5}$$

To minimize the current, $A_{V2}$ should be minimized and $\tau_2$ should be maximized; however, that would cause the constraint

[1]The actual current density is chosen as discussed in Section IV-C.

$\alpha\beta\nu A_{V1} \ll \tau_1$ to be violated. In addition, using low gain stages was necessary to implement the preamplifiers in deep submicron processes with limited output resistance and low voltage supplies. Therefore, a near-optimal result is to fix $A_{V1} = A_{V2}$ and $\tau_1 = \tau_2$. Substituting (1) and (2) into (5) produces

$$\begin{aligned} I_{pre} &= 2\alpha\sqrt{\frac{2^{b+1}V_{OL}}{\nu V_{FS}}} \cdot 4\ln 2 \cdot (b+1) f_s C_{ilatch} \\ &\approx \frac{\alpha 2^{7/2}\ln 2}{\nu^{1/2}V_{FS}^{1/2}} \cdot b 2^{b/2} f_s \sqrt{V_{OL}} C_{ilatch} \\ &= \xi b 2^{b/2} f_s \sqrt{V_{OL}} C_{ilatch}. \end{aligned} \tag{6}$$

The last two terms above represent the preamplifier current dependency upon the latch. The offset and input capacitance of the latch is related by the matching properties of transistors. When threshold voltage variation is the dominant source of mismatch, $V_{OL} \propto 1/\sqrt{A_{latch}} \propto 1/\sqrt{C_{ilatch}}$, where $A_{latch}$ is the area of the latch transistors [15]. Thus, the product term $\sqrt{V_{OL}}C_{ilatch}$, and correspondingly the preamplifier current, can be minimized by designing a latch with smaller transistors and larger input referred offsets. This tradeoff is limited by the maximum gain available from the two-stage preamplifier.

The total comparator energy per conversion, including the contribution of the latch, is

$$E_{comp}^{SAR} = \frac{b+U}{f_s} I_{pre} V_{DDA} + b C_{latch} V_{DD}^2. \tag{7}$$

Here, $V_{DDA}$ and $V_{DD}$ are the analog and digital voltage supplies, respectively, and $C_{latch}$ represents the total switched capacitance in the latch, which scales in proportion with its input capacitance. Conveniently, increasing the latch offset to reduce comparator bias currents also reduces the latch energy.

*2) DAC Capacitor Array:* The capacitor array is a set of $b$ binary-scaled capacitors and an extra unit capacitor. The well-known procedure to switch the array can be found in [16]. During the bit-cycling, an amount of charge proportional to the size of the array and the full-scale input voltage is switched onto the array. Assuming that this charge is supplied by a linear regulator or buffer connected to the analog voltage supply $V_{DDA}$, the total array energy per conversion is

$$E_{array} = 2\eta 2^b C_0 V_{DDA} V_{FS}. \tag{8}$$

The total energy drawn is input-signal dependent, which can be modeled using $\eta(V_{IN})$ (see, e.g., [17]), but setting $\eta = 0.7$ is a reasonable approximation. The initial factor of 2 arises from the use of a fully differential capacitor array.

The unit capacitor size $C_0$ is chosen to meet the linearity specification. The expected worst case linearity error occurs at the MSB transition, with a ratio error of

$$\frac{\Delta C}{C} = \frac{1}{\sqrt{2^{b-1}}} \frac{\Delta C_0}{C_0} \tag{9}$$

where $\Delta C_0$ represents the standard deviation of the unit capacitance. In order to maintain this error below the level of the least significant bit (LSB), $\Delta C_0/C_0$ is proportional to $1/2^{b/2}$. Noting that $\Delta C_0/C_0 \propto C_0^{-\zeta}$ with $\zeta$ equal to 3/4 or 1/2 if the capacitance mismatch is dominated by edge effects or oxide variation, respectively, [18] the total array energy for one conversion is

$$E_{array}^{SAR} = 2\eta 2^{(1+1/2\zeta)b} \frac{C_0'}{2^{b'/2\zeta}} V_{DD} V_{FS} \tag{10}$$

where $C_0'$ is the process-dependent capacitance required for matching to the $b'$-bit level.

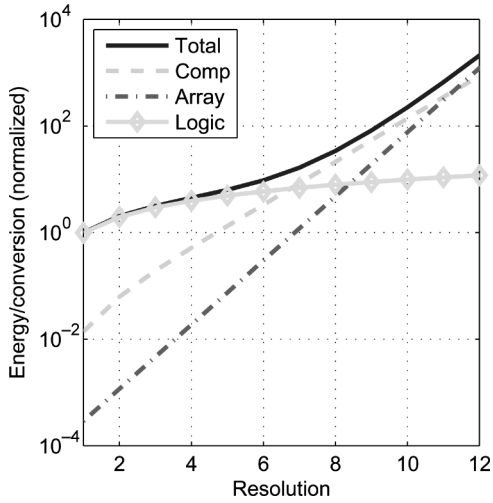


Fig. 3. Theoretical SAR energy versus resolution, along with the individual comparator, array, and logic components, all normalized to the 1-bit level.

*3) Control Logic:* The control logic for a SAR converter is based on a shift register of width $b$ and consumes energy that grows approximately with $b$. For a given logic style that does not draw static current (e.g., static CMOS, dynamic, etc.), the total energy consumed by the switching of the control logic over one conversion is

$$E_{logic}^{SAR} \approx b C_{SWeq}^{SAR} V_{DD}^2 \tag{11}$$

where $C_{SWeq}^{SAR}$ is the total switched capacitance normalized to the 1-bit level.

In a practical implementation, the total energy is expected to grow faster than $b$. The digital logic directly drives the switches in the capacitor array. These switches must increase with the resolution to ensure sufficient settling time of the larger capacitor array. Thus, the total digital energy is the sum of the internal switching energy, which grows linearly with resolution, and the fanout energy to drive the swtiches. For the resolutions considered here, the fanout is less than the internal energy and is therefore ignored.

Summing (7), (10), and (11), the total SAR energy per conversion is

$$\begin{aligned} E_{SAR} = {} & \xi b(b+U) 2^{b/2} \sqrt{V_{OL}} C_{ilatch} V_{DDA} + 2\eta 2^{(1+1/2\zeta)b} \\ & \times \frac{C_0'}{2^{b'/2\zeta}} V_{DD} V_{FS} + b\left(C_{latch} + C_{SWeq}^{SAR}\right) V_{DD}^2. \end{aligned} \tag{12}$$

A plot of (12) versus resolution is shown in Fig. 3, where three different regions are clearly seen. At low resolutions, the digital energy dominates, and the energy grows linearly with $b$. At some point, the comparator begins to dominate, with energy growing as $b^2 2^{b/2}$. Finally, at high resolutions, the growing

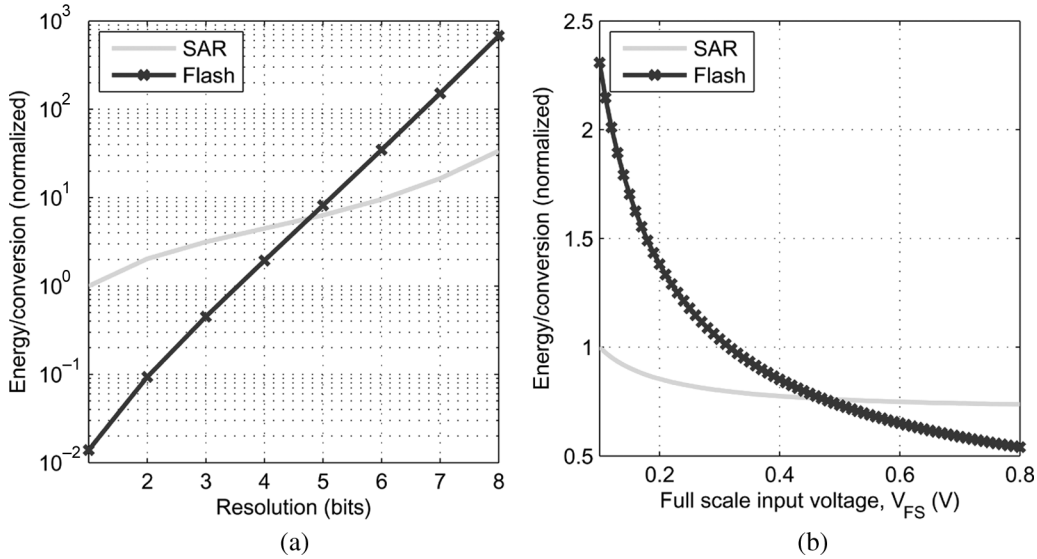


Fig. 4. Modeled SAR and flash ADC energies versus (a) resolution and (b) full scale input voltage. (a) $V_{FS} = 300$ mV; (b) $b = 5$.

size and matching requirements of the capacitor array dominate, and the energy grows as $2^{(1+1/2\zeta)b}$; however, the model is valid for at most 7 bits of resolution due to the gain limitation in the preamplifier and the neglect of noise and other nonidealities.

### B. Flash Energy Model

A flash ADC is composed of a bank of $2^b - 1$ comparators (neglecting those used for overrange detection), a resistor reference ladder, and a thermometer-to-binary encoder [16]. For the same sampling rate and full scale voltage, each of the flash comparators has the same requirements as the SAR comparator. The reference resistor ladder and thermometer-to-binary encoder energies scale roughly as $2^b$ but are usually less than the total comparator energy. Therefore, the energy per conversion for a flash ADC is

$$E_{flash} = 2^b \left( \xi b 2^{b/2} \sqrt{V_{OL}} C_{ilatch} V_{DDA} + C_{latch} V_{DD}^2 \right). \tag{13}$$

### C. Architecture Comparison

The theoretical SAR and flash energies are plotted versus resolution and full scale input voltage in Fig. 4(a) and (b), respectively, with all of the process-dependent constants derived from simulations in the chosen 0.18-$\mu$m CMOS technology. At 5 bits and above, the SAR ADC has the better energy efficiency, whereas its digital overhead limits its performance at the lowest resolutions; however, the savings at 5 bits are slim (approximately 30%), so the design must be careful so as not to increase the digital power consumption significantly. Similarly, at large full scale input voltages, the comparator energy becomes relatively small compared to the array and digital energies, with the flash outperforming SAR for $V_{FS}$ greater than about 0.45 V.

One observation from (12) and (13) is that, as a result of the simplified preamplifier current of (5), neither topology's energy depends upon the sampling rate. This holds as long as the preamplifiers are operating well below their cutoff frequencies and the delay through digital logic is much less than the time available for analog settling.

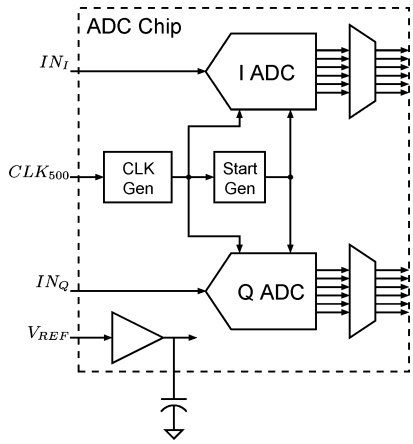


Fig. 5. Simplified chip block diagram.

Finally, this energy model can be used to provide some insight into expected energy advantages of different design choices and process generations. The principal advantage that SAR has over flash is that it requires only $b$ instead of $2^b$ comparators. As the energy of an individual comparison decreases relative to the SAR digital power, flash will be more attractive. Conversely, as the digital power decreases, SAR will outperform flash. In deep-submicron CMOS, the digital energy experiences the greatest benefit (both $V_{DD}$ and $C_{SWeq}^{SAR}$ shrink). The comparator energy also improves, as $V_{DDA}$ and $C_{ilatch}$ decrease but not at the same rate as the digital. One potential limitation is the reduction of $V_{FS}$, which tends to increase preamplifier current [see (6)].

## III. Top-Level Implementation

Time-interleaved SAR has been chosen here because it is expected to be lower power than flash at 5 bits. The prototype contains two identical ADCs, a start signal generator, a reference voltage buffer, and a clock generation block, as shown in Fig. 5. The reference voltage buffer is used to drive the bottom plate of the capacitor arrays with a reference voltage that is externally set between 100–500 mV. It must have sufficiently low output

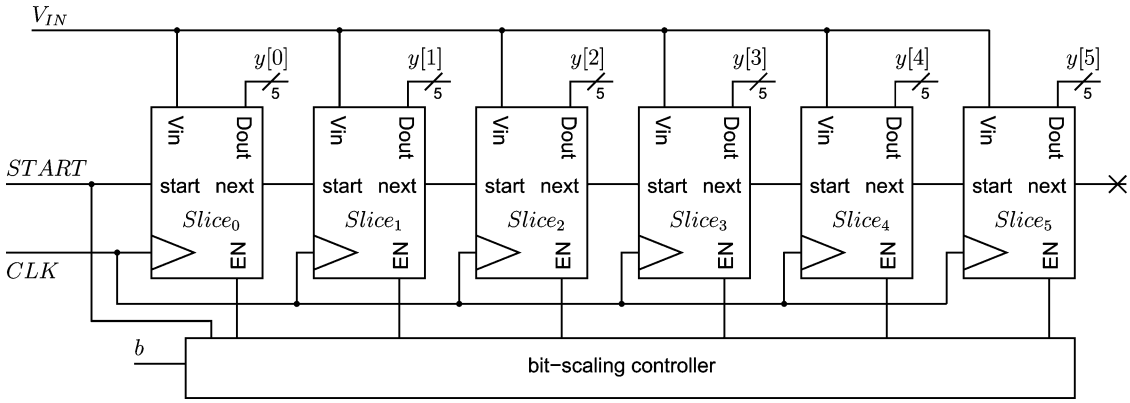


Fig. 6. Top-level block diagram of one of the two ADCs on chip.

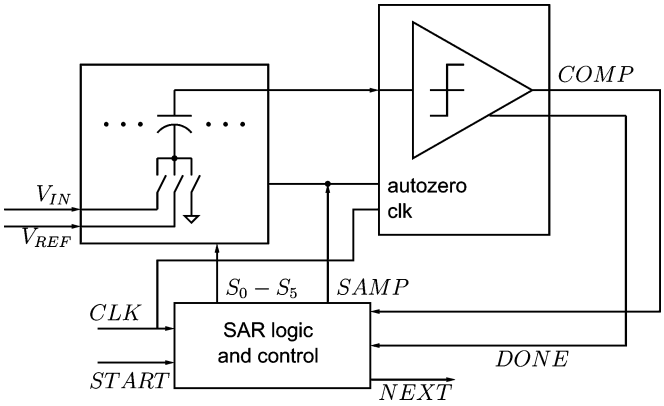


Fig. 7. Channel block diagram.

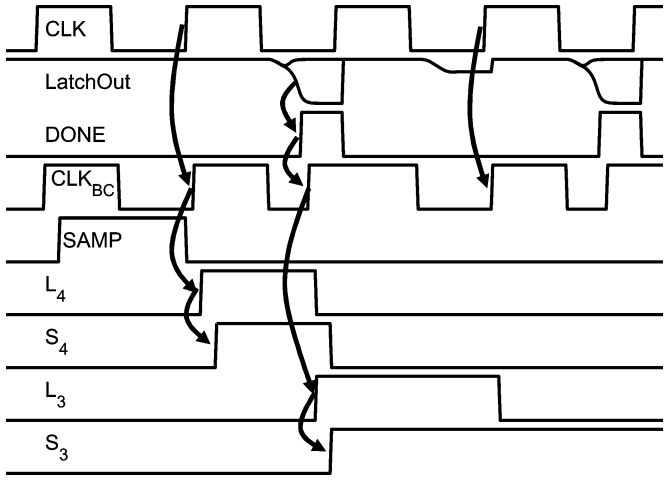


Fig. 8. Timing diagram showing sampling and the first three periods of bit-cycling. In the first bit-cycle, the *DONE* signal triggers $CLK_{BC}$ to start the next bit-cycle, whereas the second period shows that bit-cycling is triggered by *CLK* when the latch is metastable.

impedance to supply the roughly 500 $\mu$A average current drawn by the capacitor arrays. An external 0.1 $\mu$F decoupling capacitor is used to filter out the high-frequency current pulses that are drawn at the sampling frequency. The clock generation unit contains a high-speed amplifier chain for use with a low-swing external clock.

To make the channel internal clock synchronous with the sampling clock, thereby minimizing clock distribution overhead, six time-interleaved channels are used for the 5-bit converter (one of the assumptions in Section II-A with $U = 1$). Therefore, only a single global clock is shared by all the channels, eliminating complex circuitry to produce multiple phase shifted clocks. A second benefit of this choice is that all critical sampling edges are aligned to the same shared clock; timing skew is minimized by careful layout matching of the input and clock paths. Each of the channels begins a conversion upon receiving a start signal generated by the previous channel. A global start signal triggers the first channel in both the I and Q ADCs on the chip. The top-level block diagram of one ADC is shown in Fig. 6. The start generation block is common to both ADCs to ensure synchronized outputs. A full clock period is devoted to the generation and propagation of the start path between channels, so time-interleaving and synchronization are achieved with minimal overhead.

Each channel, as shown in Fig. 7, is similar to a generic SAR ADC, with the addition of the signals for synchronization with the other channels and a *DONE* feedback signal from the comparator needed for self-timed bit-cycling, described below. The figure shows a single-ended path, but the actual implementation is fully differential. The circuit details of the channel sub-blocks are described in the next section.

## IV. Channel Circuits

### A. Self-Timing

One disadvantage of the SAR architecture is the feedback required between successive clock periods. Specifically, the result of the previous comparison is necessary to generate an improved estimate for determining the next bit. While this feedback path is entirely digital, its latency must be minimized to allow maximum time for analog signals to settle in the DAC capacitor array and preamplifiers.

To decrease the latency during bit-cycling, self-timing is used [19], wherein the latch triggers the start of the next bit-cycle when it has resolved a value. In effect, after the latch output has settled, the remainder of the second half of the clock period is borrowed by the DAC and preamplifiers for the next bit. Self-

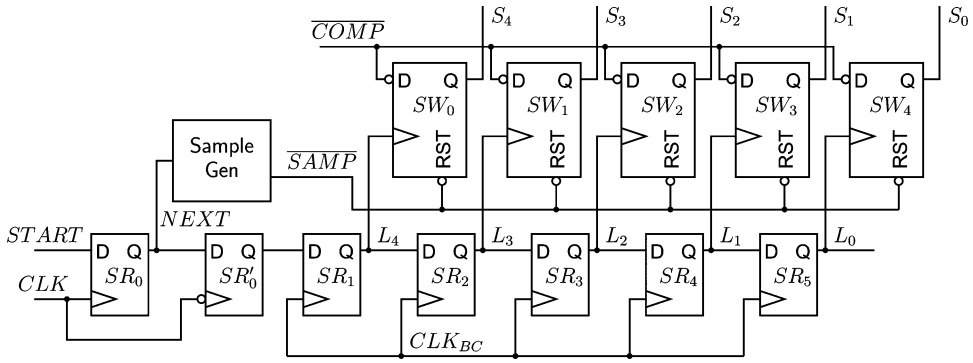


Fig. 9. The SAR logic implementation. The shift registers $SR_0$–$SR_5$ clock one of the switch drive registers $SW_0$–$SW_4$ during every phase of bit-cycling. The outputs $S_0$–$S_4$ control the DAC capacitor array.

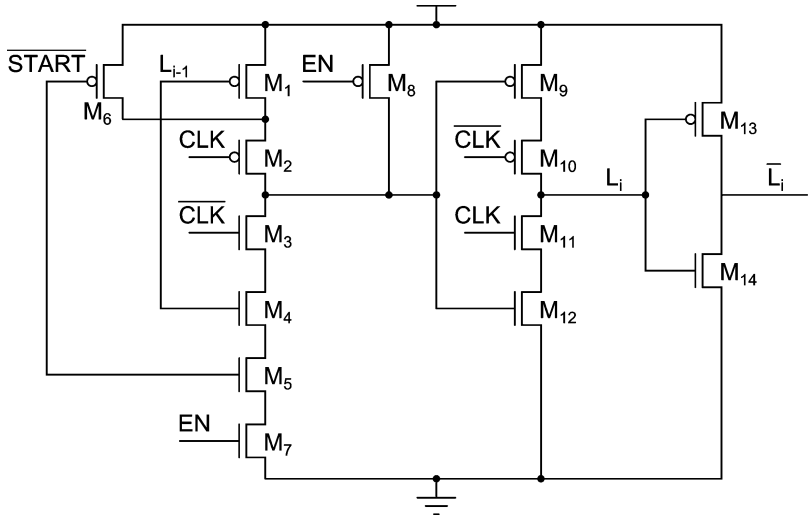


Fig. 10. Resettable shift register built on C$^2$MOS latch.

timing is particularly useful because the latch typically resolves in much less than 1 ns (half the clock period).

The timing of the ADC is shown in Fig. 8, which considers the sampling operation and the first three bit-cycles. The assertion of *SAMP* is delayed from the rising edge of the shared system clock (*CLK*) to avoid a high-frequency current impulse on the analog inputs at the same time that the previous channel finishes sampling. During bit-cycling, the regeneration of the latch is always triggered by the falling edge of *CLK*. In the first bit-cycle, the latch resolves quickly, asserting the *DONE* signal (XOR of the latch outputs). This causes $CLK_{BC}$, the bit-cycling clock, to transition high immediately, rather than waiting for the rising edge of *CLK*. During the second period, the latch output is metastable and does not resolve. In this case, the rising edge of $CLK_{BC}$ is triggered by *CLK*, and bit-cycling continues as normal. In simulation, self-timed bit-cycling extends the period given to settling of the capacitor array and preamplifiers by up to 20%.

### B. SAR Logic

To implement a fast SAR controller, the logic, shown in Fig. 9, consists of a shift register ($SR_0$–$SR_5$) and a set of switch drive registers ($SW_0$–$SW_4$). This topology allows the larger switch drive registers to be clocked only once per conversion as opposed to every clock period like the smaller shift registers, while keeping the critical path delay to only $2t_{c-q}$, where $t_{c-q}$ is the delay from the rising clock edge to valid outputs of a flip-flop. The current bit being resolved is determined by $L_4$–$L_0$, only one of which is high every period. $S_i$ goes high on the rising edge of $L_i$ at the start of the $i$th bit-cycle. When $L_i$ falls, the decision for that bit is made, bringing $S_i$ back low only if *COMP* is high.

Both the shift registers and the switch drive registers are implemented using full custom logic. The shift registers $SR_0$–$SR_1$ are conventional C$^2$MOS registers, while $SR_2$–$SR_5$ have been modified as shown in Fig. 10. Transistors $M_1$–$M_4$ and $M_9$–$M_{12}$ form two C$^2$MOS latches, with $M_{13}$–$M_{14}$ producing the complementary output. $M_5$–$M_6$ provide a reset operation, ending bit-cycling whenever *START* is received by the channel. When this channel is not enabled (e.g., due to bit scaling, see Section IV-D), $M_7$–$M_8$ force $L_i$ low.

The switch drive logic function is implemented in the single register shown in Fig. 11. Transistor $M_1$ provides a fast charge path for $S_i$ upon the rising edge of $L_i$. $M_4$–$M_7$ form a C$^2$MOS latch that holds the value of $\overline{COMP}$ after the falling edge of $L_i$ and discharges $S_i$ through $M_2$–$M_3$. During sampling, $M_{12}$–$M_{14}$ reset $S_i$ low. Transistors $M_8$–$M_{10}$ are used to precharge node $a$ to avoid charge sharing effects when $M_2$

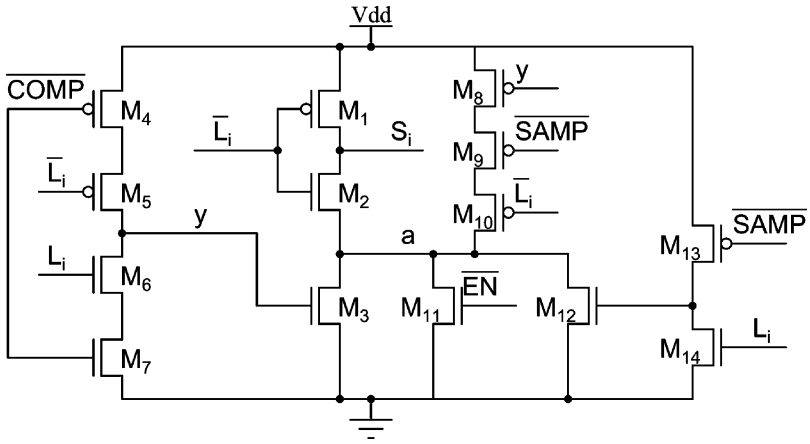


Fig. 11. Schematic of the switch drive registers.

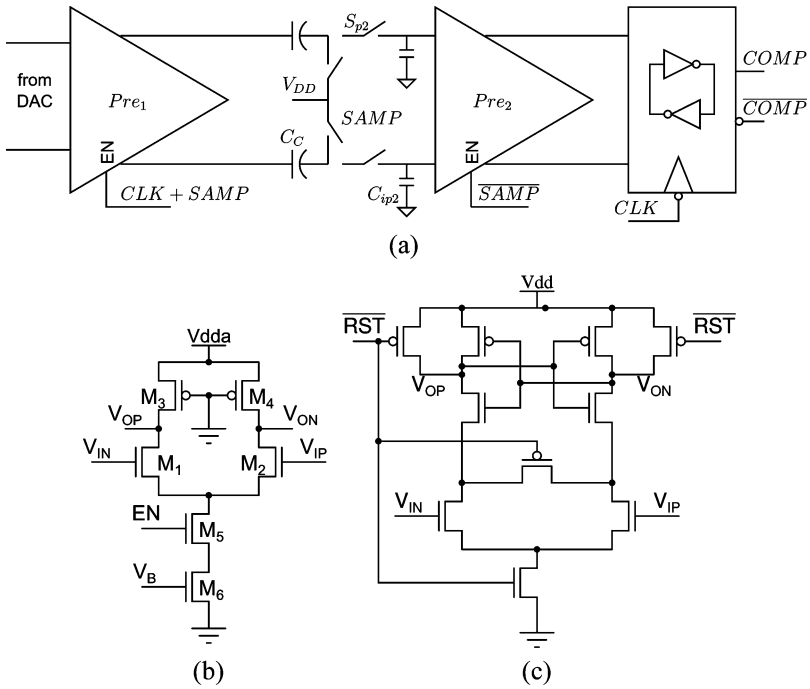


Fig. 12. (a) Comparator diagram with (b) duty-cycling preamplifier and (c) conventional latch schematics.

turns on. Finally, $M_{11}$ puts the register in a known state when disabled.

Using this custom logic allows a faster and lower power SAR implementation. In simulations, the custom logic was 58% faster while consuming only 20% of the power of an equivalent SAR built using standard cells and static feedback flip-flops.

### C. Comparator Design

The comparator of Fig. 1 has been modified as shown in Fig. 12(a) by adding preamplifier enable signals and switches $S_{p2}$. The preamplifiers, shown in Fig. 12(b), have been designed using the equations presented in Section II-A1, with $M_5$ added to enable duty cycling. The pMOS transistors $M_3$–$M_4$ operate in the linear region and function as the loads $R_L$. The bias current density has been set by considering (4). Ignoring the second term, minimum energy corresponds to operating at low $\alpha$ (high $g_m/I_D$), which suggests operating in moderate to weak inversion. Unfortunately, the $f_T$ of the transistors drops in moderate inversion, and a suitable current density in strong inversion has been chosen to enable the high operating speeds $(A_{V2}/(2\pi\tau) \approx 2$ GHz$)$. The preamplifiers' simulated frequency performance is shown in Fig. 13. The latch, Fig. 12(c), is a conventional sense-amplifier flip-flop [20].

In order to reduce average current draw, the preamplifiers are duty-cycled using $M_5$ and $S_{p2}$ to turn off their currents when appropriate. While sampling of the input, the output offset voltage of $Pre_1$ is stored on capacitors $C_C$, while $Pre_2$ is disabled. During the first half of every bit-cycling period, *CLK* is high (see Fig. 8) and the preamplifiers are actively settling. When *CLK* goes low, the preamplifiers are assumed to have settled and are holding their outputs steady, so switches $S_{p2}$ are opened, storing the first preamplifier's output on $C_{ip2}$, the parasitic capacitance at the input to the second preamplifier, and the current

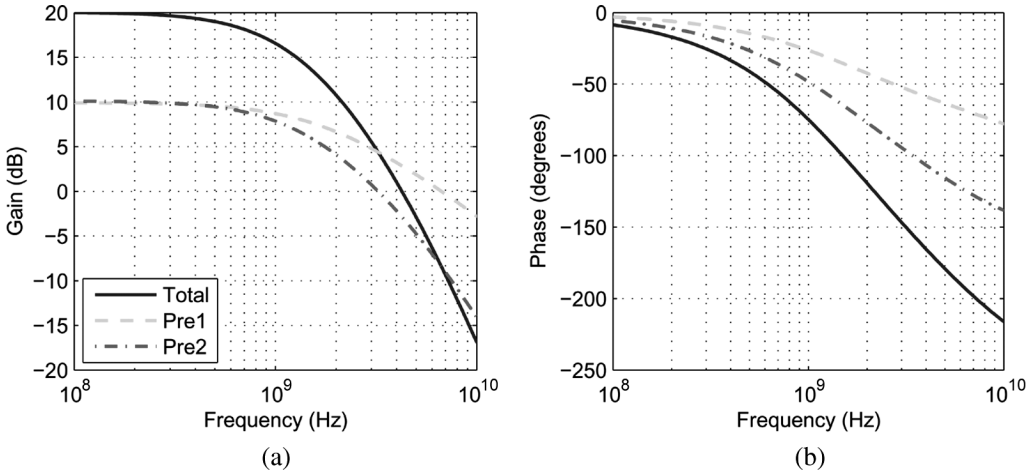


Fig. 13. Simulated (a) gain and (b) phase of the preamplifiers.

through $Pre_1$ is disabled. The energy savings are proportional to the amount of time that $Pre_1$ is disabled; however, due to the self-timed bit-cycling, this might be very short. In this prototype, $Pre_1$ is clocked by the 50% duty cycle *CLK*. The extra time from early switching of $CLK_{BC}$ is used to for the settling of the capacitor array. Even though this extra time is not used directly by the preamplifiers, duty cycling does improve the settling time because after $Pre_1$ is disabled by turning off $M_5$, both $V_{OP}$ and $V_{ON}$ float to $V_{DDA}$, yielding a zero differential output and effectively recovering from any overdrive condition that occurred in the previous bit-cycle.

### D. Bit-Scaling and I/O Circuits

For flexibility in response to varying system requirements, the ADC is capable of scaling the output resolution $b$ from 1 to 5 bits at a constant sampling rate. Since each channel takes $b+1$ periods to resolve output, fewer channels are needed to maintain the same throughput; the unused 5-bit channels are disabled by stopping the propagation of the *START* signal, gating the clocks, and shutting off all bias currents. The start generation block triggers the first channel at a higher rate. When a channel receives the *START* signal, it samples during the next clock period, and the sampling operation automatically resets bit-cycling at the correct, lower resolution.

To reduce circuit board requirements between the ADC and the digital back-end of the UWB transceiver, the outputs of the channels are not serialized, yielding an output frequency of 83 MHz. When not operating in the full 5-bit mode, some of the channels are deactivated. Rather than placing the burden on the back-end chip to sort the ADC outputs, a mux tree (see Fig. 5) is implemented to maintain a constant 83 MHz output rate independent of the resolution, with the unused LSBs of each word forced to 0. Level conversion circuits are placed between the core ADC and the I/O circuits to allow an internal digital supply lower than 1.8 V while still maintaining the proper voltage for inter-chip communication.

## V. Measured Results

The dual ADC chip was fabricated in a 0.18-$\mu$m CMOS process with poly-poly capacitors. The photograph of the

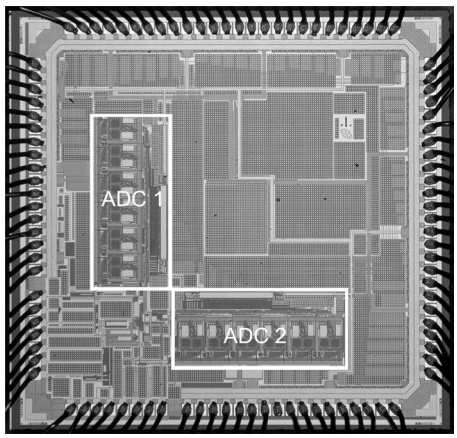


Fig. 14. Die photograph of ADC chip in 0.18-$\mu$m CMOS. Total active area is 1.1 mm$^2$.

5.5 mm$^2$ die is shown in Fig. 14. The active area of each ADC is 1 mm $\times$ 0.5 mm. With a 500-MHz sampling clock, the ADC exhibits an INL and DNL of $-0.26/0.42$ and $-0.39/0.33$ LSBs, respectively, as shown in Fig. 15 and measured using a code density test with a full swing sinusoidal input [21].

For dynamic testing, the Tektronix AWG710 arbitrary waveform generator was used to generate the sinusoidal input using an 8-bit 4 GS/s DAC. The AWG710 also provided the 500-MHz system clock; this clock source provides $<5$ ps rms jitter. The dynamic performance at 500 MS/s is shown in Fig. 16(a). The periodic behavior of the signal-to-noise-plus-distortion ratio (SNDR) is due to the time-interleaving. At the peak of the SNDR curve, the input frequency is aliased, with reference to the channel sampling rate, to low frequencies. The low effective resolution bandwidth (ERBW) is a result of insufficient settling time in the input sampling network. This is verified with the SNDR plot of Fig. 16(b) measured at 125 MS/s, where the ERBW exceeds Nyquist and the ADC has a figure of merit $(P/(2\text{ERBW}\cdot 2^{\text{ENOB}}))$ of 1.1 pJ/conversion step.

The fast Fourier transform (FFT) of a 170.56-MHz input sampled at 500 MS/s is shown in Fig. 17. The dominant harmonics are labeled. The spurs from offset between channels at multiples of $f_s/6$ and from timing skew at $f_s/6 \pm f_{\text{in}}$ are comparable to

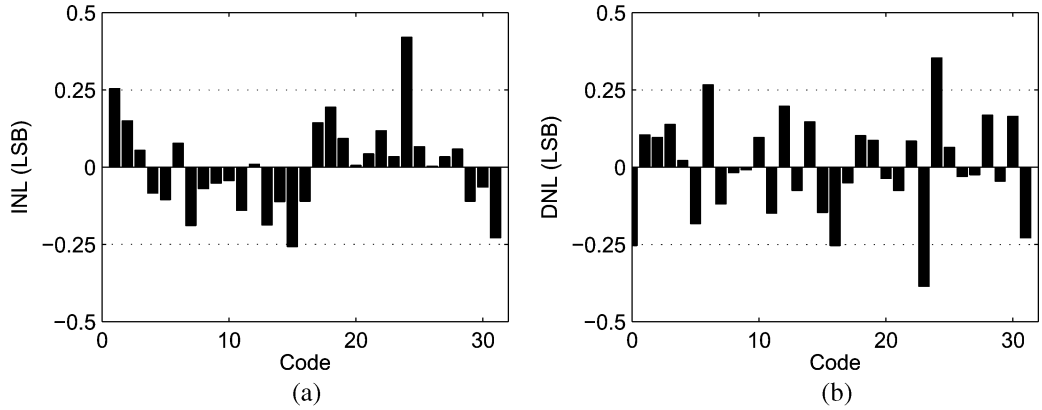


Fig. 15. Plot of the (a) INL and (b) DNL versus output code at 500 MS/s.

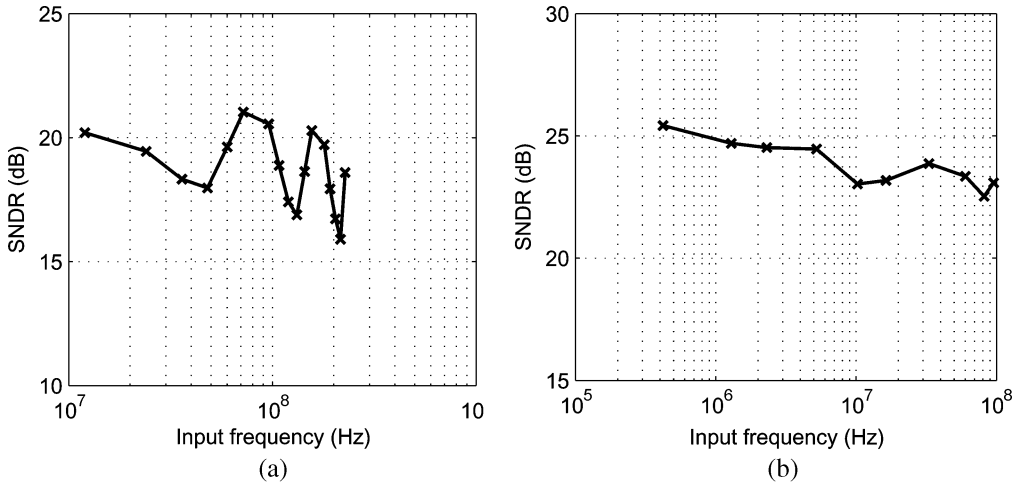


Fig. 16. Plot of SNDR versus input frequency at (a) 500 MS/s and (b) 125 MS/s.

those of the third harmonic at −38 dBFS. The spurious free dynamic range (SFDR) is better than 24 dB, and the total harmonic distortion (THD) is better than −15 dB for input frequencies up to over 300 MHz.

Each ADC draws 810 $\mu$A from a 1.2-V analog supply and 3.6 mA from a 1.8-V digital supply, for a total I/Q power consumption of 14.9 mW. Separating out the power for the comparators' latches (1.25 mW) from the total digital power, the logic consumes roughly 2.4 times the power of the comparators (the power drawn by the capacitor array is negligible). The energy model presented above predicts that this ratio should be 3.7 (see Fig. 3). The difference is a result of optimization of the digital logic compared to the first model and the preamplifiers operating at a nonoptimum bias point; as the ratio is lower than predicted, this further supports the original choice of SAR over flash.

The prototype includes an optional mode to disable the duty cycling of the preamplifiers. Duty cycling reduces the analog power by 15% at 500 MS/s and by 26% at 125 MS/s. At lower clock frequencies, the savings are greater because the overhead to charge and discharge the output capacitances of the preamplifiers is reduced in comparison to the integrated bias currents over the longer clock period. Power dissipation versus resolution is shown in Fig. 18. As predicted, analog and digital power vary linearly with the resolution. The digital power does not asymptotically approach zero because bit scaling only reduces the number of bit-cycling operations. The number of sampling operations remains constant, and sampling requires more energy than bit-cycling. The measurements are summarized in Table I.

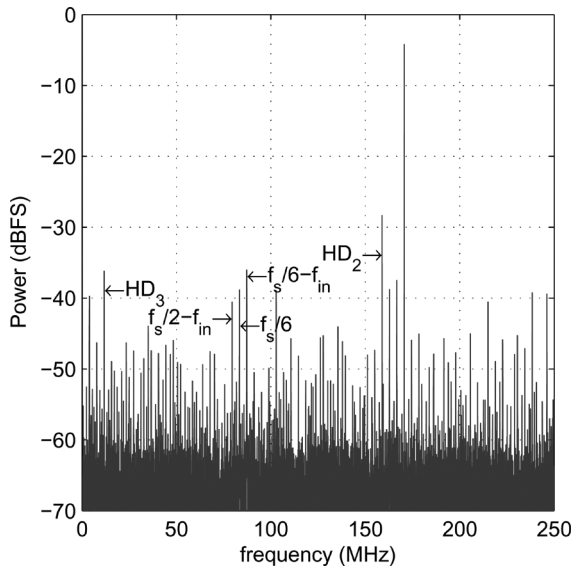


Fig. 17. FFT of a 170.56 MHz input signal sampled at 500 MS/s.

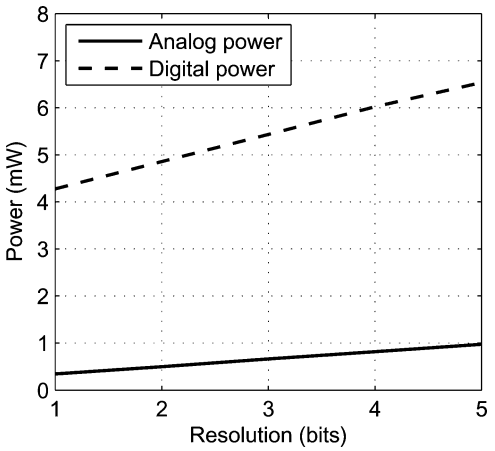


Fig. 18. Analog and digital power consumption versus resolution for 500 MS/s operation.

TABLE I
SUMMARY OF MEASUREMENTS PER ADC

| Process | 0.18$\mu$m, 1 poly, 5 metal CMOS | |
|---|---|---|
| Resolution | 5 bits | |
| Active area | 1 mm $\times$ 0.5 mm | |
| Input capacitance | 640 fF | |
| Input range | 800 $mV_{pp}$ (differential) | |
| Sampling rate | 500 MS/s | 125 MS/s |
| Analog power | 0.97 mW @ 1.2 V | 0.85 mW @ 1.2 V |
| Digital power | 6.5 mW @ 1.8 V | 0.82 mW @ 1.4 V |
| SNDR (DC) | 20.2 dB | 25.4 dB |
| SFDR | 24 dB | 39 dB |
| THD | -16 dB | -36 dB |

In addition, the ADC has been successfully tested as part of a complete UWB receiver capable of 100 MS/s wireless transmission [22].

## VI. CONCLUSION

A chip containing two 5-bit, 500-MS/s ADCs has been presented. Based on the results of a comparative energy model, a 6-way time-interleaved successive approximation register topology has been used. Each channel uses full custom logic and self-timing to minimize digital power dissipation and propagation delays. Duty cycling of the static bias currents in the comparator further saves power. A resolution scaling mechanism has also been included to conserve power in response to changing system requirements. The two synchronized ADCs are suitable for use in a low-power I/Q receiver for ultra-wideband radio. While the effective resolution bandwidth is limited at the maximum sampling rate, peak dynamic performance and good energy efficiency are achieved at 125 MS/s.

## APPENDIX

Below is a listing of all the variables used in the energy models and their definitions.

| | |
|---|---|
| $\alpha$ | Ratio of drain current to transconductance ($\equiv I_D/g_m$) |
| $A_V$ | Total gain of preamplifiers |
| $A_{Vi}$ | Gain of preamplifier $i$ |
| $b$ | Resolution of the converter, in bits |
| $\beta$ | Ratio of input capacitance to drain current ($\equiv C_{\rm in}/I_D$) |
| $C_0$ | Unit capacitor size in array |
| $C_C$ | Size of output offset storage capacitor |
| $C_{ilatch}$ | Input capacitance of latch |
| $C_{ini}$ | Input capacitance of preamplifier $i$ |
| $C_{latch}$ | Total switched capacitance of latch |
| $C_{Li}$ | Load capacitance of preamplifier $i$ |
| $C_{SWeq}^{SAR}$ | Equivalent switched capacitance of digital SAR |
| $\zeta$ | Capacitor mismatch exponent |
| $\eta$ | Input-signal dependent coefficient of capacitor switching energy |
| $f_s$ | Sampling frequency |
| $f_T$ | Transit frequency of NFET in preamplifier |
| $g_m$ | Transconductance of NFET in preamplifier |
| $I_{Bi}$ | Current bias of preamplifier $i$ |
| $I_D$ | Quiescent drain current of NFET in preamplifier |
| $I_{pre}$ | Total current through both preamplifiers |
| $\xi$ | Coefficient for preamplifier current (see (6)) |
| $M$ | Number of parallel time-interleaved SAR channels |
| $\nu$ | Voltage loss across offset output storage capacitor |
| $R_{Li}$ | Load resistance of preamplifier $i$ |
| $\tau$ | Combined time constant of preamplifiers |
| $\tau_i$ | Time constant of preamplifier $i$ |
| $U$ | Number of periods for sampling in SAR ADC |
| $V_{DD}$ | Digital power supply voltage |
| $V_{DDA}$ | Analog power supply voltage |
| $V_{FS}$ | Full scale input voltage |
| $V_{OL}$ | Input referred offset voltage of the latch |

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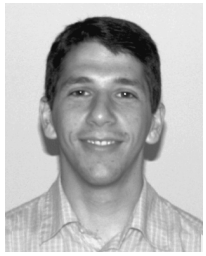

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