CDAC Sizing and Design

Known:

- A_C for 65nm MOM Caps
- ~~σ_V for 12-bit~~
- Bit resolution
- Supply voltages/Ref
- M:N expansion
- 10MHz operation

$\sigma_{V_{th}}$ for 12-bit

Signal σ_{KSNS}

2^{N-1} weights

C_{tot} minimum (plus some margin)

2^{N-}

check! $C_{tot} \sim C_{tot\,min}$?

- Differential + comp bandwidth vs switch

Reduced substrate and supply noise sensitivity

and Async switch "dubbing"

Notice here how we don't constrain power or area. We simply calculate their result in feed forward. (we just constrained performance)

~~Find weights for Cap:~~

Find tolerable σ_C for unit cap given M

costs area and worsens dynamic settling

wrong perspective!

Radix → gives radix M/N 2

Because what we actually care about is

$$\sum_{i=0}^{N-1} C_i - C_n \geq 0$$

is satisfied for all C_i, with high probability even ($\sim 3\sigma = 99.85\%$) after mismatch variation.

See: A. Hsu, 2013, pg 69-73, "Amount of Redundancy"

M. Pelgrom, 2022,
pg. 144 % Matching/FF
pg. 298 Cap mismatch models
pg. 374 – 377 mismatch @ MSB
pg. 760 – 763, SAR example calc
pg. 768 mismatch vs sampling noise

And Math from: P. Harpe 2018, pg. 3.

Choose weights (Redundancy)

For M-1 cycles since C_{DAC} is N-1 resolution given weights

Options Are

- Repeated bits insertion
- Binary compensation
- Binary recombination ✓Best
- Sub-2 Radix, quantized/normed
- Radix-2

interaction here as some weights are nicer to layout

- Determines which weight will be ~~unit device in terms of mismatch~~ correspond to the sizing of LSB device for finding mismatch.

From σ_V/unit calculate this Cunit Capacitor's Size

Choose ~~Attenuation~~ coarse-fine division pos.

- Normal/full unit caps
- RDAC VREF
- BridgeCap
- Unit Length Caps

+ (1 < ~~BP~~ CFP < M-1) coarse fine ~~Bridge~~ position

In these three cases, Linearity will be additionally degraded due to "coarse – fine" mismatch