Non-binary Successive Approximation Analog-to-Digital Converters: A Survey

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***Abstract*—Low-power successive-approximation (SA) analog-to-digital converters (ADCs) are attracting increasing attention these days in biomedical and sensor network applications. The binary search algorithm is one of the basic idea behind how they obtain a binary code representing an analog input. In practice, the imperfectness of analog circuit elements sometimes results in decision errors and decreases the resolution of A/D conversion. Thus, making accurate decisions using imperfect elements is a big challenge. This paper surveys one solution known as non-binary SA with redundancy as well as related topics and its application to state-of-the-art SA ADCs.**

I. Introduction

Analog-to-digital and digital-to-analog converters (ADCs and DACs) play an important role in information and communications technology (ICT), because when computers and cellular phones communicate with one another, digital data should be converted into analog signals in the real world, such as electromagnetic waves. For further progress in ICT, various types of ADCs and DACs have been investigated intensively. Among such studies, the successive approximation (SA) algorithm [1], [2] has recently attracted increasing attention because of its high energy efficiency, which is a big advantage when used in low-power applications, such as wireless sensor networks and biomedical sensing [3–10].

The SA algorithm is based on a binary decision step, where the analog input signal is converted into a binary output word from the most significant bit (MSB) to the least significant bit (LSB), as shown in Fig. 1. If an N-bit output is required, the step is repeated by N times. Conventionally, this limits the conversion speed of SA ADCs compared with other types of ADCs, such as pipelined and flash ADCs. Recently, however, the operating speed of SA ADCs has been greatly improved as the transistor size has shrunk. Moreover, the time-interleaved scheme and two-bits-per-step (2b/step) decisions have led to the demonstration of multi-gigahertz ADCs based on SA [11–16].

In binary SA ADCs, if an error occurs somewhere during the decision steps, the following steps to determine LSBs do not make sense. In practical circuits, decision errors can occur for several reasons, including variations in MOSFET properties, mismatches between passive elements, and insufficient settling of the DAC output V_{DAC} shown in Fig. 1. The settling, in particular, is critical in high-speed operation. To solve this problem, many state-of-the-art SA ADCs use

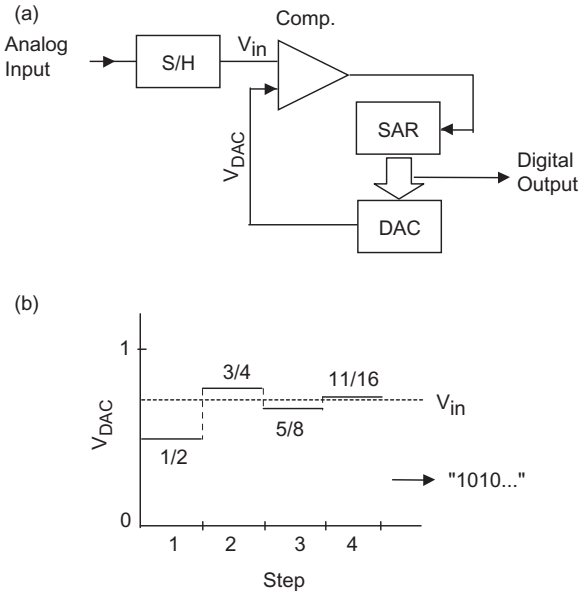

Fig. 1. (a) Block diagram of successive approximation (SA) ADC and (b) the output of a DAC.

non-binary approaches, which introduce redundancy in the bit-decision steps so that an error can be corrected in the following steps, as reviewed in [17], [18].

The purpose of this survey is to share a common understanding of the present status of non-binary SA ADCs among not only circuit and logic designers but also those persons interested in such an attractive algorithm that enables an appropriate digital output to be obtained using practical circuits with non-idealities. Section II describes the survey method and some statistics. Section III reviews several types of non-binary SA ADCs. Section IV briefly covers alternative error-correction techniques.

II. Survey method and statistics

Papers were surveyed mainly by using IEEE Xplore (ieeexplore.ieee.org) with keywords like non-binary, successive approximation, and redundancy. The survey also used Google

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Scholar. It turns out that 62% of articles extracted by Google Scholar were included in IEEE Xplore, 24% were patents, and 14% were papers published elsewhere. The last category includes university theses and transactions, some of which were also published in IEEE articles. Thus, we believe that our survey covered significant publications. Patents were not included in this survey.

The journal and conference titles where the papers were published are shown in Fig. 2. JSSC (IEEE Journal of Solid-State Circuits), ISSCC (International Solid-State Circuits Conference), and TCAS (IEEE Transactions on Circuits and Systems) were found to be major journals and a conference where SA ADCs appeared. The trend of the number of papers on SA ADCs over time (1966-2013) is shown in Fig. 3. The number increased exponentially, indicating the high level of activity in this field recently. It should be noted that a considerable number of papers were on SA ADCs using non-binary algorithms.

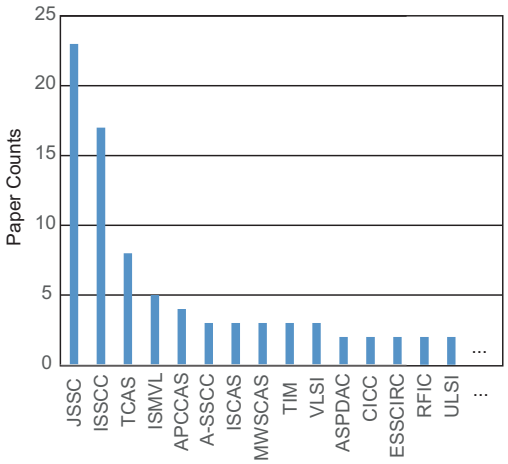

Fig. 2. Number of papers appearing in journals and conferences.

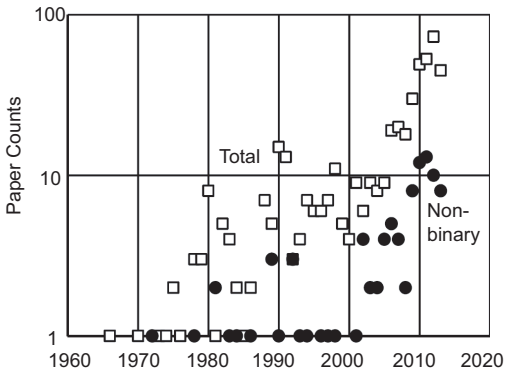

Fig. 3. Number of papers on SA ADCs.

III. Non-binary SA

A. *Radix* < 2

Since the input signal is compared with the internal DAC output in the SA algorithm, as shown in Fig. 1, the conversion resolution depends on the DAC output accuracy. The internal DAC conventionally consists of a binary-weighted capacitor array and/or an R-2R resistor ladder. However, the mismatches in capacitors and in resistors result in nonlinearity and/or non-monotonicity of the DAC output. To improve the characteristics even if the mismatches exist, non-binary SA algorithms were theoretically investigated [19–24].

A binary decision and a non-binary redundant decision are schematically shown in Fig. 4. In the former case, successive search areas denoted by the vertical bars decrease by a factor of 2 as the step is repeated. By contract, in the latter case, successive search areas are more than half the previous ones. Therefore, even if the first decision corresponding to the MSB was "0" (error) instead of "1" (correct) in this example, the error can be corrected by the following steps.

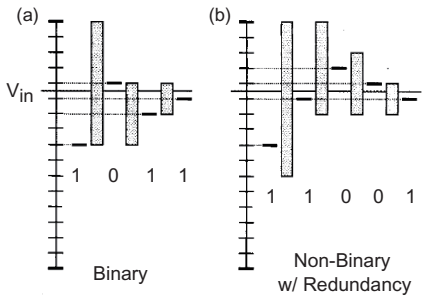

Fig. 4. (a) Binary decision ($radix = 2$) and (b) non-binary decision with redundancy ($radix < 2$) [25].

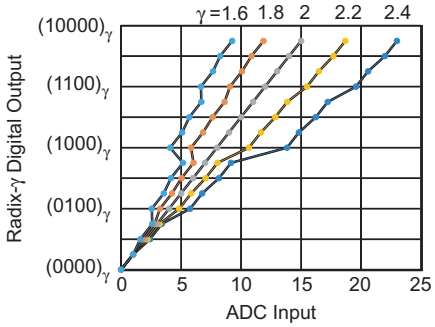

Fig. 5. Decimal number represented by different radixes (γ) from 1.25 to 3.

Consider an example of a 4-bit ADC. The function of the binary ADC is to find the digital output $(b_0 b_1 b_2 b_3)_2$ for the analog input V:

$$floor(V) = \sum_{i=0}^{3} 2^{3-i} b_i, \tag{1}$$

where $0 \leq V < 16$ is assumed. For a non-binary ADC with a radix γ, the above equation is modified to

$$floor(V) = \sum_{i=0}^{3} \gamma^{3-i} b_i. \quad (2)$$

The relation between the analog input V and digital output $(b_0 b_1 b_2 b_3)_\gamma$ is shown in Fig. 5. For $\gamma < 2$, the ADC input corresponding to $(1000)_\gamma$ is smaller than that corresponding to $(0111)_\gamma$. This means that there is redundancy in the bit-decision step, which is needed in correcting a decision error, and it is the reason $radix < 2$ is used in non-binary ADCs.

If $\gamma > 2$, a large quantization noise occurs for the input corresponding to the digital output between $(0111)_\gamma$ and $(1000)_\gamma$. This implies that in a practical circuit implementation of binary ADCs, where binary-weighted elements are used in the bit-decision steps, if the weighting factor happens to be slightly larger than two, then the quantization noise might be unacceptably large. This results in undesired distortions in the digital output. Thus, practical binary ADCs are regarded as being based not just $radix = 2$, but on mixed radixes where $radix \cong 2$ [19]. Thus, to avoid such errors, choosing a radix smaller than two is quite reasonable.

How to chose the optimum radix for a given tolerance was discussed in [21], for example, for the case of an R-bR ladder. The following condition was presented:

$$b > 2\frac{1+\epsilon}{(1-\epsilon)^2}. \quad (3)$$

Here, the tolerance ϵ is defined by $R_0(1-\epsilon) < R < R_0(1+\epsilon)$, where R_0 is the nominal resistance. The associated radix is given by

$$b = \frac{\gamma}{(\gamma-1)^2}. \quad (4)$$

Therefore, once the tolerance is known, an appropriate value for b, or radix γ, can be determined.

B. Circuit Implementation

There have been many reports on circuit implementation of non-binary SA ADCs [25–70]. Similar ideas are also applied effectively to pipelined ADCs [71–78], two-step ADCs [79–82], and algorithmic (or cyclic) ADCs [83]. The radixes used include 1.8 [27], [28], [70], 1.85 [26], 1.86 [42], [60], and 1.93 [75].

In conventional binary decision SA ADCs, a binary-weighted capacitor array is frequently used in circuit implementation. To minimize the mismatch between capacitors, they are arranged as follows: First, a unit capacitor C_u is defined, and then it is copied M times to make a parallel connection of M unit capacitors, which results in a capacitor with capacitance MC_u. For example, for a 4-bit SA ADC, a capacitor array consisting of $8C_u$, $4C_u$, $2C_u$, C_u is used. This makes it difficult to implement a $radix < 2$ SA ADC because the straightforward implementation requires a non-integer ratio in the capacitor values.

One can still use such a binary-weighted capacitor array [25], [32], but a lookup table and complicated switching sequences are required to obtain the non-binary decision. A smart solution to the implementation of a $radix < 2$ SA ADC is shown in Fig. 6 [31], [36], [40], [81]. The radix can be adjusted by choosing α and β, and a simple switching sequence similar to that used in the binary SA ADCs can be applied.

Another technique is known as a generalized non-binary algorithm, where a non-integer ratio of capacitances is not needed [33], [43], [45–47], [52], [54], [58], [59], [61], [63], [65], [69]. For example, a non-binary weight such as $\{128,46,26,20,14,8,6,4,2,1\}$ instead of the binary weight of $\{128,64,32,16,8,4,2,1\}$ was used to obtain 8-bit resolution [69]. The total capacitance was unchanged, which meant that the required Si area was also constant. In this case, 10 steps rather than 8 steps were required to complete the conversion. However, the sampling frequency was higher than that of conventional binary ADCs because the accurate settling, which sometimes took a long time, was not needed here.

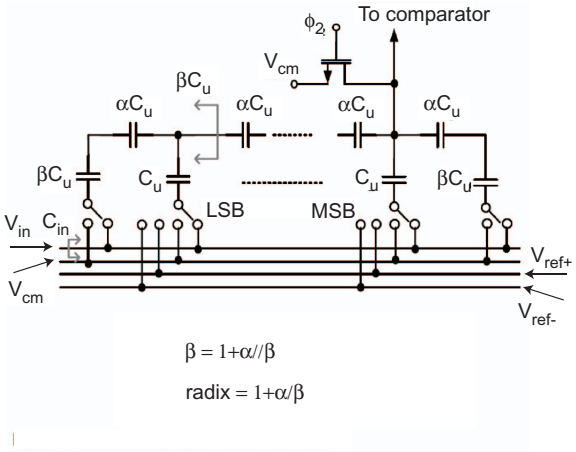

Fig. 6. Capacitance array used for SA ADC with $radix = 1 + \beta/\alpha$ [29].

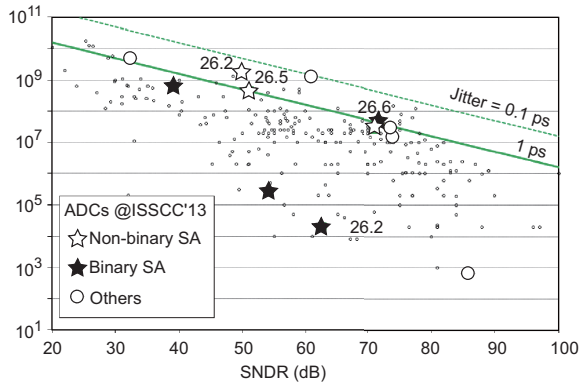

Fig. 7. ADC performance comparison. The numbers 26.2, 26.5, and 26.6 represent data reported in refs. [64], [65], and [66] (After http://isscc.org/doc/2013/2013_Trends.pdf).

The operating speed of non-binary SAR ADCs can be even

higher if one uses time-interleaved architectures and asynchronous operation modes, which result in over-GHz operation [35], [49], [56], [64–66]. ADC performances are compared in terms of bandwidth BW and signal-to-noise-and-distortion ratio (SNDR) in Fig. 7. BW is limited by the sampling-timing jitter, which is represented by the solid and dashed lines in Fig. 7 with jitters of 1 ps and 0.1 ps, respectively. The three plots labeled 26.x are for the non-binary SA ADCs presented at ISSCC 2013, which lead the technology trend towards wider BW, or in other words, higher speed operation.

The non-binary approach is also useful to obtain low-power operation, because of the relaxed settling condition. An 8.9-bit 150kS/s SA ADC based on a generalized non-binary redundant algorithm, such as $\{224,136,68,40,20,10,6,4,2,1\}$, has been demonstrated for bio-implantable devices. It was made possible by utilizing energy-efficient split-capacitor arrays and 0.18-μm CMOS technology [43].

IV. Alternatives

Various correction techniques have been proposed that differ from the non-binary approaches described above [84–96]. One basic idea behind them is measuring the effect of non-idealities, such as variations in circuit elements, by using a test signal, and storing the deviation in a memory unit fabricated on the same Si chip. The final corrected digital output is obtained by subtracting the value in memory from the output of the SA ADC unit [85], [86], [88], [95], [96]. Another idea is to use a replica of an ADC unit and adjust the circuit parameters to minimize the difference in the output of the two units [92], [93].

It is too early to conclude that the non-binary approach is superior to these competitors, but it is also true that there are many state-of-the-art SA ADCs using non-binary algorithms in particular for high-speed applications because the settling condition can be considerably relaxed by introducing decision redundancy. This also leads to the possibility of low-power operation if the conversion speed is kept constant.

V. Conclusion

Papers on non-binary SA ADCs were surveyed mainly by using IEEE Xplore. The number of papers has increased considerably, indicating recent growth in attention to this field. Several circuit implementations, as well as a method for selecting an appropriate radix, to extract the digital word corresponding to the analog input signal as far as possible by using imperfect circuit elements, were described. In addition, some state-of-the art examples aiming at high-speed or low-power applications were presented.

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