Proceedings of the 25th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 21-23, 2018, Gdynia, Poland

Redundant Double Conversion based Digital Background Calibration of SAR ADC with Convergence Acceleration and Assistance

Xiang Ding, Klaus Hofmann
Integrated Electronic System Lab
Technical University of Darmstadt
Merckstr. 25, 64283, Darmstadt, Germany
e-mails: {xiang.ding, klaus.hofmann}@ies.tu-darmstadt.de

Liang Zhang, Dongbai Yi, Yingjiang Ma
Communication Technology Research Institute
Gree Electric Appliances Inc.
West Jinji Rd, Qianshan, 519070, Zhuhai, China
e-mails: {eric.zhang, jacky.yi, yjm}@cn.gree.com

***Abstract*—A redundant double conversion (RDC) based digital background technique for successive approximation analogue-to-digital converters (SAR ADCs) with convergence acceleration and assistance is presented. The convergence time of the RDC based calibration is reduced by monitoring the error between two raw conversion results of a sub-2 SAR ADC and increasing the step-size parameter of the least mean square (LMS) filter, if the detected error is less than a threshold. The convergence assistance is accomplished by injecting a random perturbation signal to a stationary input. Behavioral simulation shows that the proposed technique reduces convergence time of the RDC calibration by 30% while maintains a comparable resolution and power consumption. With the random perturbation signal generated by a 5-bit digital-to-analog converter (DAC) RDC calibration can be started and an ENOB about 10 is obtainable.**

***Keywords*—SAR ADC, background calibration, LMS, RDC, device mismatch, mixed-signal integrated circuit, high-level modeling and simulation**

I. Introduction

Charge redistribution (CR) successive approximation register (SAR) analog-to-digital converters (ADCs) have found a wide usage in low-power applications with medium resolution and sampling rates of several tens of MS/s [1]. Since its debut the performance of this kind of ADCs has been continuously improved by taking advantage of technology scaling. However, stringent device matching requirements in the deep nano-CMOS era make further performance improvement of CR SAR ADCs a challenging task. Accuracy of CR SAR ADCs relies heavily on capacitor matching of its capacitive digital-to-analog converter(CDAC) [2].

Over the past decade, digital background calibration of CR SAR ADCs has been actively researched to solve the matching problem. CR SAR ADCs with more than 11 effective number of bit (ENOB) and a sampling rate up to 100 MHz has been reported. Die overhead and power consumption are reduced since CR SAR ADCs can be sized according to the kT/C noise requirement with the help of calibration [3].

Despite the remarkable performance, slow convergence and dependence on input signal obstacle the proliferation of digital calibration techniques [4]. Only a few publications address these issues, while most calibration techniques lay their emphasis on devising calibration techniques [4]-[11]. In [5], a shuffling scheme has been adopted to guarantee convergence in the presence of a steady input signal. In [6], an 8-bit reference ADC is employed to reduce the lengthy convergence time of the calibration method based on independent component analysis (ICA).

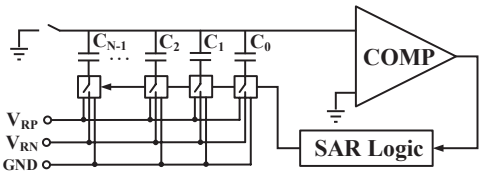

Fig. 1. Block diagram of a charge-redistribution SAR ADC.

In this work, we report a novel digital background calibration technique capable of eliminating the dependence on input signal and reducing convergence time of the RDC based calibration technique. Instead of blindly randomizing the input signal through segmentation or with a coarse ADC, we focus on increasing the effective number of calibration (ENOC) of the RDC technique.

This paper is structured as follows. Basics of digital background calibration and RDC are introduced in Section II and Section III, respectively. The bit-weights update the RDC calibration is analyzed and the concept of ENOC will be defined in Section IV. In Section V, principle, implementation considerations, and simulation results of the proposed technique are introduced. Section VI concludes this work.

II. Basics of Digital Background Calibration of CR SAR ADCs

Fig. 1 shows a simplified block diagram of a conventional N-bit CR SAR ADC [8]. In the sampling phase, the input signal V_{in} is sampled on N capacitors $C_i = 2^i C_0, i = 1 \cdots N$. In the subsequent conversion phase, capacitors $C_{N-1} \cdots C_1$ are configured to be a CDAC. In the first cycle of the conversion phase, the most-significant-bit (MSB) capacitor C_{N-1} is

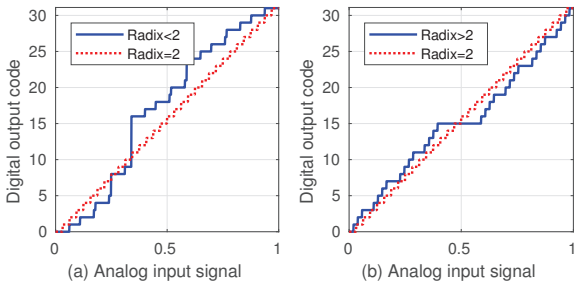

Fig. 2. Impact of capacitor mismatch on transfer characteristics of CR SAR ADCs: (a) A $Radix < 2$ CR SAR ADC (b) $Radix > 2$ CR SAR ADC

connected to V_{rp} (or V_{ref}) and the remaining capacitors are connected to the ground. Using the superposition principle, the voltage of top plates of the CDAC becomes

$$V_X = -V_{in} + V_{ref}\frac{C_N}{\sum_{i=1}^{N} C_i + C_0}. \tag{1}$$

In case of binary CDAC, the second term in Equation 1 is just $V_{ref}/2$. By comparing V_X to ground, the MSB of the conversion result can be determined. $V_X > 0$ indicates current decision threshold is larger than V_{in}. Thus, the MSB capacitor must be reconnected to ground and the MSB is 0. Conversely, connection of MSB capacitor is retained and the MSB is 1. This process continues until all bits are resolved and voltage on the top plate of the CDAC can be written as

$$V_X = -V_{in} + V_{ref}\sum_{i=1}^{N}\frac{C_i D_i}{\sum_{i=1}^{N} C_i + C_0}, \tag{2}$$

where D_i is the final conversion result. If quantization noise is ignored, the second term in Equation 2 approaches V_{in}.

Without mismatch, the transfer characteristics of a CR SAR ADC should be a staircase with equal width and height, as shown in Figure 2. In presence of mismatch, wrong decision thresholds are generated and conversion error occurs. As can be seen from Figure 2, transfer characteristics of non-ideal CR SAR ADCs deviate from the ideal curve.

The digital calibration is a process that tries to recover the correct conversion result from the raw output code of SAR ADCs. To this end, a digital bit weight defined as $W_i = C_i/\left(\sum_{i=0}^{N-1} C_i + C_0\right)$ is assigned to each capacitor C_i. If bit weights can be inferred by any means and ignore quantization noise and other non-idealities, then original input can be recovered by calculating the weighted sum of the raw output code

$$V_{in} = V_{ref} \cdot \sum_{i=0}^{N-1} W_i D_i. \tag{3}$$

Equation 3 resembles the transfer function a linear transversal filter. It is well-known that identification of tap-weights of the transversal filter can be accomplished by using adaptive filter. Likewise, the adaptive filter can also be used to learn bit-weights.

A mandatory requirement of bit-weights learning is that digital output codes of the ADC must contain sufficient mismatch information. Two mismatch scenarios may occur in a binary capacitor array: super-binary and sub-binary. In the super-binary case, the size of a MSB capacitor is larger than sum of sizes of all its LSB capacitors. In this case, the radix of the SAR ADC is larger than 2. Conversely, if the size of a MSB capacitor is smaller than sum of sizes of its LSB capacitors, then the radix of the SAR ADC is smaller than 2. Both mismatch scenarios lead to linearity errors of transfer characteristics of the CR SAR ADC. Figure 2 plots the impact of capacitor mismatch on transfer characteristics of two 5-bit CR SAR ADCs. As can be seen from Figure 2 (b), the transfer characteristics of super-binary CDAC contains a large input range corresponding to one digital code. This many-to-one mapping indicates information loss and prohibits the digital correction. Conversely, a sample in certain input ranges can be converted to multiple digital codes in the sub-binary case. The one-to-many mapping, which is often termed as redundancy, not only preserves all analog information and enables subsequent digital correction, but also eases the settling requirement of the CDAC. Thus, a sub-binary CDAC should be used in the digital calibration of CR SAR ADC [9].

Various digital calibration techniques have been reported. These calibration techniques can be roughly categorized as the equalization based and the correlation based algorithm. The technique introduced in this work is mainly based on the RDC based calibration algorithm reported in [7]. Thus, implementation details of the RDC calibration is discussed in the next section.

III. Principles of RDC Based Background Calibration

In the RDC calibration bit-weights are learned in a manner similar to that of adaptive equalization: a LMS filter forces errors between a reference input and its conversion results to zero. The reference signal of RDC calibration is generated by converting each sample twice. Namely, each sample is first converted according to the procedure described in Section II. This switching mode is often termed as the direct switching (DS) mode. After the first conversion the same analog sample is converted again, but with the so-called reverse conversion (RS) mode.

Conversion of the MSB is taken as an example to explain the principle of RS. In RS mode the top plate of the MSB capacitor C_{N-1} is grounded, while top plates of capacitors $C_{N-2}\cdots C_1$ are tied to V_{ref}. Input to the comparator can thus be written as

$$V_X = -V_{in} + V_{ref}\frac{\sum_{i=1}^{N-1} C_i}{\sum_{i=1}^{N} C_i + C_0}. \tag{4}$$

If $V_X > 0$, MSB is resolved to 1 and the MSB capacitor is reconnected to V_{ref}, so that in next clock cycle a larger decision threshold can be generated. Otherwise MSB is resolved to 0 and the connection of MSB capacitor is kept. Identical procedure repeats until all bits are resolved.

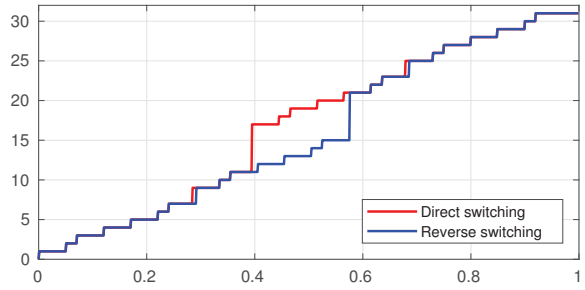

Fig. 3. Transfer characteristics of 5-bit radix-2 SAR ADC in DS and RS modes.

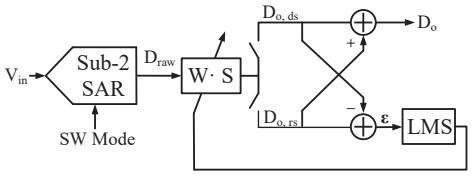

Fig. 4. Block diagram of RDC based digital calibration

Without mismatch both SW modes generate the same decision thresholds and identical conversion results. Different decision thresholds are generated due to capacitor mismatch, which may lead to two different digital words. Thus, transfer characteristics of DS and RS modes have distinct trajectories. Figure 3 illustrates transfer characteristic curves of a 5-bit nonideal radix-2 SAR ADC in DS and RS modes. One crucial observation made from Figure 3 is that the non-overlapping region reflects the existence of capacitor mismatch and should be calibrated. A block diagram of general RDC calibration is depicted in Figure 4. To avoid the aforementioned loss of mismatch information, the SAR ADC used in RDC has a sub-binary radix. Each weighted sum of the output of the sub-2 SAR, D_{raw}, is calculated according to

$$D_{o,ds/rs} = \sum_{i=0}^{N-1} \hat{W}_{n,i} D_{raw,ds/rs,i}, \tag{5}$$

where $\hat{W}_{n,i}$ denotes an estimate of each bit-weight in n-th iteration. Thus, two weighted sums $D_{o,ds}$ and $D_{o,rs}$ are obtained after each double conversion. The reference signal, or more exactly the error signal can thus be written as

$$\epsilon = D_{o,d} - D_{o,r} = \sum_{i=0}^{N-1} \hat{W}_{n,i} \left(D_{raw,d,i} - D_{raw,r,i} \right). \tag{6}$$

In the LMS engine, estimated bit-weights of the next iteration are updated according to

$$\hat{W}_{n+1,i} = \hat{W}_{n,i} - 2\mu\epsilon \left(D_{raw,d,i} - D_{raw,r,i} \right), \tag{7}$$

where μ is a step size parameter. Size of μ determines the convergence rate and mean square error (MSE) when the adaptive filter is in steady state [12]. A large μ may lead to a fast convergence and ENOB degradation. Due to the deterministic nature of mismatch, the LMS filter is stable and convergence can be reached as long as μ satisfies

$$0 < \mu < \frac{1}{3tr\left[\mathbf{R}\right]}, \tag{8}$$

where $tr\left[\mathbf{R}\right]$ denotes the trace of the correlation matrix of the injected reference signal, which is also the power spectrum density of the input signal [13]. However, it cannot be measured in the RDC calibration due to the implicit reference signal injection. Therefore, μ is usually determined by simulations or experiments in the design phase and then hard coded on die.

Two prototypes of RDC based calibration have been reported in [7] and [20]. The SAR ADC reported in [7], takes 2500 updates to learn a mismatch of 1% and the ENOB after calibration is 10.45. However, the convergence time is proportional to the number of bit-weights to be learned and each extra bit may double the convergence time. In the latter prototype, its takes about 50,000 samples to learn the 14 bit-weights. In view of many merits of the RDC calibration, such as no dynamic range loss caused by offset injection and the simple hardware architecture, it is worthwhile to further reduce the convergence time and assist the start-up of calibration in case of a quasi-stationary input. Therefore, the convergence process of the RDC calibration will be analyzed in the next section.

IV. Analysis of Bit-weights Update in the RDC Based Calibration

Two observations regarding convergence rate can be made from the foregoing analysis. First of all, when direction of bit-weights adjustment is correct, the convergence rate mainly depends on how fast the second term of Equation 7 approaches zero. In other words, a large update of bit-weights are desirable in each iteration along the deepest descent.

Another important observation made from Figure 3 is: transfer curves of DS and RS modes overlap with each other in multiple input ranges. Analog samples falling into these overlapping ranges cannot trigger effective update, which slows down the bit-weights learning. The situation is more severe in case of DC input. While no updates can be triggered when the input falls into the overlapped region, an input located in the non-overlapping region forces the left-hand side of Equation 7 to zero due to a constant ϵ. Then, the LMS loop is trapped in a local optimum point and a false convergence is reached.

These two observations can be verified by running simulations on a RDC calibration model in MATLAB. To facilitate the comparison the efficiency of bit-weights updating in various simulation configurations, we define the ENOC of a convergence process as

$$ENOC = \frac{N_{\epsilon>1LSB}}{N_{total}}, \tag{9}$$

where $N_{\epsilon>1LSB}$ denotes the number of iterations, in which ϵ is larger than one LSB, whereas N_{total} denotes the total number

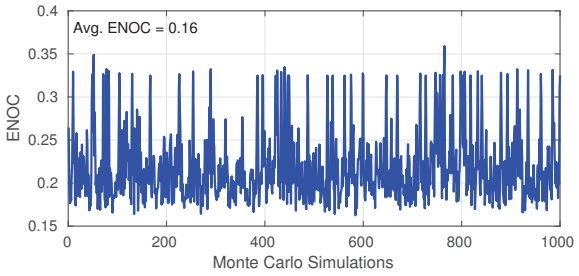

Fig. 5. Monte Carlo simulation results of ENOC of a RDC SAR ADC.

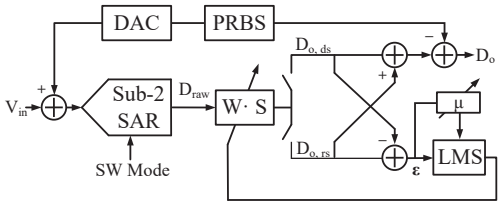

Fig. 6. Block diagram of the RDC based digital calibration with convergence acceleration.

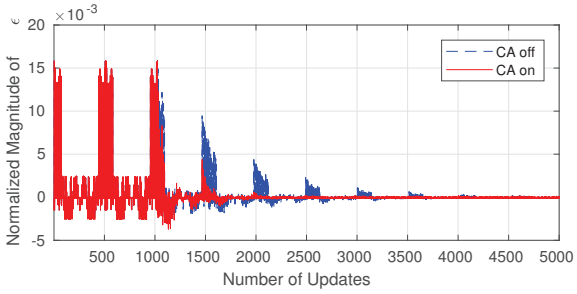

Fig. 7. Comparison of ϵ updating history during RDC calibration with and without CA.

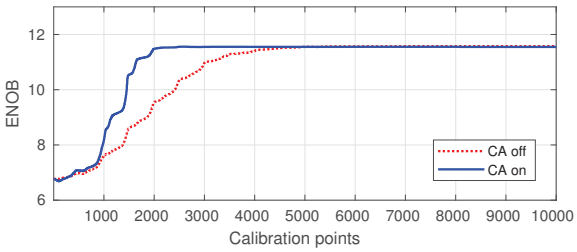

Fig. 8. ENOB improvement during calibration.

of updates before convergence. Figure 5 plots the ENOCs obtained from a 1000-run Monte Carlo simulation. In each run of the Monte Carlo simulation capacitor mismatch and analog samples are randomly generated. The average ENOC of the RDC calibration is only 0.16, which can be interpreted as: only one of every 6 iterations triggers a substantial update. Also, 10 calibration failed to reach convergence has been observed, which corresponds to a DC or a quasi-DC input. Thus, the learning efficiency is quite low. In order to speed up the convergence one could focus on find out new learning algorithms or try to increase the update efficiency of existing algorithms. In this work the latter method is used. In the next section, the convergence acceleration and assistance (CA) techniques of RDC calibration are introduced.

V. Convergence Acceleration and Assistance Techniques of RDC Calibration

A block diagram of the proposed RDC calibration of SAR ADC with CA is shown in Figure 6. The convergence acceleration is realized by a simplified variable step size adaptive filtering algorithm, which is implemented in the block labelled μ. This block monitors the value of ϵ in each iteration. If ϵ is less than a predetermined threshold Th_{AC}, current iteration is assumed to be an ineffective update. To avoid such ineffective updates, the step size parameter μ is increased temporarily to μ_{AC}. To facilitate the hardware implementation, μ_{AC} can be chosen as $2^N \times \mu$. In the next iteration μ is set back to its initial value if ϵ is larger than the threshold.

Argument for increasing μ is due to the fact that $\epsilon < Th_{AC}$ indicates current iteration has a large possibility on the direction of the deepest descent. As analyzed in Section IV, increasing μ can accelerate the convergence in this situation. Conversely, if the temporary increment of μ deviates the iteration from the desired direction, a larger ϵ will be generated in the subsequent iterations and μ is reset once $\epsilon > Th_{AC}$ is detected, which directs current iteration back to the direction of steepest descent. Moreover, the performance of the SAR ADC after convergence is also guaranteed since the term $\epsilon\,(D_{raw,d,i} - D_{raw,r,i})$ is much smaller than 2^{-N}, if N is properly chosen. Thus, in steady state the SAR ADC is capable of providing a stable resolution.

The validity of this simplified variable step size adaptive filtering algorithm can be proved by MATLAB simulation. Figure 7 shows the updating history of ϵ in a 14-bit, radix-1.86 SAR ADC during the RDC calibration. Here, capacitor mismatch is set to 5% and $\mu_{AC} = 4\mu$. Before the CA is enabled significant ϵ jump can still be observed after 3000 updates. After switching on the CA in the same ADC, high frequency significant jumps of ϵ can be observed in the first 1000 updates, after which ϵ dampes quickly to the steady state value, which has similar magnitude as that in the calibration without CA.

In view of the fast damping of ϵ, a fast convergence rate is expected. Figure 8 shows the evolution of ENOB during calibration. As expected, the RDC calibration with CA reaches an ENOB of about 11.5 after 2000 updates, whereas without CA it takes about 5000 updates to reach the same ENOB.

The power spectrum density plots before and after the SAR ADC is calibrated by the proposed RDC with CA is shown in Figure 9. By comparing power spectrum density plots before and after calibration, one can readily see that the RDC calibration with CA added can provide an ENOB comparable to that of the conventional RDC calibration. In other words, the selectively increased step size parameter does not jeopardize the performance of the SAR ADC.

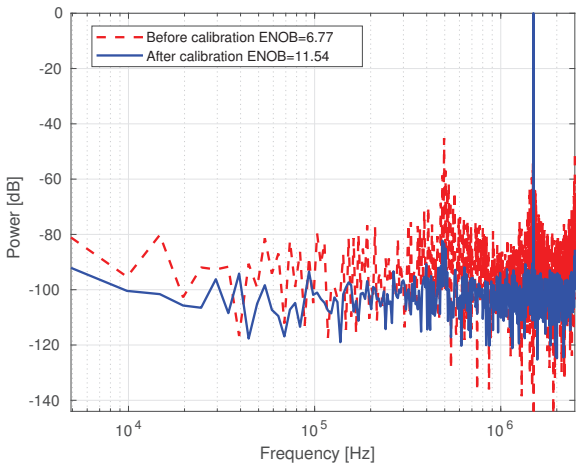

Fig. 9. Power spectrum densities of the SRA ADC before and after calibration.

The convergence assistance during the start-up with a quasi-DC input is accomplished by a radix-2 CDAC and a Pseudo Randomness Binary Sequence (PRBS) signal generator, as shown in Figure 6. The detection of a quasi-DC signal is performed by caching the last N pairs of consecutive raw conversion results and checking whether they are identical. A cache size of N is used, because the minimum requirement to determine N variables is to build a equation systems with N equations. If the conversion results have not been updated for N iterations, then W_i is mathematically not solvable, which also prohibits a solution of approximation. To lift the calibration from being trapped in local minimum, the PRBS module generate a M-bit random number, and the CDAC converts the digital code into analog. The injected signal shifts the quasi-DC signal to a new voltage level and triggers the adaption. Convergence can be reached if sufficient voltage levels have been exercised. In other words, the actual input signal of the SAR ADC should be busy enough. Ideally, actual input signal to the SAC ADC is busy enough, if the injected signal is able to shift the quasi-DC signal to fall in all non-overlapping regions in Figure 3. To fullfil this requirement, size of the radix-2 CDAC should have the same size as the SAR ADC under calibration, which increases the design burden of the whole system. If the injected signal is not able to produce a busy actual input signal, non-overlapping regions can be partially identified and calibrated, which leads to an ENOB degradation after calibration. Therefore, there is a trade-off between the size of the radix-2 CDAC and the final ENOB. Due to the randomness of the capacitor mismatch, size of the radix-2 CDAC can be determined through high-level modelling and simulation.

At the output end, the injected signal can be either removed from the input digitally. Or the injected signal is not extracted since the conversion result at the beginning of CA has very large error. Simulations have also been performed on the convergence assistance function. Figure 10 tracks the ϵ before and after convergence assistance is activated at 5000th update.

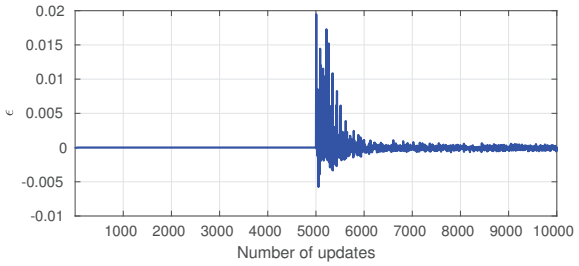

Fig. 10. Update of ϵ with a DC input.

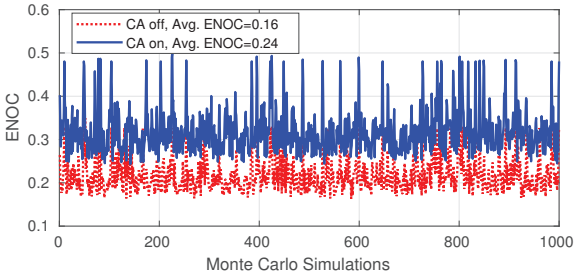

Fig. 11. Monte Carlo simulation of ENOC with convergence acceleration.

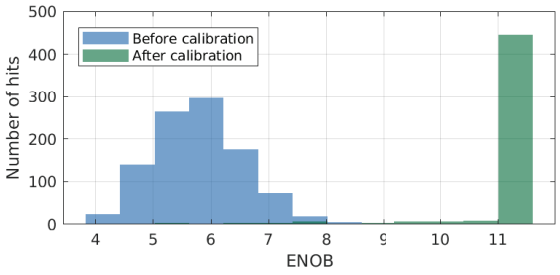

Fig. 12. Monte Carlo simulation of ENOB improvement after RDC calibration with convergence acceleration.

As can be seen from the plot, there is no updates of ϵ in first 5000 updates. With the help of the injected signal, update of ϵ starts and the calibration ends within 2000 samples.

To validate the model more thoroughly, a 1000-run Monte Carlo simulation has been performed. In each run capacitance values of CDAC are randomly generated with a 1% mismatch, frequency of the input signal is also randomly chosen from DC to near Nyquist-rate, and μ_{AC}/μ is set to 4. As shown in Figure 11, ENOC of the calibration runs with CA enabled is enhanced significantly. ENOB distributions before and after calibration is shown in Figure 12. Before calibration, ENOBs conform a Gaussian distribution with a mean ENOB around 6. After calibration, most of the ENOB concentrates near 11.3. Thus, it can be concluded that the RDC calibration with CA is robust.

The circuit implementation of the proposed RDC calibration with CA is illustrated in Figure 13. The PRBS and the ineffective update detecting blocks can be implemented either with digital circuit or with software without modifying the circuit architecture that has been silicon proved in [7]. The

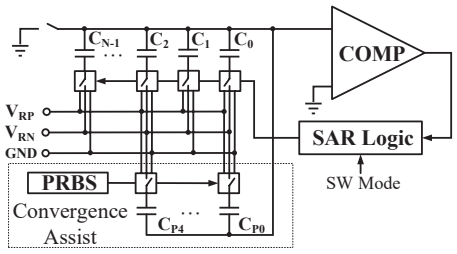

Fig. 13. Schematic of convergence assisting circuit.

CDAC can be implemented by a binary weighted capacitor array. Capacitor matching in this CDAC is not critical, since there is no accuracy requirement on the perturbation signal generated by this radix-2 CDAC. Simulation shows that a 5-bit CDAC is sufficient to calibrate the SAR ADC to 10 ENOB. If the SAR ADC is a building block of a system-on-a-chip (SOC), such as an MCU, the design burden of the CDAC can be eased by simply sharing the on-chip available DAC with other circuits. It is also worthy to note that calibration scheme of the proposed SAR ADC shares identical hardware of the offset double conversion based (ODC) calibration architecture proposed in [19]. With minor modification in the digital circuit, the two calibration technique can be implemented on the SAR ADC, which makes the SAR ADC more flexible.

VI. Conclusion

In this work we have presented a RDC based digital background calibration of SAR ADC with convergence acceleration and assistance function with very little hardware cost. Simulations show that the proposed technique is capable of increasing the ENOC by 50% and reduce save 30% convergence time. Also, calibration of the SAR ADC is enabled with the aid of a pertuation signal generated by a 5-bit DAC.

References

[1] B. Murmann, "The successive approximation register ADC: a versatile building block for ultra-low- power to ultra-high-speed applications," in IEEE Communications Magazine, vol. 54, no. 4, pp. 78-83, April 2016.

[2] Hae-Seung Lee and D. Hodges, "Accuracy considerations in self- calibrating A/D converters," in IEEE Transactions on Circuits and Systems, vol. 32, no. 6, pp. 590-597, Jun 1985.

[3] Jiang, X. (Ed.). (2015). Digitally-Assisted Analog and Analog-Assisted Digital IC Design. Cambridge: Cambridge University Press.

[4] J. McNeill, M. Coln and B. Larivee, "A split-ADC architecture for deterministic digital background calibration of a 16b 1 MS/s ADC," ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005., San Francisco, CA, 2005, pp. 276-598 Vol. 1.

[5] J. A. McNeill, K. Y. Chan, M. C. W. Coln, C. L. David and C. Brenneman, "All-Digital Background Calibration of a Successive Approximation ADC Using the "Split ADC" Architecture," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, no. 10, pp. 2355-2365, Oct. 2011.

[6] G. Wang, F. Kacani and Y. Chiu, "IRD Digital Background Calibration of SAR ADC With Coarse Reference ADC Acceleration," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 61, no. 1, pp. 11-15, Jan. 2014.

[7] D. Stepanovic and B. Nikolic, "A 2.8GS/s 44.6mW time-interleaved ADC achieving 50.9dB SNDR and 3dB effective resolution bandwidth of 1.5GHz in 65nm CMOS," 2012 Symposium on VLSI Circuits (VLSIC), Honolulu, HI, 2012, pp. 84-85.

[8] J. L. McCreary and P. R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques. I," in IEEE Journal of Solid-State Circuits, vol. 10, no. 6, pp. 371-379, Dec. 1975.

[9] W. Liu, P. Huang and Y. Chiu, "A 12-bit, 45-MS/s, 3-mW Redundant Successive-Approximation-Register Analog-to-Digital Converter With Digital Calibration," in IEEE Journal of Solid-State Circuits, vol. 46, no. 11, pp. 2661-2672, Nov. 2011.

[10] W. Liu and Y. Chiu, "Background digital calibration of successive approximation adc with adaptive equalisation," in Electronics Letters, vol. 45, no. 9, pp. 456-458, April 23 2009.

[11] W. Liu, P. Huang and Y. Chiu, "A 12-bit 50-MS/s 3.3-mW SAR ADC with background digital calibration," Proceedings of the IEEE 2012 Custom Integrated Circuits Conference, San Jose, CA, 2012, pp. 1-4.

[12] Adaptive Filter Theory,Haykin, S.S.,9788131708699,2008,Pearson Education

[13] Farhang-Boroujeny, B., "Adaptive Filters: Theory and Applications, John Wiley & Sons, Inc. 1998.

[14] M. J. M. Pelgrom and A. C. J. Duinmaijer, "Matching properties of MOS transistors," Solid-State Circuits Conference, 1988. ESSCIRC '88. Fourteenth European, Manchester, UK, 1988, pp. 327-330.

[15] C. C. Liu et al., "A 10b 100MS/s 1.13mW SAR ADC with binary-scaled error compensation," 2010 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, 2010, pp. 386-387.

[16] F. Kuttner, "A 1.2V 10b 20MSample/s non-binary successive approximation ADC in 0.13/spl mu/m CMOS," 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315), San Francisco, CA, USA, 2002, pp. 136-137.

[17] Shuo-Wei Mike Chen and R. W. Brodersen, "A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13/spl mu/m CMOS," 2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers, San Francisco, CA, 2006, pp. 2350-2359.

[18] W. Liu et al., "A 600MS/s 30mW 0.13µm CMOS ADC array achieving over 60dB SFDR with adaptive digital equalization," 2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, San Francisco, CA, 2009, pp. 82-83,83a.

[19] W. Liu, P. Huang and Y. Chiu, "A 12b 22.5/45MS/s 3.0mW 0.059mm2 CMOS SAR ADC achieving over 90dB SFDR," 2010 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, 2010, pp. 380-381.

[20] Y. Chiu, F. Kacani, P. Huang, and W. Liu, "A digitally calibrated 14-bit 36-MS/s 65-nm CMOS SAR ADC with redundant double conversion," in Proc. IEEE Int. Conf. Solid-State and Integrated-Circuit Tech., 2