12.1 An 820µW 9b 40MS/s Noise-Tolerant Dynamic-SAR ADC in 90nm Digital CMOS

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Current trends in analog/mixed-signal design for battery-powered devices demand the adoption of cheap and power-efficient ADCs. SAR architectures have been recently demonstrated as able to achieve high power efficiency in the moderate-resolution/medium-bandwidth range [1]. However, when the comparator determines in first instance the overall performance, as in most SAR ADCs, comparator thermal noise can limit the maximum achievable resolution. More than 1 and 2 ENOB reductions are observed in [1] and [2], respectively, because of thermal noise, and degradations could be even worse with scaled supply voltages and the extensive use of dynamic regenerative latches without pre-amplification. Unlike mismatch, random noise cannot be compensated by calibration and would finally demand a quadratic increase in power consumption unless alternative circuit techniques are devised.

A noise-robust design approach to fully dynamic SAR ADCs by leveraging redundancy in the search algorithm is reported. Most solutions in the literature, relying on redundancy to cope with noise, as well as other error sources (capacitor mismatch, finite sampling bandwidth, comparator hysteresis), bring significant overhead either in speed, in terms of additional conversion steps [3, 4], or in area and digital complexity [2, 5]. In this work, only one additional cycle combined with a noise-programmable comparator and low-cost digital post-processing are required to guarantee the target ENOB in the Nyquist bandwidth.

The system shown in Fig. 12.1.1, includes a time-interleaved (TI) S/H, a binary-scaled capacitor array, a flexible regenerative comparator, an asynchronous SAR controller and the error-correction logic. A passive charge-sharing architecture that processes the sampled signal in the charge domain avoids the use of power-consuming reference buffers [1]. The capacitor array is pre-charged to the power supply and, during conversion, its binary-scaled charge units are added or subtracted until the comparator input converges to zero.

The time-interleaved sampling circuit, shown in Fig. 12.1.2, processes a $0.8V_{pp}$ single-ended input signal with 0.5V common-mode voltage V_{CM}. The circuit is based on bootstrapped NMOS switches at the input (BM1) [6], offering a low signal-independent on-resistance, and pass-gates at the output (TG1). When phase Φ_2 is active, the input signal is tracked on capacitors C_{TL1}+C_{TH1} (5pF) while the charge previously sampled on C_{TL2}+C_{TH2} is already available for conversion. After the MSB is determined via charge-sharing and the voltage on the node OUTp becomes small enough to avoid clipping, the common-mode voltage, V_{CM}, is lowered. This decreases the on-resistance of the charge-sharing NMOS switches ($S_{m,p}$ in Fig. 12.1.1) and their time constants, that have a great impact on the overall conversion speed. As soon as Ψ_2 resets, the sampling capacitor is split in the two units C_{TL} and C_{TH} (C_{TH}= C_{TL}/R) and charge redistributes, causing a decrease in V_{CM} related to the capacitor ratio R.

The flexible comparator (Fig. 12.1.3) leverages two parallel fully dynamic regenerative comparators, adequately sized to present a different input-referred noise, and hence, power consumption. Both comparators share the input connections and see the same equivalent load. However, they never work at the same time as the bit noise driven by the SAR controller decides when each of them needs to be activated. Comparator offset is calibrated by two binary-scaled capacitor arrays placed at the output nodes and digitally set through a serial register. Relative deviation between the 2 comparators offsets worsens the DNL performance and must be minimized. Moreover, when the common mode is lowered, after the second conversion step, the offset of the comparator in use changes, thus requiring an additional digital word to be loaded in the calibration registers.

The strategy behind the correction technique relies on the fact that if the input comparator rms noise is properly sized, at most 2 out of N comparisons during the SAR operation are likely to be critical because of thermal noise, i.e., the one when the signal is right below the threshold and the one when it is right above. One of those critical decisions will certainly be the last one: an error in this decision can be avoided by using the comparator in its low-noise/high-power state. The other one can be any of the previous (N-1) comparisons, and avoiding it with a low-noise comparator is not power efficient. As shown in Fig. 12.1.4 for a 5b example, the SAR algorithm uses the comparator in its high-noise state during the first (N-1) iterations, thus allowing errors in these cycles. However, if σ_H, the input comparator rms noise in that mode, is less than one half of the LSB value, only one error can be made. The ADC then switches into its low-noise mode (with comparator input noise $\sigma_L \approx \sigma_H/2$) to avoid errors for the N^{th} comparison, and an extra $(N+1)^{th}$ iteration is added to correct for the error possibly made in the first phase. As shown in Fig. 12.1.4 (a), if the last 2 comparisons give different results, no error was made and no action has to be taken. On the other hand, in case the last 2 bits are equal, then a digital addition or subtraction needs to be performed on the final N-bit result. Being pipelined to the SAR conversion, the simple digital adder needed to correct does not work at the internal SAR frequency (N times the sampling frequency), thus limiting its power consumption. Importantly, the correction is effective not only for thermal noise, but also for other noise sources, including static non-linearities, as far as they are not bigger than 1 LSB.

The ADC prototype, fabricated in a 90nm 1P9M digital CMOS process (micrograph in Fig. 12.1.7), occupies less than 220×410µm². Figure 12.1.5 (b) shows the static performance when the correction is not active. The peaks in DNL and INL are due to incomplete settling during the common-mode switching because of under-estimated parasitic capacitances and due to mismatches between C_{TL} and C_{TH}. When the error correction is active (Fig. 12.1.5 (a)), DNL and INL result to be respectively 0.7/-0.45 and 0.56/-0.65. As shown in Fig. 12.1.6, when the input signal is sampled at 40MS/s, the ENOB is 8.56 (53.3dB SNDR) at low frequencies, mainly limited by static distortion, and lowers to 8.23 at Nyquist. The effective resolution bandwidth extends up to 32MHz. At 40MS/s, the ADC consumes 820µA from a 1V supply voltage, of which, 290µA are drawn by the asynchronous controller, and 530µA are shared between the S/H, the pre-charging phase of the capacitor array, and the flexible comparator. Because of the dynamic architecture, power scales linearly with the sampling frequency. The resulting FoM, calculated as, $Power/(2^{ENOB} \cdot F_s)$ is 54fJ/conversion-step, reporting a 16% improvement with respect to state-of-the-art comparable designs.

References:

[1] J. Craninckx and G. Van der Plas, "A 65fJ/Conversion-Step 0-to-50Ms/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS", *ISSCC Dig. Tech. Papers*, pp. 246-247, Feb. 2007.

[2] F. Kuttner, "A 1.2V 10b 20MSample/s Non-Binary Successive Approximation ADC in 0.13µm CMOS", *ISSCC Dig. Tech. Papers*, pp. 176-177, Feb. 2002.

[3] A. Shrivastava, "12-bit Non-Calibrating Noise-Immune Redundant SAR ADC for System-on-a-Chip", *Proc. IEEE ISCAS*, pp. 1515-1518, May 2006.

[4] K.S. Tan, S. Kiriaki, M. de Wit et al., "Error Correction Techniques for High-Performance Differential A/D Converters", *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1318-1327. Dec. 1990.

[5] M. Hesener, T. Eichler, A. Hanneberg, et al. "A 14b 40MS/s Redundant SAR ADC with 480MHz Clock in 0.13µm CMOS", *ISSCC Dig. Tech.* Papers, pp. 248-249, Feb. 2007.

[6] A.M. Abo, P.R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter", *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599-606, May 1999.

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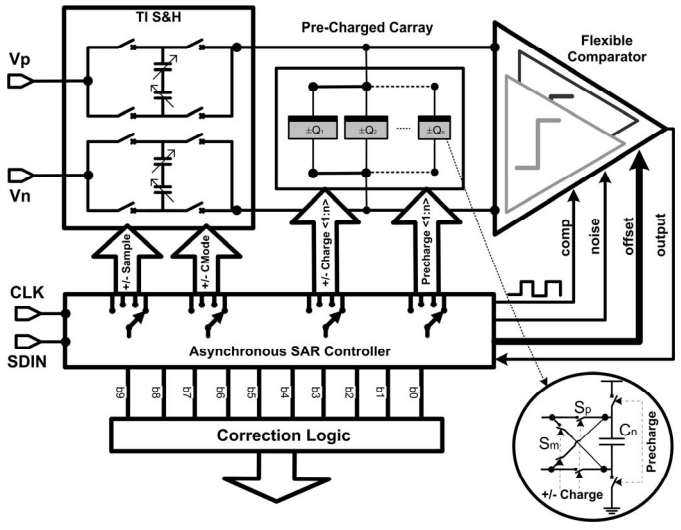

Figure 12.1.1: Diagram of the noise-tolerant charge-sharing SAR ADC.

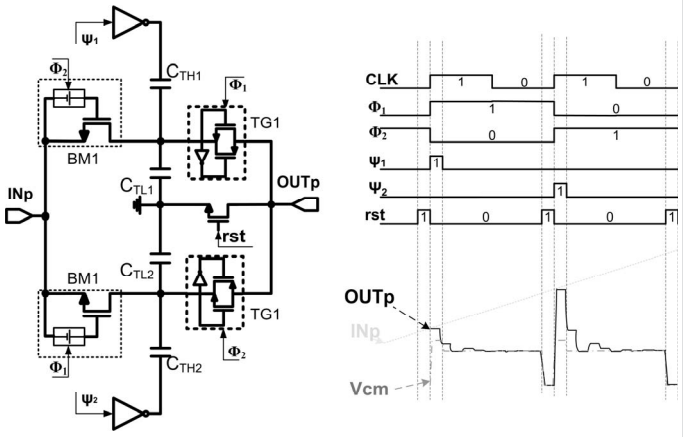

Figure 12.1.2: Time-interleaved S/H and relevant waveforms.

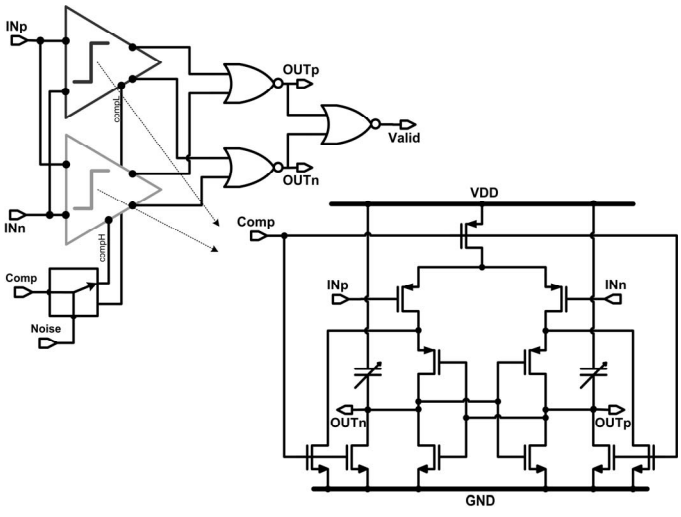

Figure 12.1.3: Flexible comparator circuit schematic.

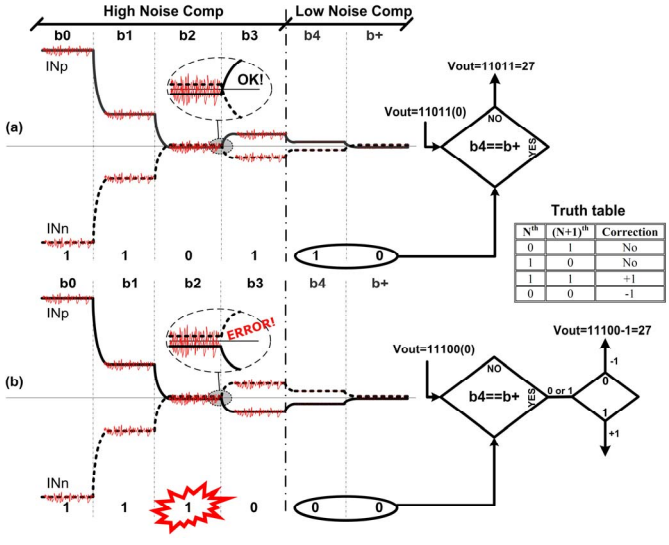

Figure 12.1.4: Correction algorithm in case of no error (a) and error (b).

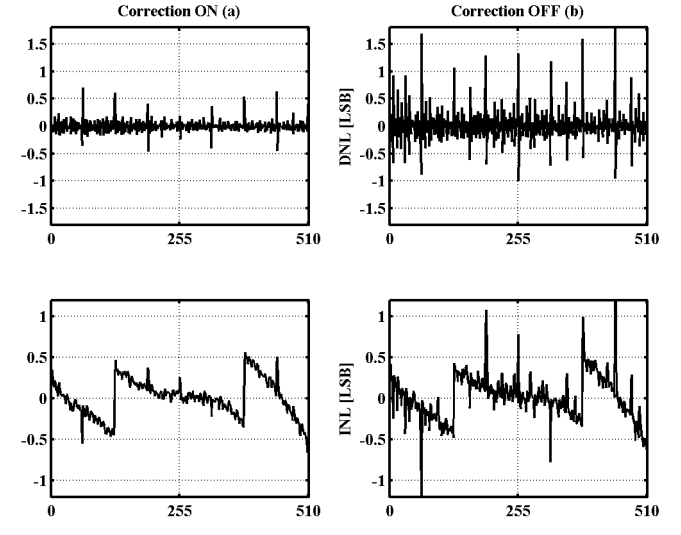

Figure 12.1.5: INL/DNL plot with (a) and without (b) correction.

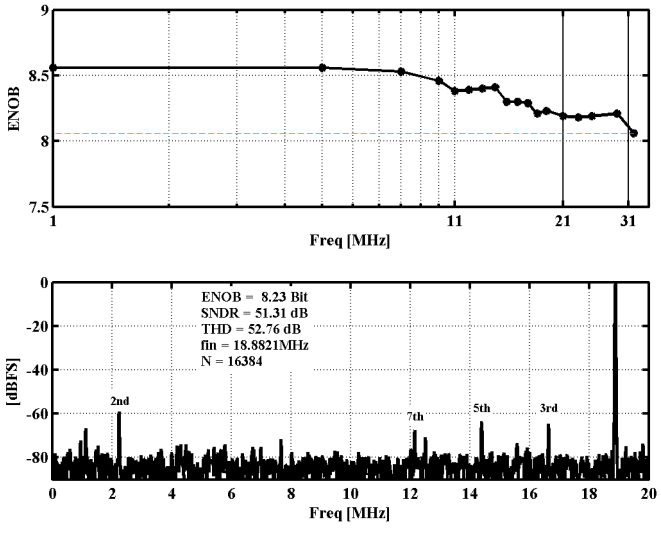

Figure 12.1.6: ENOB versus frequency and near-Nyquist FFT at 40MS/s.

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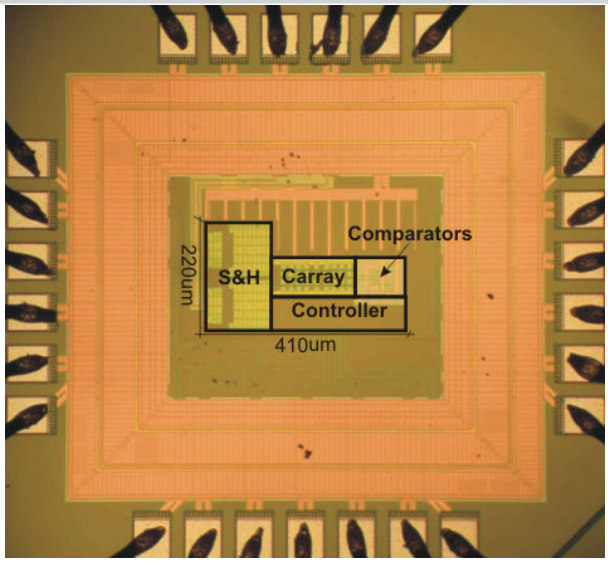

Figure 12.1.7: Die micrograph.

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