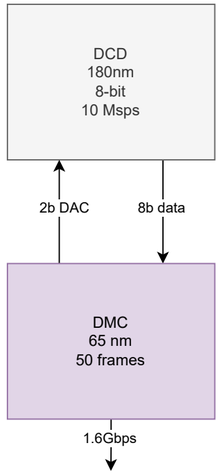
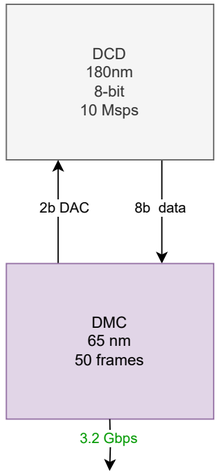
Current Architecture:



Potential Improvements?

increase frames per burst
increase measurement resolution
increase bursts per second

Proposal A:



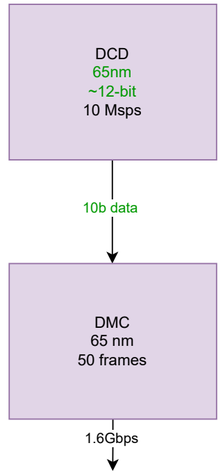
Changes:

no DCD change

no increase in frame memory

improve PLL speed
2x bursts per second
(2x less dead time)

Proposal B:



Changes:

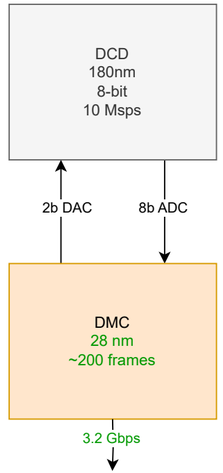
port DCD to 65nm

redesign ADC as ~12-bit
built-in pedestal DAC frees full 10-wide bus
10-bit ENOB measurments resolutions

potentially increased DCD power

no change in DMC

Proposal C:



Changes:

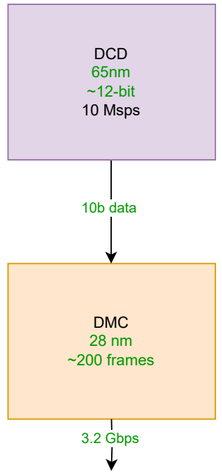
no DCD change

port DMC to 28nm

increase frame memory
4x frames per burst (200)

2x improved PLL speed, but
bursts/second will likely degrade 0.5x
(2x longer dead time)

Proposal D:



Changes:

Essentially Plan B + Plan C

port DCD to 65nm

redesign ADC as ~12-bit

built-in pedestal DAC frees full 10-wide bus
10-bit ENOB measurments resolutions

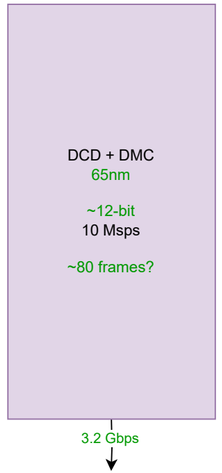
port DMC to 28nm

increase frame memory
4x frames per burst (200)

2x improved PLL speed, but
bursts/second will likely degrade 0.5x
(2x longer dead time)

potentially increased DCD and DMC power

Proposal E:



Changes:

monolithic DCD + DMC in 65nm
requires ASM balcony redesign
more total silicon area

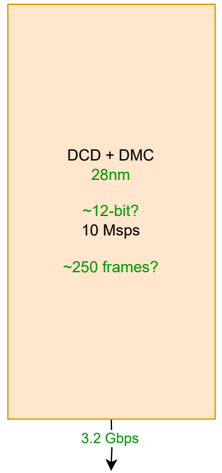
redesign ADC as ~12-bit, similar to plan B
10-12 bit measurement resolution?

minor increase to frame memory
1.5x frames per burst (80) ?

2x improved PLL speed, but
0.5x bursts/second will likely degrade 0.5x
(2x longer dead time)

power difference?

Proposal F:



Changes:

monolithic DCD + DMC in 28nm
requires ASM balcony redesign
more total silicon area

redesign ADC as ~12-bit
supply may limit measurement resolution?

increase frame memory
5x frames per burst (250) ?

2x improved PLL speed, but
bursts/second will likely degrade 0.5x
(2.5x longer dead time)

power difference?