4.5 A 600MS/s 30mW 0.13µm CMOS ADC Array Achieving Over 60dB SFDR with Adaptive Digital Equalization

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At high conversion speed, time interleaving provides a viable way of achieving analog-to-digital conversion with low power consumption, especially when combined with the successive-approximation-register (SAR) architecture that is known to scale well in CMOS technology. In this work, we showcase a digital background-equalization technique to treat the path-mismatch problem as well as individual ADC nonlinearities in time-interleaved SAR ADC arrays. This approach was first introduced to calibrate the linearity errors in pipelined ADCs [1], and subsequently extended to treat SAR ADCs [2]. In this prototype, we demonstrate the effectiveness of this technique in a compact SAR ADC array, which achieves 7.5 ENOB and a 65dB SFDR at 600MS/s while dissipating 23.6mW excluding the on-chip DLL, and exhibiting one of the best conversion FOMs among ADCs with similar sample rates and resolutions [3].

The block diagram of the time-interleaved ADC array is shown in Fig. 4.5.1, which aggregates the throughputs of 10 parallel ADCs, each clocked at 60MS/s and utilizing a power-efficient SAR architecture. The raw output of each path is post-processed by an adaptive digital filter (ADF) assisted by a parallel, slow-but-accurate reference ADC, which continually updates the ADFs using an LMS algorithm to track PVT variations. A unique feature of this treatment is that upon training, the characteristics of the individual ADCs are uniformly equalized to that of the reference ADC, thus eliminating conversion errors inherent to time interleaving, including gain, offset, and linearity mismatch errors. A front-end T/H stage is utilized to eliminate the sampling clock-skew problem among the conversion paths. Two source followers buffer the T/H output, feeding the ADC array and the reference ADC, respectively. The analog signal paths are fully differential.

The schematic of the SAR ADC is shown in Fig. 4.5.2, which performs a radix-1.86 search algorithm to facilitate digitization. To achieve an effective 8b resolution, 9 raw bits are resolved. The conversion radix is chosen to allow sufficient redundancies for digital calibration [2], while minimizing the total capacitance. Since the exact bit weights (corresponding to the DAC capacitances) are to be determined by the ensuing equalization step, the capacitors can then be scaled down to save power with little concern for matching (the unit capacitance is around 0.75fF in this design). This in turn maximizes the T/H buffer bandwidth and improves the overall ADC power efficiency. The built-in redundancy of the radix-1.86 conversion is further exploited in the dynamic threshold comparison scheme illustrated in Fig. 4.5.2, wherein 4 properly sized capacitors ($C_{8,d}$, …, $C_{5,d}$) are utilized to shift the decision thresholds of the 4 MSBs to the center of the redundant regions, allowing maximum tolerance to incomplete DAC settling as well as to various coupling noise sources.

$$D_{in} = \frac{V_{in}}{V_R} = \sum_{i=0}^{8} \frac{C_i}{C_{tot}} \cdot (2d_i - 1) + \frac{V_{os}}{V_R} + QN \quad (1)$$

Equation (1) formulates the 10-tap linear equalizer that is implemented in the post-processing ADFs [2]. The first term on the RHS is the weighted sum of the digital bits, the second term is the input-referred offset, and the last term is the quantization noise (neglected). The ratio C_i/C_{tot} is the bit weight of d_i, and C_{tot} is the total sampling capacitance in Fig. 4.5.2. The 10 ADFs receive the digital codes from the reference ADC in a round-robin fashion, and adaptively adjust their tap values by comparing the reference codes to their outputs. In steady state, the transfer function of each individual SAR ADC in conjunction with its trailing ADF resembles that of the reference ADC in the mean-square sense. Conversion nonlinearities and path mismatches are automatically eliminated.

Since the front-end T/H stage and the two buffers are out of the calibration loop, it is crucial for them to maintain better-than-8b linearity at 600MS/s. A pseudo-differential topology is utilized as shown in Fig. 4.5.3. The top-plate sampler is designed to achieve a 3dB bandwidth of 2.5GHz. Dummy switch and replica well-bias techniques are adopted to improve the THA linearity. Since the reference ADC always samples at the same time as one of the interleaved ADCs, driving them with two separate source followers effectively eliminates any potential interference.

An area and power-efficient algorithmic architecture is selected for the reference ADC. As the random noise in the reference path tends to be averaged out in the LMS loop, its size can be aggressively reduced to save power. To ensure sufficient linearity, a ratio-independent and offset-insensitive 1.5b/stage conversion architecture is adopted. It resolves 9b, consumes 2.4mW, and achieves an SFDR of 60.5dB in experiments.

Fig. 4.5.1 also shows the timing diagram of the ADC array. A dual-loop digital DLL synthesizes 10 uniformly spaced clock phases at 60MHz for the 10 paths, and further aligns them to a 600MHz clock that is generated off-chip [4]. The dual-loop scheme ensures that the 600MHz clock, which is used for the input sampling, experiences minimum on-chip processing, thus minimizing its jitter. A digital duty cycle control of the 60MHz clocks warrants a non-overlapping time (t_{nov}) in anticipation of clock-phase skews arising from distribution. An on-chip clock generator derives a 599.4kHz (600MHz/1001) clock to drive the algorithmic ADC with the same pulse width as those of the interleaved ones.

The prototype chip is fabricated in a 0.13µm 1P8M CMOS process, and occupies an active area of 1.1mm^2. All measurements described below are performed at 600MS/s, 1.2V supply, and room temperature. The digital equalization and data aggregation are performed in software. Due to a digital timing error, we are not able to capture the output data of the algorithmic ADC for the input frequencies above 2MHz. Therefore, the ADFs are trained at 2MHz, and their tap values are frozen for measurements at higher input frequencies. Fig. 4.5.4 shows the measured output spectra of the ADC array before and after calibration with an input frequency of 7.8MHz. Equalization results in an SNDR improvement from 31.2dB to 46.7dB, and an SFDR improvement from 33.0dB to 65.2dB. The large spurs due to path mismatch are largely eliminated. The measured peak INL/DNL is 1.7/1.3LSBs and 0.23/0.3LSBs at 8b level before and after calibration, respectively. Fig. 4.5.5 shows the measured SNDR and SFDR versus the input frequency. The SNDR is maintained above 40dB up to 460MHz. In the experiments, it takes 200k reference samples (0.33s) to train all 10 interleaved paths. The array SNDR during a typical adaptation process is shown in Fig. 4.5.6. The peak-to-peak SNDR fluctuation of the ADC array is <0.5dB in steady state due to continuous background tracking. The analog, digital, and DLL power consumption values are 13.7, 7.6, and 6.7mW, respectively. The area and power of the calibration logic (10 ADFs mainly) are estimated to be 0.08mm^2 and 2.3mW. This time-interleaved ADC array achieves an FOM of 0.208pJ/conversion-step with a 62.1MHz input and 0.340pJ/conversion-step with a 302.1MHz input, when the DLL power is excluded.

Acknowledgments:
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References:
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[2] W. Liu and Y. Chiu, "An Equalization-Based Adaptive Digital Background Calibration Technique for Successive Approximation Analog-to-Digital Converters," *Int. Conf. on ASIC*, pp. 289-292, Oct. 2007.
[3] B. P. Ginsburg and A. Chandrakasan, "Highly Interleaved 5b 250MS/s ADC with Redundant Channels in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 242-243, Feb. 2008.
[4] P. Bhoraskar and Y. Chiu, "A 6.1-mW Dual-Loop Digital DLL with 4.6-ps RMS Jitter using Window-Based Phase Detector," *Asian Solid-State Circuits Conf.*, pp. 79-82, Nov. 2007.

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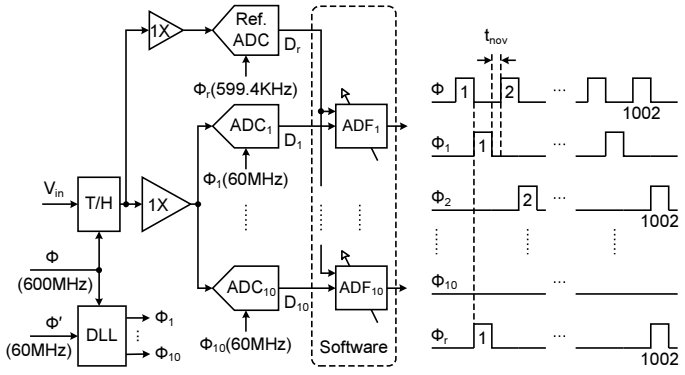

Figure 4.5.1: Block and timing diagrams of the ADC array.

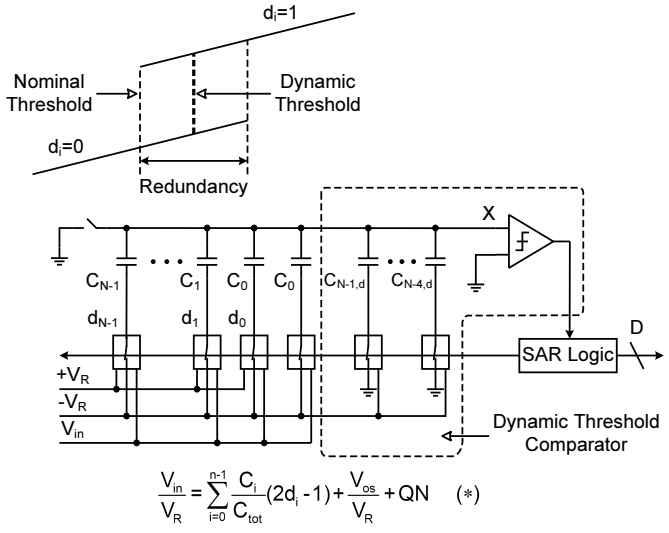

Figure 4.5.2: SAR ADC with dynamic threshold comparison scheme.

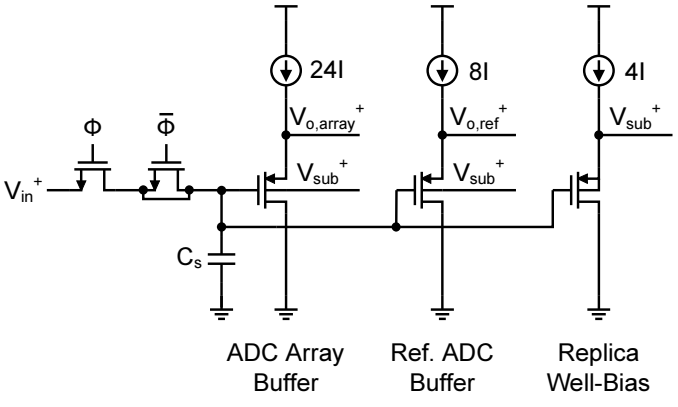

Figure 4.5.3: Front-end T/H and buffers.

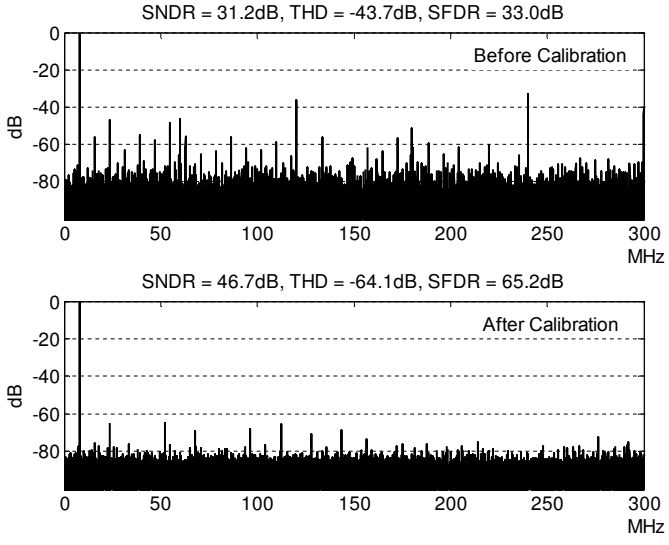

Figure 4.5.4: ADC array output spectra at 600MS/s with a 7.8MHz input.

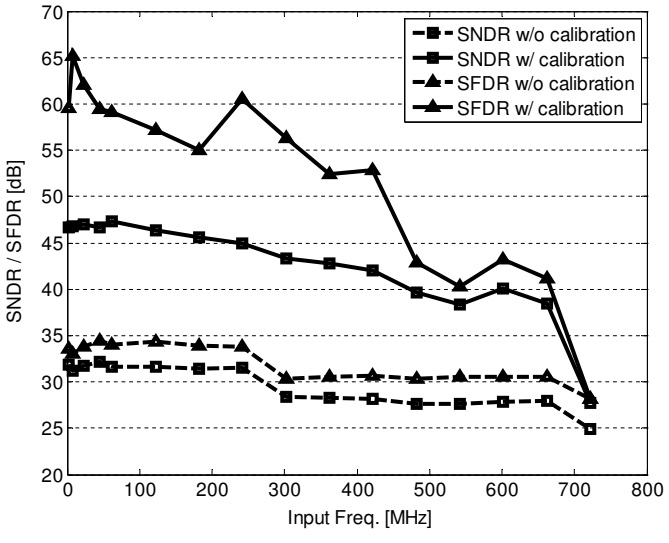

Figure 4.5.5: SNDR and SFDR of the ADC array at 600MS/s.

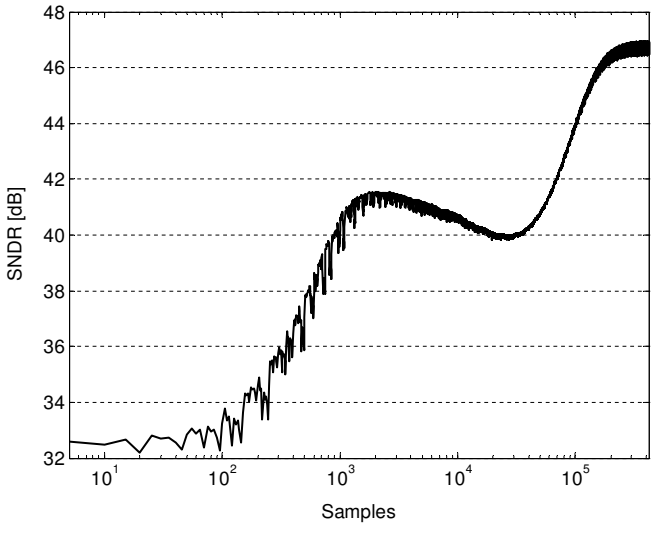

Figure 4.5.6: Learning process of the ADC array versus the reference samples.

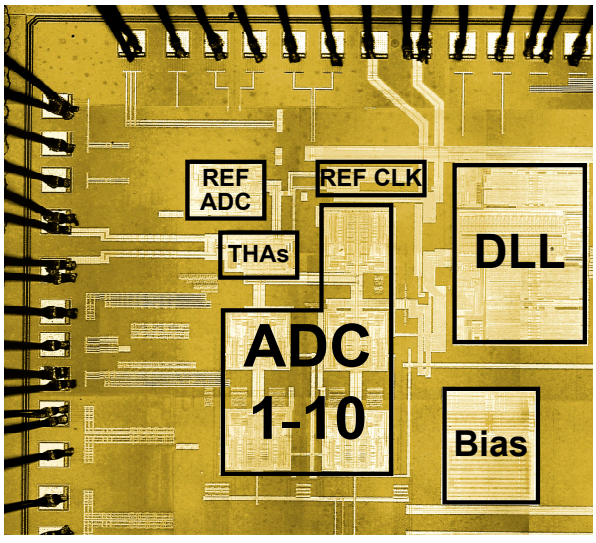

Figure 4.5.7: Die micrograph.

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