An Equalization-Based Adaptive Digital Background Calibration Technique for Successive Approximation Analog-to-Digital Converters

Wenbo Liu and Yun Chiu

Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA
Email: {wliu8, chiuyun}@uiuc.edu

Abstract

This paper presents an equalization-based digital background error-correction technique for successive approximation analog-to-digital converters (SA-ADCs). Computer simulation indicates that large differential and integral nonlinearities resulting from component errors including capacitor mismatch, comparator offset, and switch-induced offset can be corrected in the digital domain by an FIR adaptive filter, which essentially performs a linear equalization (LE) to align the digital codes of the SA-ADC to those of a slow-but-accurate reference ADC. In return, the size of the sampling capacitors can be scaled down to the kT/C limit without matching concerns. For SA-ADCs with resolutions of 10 bits and above, a large power saving is envisioned using the proposed low-cost, power-efficient digital calibration technique. The treatment improves the scalability and power efficiency of SA-ADCs in deeply scaled CMOS technology.

1. Introduction

At medium conversion speeds, switched-capacitor successive approximation architecture provides a useful method of analog-to-digital conversion with low power consumption. Due to its inherent structural simplicity, SA-ADC is more amenable to CMOS technology scaling than pipeline, algorithmic, and sigma-delta architectures. Nowadays, SA-ADCs with moderate resolutions, e.g., 6-8 bits, can digitize a bandwidth of a few hundred megahertz with an excellent figure of merit (FoM) [1]. However, at resolutions of 10 bits and beyond, the performance of the SA-ADC is likely to be limited by the matching accuracy of the digital-to-analog converter (DAC), which usually leads to large sampling capacitors and complicated analog circuits and layout, degrading the power efficiency and the signal tracking bandwidth of the converter [2]-[4].

This paper presents a digital background calibration technique to correct the conversion errors of SA-ADCs. An FIR adaptive digital filter (ADF) is used to treat all component errors simultaneously. The coefficients of the filter are updated with a sign-sign least-mean-square (LMS) algorithm by comparing the filter output with that of an accurate-but-slow (therefore extremely low power) reference ADC. With the error correction performed completely in the digital backend, the analog signal path is kept as simple and minimal as possible, improving the conversion speed and power efficiency of the SA-ADC. A similar calibration approach has been applied to the pipeline ADCs [5].

This paper is organized as follows: the successive approximation architecture and error mechanisms are briefly reviewed in Section 2, followed by the introduction of the equalization-based calibration approach in Section 3, and simulation results are presented in Section 4.

2. Review of SA-ADC

2.1 Architecture

A conventional N-bit switched-capacitor SA-ADC is shown in Fig. 1, which consists of an N-bit binary-weighted DAC, a single zero-crossing comparator and some logic gates. An analog input signal is quantized in N clock cycles using a binary search algorithm.

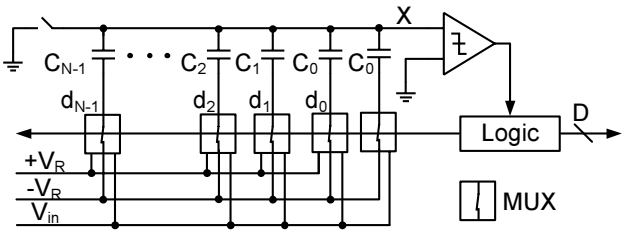

Figure 1. Switched-capacitor SA-ADC architecture

The circuit operates as follows. In the first conversion phase, all capacitors in the N-bit DAC are tied together to sample the input. Following this, the bottom plate of C_{N-1} (the MSB capacitor) is switched to $+V_R$, while all other capacitors are switched to $-V_R$. Charge redistribution forces the voltage at the summing node X to be

$$V_X = -V_{in} + \frac{C_{N-1}}{C_{tot}} V_R - \frac{\sum_{i=0}^{N-2} C_i + C_0}{C_{tot}} V_R, \qquad (1)$$

where $C_{tot} = \sum_{i=0}^{N-1} C_i + C_0$. The comparator then resolves the MSB d_{N-1} by determining the polarity of V_X. If $V_X > 0$,

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then $d_{N-1} = 0$, otherwise, $d_{N-1} = 1$. This process iterates N times and all N bits are resolved. Note that V_X approaches zero toward the end,

$$V_X = -V_{in} + \sum_{i=0}^{N-1}(2d_i - 1)\frac{C_i}{C_{tot}}V_R - \frac{C_0}{C_{tot}}V_R, \quad (2)$$

where C_i/C_{tot} is the weight of bit i. Typically, the capacitors are binary-weighted such that $C_i = 2^i C_0$ and C_0 is the unit capacitance. This is also known as the radix-2 conversion scheme.

2.2 SA-ADC Error Mechanisms

The conversion linearity of the SA-ADC is subject to circuit component nonidealities. Among these, capacitor mismatch and various offset errors are most noteworthy.

Capacitor Mismatch

When matching is accurate, the SA-ADC performs an ideal binary search to convert the sampled analog input into an N-bit binary code. The resulting ADC transfer curve is shown as the dotted line in Fig. 2 for a 12-bit example. In this case, the conversion is free of any differential or integral nonlinearity.

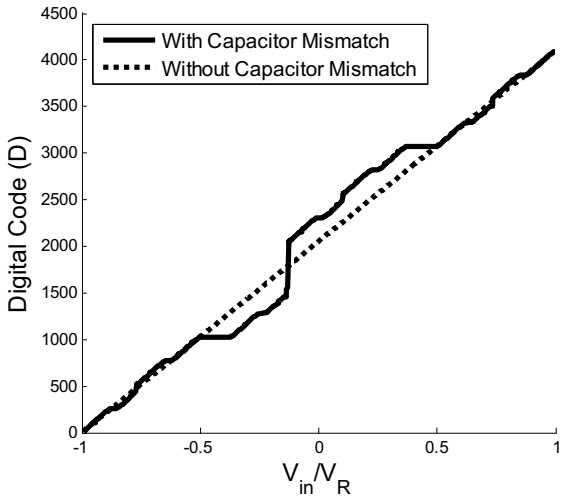

Figure 2. Transfer curves of a 12-bit SA-ADC

When capacitor mismatch is present, the ADC transfer curve is highly distorted, especially when small capacitors are used for fast settling and to reduce power consumption. As a result, the decision levels may no longer be uniformly distributed over the full input range, e.g., the one indicated by the solid line in Fig. 2. The vertical and horizontal misalignments are known as missing codes and missing decision levels, respectively. Note that a missing code can be corrected by a digital calibration, while a missing decision level is difficult to treat digitally [5].

Offsets

The comparator and switches contribute offsets to the SA-ADC. Since a bottom-plate sampling is typically performed, the injected charge Q of the summing-node switch is approximately independent of the input signal and only contributes a fixed offset. Equation (2) can be re-derived as

$$V_X = \frac{C_{tot}}{C_{tot} + C_p} \cdot (-V_{in} + \sum_{i=0}^{N-1}(2d_i - 1)\frac{C_i}{C_{tot}}V_R - \frac{C_0}{C_{tot}}V_R - \frac{C_{tot} + C_p}{C_{tot}}V_{os} - \frac{Q}{C_{tot}}), \quad (3)$$

where C_p is the parasitic capacitor at the summing node and V_{os} is the input-referred offset of the comparator. Although in principle the offset terms in (3) are signal-independent and do not affect the overall ADC linearity, certain applications (e.g., instrumentation) may require zero offset. Comparator auto-zeroing and correlated double sampling (CDS) techniques are often used to treat these offset errors, leading to complicated analog circuits and, more importantly, degrading the conversion speed and power efficiency.

3. Adaptive Digital Calibration

Based on the above analysis, the conversion linearity of a SA-ADC is mainly limited by the capacitor mismatch, and the signal-to-noise ratio (SNR) is limited by the kT/C noise for high resolutions. For example, assuming a 12-bit SA-ADC implemented in a 0.13-μm process with a 1.2-V supply, the calculated total sampling capacitance is listed in Table 1 for matching-limited and kT/C noise-limited scenarios.

Table 1. Total sampling capacitance of a 12-bit SA-ADC

Matching limited†	46.8 pF
kT/C noise limited	3.3 pF
This work	3.4 pF

It is evident that excessive power will be consumed in this case if capacitors are sized for matching accuracy. To eliminate this constraint, we introduce an adaptive digital technique that calibrates the capacitor mismatch error (and various offset errors simultaneously).

3.1 Sub-Radix-2 Conversion Algorithm

The conditions for missing codes and missing decision levels can be derived as shown in the following equations, respectively:

$$\sum_{j=0}^{i-1} C_j + C_0 - C_i > 0, \quad (4)$$

† Matching data is foundry supplied for metal-insulator-metal (MIM) capacitors of a 0.13-μm CMOS MMRF process.

$$\sum_{j=0}^{i-1} C_j + C_0 - C_i < 0, \tag{5}$$

where i = 1, 2 … N-1. As long as all capacitors are appropriately sized for a conversion radix ($\alpha = C_i/C_{i-1}$) less than 2, (4) is satisfied and (5) is prohibited. A subsequent digital-domain error correction is sufficient to remove all missing-code errors. This results in a sub-radix-2 conversion architecture. In this approach, note that the overall resolution of the SA-ADC can be maintained by a slight increase in the number of capacitors (N) to counteract the elevated quantization noise. Specifically, the relationship between N and the effective number of bits (ENOB) of the ADC is given by

$$ENOB \le \log_2 \frac{C_{tot}}{C_0} = \log_2\left(\frac{1-\alpha^N}{1-\alpha} + 1\right). \tag{6}$$

3.2 Capacitance Variation

When small capacitors are used, random variations in capacitance may impact the validity of (4). Let C_i be written as

$$C_i = (1+\Delta_i)C_{i,nom} = (1+\Delta_i)\alpha^i C_{0,nom}, \tag{7}$$

where we assume: (1) all Δ_i's are independent and observe a normal distribution $N(0, \sigma^2)$; (2) the conversion radix is α (< 2). Then the standard deviation of C_i is

$$\sqrt{\overline{(C_i - \overline{C_i})^2}} = \sigma\alpha^i C_{0,nom}. \tag{8}$$

Since C_i's observe independent normal distributions, letting (4) be true with a probability close to 1 (e.g., 0.95) leads to the following inequality relating σ and α:

$$\frac{1-\alpha^i}{1-\alpha} + 1 - \alpha^i - 1.65\sigma\sqrt{\frac{1-\alpha^{2i+2}}{1-\alpha^2} + 1} \ge 0. \tag{9}$$

Similarly, (6) is true with a probability of 0.95 if the following inequality holds:

$$\frac{1-\alpha^N}{1-\alpha} + 1 - 2^{ENOB} - 1.65\sigma\sqrt{\frac{1-\alpha^{2N}}{1-\alpha^2} + 1 + 2^{2ENOB}} \ge 0. \tag{10}$$

Given σ, (9) determines the maximum radix that can be used, and (10) determines the minimum number of capacitors N required to achieve a target ENOB. For example, given a 12-bit target ENOB, the tradeoffs between σ, N, and α are summarized in Table 2.

Table 2. Tradeoffs between σ, N, and α of a 12-bit SA-ADC

ENOB	σ	N	α
12	5%	13	1.91
12	10%	14	1.83
12	15%	15	1.77

Note that a larger capacitor mismatch requires a smaller conversion radix and more capacitors to compensate for.

3.3 Linear Equalization

Equation (3) can be rewritten as

$$D_{in} = \sum_{i=0}^{n-1} \frac{C_i}{C_{tot}}(2d_i - 1) + D_{os} + D_{qn}, \tag{11}$$

where $D_{in} = \frac{V_{in}}{V_R}$, $D_{os} = -\frac{C_0}{C_{tot}} - \frac{C_{tot}+C_p}{C_{tot}}\frac{V_{os}}{V_R} - \frac{Q}{V_R C_{tot}}$, and $D_{qn} = -\frac{C_{tot}+C_p}{C_{tot}}\frac{V_X}{V_R}$. Equation (11) formulates the linear equalizer to be used in the proposed digital calibration – the first term is the weighted sum of the digital bits, the second term is the total input-referred offset, and the last term is the quantization noise. An LMS algorithm is adopted to learn the unknown tap values of the LE.

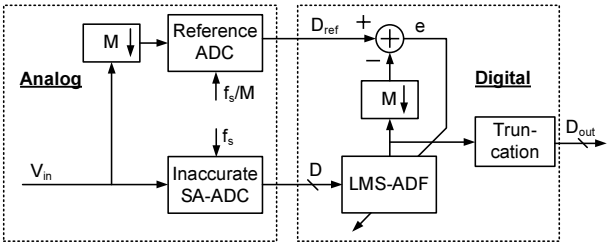

Figure 3. Equalization-based adaptive background digital calibration architecture of the SA-ADC

The resulting equalization-based SA-ADC calibration scheme is shown in Fig. 3. The raw output digital bits of the inaccurate SA-ADC under calibration are decimated by a large factor M and fed into an ADF, which equalizes these bits to those of the slow reference ADC. The ADF tap values are updated at the sample rate of the reference ADC. All signal processing is performed in the digital domain, avoiding complicating the analog circuitry with unnecessary calibration peripherals. Thus, the analog signal path is kept as simple and minimal as possible to exploit the intrinsic speed of deeply scaled process technologies. Note that this calibration scheme is also insensitive to the sampling clock skew between the reference ADC and the SA-ADC paths as long as the input signal exhibits equal rising and falling probabilities, and the resulting error is averaged out in the LMS loop.

3.4 Calibration Overhead

In this approach, the calibration overhead is the slow reference ADC and the digital calibration logic.

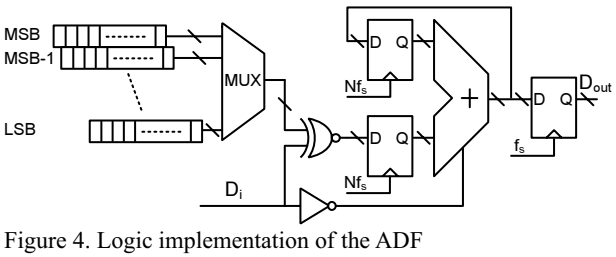

Figure 4. Logic implementation of the ADF

The reference ADC can take the form of an integration type. It digitizes the input signal at a much lower speed than that of the SA-ADC, and the associated power is negligible. A straightforward implementation of the ADF is shown in Fig. 4, where the output bits of the SA-ADC are serially fed into the FIR-type filter that performs N cyclic additions/subtractions every sample to convert the N-bit sub-radix-2 raw code to an accurate binary output word. The simple calibration logic involved here results in a low power and area overhead. The tap value update circuit, which is not shown in Fig. 4, runs at the same speed as that of the reference ADC; thus, its power consumption is also negligible.

4. Simulation Results

A 12-bit 10-MS/s prototype SA-ADC is simulated and calibrated in SIMULINK to demonstrate the effectiveness of the proposed LE-based calibration technique. Considering the non-binary capacitor array with a large capacitance spread and an LSB capacitance as small as 0.6 fF (the total input capacitance is 3.4 pF), a 10% capacitor mismatch error is assumed for the SA-ADC. Based on the second row of Table 2, this results in a radix-1.83 SA-ADC with a 14-bit raw code. In addition, a 100-ps sampling clock skew is also assumed between the two ADC paths. The SA-ADC output is calibrated with a 12-bit ideal ADC. To minimize the simulation time, the reference ADC converts the input at the same rate as that of the SA-ADC and the tap values of the LMS-ADF are also updated at this speed.

With a sine-wave input near Nyquist frequency, the convergence of the LMS algorithm with gear shifting takes about 60,000 samples. The FFT spectra of the input sine wave before and after calibration are shown in Figs. 5 and 6, respectively. The spurious-free dynamic range (SFDR) is improved from 40.7 dB to 92.9 dB, and the ENOB is improved from 5.55 bits to 11.98 bits. No harmonics are clearly visible after calibration.

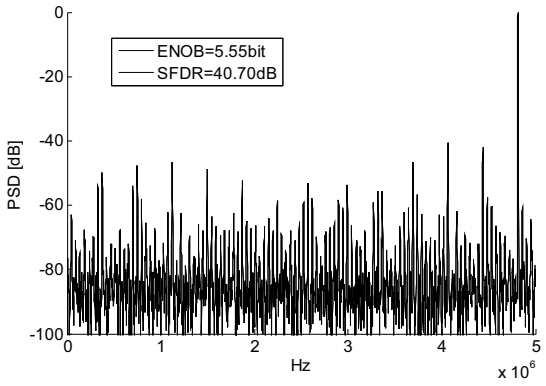

Figure 5. SA-ADC output spectrum before calibration

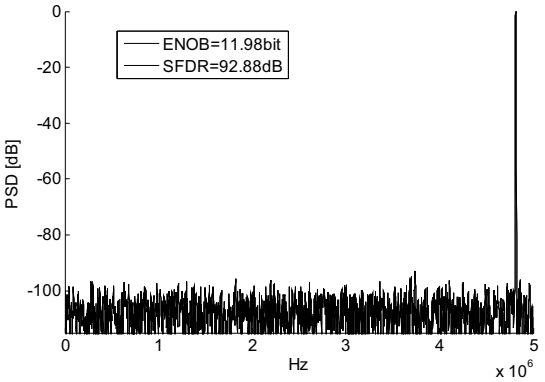

Figure 6. SA-ADC output spectrum after calibration

5. Conclusion

In this paper, a digital background calibration algorithm is introduced for SA-ADCs. Dominant analog error sources affecting the conversion linearity are analyzed and shown to be correctable in the digital domain, provided that a sub-radix-2 conversion architecture is employed. A linear equalizer is formulated, and the simulation results demonstrate the effectiveness of the equalization-based, digital error-correction technique. The greatly relaxed matching requirement of the sampling capacitors leads to simple analog circuit realizations and improved ADC performance. The approach will improve the scalability of the SA-ADC in deeply scaled CMOS processes with an accompanying reduction in power consumption.

References

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