A New Figure of Merit Equation for Analog-to-Digital Converters in CMOS Image Sensors

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***Abstract*—This paper presents a new figure-of-merit (FoM) equation for column analog-to-digital converters (ADCs) in CMOS image sensors. The proposed FoM incorporates the dynamic range, resulting from the minimum dark-level random noise and the maximum full well capacity, as well as AD conversion time, power consumption, and area. Using this FoM, we have analyzed various ADC architectures including cyclic, delta-sigma, successive approximation register, single-slope (SS), two-step and hybrid topologies. Using the suggested equation and data collected over the past ten years, we elucidate the reasons behind the dominance of the column-based SS ADC in commercial products. The proposed FoM is therefore useful for gauging the potential of new architectures and for architecture selection at an early stage of the design process.**

Keywords—CMOS image sensor (CIS), Analog-to-digital converter (ADC), Figure-of-Merit (FoM).

I. Introduction

Image sensors have become important components not only for cellular phones, cameras, automotive vehicles and medical devices, but also for the Internet of Everything (IoE). Especially in CMOS image sensor (CIS) design, it is critical to choose a proper analog-to-digital converter (ADC) architecture to convert the signals from all pixels into digital data. During the past two decades, various single or column-parallel ADCs have been introduced with low power consumption and high sampling rate. However, the pixel pitch has become smaller, making it more difficult to identify an ADC architecture with a good trade-off between noise, speed, power consumption, and area. Generally, it has become increasingly challenging to design an efficient ADC without degrading the overall CIS performance.

The single ADC architecture [1] was used extensively in the past, but comes with large power consumption for today's high-resolution imagers due to the commensurately high conversion rate. Currently, column-parallel ADC architectures with low power, high speed and high resolution are being deployed in place of the single ADC architecture. Fig. 1 shows the pixel rate (*PR*) trend over the past decades for various column ADCs, such as cyclic [2]–[6], delta-sigma (ΔΣ) [7]–[8], successive approximation register (SAR) [9]–[15], single-slope (SS) [16]–[27], and two-step or hybrid topologies [28]–[38]. *PR* is defined by the product of the frame rate and the number of pixels and is expected to increase further in the future.

All ADC topologies in Fig. 1 have characteristic benefits and limitations. Cyclic ADCs provide relatively fast conversion, but require a very high gain analog amplifier, leading to high power consumption. ΔΣ ADCs achieve low temporal noise by taking multiple samples of each pixel output, but they necessitate high

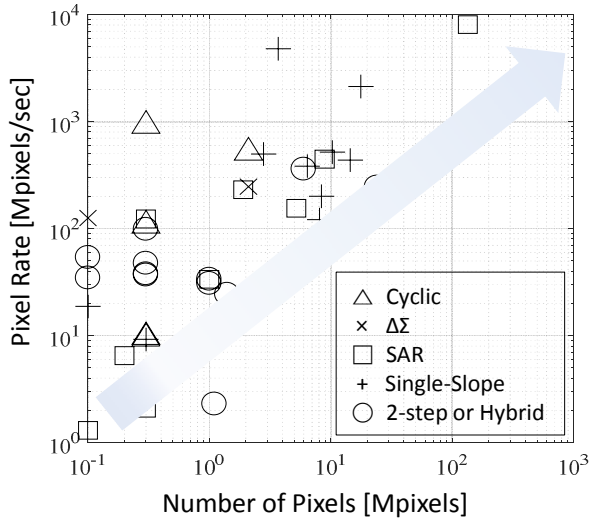

Fig. 1. Pixel rate vs. number of CIS pixels (from published data).

complexity due to gain control and mismatch mitigation in their feedback digital-to-analog converters (DACs). SAR ADCs have the best power efficiency but impose large silicon area because of the binary-weighted capacitor array and the (typically) required calibration circuitry. SS ADCs have been adopted as the result of their good linearity and relatively low power consumption. However, a main drawback is that the quantization period grows exponentially with ADC resolution. In addition, two-step or hybrid ADCs not only have gain mismatch between the coarse and the fine conversion steps, but they also suffer from circuit complexities due to the use of multiple reference voltages and the combination of several ADC architectures.

The figure-of-merit (FoM) equation presented in this paper was designed to consider the above-mentioned tradeoffs through the ADC's noise, speed, power consumption and area. The FoM results aid the designer in selecting the best topology among the various options. Until now, several FoM equations have been introduced in [7], [15], [34], [39]. However, these have proven insufficient for an objective comparison of image sensor ADCs and fail to explain the dominance of the SS approach.

II. Conventional ADCs FoM Equations

A commonly used FoM for ADCs in applications such as wireless and wireline communication is given by:

$$\text{FoM} = \frac{P}{f_s \times 2^{ENOB}} \left[\frac{\text{fJ}}{\text{conv.–step}}\right]. \quad (1)$$

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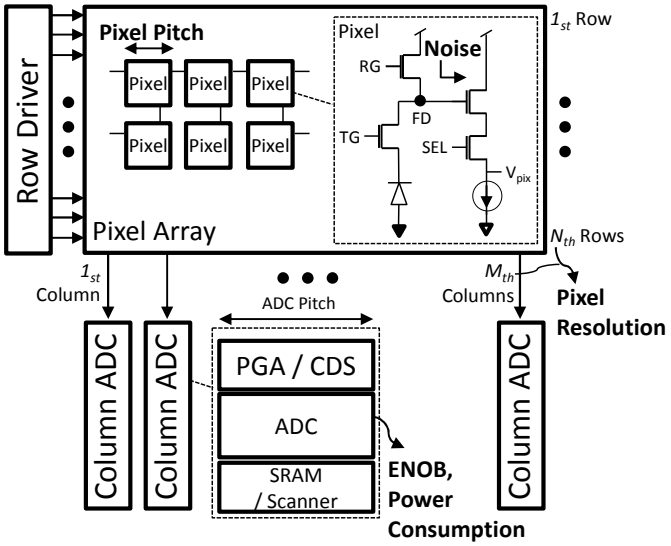
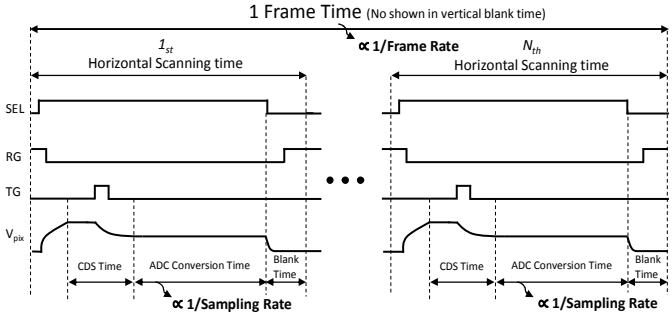
Here, P is the power consumption, f_s is the sampling rate, and *ENOB* is the effective number of bits. For image sensors, (1) is inappropriate when *ENOB* is limited by thermal noise, which leads to a power scaling proportional to 2^{2ENOB} (4x per bit or 6 dB). For proper benchmarking, the total noise of an image sensor is taken as the input-referred random noise (*N,* in electrons RMS) on the floating diffusion (FD) as shown in Fig. 2(a). Furthermore, (1) does not account for the impact of correlated double sampling (CDS) on the AD conversion time, as shown in Fig. 2(b).



(a)



(b)

Fig. 2. (a) Block diagram and (b) timing diagram for image sensors.

To address a subset of these deficiencies, CIS-specific FoMs have been proposed, reflecting the frame rate, pixel resolution and input-referred random noise in addition to the *ENOB*:

$$\text{FoM} = \frac{P \times N}{PR} \times 10^9 \ [\text{nJ} \cdot \text{e}^-] \tag{2}$$

$$\text{FoM} = \frac{P \times N}{PR \times 2^{ENOB}} \times 10^{12} \left[\frac{\text{pJ}\cdot\text{e}^-}{\text{conv.}-\text{step}}\right]. \tag{3}$$

Even though (2) and (3) represent the sensor's characteristics, the area constraint is still not considered. Only the work of [39] has introduced an FoM containing the pixel pitch:

$$\text{FoM} = \frac{P \times N \times Pitch^2}{f_s \times 2^{ENOB}} \left[\frac{\text{pJ}\cdot\text{V}\cdot\mu\text{m}^2}{\text{conv.}-\text{step}}\right]. \tag{4}$$

Here, *Pitch* is defined by the size of a single pixel. However, a state-of-the-art column ADC tends to be twice as wide as a pixel, because it is difficult to fit within the small pixel pitch. Consequently, using the pixel pitch in (4) is not appropriate when the pitch of the ADCs is larger than this number. Moreover, (3) and (4) are still unsuitable when the *ENOB* is limited by thermal noise.

III. The Proposed ADC FoM Equation

ADC design for image sensors must not only consider power consumption and conversion time, but is also constrained by noise performance and area. The proposed FoM equation accounts for noise via dynamic range (*DR*), and includes the effect of programmable gain amplifiers (PGA) and CDS:

$$\text{FoM} = \frac{P \times ConvTime \times A}{10^{\frac{(DR_{dB}-1.76)}{10}}} \left[\frac{\text{fJ}\cdot\mu\text{m}^2}{\text{conv.}-step}\right]. \tag{5}$$

In (5), *ConvTime* is the normalized AD conversion time for processing the number of pixels via the designed ADC. *A* is the area defined by pitch times height of the ADC. *DR* is obtained from the full well capacity (FWC) and dark level read noise when the analog gain (AG) is unity. Dividing the *DR* by 10 in the denominator leads to the desired 4x per 6 dB power trade-off (limited by thermal noise).

In the following subsections, we describe the purpose of all variables in (5) and draw comparisons to other FoMs.

A. AD Conversion Time

Based on the frame rate and the number of pixels, the readout time of the column ADC is determined by the horizontal scanning time as shown Fig. 2(b). For example, the horizontal scanning time (1H time) consists of four components: reset settling, signal settling, AD conversion (CDS and quantization) and blank time. Digital CDS doubles the AD conversion time compared to analog CDS. However, analog CDS leads to inferior column fixed pattern noise (CFPN), because the reset switches of each CDS circuit yield different initial conditions (offsets) due to mismatch. Consequently, most commercial products use digital CDS.

The ADC pitch can be the same as the pixel pitch but making the ADC pitch twice as large can help alleviate the tight area constraints. Among the four types of layout placements shown in Fig. 3, the two-column shared ADC is operated at half the horizontal scanning time (H/2). On the other hand, if the ADCs are divided above and below the active pixel sensor (APS) and operate concurrently, the two-sided column ADC is operated at twice the horizontal scanning time (2H). Thus, the horizontal scan time can be reduced or extended depending on the ADC layout.

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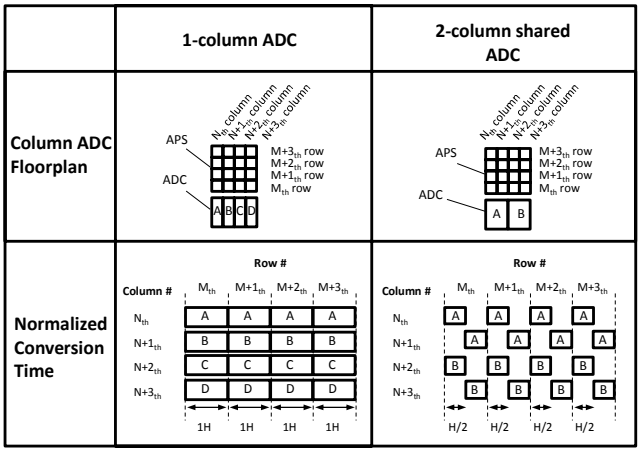
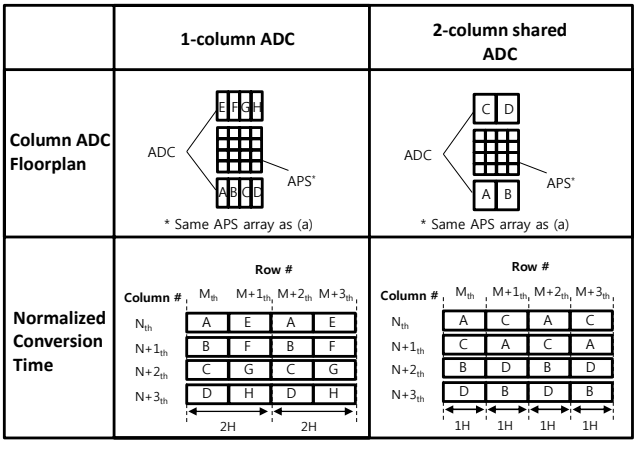
B. Dynamic Range

DR quantifies the ability of a sensor to take images from the darkest to the brightest illumination in a scene. Typically, the random noise is minimized, and the ADC's full-scale range is designed to accommodate the maximum pixel output (set by the FWC) with some margin. For example, the ADC full-scale range may be set between 1 and 1.5 times the output range of the pixel signals. As a result, the FWC is measured whereas the SNDR of ADCs is limited by the saturation level of pixel outputs, and therefore the proposed FoM uses the imager's *DR* instead of the ADC's peak SNDR.

As detailed in Fig. 4, *DR* is expressed by the read noise (n_I) as the lowest signal level and the FWC as the highest signal level. In a high illumination condition, the read noise is negligible so that DR is only limited by the maximum FWC. In contrast, at dark levels, the read noise is dominated by circuit noise and quantization noise (n_Q) if AG is unity. Here, the circuit noise is categorized according to gain dependency like gain-independent noise (n_{C_1}) and gain-dependent noise (n_{C_2}). In practice, it is possible to estimate the noise split between pixels and ADCs using thermal and flicker noise models of the pixels, but the noise model of pixel transistors is usually confidential.



(a)



(b)

Fig. 3. (a) One-sided and (b) two-sided column ADC layouts for imagers.

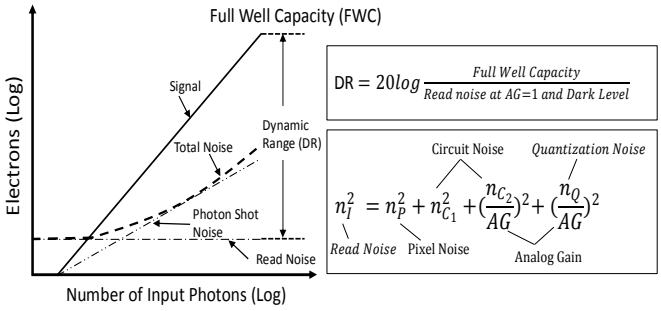


Fig. 4. Dynamic range definition with full well capacity and noise.

C. Power Consumption and Area

Fig. 5 compares the measured power consumption of different ADC architectures in CIS over 2 Mpixel/s, based on published papers during the past decade. In Fig. 5, although SAR ADCs and the ΔΣ ADC have lower power consumption, their architectures excludes PGA and CDS [7], [9]–[11], whose power consumption scales with the number of columns. Better estimates are obtained when the PGA and CDS power is added to the total power consumption.

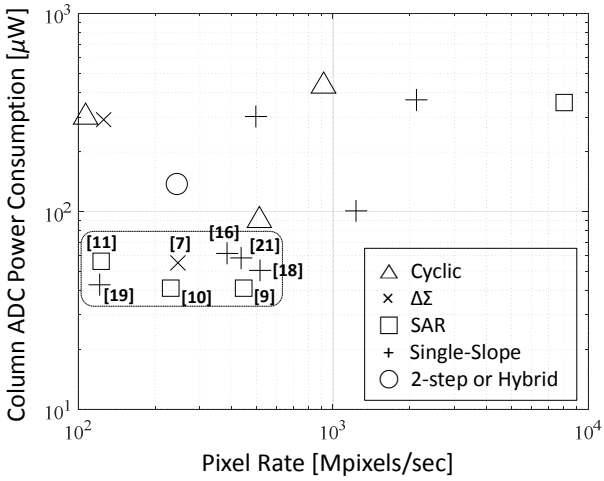


Fig. 5. Column ADC power consumtion vs. pixel rate.

As we have already explained, the column ADC layout and its area are important because they affect the conversion time budget and power consumption. Thus, we include area in the FoM, assuming direct proportionality (like power and conversion time). To study the relationship between ADC area and pitch, we consider the data of Fig. 6. The column ADC area (red markers) includes CDS and PGA and was estimated using chip microphotographs. We see that the square of the ADC pitch could be used as a good proxy in the FoM equation, because the trends are well aligned (black vs. red markers in Fig. 6).

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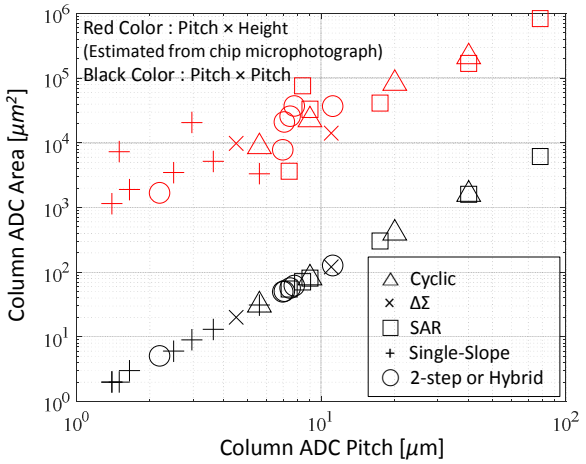

Fig. 6. Comparison of column ADC area for several ADC architectures.

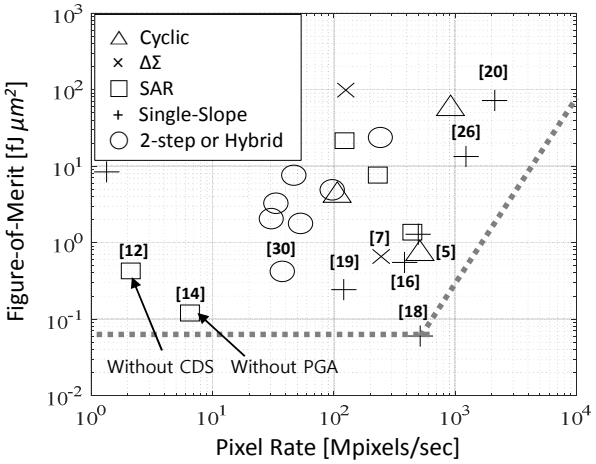

Fig. 7. FoM plot for various ADCs.

D. Results from the Proposed FoM Equation

Fig. 7 illustrates FoM data for various ADCs using (5). Based on the proposed FoM, the SS ADCs have the best (or lowest) FoM results and define the dotted boundary lines. The SS ADC has the advantages of small area within a column, and it overcomes the limit of conversion time by layout placement, and by having no additional PGAs. The SS ADC is especially attractive due to demanding cost reduction and development of slim sensors, which have led to 1-μm pixel pitch. Major companies like SONY [18] and Samsung Electronics [19] prefer to use SS ADCs for commercial products.

In Fig. 7, although SAR ADCs like [12] and [14] are implemented with better FoM, they are considered only as ADCs without CDS and PGA. Without PGA, the ΔΣ ADC [7] could provide AG by increasing its resolution through increased sampling frequency, but this consumes additional power. For example, a 12b ΔΣ ADC could be used for the design of a 10b ΔΣ ADC with 4x AG. Alternatively, many two-step or hybrid ADCs have been optimized with reused architectures like [30], [37] to overcome the disadvantage of SS ADCs. However, to achieve the best FoM, the ADC design must minimize the noise and the area including CDS and PGA. Thus, forming a hybrid architecture based on the SS ADC is one solution for supporting CDS and PGA. New ADC architectures continue to be invented and may lead to improved performance trade-offs.

IV. Conclusions

A new ADC FoM equation was devised for comparing column ADCs for image sensors. To implement the best ADC architecture for image sensors, circuit designers must choose a suitable trade-off between power consumption, conversion time, layout placement and area, all of which are captured in the FoM. The suggested FoM not only provides guidance for the design of column ADCs, but also enumerates the competitiveness of various ADCs with respect to criteria that are important in image sensors. We plan to embed the ADC FoM within an image design assistant system (IDAS) for next-generation sensor product development.

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