A Low-Power Pilot-DAC Based Column Parallel 8b SAR ADC With Forward Error Correction for CMOS Image Sensors

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***Abstract*—Successive-Approximation-Register (SAR) Analog-to-Digital Converters (ADC) have been shown to be suitable for low-power applications at aggressively scaled CMOS technology nodes. This is desirable for many mobile and portable applications. Unfortunately, SAR ADCs tend to incur significant area cost and reference loading due to the large capacitor array used in its Digital-to-Analog Converter (DAC). This has traditionally made it difficult to implement large numbers of SAR ADC in parallel. This paper describes a compact 8b SAR ADC measuring only 348 μm $\times$ 7 μm. It uses a new pilot-DAC (pDAC) technique to reduce the power consumption in its capacitor array; moreover, the accuracy of the pDAC scheme is protected by a novel mixed-signal Forward Error Correction (FEC) algorithm with minimal circuit overhead. Any DAC error made during pDAC operation can be recovered later by an additional switching phase. Prototype measurements in 0.18 μm technology shows that the DAC's figure-of-merit (FoM) is reduced from 61.3 fJ/step to 39.8 fJ/step by adopting pDAC switching with no apparent deterioration in Fixed-Pattern Noise (FPN) and thermal noise.**

***Index Terms*—CMOS image sensor, error correction, SAR ADC.**

I. Introduction

THE solid-state image sensors market has experienced explosive growth over the past decade, accelerated by growth in mobile imaging, digital still and video imaging cameras, optical sensors, and industrial machine vision. This trend is expected to continue with rising demands from emerging applications in sensor networks, biomedical imaging, man-machine interfacing, digital surveillance, robotics, etc [1].

New challenges now confront CMOS imagers as fabrication technologies continue to scale down. At 0.25 μm and below, digital CMOS technology is not directly suitable for building high quality image sensors due to poor optical transmission, signal capacity, and noise [2]. The general trend is that analog performance is worsening at these deep-sub-micron technologies [3], [4]. Yet the adoption of even more aggressively scaled technologies seems inevitable as the steady increase in image resolution, frame-rate, and mobility demands ever higher data throughput at tightly constrained power budgets. Successive Approximation Register (SAR) ADCs have received renewed interest in recent years because their architecture is inherently suited for low-power applications with moderate sampling rate and resolution at aggressively scaled technology nodes. Column parallel SAR implementations have recently become popular in state-of-the-art high resolution image sensors [5]–[8]. The ideal ADC for column parallel architectures should be compact, low-power, and fast. Modern image sensors typically have pixel pitches in the order of 1 um to 5 um depending on their application [3]. The column circuit must fit into a pitch of the same order. Typical commercial 5 mega-pixel image sensors for mobile applications have power consumptions of approximately 260 mW. If half of this power budget is allocated to the column parallel ADCs, then each column will have a power budget of 50 μW. Such an image sensor will typically have frame-rates of around 10 frames-per-second (fps) at full resolution; therefore, each column ADC must have a sampling frequency of no less than 20 KSa/s even if analog Correlated Double Sampling (CDS) is used. In a SAR ADC, these specifications are largely constrained by the performance of its Digital-to-Analog Converter (DAC). Modern low-power SAR ADCs typically use capacitor array DACs. It is therefore not surprising that much of the recent SAR ADC research effort has focused on reducing the effective capacitive load presented by the DAC to the rest of the system. The benefit is two-fold: a smaller capacitor consumes less switching power in the column circuit during conversion; but just as importantly, the smaller load presented to the reference generator allows the reference generator to use smaller bias currents at the same sampling frequency. The later leads to further power saving at the system level.

The DAC capacitor array size can be reduced if additional voltage references are used to resolve the LSBs instead of using smaller capacitors. Matsuo *et al.* [7] used 3 scaled reference voltages (V_{ref}, $V_{ref}/2^2$, and $V_{ref}/2^4$) to reduce the capacitor array size by a factor of 2^4. The additional reference voltages need to be carefully matched to achieve the target resolution and guarantee monolithic ADC codes. Shin *et al.* [6] took this

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idea one step further. The binary weights are generated by a converging differential reference voltage during the binary search. The column level DAC is basically an analog integrator that integrates a signed reference voltage whose magnitude is halved at each clock. The integrating capacitor can be made very small, but a very accurate programmable reference voltage generator is needed to make this circuit work. The analog integrator must be sized to meet the same thermal noise requirement as it is the case for conventional pipeline ADCs. In more aggressive technology nodes, an analog integrator with high gain operational amplifier may be challenging to design. The ADC input range is limited to 0.9 V and elaborate off-chip calibration is also needed to achieve the target resolution.

Another way to reduce the size of the DAC capacitor array is to split it into smaller sub-arrays and connect them by a bridging capacitor [9]. In the Split Capacitor Array (SCA), one or more attenuation capacitors are connected in series to divide the DAC array into smaller sub-partitions so the total capacitance required for a given resolution is exponentially smaller. A special case of this implementation is the C-2C network where an attenuation capacitor is connected in series to every switching capacitor. Neither of these techniques are immune to capacitance mismatch and bottom-plate parasitic. They often require calibration to achieve reasonable resolution.

In the case of split capacitor arrays, digital calibration is typically needed to achieve capacitance reduction without suffering resolution loss. For C-2C networks, the pseudo-C2C network [10] can be used to compensate for the bottom-plate parasitic capacitance, but only if this parasitic effect can be accurately modelled. Since the unit capacitors used in the pseudo-C2C network are subject to the same device mismatch, thermal noise, and charge injection error requirements as the conventional case, they must be sized accordingly.

Another category of techniques for improving DAC performance involves modifying the capacitor switching sequence. Several methods in literature [11], [12] have sought to extend the DAC resolution for a given capacitor array size by performing charge sharing among differently sized capacitors. In addition to the conventional array switching scheme, binary-weighted capacitors are switched in and out of the array to resolve the DAC output at finer resolutions. This multi-step approach can exponentially reduce the total array capacitance necessary to achieve a given ADC resolution. Unfortunately, these schemes all require a large number of switches (typically connected to the top-plate) whose charge injection error can make it difficult to implement high resolution DACs. Boot-strapped switches will alleviate the problem to some extend, but they themselves will introduce a significant amount of overhead.

Ginsburg [13] has shown with theoretical analysis that the amount of energy dissipated (and equivalently, the amount of current drawn) in the capacitor array is asymmetric between a 1 (up) and 0 (down) bit-decision. If the SAR controller can take advantage of this information, the same DAC output sequence can be achieved with less energy, and hence faster settling in the reference supply. Several techniques have been proposed by Ginsburg [13] to improve capacitor switching efficiency. This class of methods typically incur significant complexity in digital control since the switching sequence is now input dependent. This overhead is expensive for column-parallel implementations used in CMOS image sensors. In schemes with simpler digital control [14], undesirable reference drifts may require additional Correlated Double Sampling (CDS) to maintain comparator accuracy. This will typically lead to additional energy dissipation in the comparator.

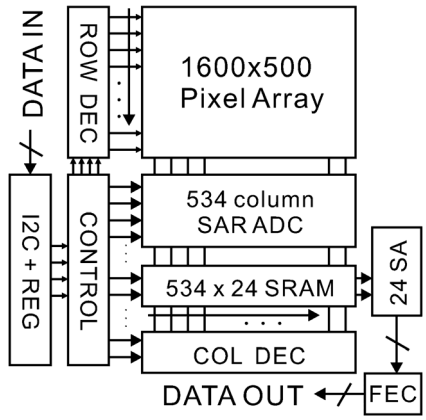


Fig. 1. Block diagram of the image sensor chip.

In Merged Capacitor Switching (MCS) [15] or similar methods [16], an additional reference (typically the $Vdd/2$ common mode voltage) is used to halve the required capacitor array (the LSB resolution is extended by the smaller reference range). The MSB can be determined without trial-and-error, and subsequent capacitor switching is determined by the previous bit; therefore, no wasteful switching pattern will be introduced. What needs to be taken into account though, is that this approach would double the number of references and increase the reference generator's power consumption.

The DAC speed in a SAR ADC is primarily limited by the RC time constant needed for the DAC voltage to settle. This time constant grows exponentially with the number of binary weights in the DAC. Error correction techniques [17] are useful for compensating against dynamic errors such as improper settling. The common disadvantage in this class of methods is that they all require some form of re-switching ($+/-1$ operation) in the DAC and the re-switching sequence is not guaranteed to be optimal. An optimal switching sequence should avoid the recharging of MSB capacitors whenever possible to minimize the reference supply power consumption. The digital controller for error correction also needs a MSB-section-wide adder to re-calculate the MSB bits during error correction.

In this article, a compact SAR ADC with novel pilot-Digital-to-Analog-Converter (pDAC) switching is proposed to address the above mentioned issues. The pDAC scheme can reduce the DAC power consumption in SAR ADCs while relaxing the reference generator's load driving requirement. The pDAC is combined with an error correction technique which uses a small redundant capacitor split from the MSB capacitor to perform re-switching in the charge domain. This redundant re-switching will help to correct any error induced during the pDAC phase because of device mismatch. The re-switching energy consumption is low compared to the conventional

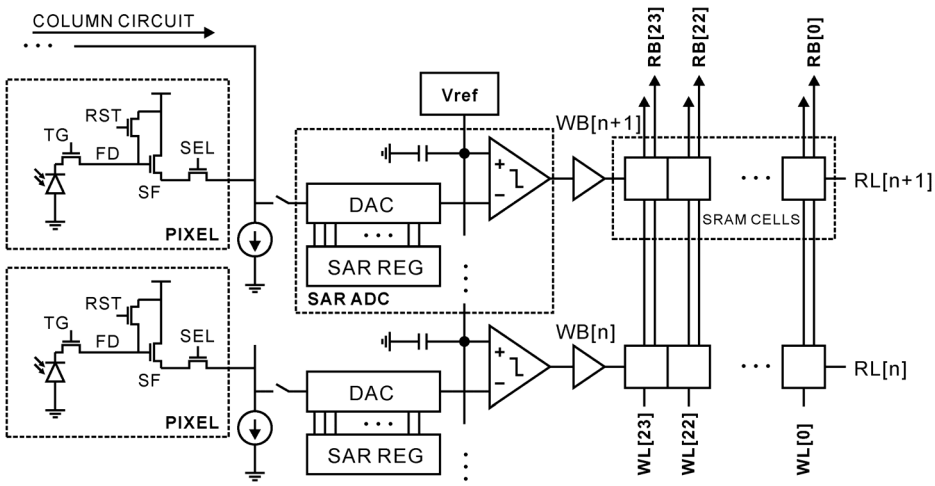


Fig. 2. The column circuit: from pixel to source follower to SAR ADC to SRAM.

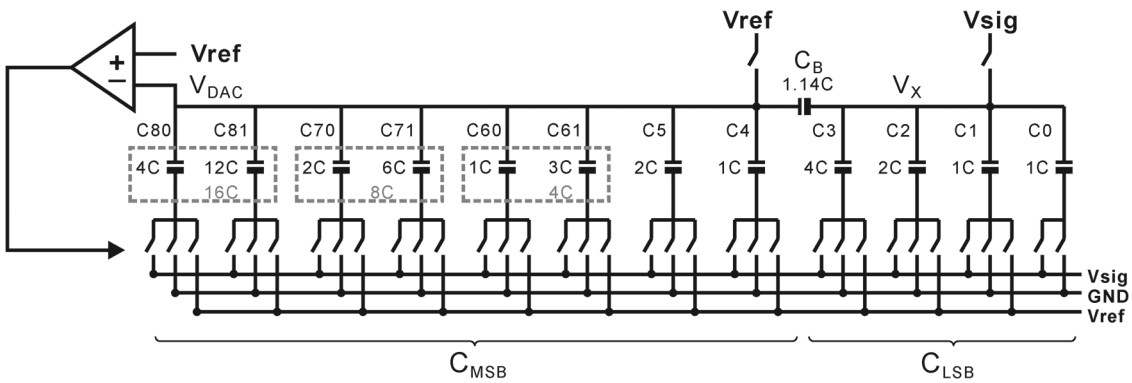


Fig. 3. SAR ADC with pilot-DAC (pDAC) and labeled capacitors.

MSB-to-LSB capacitor switching and no feedback is required to recalculate the MSB bits during conversion, so the correct digital word can be calculated from the redundant bit at a later stage when the results are read from the ADC array.

The overall sensor architecture will be presented in Section II, where the working principle of the pDAC is explained. In Section III, the key circuit blocks and their operation are described. Measurement results are discussed in Section IV before final conclusions are made in Section V.

II. Image Sensor System Architecture

A CMOS image sensor featuring column parallel SAR ADCs is designed as a demonstration vehicle. The block diagram of this system is shown in Fig. 1. The pixel array is 1600 by 500. Each ADC and SRAM column circuit is shared between 3 pixel columns via a transfer-gate multiplexer (MUX). The details of this column circuit will be elaborated in the next section.

The ADC generates 9 bits of data for each sample including an error correction bit. There are 24 bits of SRAM in each column, 18 of which are used for on-chip digital CDS, while the remaining 6 bits are used for test purposes. One third of the selected row from the pixel array is quantized before the SRAM data is read out by the column decoder (COL DEC). This process is repeated 3 times to obtain the entire row of 1600 pixels, after which the row decoder (ROW DEC) increments to the next row. The row decoder has two multiplexers, one for pixel select and one for pixel reset. The exposure time can be controlled by setting the time difference between these two multiplexers.

The SRAM array has 24 pairs of differential output bit lines and each complementary pair of bit lines has its own sense amplifier (SA) at the output. The forward error correction (FEC) module performs digital CDS and ADC error correction before the pixel data is read off the chip.

The chip controller can be configured by the on-chip I^2C module with parameters such as exposure time, DAC mode, and test modes.

A. Pixel and Column Circuit

The column circuit starting from the pixel in the selected row is shown in Fig. 2. A 4 T pixel is chosen in this design to obtain greater sensitivity through the amplifying action of the TG transistor. The FD node voltage is sampled onto the SAR DAC's bottom-plate via the standard source follower twice: once after FD reset and once after pixel charge transfer. Two SAR ADC quantizations are performed and digital CDS is carried out during column readout. The two quantized digital words are bit-serially written into the SRAM bank during quantization. At the end of the two conversion cycles, the SRAM contents are scanned out one column at a time and the data is recovered by the sense amplifiers.

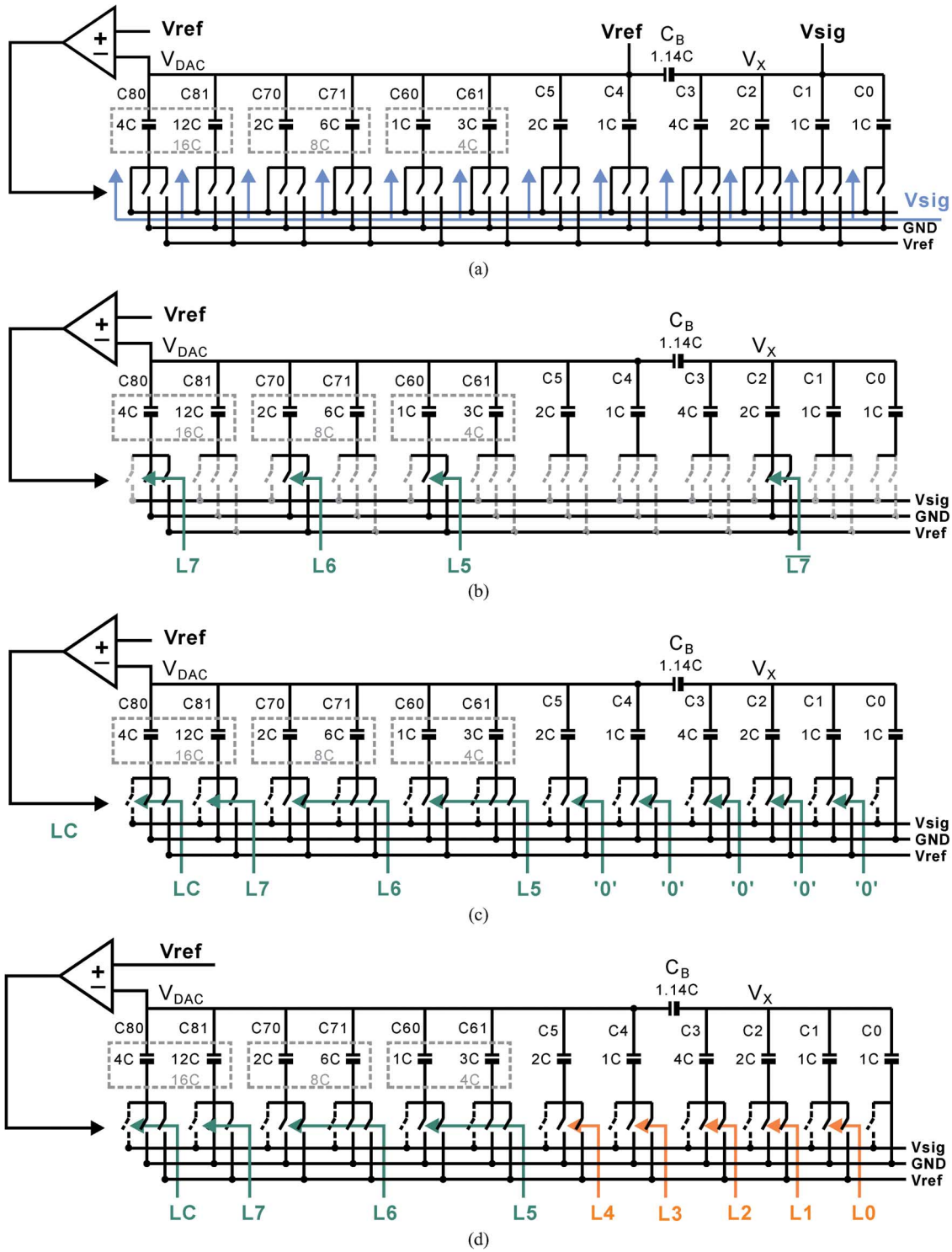


Fig. 4. (a) Sampling Phase. (b) Resolve the first 3 MSBs by pDAC switching. (c) Decide whether the sub-MSB capacitor (the 4C capcitor in the 16C MSB capacitor) needs to be reconnected. (d) Resolve the rest of the LSBs by conventional DAC switching.

B. Operation of pDAC

The basic concept of the SAR ADC is explained in this section. A control bit can set the ADC to operate in the conventional mode (for debugging purposes) if necessary. The ensuing discussions will focus on the pilot-DAC (pDAC) mode of the ADC which provides the low-power and fast-settling benefits.

The basic SAR topology is shown in Fig. 3. The split capacitor array consists of a k bit MSB section and a m bit LSB section.

$$N = k + m \tag{1}$$

$$C_{MSB} = \sum_{i=N-k+1}^{N} C_i \tag{2}$$

$$C_{LSB} = \sum_{i=0}^{N-k} C_i \tag{3}$$

$$C_B = \frac{2^m}{2^m - 1} C \tag{4}$$

The unit capacitor, C, is a 5 μm $\times$ 5 μm MIM capacitor with approximately 30 fF of capacitance. A comprehensive analysis on the parasitics effects related to the bridging capacitor, C_B, is detailed in [18].

$$C_i = \begin{cases} 2^{i-1-m}C & \text{if } m < i \leq N \\ 2^{i-1}C & \text{if } 0 < i \leq m \\ C & \text{if } i = 0 \end{cases} \tag{5}$$

In the sampling phase (Fig. 4(a)), the input signal is sampled onto the bottom-plate of the capacitor array. The capacitive load seen by the signal source and reference generator at this point is $32C$, so the usual settling requirements apply. During the SAR clock cycles, each of the binary weighted capacitors are tried to converge the DAC output, V_{DAC}, towards V_{ref}. Switching an array of these DACs in parallel, each with a $32C$ load, will pose a formidable challenge both in terms of capacitor charging power consumption and reference settling speed.

The core of the pDAC scheme is the idea of using only a small *pilot* portion of the total capacitor array, the pDAC, to determine the MSBs (Fig. 4(b)). The rest of the capacitor array is disconnected during this phase. The first $k-2$ capacitors in the MSB array (C_{MSB}) are split into two smaller capacitors. The pDAC array in this design is one quarter of the size of the MSB array:

$$C_{pDAC} = \sum_{j=N-k+3}^{N} C_{j0} \tag{6}$$

$$C_i = C_{i0} + C_{i1} \tag{7}$$

$$C_{i0} = \frac{1}{4} C_i \tag{8}$$

$$C_{i1} = \frac{3}{4} C_i \tag{9}$$

Once the 3 MSBs are determined, the rest of the MSB and LSB capacitors are connected on the fourth clock without any trial-and-error. The binary search can continue at this point using the conventional switching scheme.

While the pDAC scheme introduces savings in power consumption (shown in Section II-D), it requires very accurate matching between the pDAC and the rest of the capacitor array. This is difficult to do in practice. Instead, a mixed-signal Forward Error Correction (FEC) algorithm is proposed in Section II-C to address the quantization errors made during the pDAC phase.

In a conventional split capacitor array [19], the DAC output, V_{DAC}, can be calculated as:

$$V_{DAC} = V_{ref} \left(\sum_{i=N-k+1}^{N} \frac{C_i L_i}{C_{MSB} + C_B \parallel C_{LSB}} + 2^{-k} \sum_{i=1}^{N-k} \frac{C_i L_i}{C_{LSB}} \right) + (V_{ref} - V_{sig}) \tag{10}$$

where V_{ref} is the reference supply voltage, V_{sig} is the input signal sampled on the bottom-plate, and L_i is the digital value stored in the SAR register, which is initialized to 0 at the start.

In the pDAC scheme, the three MSB bits (L_8, L_7, and L_6) are determined using only C_{pDAC} (C_{80}, C_{70}, C_{60} and C_2 in Fig. 4(b)). The C_2 capacitor is asserted with C_{80} during the first trial clock (T_8, Fig. 10), and it is set to the inverse of the L_8 bit in subsequent clocks. This is necessary for introducing an offset for bipolar error correction range.

1) The pDAC Phase: In the pDAC phase, for $N \geq i > N-k+2$,

$$V_{DAC_i} = V_{ref} \left(\frac{C_{i0} + \sum_{j=i+1}^{N} C_{j0} L_j + (C_{N-k-1} \parallel C_B)\overline{L_N}}{C_{pDAC} + C_{N-k-1} \parallel C_B + C_{par}} \right) + (V_{ref} - V_{sig}) \tag{11}$$

The parasitic capacitance, C_{par}, is mostly contributed from the floating bottom-plates during the pDAC phase. For a DAC with $N = 8$ and $k = 5$, it is approximately the size of the unit capacitor.

$$C_{par} \approx C \tag{12}$$

This is verified in SPICE simulation. Once the bottom plates are connected to active supplies after the FEC phase, the parasitic capacitance becomes negligible.

2) The FEC Phase: In the FEC phase, the rest of C_{MSB} and C_{LSB} are connected. The FEC capacitor, C_{80} is retried to correct for errors made during the pDAC phase (Fig. 4(c)). For $i = N-k+2$,

$$V_{DAC_i} = V_{ref} \left(\frac{C_{N0} + \sum_{j=i+1}^{N-1} C_{j0} L_j + \sum_{j=i+1}^{N} C_{j1} L_j}{C_{MSB} + C_B \parallel C_{LSB}} \right) + (V_{ref} - V_{sig}) \tag{13}$$

3) The LSB Phase: After the FEC phase, the DAC reverts back to the conventional switching scheme to resolve the remaining LSBs (Fig. 4(d)). The DAC output can be calculated by (10).

C. Forward Error Correction in pDAC

If the pDAC is not exactly one quarter of the MSB capacitor array, the scaling error made during pDAC switching will be much larger than 1 LSB. Missing codes will occur because V_{DAC} can never converge to V_{ref} in subsequent LSB trials. This scenario is probable because the smaller pDAC is likely to have worse device matching than the larger full sized capacitor array. This problem is addressed here by introducing redundancy into the DAC output function. Any error made during the pDAC phase will be corrected for during a redundant bit trial under the accuracy of the full sized capacitor array. The error resulting from mismatch in the pDAC can be written as:

$$\begin{aligned} E &= \widehat{V}_{DAC_{N-k+2}} - V_{DAC_{N-k+2}} + \varepsilon \\ &= V_{ref} \frac{\sum_{j=N-k+3}^{N} C_j L_j}{C_{MSB} + C_B \parallel C_{LSB}} \\ &\quad - V_{ref} \frac{\sum_{j=N-k+3}^{N} C_{j0} L_j + C_{N-k-1}\overline{L_N}}{C_{N-k-1} \parallel C_B + C_{pDAC} + C_{par}} + \varepsilon \end{aligned}$$

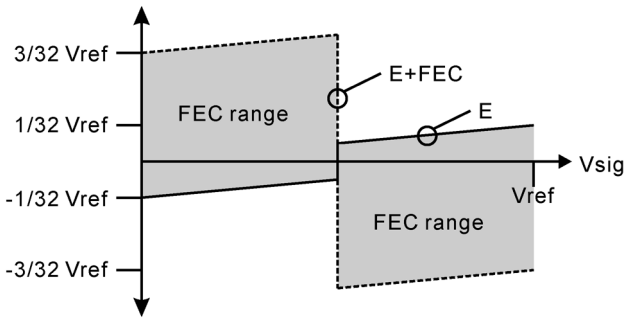


Fig. 5. Error correction range of the proposed FEC algorithm.

$$\begin{aligned} &\approx V_{ref}\frac{C}{C+C_{MSB}} \times \frac{\sum_{j=N-k+3}^{N} C_j L_j}{C+C_{MSB}} \\ &\quad - V_{ref}\frac{C\overline{L_N}}{C+C_{MSB}} + \varepsilon \\ &\approx \frac{C}{C+C_{MSB}}V_{sig} - V_{ref}\frac{C\overline{L_N}}{C+C_{MSB}} + \varepsilon \end{aligned} \tag{14}$$

where $\widehat{V}_{DAC_{N-k+2}}$ is the $N-k+2$ th DAC output in an ideal SAR ADC with no mismatch and error compensation. The ε term represents the mismatch error.

During the FEC phase, if L_8 is 0, C_2 is set to V_{ref}. This creates an offset error in the DAC output (approximately 8 LSB). The 3 MSB result will always be smaller than what it ought to be. During the error correction clock, C_{80} can be reconnected to V_{ref} to add 2^5 LSBs to the result.

Alternatively, if L_8 is 1, C_2 is connected to GND. This creates a scaling error in the quantized MSB bits (less than 16 LSBs). The 3 MSB results will always be bigger than what it ought to be. During the error correction clock, C_{80} can be reconnected to GND to subtract 2^5 LSBs from the result.

$$FEC = V_{ref}\frac{C_{N0}\overline{L_N}L_C}{C+C_{MSB}} - V_{ref}\frac{C_{N0}L_N\overline{L_C}}{C+C_{MSB}} \tag{15}$$

After the FEC bit decision,

$$\begin{aligned} R = E + FEC \approx &\frac{C}{C+C_{MSB}}V_{sig} - V_{ref}\frac{C\overline{L_N}}{C+C_{MSB}} \\ &+\varepsilon + V_{ref}\frac{2^{k-3}C\overline{L_N}L_C}{C+C_{MSB}} - V_{ref}\frac{2^{k-3}CL_N\overline{L_C}}{C+C_{MSB}} \end{aligned} \tag{16}$$

and the R residual is quantified by the remaining LSBs. Fig. 5 illustrates the FEC range for $N=8$, $k=5$, and $\varepsilon=0$. The FEC range is not centred around 0 because it needs to account for non-zero ε resulting from parasitic capacitance in the DAC. The ε profile can be found by post-layout simulation.

In either case, the final DAC output, V_{DAC}, will converge towards V_{ref}, and L_C is added to $L_{8:1}$ to obtain the correct result:

$$D_{result} = (L_{8:6} + L_C - L_8) \times 2^5 + L_{5:1} \tag{17}$$

The 5 LSBs are obtained using the conventional switching sequence (Fig. 4(d)). Since the entire array is connected at this point, the final conversion result will enjoy the same precision and accuracy as the conventional switching scheme.

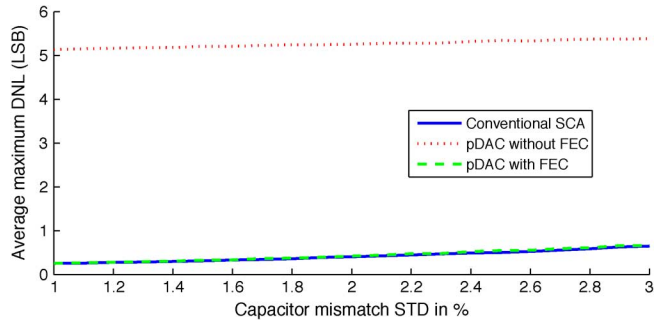


Fig. 6. Maximum DNL averaged over 100 Monte Carlo simulations for different capacitor mismatch standard deviations.

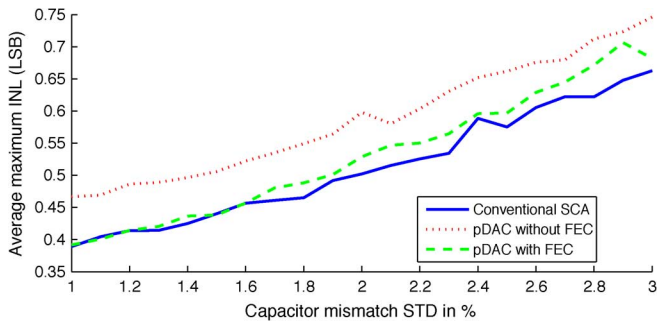


Fig. 7. Maximum INL averaged over 100 Monte Carlo simulations for different capacitor mismatch standard deviations.

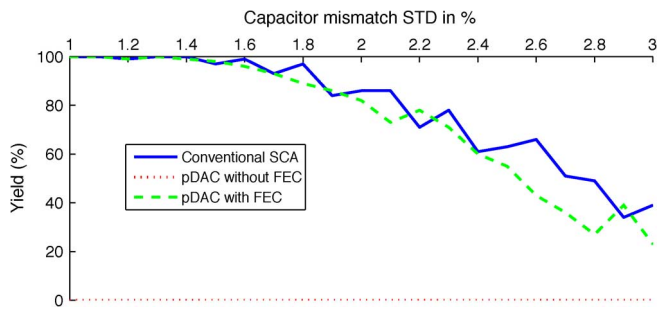


Fig. 8. Yield over 100 Monte Carlo simulations for different capacitor mismatch standard deviations.

In order to verify the FEC algorithm, 100 instances of Monte Carlo simulations are performed for the conventional Split Capacitor Array (SCA), pDAC SCA without FEC, and pDAC SCA with FEC. The definition of FEC includes both the mixed-signal circuit and the correction algorithm. So for the pDAC SCA without FEC, it has neither the C_{N-k-1} offset nor the C_{N0} FEC switching phase, and the D_{result} is calculated directly from the pDAC results. The maximum DNL and INL from each Monte Carlo instance is averaged over the 100 instances and the results are plotted in Fig. 6 and Fig. 7 for increasing capacitor mismatch. The capacitor mismatch is defined to be a Gaussian distribution with a standard deviation (STD) normalized to the unit capacitor. Parasitic effects are accounted for in these simulations. Assuming both DNL and INL must be under 1 LSB, the yield is calculated for each Monte Carlo batch and plotted in Fig. 8. Clearly, large MSB errors are made in the pDAC without FEC due to mismatch. The yield is zero in this case because the maximum DNL and INL always exceed 1 LSB. Once FEC is added, the pDAC error matches those of the conventional SCA.

D. Power Consumption Analysis

The DAC power consumption and speed are dominated by the MSB capacitors because they have the largest load and signal magnitude. Using a decimated array to calculate these MSBs will result in significantly smaller switching loads. When the rest of the array is connected at a later stage to determine the LSBs, the DAC output, $(V_{DAC_{i+1}} - V_{DAC_i})$, will already be very small. The benefit of this is two folds: the smaller switching load reduces the DAC's power consumption, and the load capacity of the reference generator is relaxed for the same sampling speed.

The power drawn from the V_{ref} supply is related to the total amount of charge drawn by the DAC capacitor array during each conversion period:

$$P_{V_{ref}} = F_s V_{ref} \sum_{i=0}^{N} Q_i \tag{18}$$

where F_s is the sampling frequency, and Q_i is the charge drawn from the V_{ref} supply during each clock. Using the simplification provided in [19], the V_{ref} power consumption for a simple n bit binary weighted capacitor array with no splitting can be written as:

$$P_{V_{ref}CBW}(n) \approx 2^n F_s C \left(\left[\frac{5}{6} - \left(\frac{1}{2}\right)^n - \frac{1}{3}\left(\frac{1}{2}\right)^{2n} \right] V_{ref}^2 - \frac{1}{2} V_{sig}^2 - \left(\frac{1}{2}\right)^n V_{sig} V_{ref} \right) \tag{19}$$

For a binary weighted split capacitor array with a k bit MSB array and m bit LSB array using the conventional switching scheme, its V_{ref} power consumption can be written as:

$$P_{V_{ref}}(conv) = P_{V_{ref}CBW}(k) + P_{LSB}(m) \tag{20}$$

The P_{LSB} term is the power consumption of the m bit LSB array. It has some terms related to the MSB results due to the bridging capacitor, C_B. Interested readers are directed to [19] for the explicit form of P_{LSB}.

The power consumption of the pDAC switching scheme for a N bit split capacitor array with k MSBs can be written as:

$$P_{V_{ref}}(pDAC) = P_{MSB} + P_{FEC} + P_{LSB} \tag{21}$$

where P_{MSB} is the power consumption of the MSB array (with pDAC switching), P_{FEC} is the overhead from the FEC phase, and P_{LSB} is the power consumption of switching the LSB array. If the MSBs are corrected after the FEC phase, compared to the conventional switching scheme, then the P_{LSB} term in (21) will be identical to the P_{LSB} term in (20).

The MSB array power consumption, P_{MSB}, can be determined by considering a conventional k bit CBW array whose $k-2$ MSBs have a power consumption of $P_{V_{ref}CBW}(k-2)$ instead of $2^2 \times P_{V_{ref}CBW}(k-2)$:

$$\begin{aligned} P_{MSB} &= P_{V_{ref}CBW}(k) - 2^2 \times P_{V_{ref}CBW}(k-2) + P_{V_{ref}CBW}(k-2) \\ &= P_{V_{ref}CBW}(k) - 3 \times P_{V_{ref}CBW}(k-2) \end{aligned} \tag{22}$$

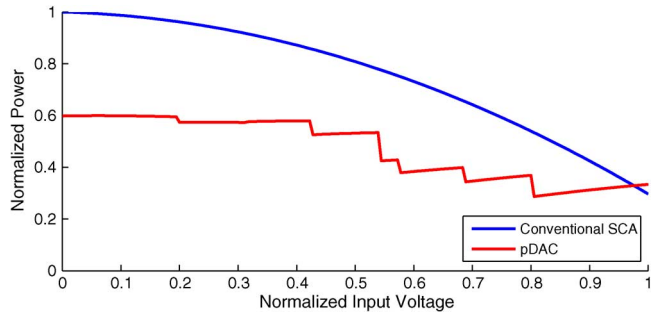


Fig. 9. DAC power consumption comparison between conventional Split Capacitor Array (SCA) switching and pDAC switching.

The amount of charge transferred from the V_{ref} supply during the pDAC phase is:

$$Q_i = C_{i0} V_{ref} + \left(C_{i0} + C_{N-k-1}\overline{L_N} + \sum_{j=i+1}^{N} C_{j0} L_j \right) \times \left(V_{DAC_{i+1}} - V_{DAC_i} \right) \tag{23}$$

The amount of charge transferred from the V_{ref} supply during the FEC phase is:

$$\begin{aligned} Q_i = {} & C_{N0} V_{ref} \overline{L_N} \\ & + \left(C_{N0}\overline{L_N} + \sum_{j=i+1}^{N-1} C_{j0} L_j \right) \left(V_{DAC_{i+1}} - V_{DAC_i} \right) \\ & + \left(\sum_{j=i+1}^{N} C_{j1} L_j \right) \left(V_{ref} - V_{DAC_i} \right) \end{aligned} \tag{24}$$

After substituting (23) and (24) into (18) and combining the result with (19),

$$P_{V_{ref}}(pDAC) = P_{V_{ref}CBW}(k) - 3 \times P_{V_{ref}CBW}(k-2) + F_s V_{ref} Q_{N-k+2} + P_{LSB}(m) \tag{25}$$

The simulated values of (25) compared to (20) for a 8 bit split capacitor array with a 5 bit MSB array ($N = 8$ and $k = 5$) is plotted in Fig. 9. On average, the power consumption of the pDAC scheme is 37% lower than the conventional split capacitor array, and the peak power consumption is reduced by 40%. Further savings can be made in a design with a larger MSB array where the $k-2$ MSBs represent a larger portion of the total power consumption. For example, if $N = 12$ and $k = 9$, the average and peak power consumptions will be reduced by 67% and 60% respectively.

E. SAR ADC Control

The main digital control signals are plotted in Fig. 10. The track and hold signal, $SAMP$, should be lowered at the positive clock edge. The pDAC enable, $EN1$, is latched high on the negative clock edge after the track and hold period is expired.

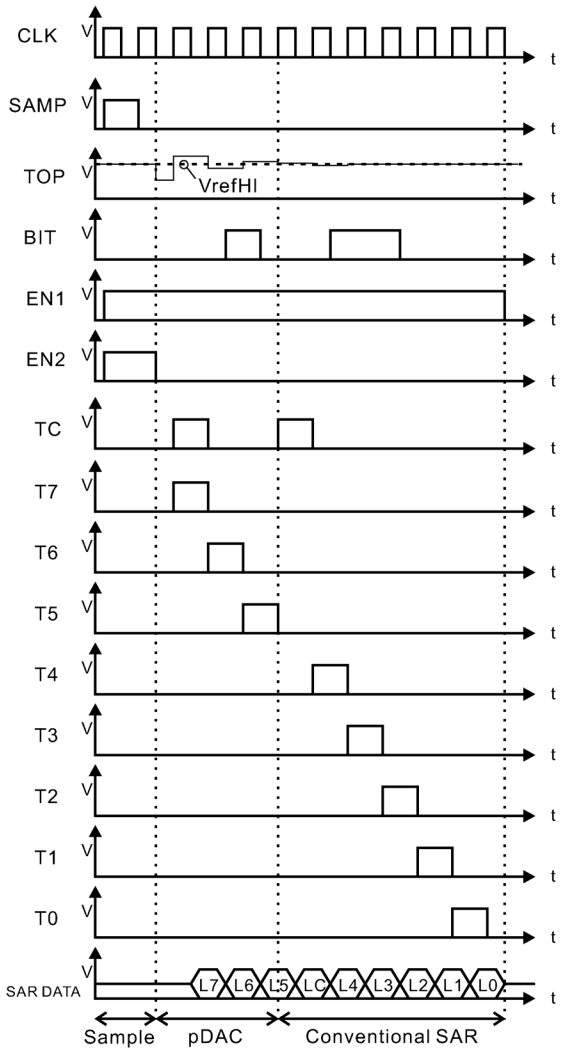


Fig. 10. Timing diagram of the SAR controller.

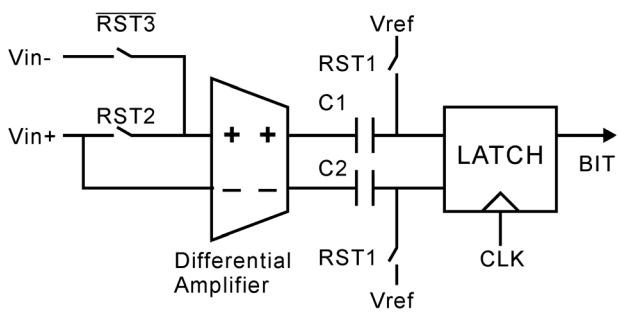


Fig. 11. Schematic of the SAR comparator.

The rest of the capacitor array is left floating at this point. The bit trial signals (T_8 down to T_1) are asserted for one clock period at each subsequent rising clock edge. Error correction trial, T_C, is set on the fourth clock cycle, before T_5 and after T_6. The SAR registers (L_8 down to L_1 and L_C) are enabled during the negative phase of CLK on the corresponding $T_{8:1}$ and T_C trial clock cycles. The comparator decision (BIT) is made on the falling clock edge. The DAC output, V_{DAC}, converges closer to V_{ref} after each comparator decision. The 8-bit quantized result, $L_{8:1}$, plus an error correction bit, L_C, are obtained after 9 clock cycles.

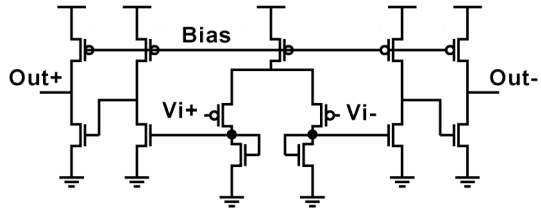


Fig. 12. Schematic of the differential amplifier used in the SAR comparator.

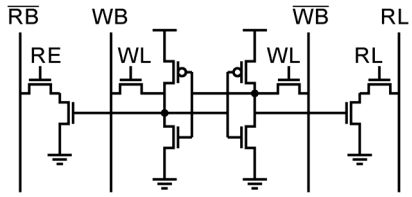


Fig. 13. Schematic of the 10T SRAM.

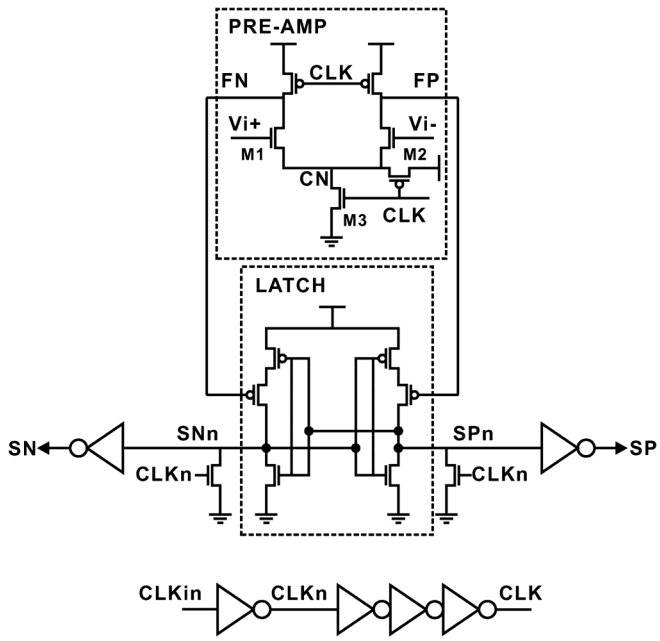


Fig. 14. Schematic of sense amplifier.

III. Circuit Implementation

A. Comparator

The SAR ADC's comparator circuit (Fig. 11) uses a three-stage differential amplifier (Fig. 12) as it pre-amplifier to provide approximately 30 dB gain before a bit decision is made by the dynamic latch. This helps to reduce the probability of entering metastability and hence minimizes power dissipation in the latch. Charge sharing and charge feed-through are attenuated by the fully differential paths. The offset error of the dynamic latch is attenuated by the gain of the pre-amp, which itself has auto-zeroing. During the auto-zeroing phase, the $RST1$ and $RST2$ switches are closed to sample the output referred offset value onto $C1$ and $C2$. During the amplification phase, only the $\overline{RST3}$ switch is closed to amplify the differential signal $Vin+$ and $Vin-$.

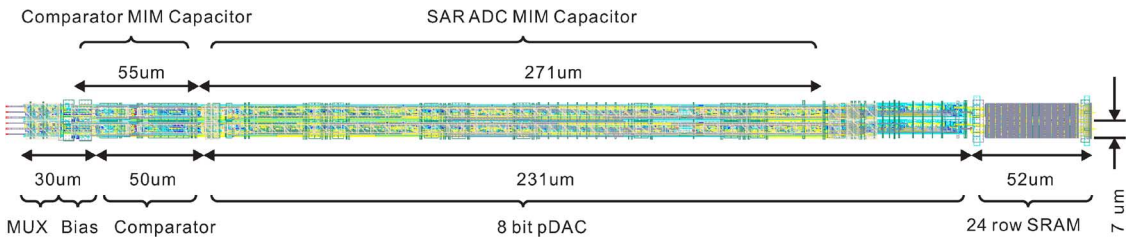


Fig. 15. Compact column circuit layout of the proposed SAR ADC. Two side-by-side columns are shown.

Since this pre-amplifier only provides modest gain without stringent requirement on the precision of its gain, a feed-forward topology is used to avoid any stability issues. The supply range is large enough to ensure that the amplifier's output does not saturate during auto-zeroing. The auto-zeroing capacitors are sized large enough to provide sufficient matching to minimize any kickback noise. The dynamic latch's thermal noise is attenuated by the pre-amp when referred to the input node, so the auto-zeroing capacitors do not need to be overly sized.

B. SRAM Readout

The 10 T SRAM in Fig. 13 was chosen as the data storage circuit because it offers a balanced trade-off between size and robustness. The SRAM cell measures $1.68\ \mu\text{m} \times 7.13\ \mu\text{m}$. Since the read ($RB$ and $\overline{RB}$) and write (WB and $\overline{WB}$) paths are now separated, the 4 feedback transistors can be sized minimally while the 4 readout transistors are sized with the largest possible width. This minimizes the write power consumption and the read delay. The differential readout permits a simpler sense amplifier design. The sense amplifier used here (Fig. 14) is similar to the one reported in [20]. Care is taken in the SRAM array layout to ensure that inter-bit-line-pair cross-talk is minimized via ground shielding. Differential mode errors coupled from neighbouring bit-line-pairs will reduce the error margin during readout.

C. Layout and Floor-Planning Considerations

Circuit area is always one of the top concerns for column parallel ADCs in CMOS image sensors. The column circuit in Fig. 15 measures only $7\ \mu\text{m} \times 463\ \mu\text{m}$. Two side-by-side columns are shown together for completeness because the SRAM array is mirrored along the column direction between neighbouring columns to save area by sharing power buses. Device layout constraints are considered during the schematic design phase. One of the toughest challenge in designing the column circuit is that it must make efficient use of its footprint while matching the pixel pitch. This often necessitates a long and narrow layout style such as the one shown in Fig. 15. In general, it is desirable to minimize the number of horizontal signals and spread the vertical control bus as widely as possible. The $7\ \mu\text{m}$ pitch is chosen for versatility in supporting different layout styles. Two different pixel pitches are used for the two prototypes in Fig. 16. For the ping-pong layout (Fig. 16(a)), $3.5\ \mu\text{m}$ pixel pitch allows one column of ADC to fit into every two pixels. In the second prototype (Fig. 16(b)), one ADC is shared between three pixels pitched at $2.34\ \mu\text{m}$.

The layout of the SAR ADCs are typically dominated by a large DAC capacitor array, but because the bottom-plates of these capacitors are driven by active signals, they are not very sensitive to bottom-plate parasitics. This property can be taken advantage of by overlapping the MIM capacitors on top of the SAR ADC's active circuit in order to minimize its overhead. The length of the layout in Fig. 15 is constrained by active devices as opposed to the capacitor array.

The auto-zeroing capacitors, C_1 and C_2, used in the comparator have their bottom-plates connected to the outputs of the pre-amplifier. The parasitic capacitance at this node will not affect the open-loop gain of the pre-amplifier. Their top plates, which have less parasitics, are connected to the latch's input, where any additional input capacitance will lower the available gain.

The height of the SRAM cells are limited by the horizontal read-out bit line pairs and their ground shielding. The 4 read-out NMOS transistors in the SRAM cell are sized as large as possible under the width restriction imposed by the column pitch. Since the SRAM circuit only occupies up to the fourth metal layer, it can be overlapped by the chip supply ring as seen in Fig. 16(b).

IV. Measurement Results

Two prototype chips have been fabricated using TSMC 1P6M 0.18 μm mixed-signal technology. Both prototypes have the same column parallel 8b pDAC SAR ADCs. The first prototype (Fig. 16(a)) is fabricated in a dedicated CMOS Image Sensor process with special pixel transistor masks and colour filter array. It has a resolution of 1600×500 and one ADC column is dedicated to each pixel column. The pixel pitch is $3.5\ \mu\text{m}$. A pre-amplifier is included in each column for testing purposes and analog CDS. The readout circuit is built using a flip-flop chain. The second prototype (Fig. 16(b)) is fabricated in a similar mixed-signal process but without the special pixel transistor masks. The main difference in the second prototype is the removal of the VGA pre-amplifier, smaller pixel layout, and compact SRAM is used in the readout circuit instead of the flip-flop chain. Its resolution is 1600×500, and each ADC column is shared between 3 pixel columns. The pixel pitch is reduced to $2.34\ \mu\text{m}$. Unfortunately, the new pixel in the second prototype suffers significant degradation in optical performance due to the lack of special pixel devices. Its results are not very meaningful; however, it serves the purpose of illustrating the application of the pDAC column parallel SAR ADC in a cost-effective implementation of image sensor where additional silicon area for the pre-amplifier and large flip-flop chains is not desirable. Since the ADCs are identical between the two prototypes, only measurement results from the first prototype will be provided. This is summarized in Table I and the characterization of a single SAR ADC with pDAC is summarized in Table II. A raw colour image captured using the test set-up in Fig. 17 is shown in Fig. 18.

A. FPN and Temporal Noise

The SAR ADC measurements are characterized by sweeping the input of the ADC with a signal generator and comparing

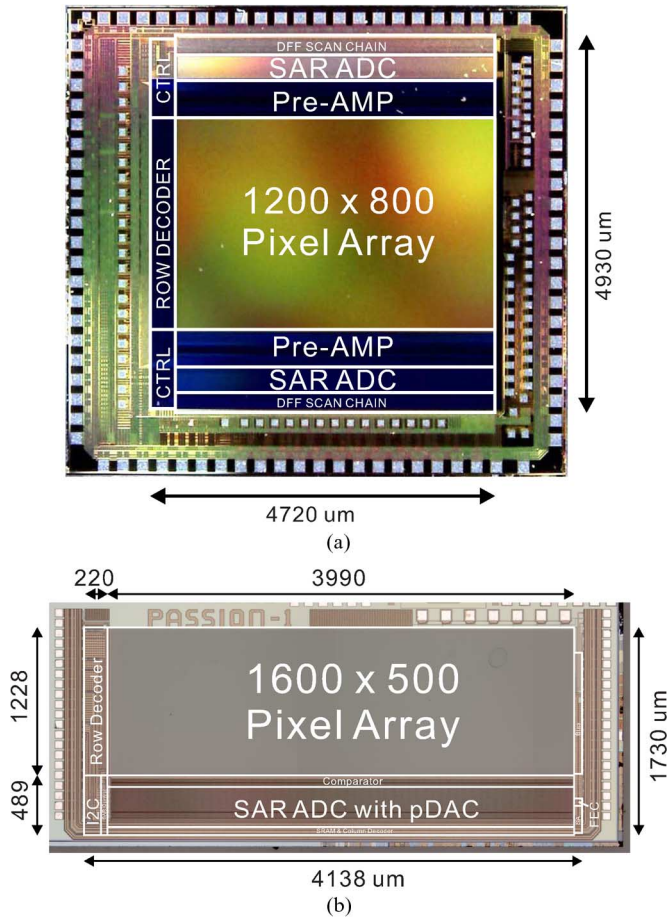


Fig. 16. (a) First prototype. (b) Second prototype.

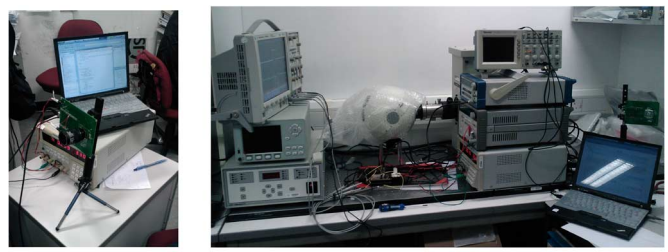
TABLE I
PERFORMANCE SUMMARY OF IMAGE SENSOR IN FIG. 16(a)

Process	0.18 μm 1P6M Mixed-signal CMOS
Supply voltage	3.3 V, 1.8 V, 1.8V (V_{ref})
Clock frequency	40 MHz
Pixel resolution	1200 $\times$ 800
Frame rate	35 fps
Pixel size	3.5 μm $\times$ 3.5 μm
Fill factor	20 %
Pixel Defect	<0.1 %
Column noise	1.5 mV_{rms}
Dark current	<100e^-/sec
Sensitivity	9722 e^-/Lux.sec @ 1148 Lux
Dynamic range	50 dB
Column resolution	11b
Power consumption	40 mW

the SAR ADC's output to the data captured from an Agilent MSO7034A oscilloscope's internal 12 bit ADC. The DNL and INL measurements are given in Fig. 19(a) and Fig. 19(b), respectively. The pDAC switching scheme yielded comparable results to the conventional case scheme with the exception of the DNL error peaks in the high code range. These error peaks coincide with the 3 MSB code transition points. They show that the error correction algorithm is working, but the correction range is not big enough to completely offset the maximum

TABLE II
PERFORMANCE SUMMARY OF A SINGLE PDAC SAR ADC

Metric	pDAC	Conventional
Process	0.18 μm 1P6M Mixed-signal CMOS	
Supply voltage	3.3 V, 1.8 V, 1.8V (V_{ref})	
Clock frequency	10.8 MHz	10 MHz
Speed	0.83 MSa/s	
Chip area	348 μm $\times$ 7 μm	
Noise	$<$ 1 LSB$_{rms}$	$<$ 1 LSB$_{rms}$
Peak DNL_{8b}	+1.65/-1.45 LSB	+0.59/-1.10 LSB
Peak INL_{8b}	+0.63/-1.34 LSB	+1.30/-0.82 LSB
DAC Power	6.5 μW	10.1 μW
Total Power	209 μW	229 μW
FoM_{DAC}	39.8 fJ/step	61.3 fJ/step
FoM_{ADC}	1.41 pJ/step	1.40 pJ/step



(a) (b)

Fig. 17. (a) Test set-up for image capture. (b) Integrating sphere for chip characterization.

Fig. 18. Captured raw image.

errors made in the MSB pilot capacitor array for the $L_8 = 1$ half of the DAC output. This error is largely caused by the mismatch of parasitic capacitance, C_{par}, between the simulation model and the fabricated chip due to the floating bottom-plates during the pDAC phase. Improvements can be made by connecting segments of the metal layer underneath the MIM capacitor bottom-plate to the pDAC section of the DAC (C_{i0}). If the size of these shielding metal segments are weighted according to the pDAC bit it is connected to, the resulting artificial parasitic capacitor will simply scale the pDAC weights and the effect of C_{par} from (11) will be minimized.

During the signal generator sweep, a range of input voltages will give the same digital output. This means that for each ADC

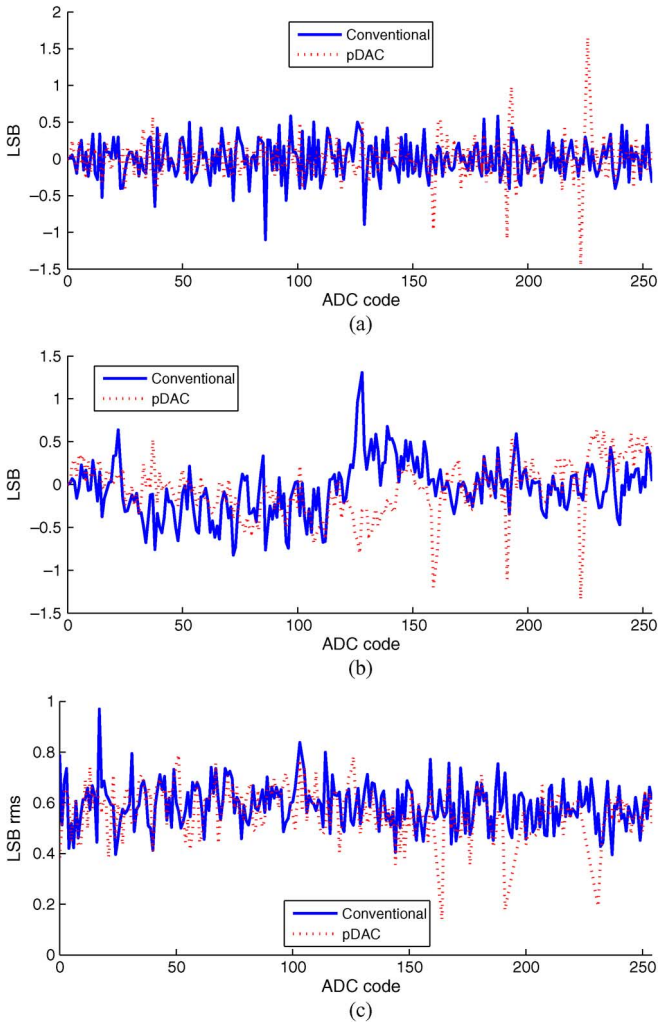


Fig. 19. (a) DNL, (b) INL, (c) and noise (normalized to the LSB) of the 8b SAR DAC.

code, there is a spread of possible input voltages, and by measuring this spread, the ADC's input referred noise power, including the quantization noise can be estimated. This is possible because the oscilloscope's internal 12 bit ADC has a much lower noise floor than the SAR ADC under test. The standard deviation of this spread, normalized to the LSB, is plotted in Fig. 19(c). From this figure, it can be deduced that the SAR ADC is Fixed-Pattern Noise (FPN) dominated because the temporal and quantization noise is bounded by a smaller envelop then the DNL and INL. The pDAC switching scheme also showed no significant disadvantage in terms of noise when compared to the conventional switching scheme. This is because the total DAC capacitance after the FEC phase is the same between the two schemes.

B. Power Consumption

The power consumption of the SAR DAC is measured across the full range of input voltages in Fig. 20. The pDAC switching scheme can nearly halve the DAC power consumption when compared to the conventional method. Given that pDAC does not suffer from significant loss in FPN and noise performance and its implementation overhead is also small, it is clear that low-power SAR applications will benefit from the proposed

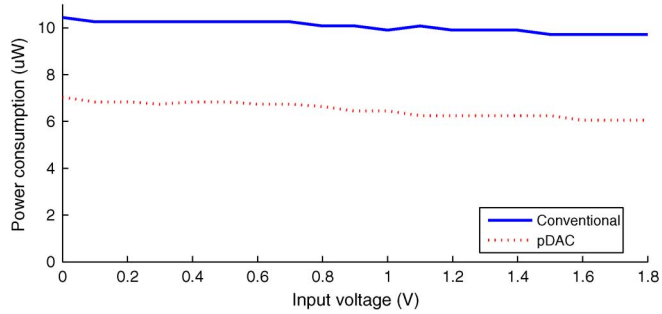


Fig. 20. Power consumption of the 8b SAR DAC under conventional and pDAC switching at 0.83 MSa/s.

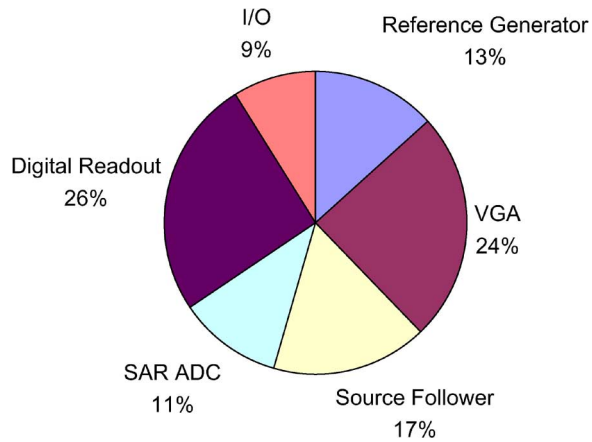


Fig. 21. Power consumption distribution of the image sensor in Fig. 16(a).

pDAC scheme, especially for array based implementations such as CMOS image sensors. The power consumption distribution across different circuit blocks is plotted in Fig. 21. The flip-flop chain makes up a large part of the digital readout power consumption. Replacing it with a SRAM readout circuit can help to optimize this block. The variable-gain amplifier (VGA) increases the sensing dynamic range, but it can be omitted for ultra low-power applications.

In Table II, Figure-of-Merit (FoM) is calculated for both the stand-alone DAC and also the whole column-level SAR ADC using the following expression:

$$FoM = \frac{P}{F_s \times \frac{2^N}{noise}} \tag{26}$$

Here, P is the circuit power consumption, F_s is the sampling frequency, N is the ADC resolution, and $noise$ is the maximum input referred noise from Fig. 19(c). This is the FoM generally accepted for image sensors since the output from the pixel array can be considered to be a DC signal. It differs from the ADC FoM based on the $ENOB$ where the input is assumed to be a full-range sinusoid. It can be seen that although the pDAC scheme yielded a much better FoM for the DAC when compared to the conventional scheme, it is penalized for its slightly slower sampling frequency due to the additional FEC phase. In the total ADC FoM, the power savings made in the DAC is overshadowed by the conservative comparator design. The ADC FoM will be more reasonable if a more energy efficient comparator such as the one proposed in [21] is used to bring the comparator power consumption into the same range as the DAC.

V. Conclusion

A CMOS image sensor with compact column-parallel SAR ADCs is presented. The 8b SAR ADC only occupies a $348\ \mu\text{m} \times 7\ \mu\text{m}$ footprint. The measurement results indicate that the ADC is still FPN limited. The DAC power consumption in the SAR ADC is nearly halved by a novel pDAC switching scheme. When combined with the proposed mixed-signal FEC, the pDAC scheme showed no significant disadvantage compared to the conventional design both in terms of noise and FPN. It is therefore a useful technique for improving power consumption and speed in SAR ADCs.

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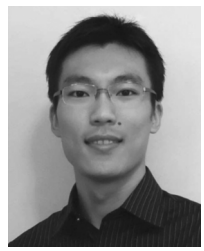

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In 1998, he joined Edith Cowan University, Perth, Australia, first as a research fellow working on smart vision sensors, then as a lecturer and a senior lecturer in the school of Engineering and Mathematics. He is currently an Associate Professor with the Electronic and Computer Engineering Department of Hong Kong University of Science and Technology (HKUST) where he is also serving as the director of Computer Engineering and the director of the M.Sc. degree in integrated circuit design (ICDE). His research interests are related to VLSI circuits and systems for signal, image processing, sensors and microsystems applications.

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