Modelling of Capacitor Mismatch and Non-Linearity Effects in Charge Redistribution SAR ADCs

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Abstract—**For embedded high resolution successive approximation ADCs, it is necessary to determine the performance limitation of the CMOS process used for the design. This paper presents a modelling technique for major limitations, i.e. capacitor mismatch and non-linearity effects. The model is based on Monte Carlo simulations applied to an analytical description of the ADC. Additional effects like charge injection and parasitic capacitance are included. The analytical basis covers different architectures with a fully binary weighted or series-split capacitor array. When comparing our analysis and measurement results to several conventional approaches, a significantly more realistic estimation of the attainable resolution is achieved. The presented results provide guidance in choosing process and circuit structure for the design of SAR ADCs. The model also enables reliable capacitor sizing early in the design process, i.e. well before actual layout implementation.**

Index Terms—**Analog-to-digital-converter ADC; charge redistribution CR; capacitor matching; modeling and simulation; CMOS process; Successive approximation register**

I. Introduction

Successive Approximation Register (SAR) ADCs offer high resolution of 12 to 16 bit at medium conversion rates up to 5 MSample/s [1]. The Charge-Redistribution (CR) technique is widely used in numerous industrially fabricated ADCs and in modern system-on-chip solutions because the integration of capacitors requires no special technology options. Implementation of capacitors with two metal or poly-silicon layers is possible in all standard CMOS processes. The required area for the capacitor array decreases by scaling of the technology since the area capacitance is increasing. Besides the comparator, no extensive analog circuitry is required. The area occupied by the large number of switches and the control logic also scales well with technology.

It is well known that the achievable resolution of charge-redistribution SAR ADC is mainly limited by the matching of the used capacitors [2][3]. The device matching depends on process parameters of the technology and on type and size of the capacitors. Enlarging the capacitor area decreases the mismatch, but increases the overall capacitance of the array along with the sampling capacitance of the ADC. Therefore matching and size of the unit capacitor strongly influence speed and power consumption of the ADC. Dimensioning a CR ADC is always a trade-off between area and resolution. Accurate estimation of the attainable resolution depending on mismatch and capacitor non-linearity is crucial for an optimal sizing. Compared to flash-ADCs, there is no well established method for analyzing the mismatch and dimensioning the capacitor size. Instead straightforward approaches or empirical data are often used. For an ADC with a resolution of 12 or more bit an accurate estimation is necessary, because an over-constraining is impossible without degrading the entire performance. An uncertain matching estimation of factor 2 leads to a 4 times larger area of the capacitor array or to a 1 bit lower resolution. SAR ADCs with more than 12 bit resolution usually require additional calibration [4][5].

An accurate model is necessary to determine the required range of the calibration circuit, predicting not only a maximum error, but also delivering statistical parameters of the INL of the complete transfer characteristic to enable yield estimation. To determine the resolution of an SAR converter a transient simulation of the entire transfer characteristic is required. At transistor level, even one single complete simulation of a 12 bit converter is often not applicable, let alone a Monte-Carlo simulation with hundreds or thousands of runs. However, several hundred samples are required to estimate the yield of the circuit with a high confidence level. In [6] the mathematical relation between yield, confidence level and sample size is presented. Tab. 1 shows the sample size of several confidence levels. Although importance sampling [7] reduces the required number of simulations, but still a high number of Monte-Carlo runs is required for a feasible accuracy and confidence level. This is unachievable for an SAR ADC in terms of circuit simulation. To run a Monte-Carlo simulation in the common design flow, a complete circuit with an initial sizing is necessary which in turn is only available after choosing technology and architecture. The conventional worst-case analysis leads to an exaggerated robustness due to the missing consideration of the distribution and actual correlations [6].

TABLE I. Required sample size for several confidence levels

Yield	Confidence level		
	90%	*95%*	*99%*
85% ± 10%	35	49	85
85% ± 5%	139	196	339
85% ± 1%	3451	4899	8461

We propose an approach that combines an analytical model and Monte-Carlo analysis. The model allows analysis of the entire transfer characteristic. Besides device mismatch, further effects like charge injection and capacitor non-linearity are included. In contrast to [8] our approach shows the matching result at all points of the ADC characteristic and not only at the MSB transition point. The model was used for the designs of two ADCs with 12 bit resolution and for sizing a 14 bit self-calibrating SAR ADC.

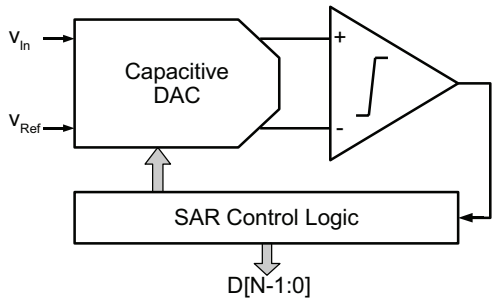

Figure 1. Block level diagram of a CR SAR ADC.

II. Model of SAR ADC

A. Fundamental Approach

A common charge redistribution SAR ADC as shown in Fig. 1 consists of a capacitor array, a comparator, several switches, and a digital control unit. The input voltage is directly sampled with the entire or part of the capacitor array, requiring no additional sample and hold stage. For ADCs with more than 10 bit resolution, fully differential circuits are nearly exclusively used. However, there are many different architectures for the configuration of the switches and capacitors. Common structures are based on a binary weighed capacitor array and operate in 3 phases. The circuit example in Fig. 2 is used as template for the following analysis.

First the analog input signal is sampled via S_{In} and held on the top plate of the capacitor array while all the bottom plates are connected to ground. In the conversion phase the switches S_N to S_1 connect one after the other the bottom plates of the capacitors C_N to C_1 to the reference voltage V_{Ref}. After changing a switch position, the comparator compares the voltage at the top plate with V_{Ref}. If V_{TP} is higher than V_{Ref}, the switch is set back to his initial state otherwise it stays in his position. The position of the switches after all N cycles represents the conversion result.

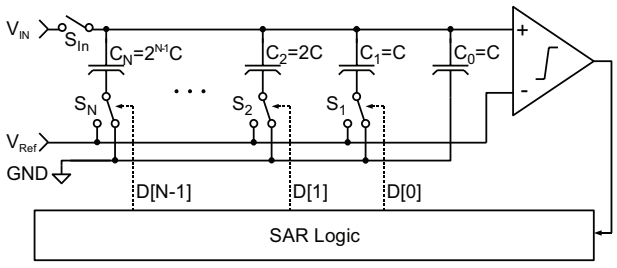

Figure 2. A conventional fully binary weighted CR SAR ADC.

The charge Q stored in the capacitor array is defined by the input voltage V_{In} and the sum of all capacitors of the array.

$$Q = V_{In} \cdot \sum_{i=0}^{N} C_i \tag{1}$$

Considering only the settled state of the network at the end of the clock cycle, calculation of all voltages based on a charge balance is possible without solving differential equations. The reduction to the settled state is feasible, because settling of the voltages during one clock cycle is crucial for an accurate operation. The top plate of the array is only connected to the high impedance input of the comparator and thus isolated during conversion. The charge Q stored during acquisition remains consequently unchanged. All bottom plates are connected to known voltages. Depending on the position of the switches and on the voltage V_{TP} at the top plate, the charge is given by

$$Q = V_{TP} \cdot \sum_{\text{to GND}} C_j + (V_{TP} - V_{Ref}) \cdot \sum_{\text{to Ref}} C_i \tag{2}$$

where the sum $\sum_{\text{to GND}} C_j$ contains all capacitors with there bottom plate connected to ground and the sum $\sum_{\text{to Ref}} C_i$ contains all capacitors which are connected to the reference voltage V_{Ref}. After equalizing and transforming Eq. 1 and Eq. 2, the voltage V_{TP} can be calculated from solely know parameters.

$$V_{TP} = V_{In} + V_{Ref} \frac{\sum_{\text{to Ref}} C_i}{\sum_{\text{to Ref}} C_i + \sum_{\text{to GND}} C_j} \tag{3}$$

The sums in the denominator together include all capacitors of the array and can be combined to

$$\sum_{i=0}^{N} C_i = \sum_{\text{to Ref}} C_i + \sum_{\text{to GND}} C_j \ . \tag{4}$$

The position of each switch is assigned to the digital control word D[N-1:0]. If the capacitor C_i is connected to ground then D[i]=0 and in inverse D[i]=1 when a capacitor is connected to V_{Ref}. With this notation Eq. 3 is transformed to

$$V_{TP} = V_{In} + V_{Ref} \frac{\sum_{i=0}^{N-1} D[i] \cdot C_{i+1} + C_0}{\sum_{j=0}^{N} C_j} \ . \tag{5}$$

Solving this equation explicitly leads to the comparator input voltage. It enables simulation of the successive approximation, where for each input voltage the digital result can be calculated within N iterations.

The stated equations are also applicable for more sophisticated architectures in a similar way. For calculating a fully differential architecture two separate equation for the positive and for the negative part of the network are required. Series-split capacitor arrays [9][10] with an attenuation capacitor consist of more than one high impedance node. This results in a linear equation system of multiple variables, which nevertheless has an explicit solution. Circuit topologies combining a resistor string DAC for the lower bits and a capacitive DAC for the higher bits are covered with this approach too.

B. Capacitor Mismatch

Assuming random capacitance values with normal distribution and a standard deviation proportional to the square root of the occupied area, the matching of capacitors is given by

$$\sigma\left(\frac{\Delta C}{C}\right)=\frac{A_C}{\sqrt{WL}} \ . \tag{6}$$

where the factor A_C depends on technology and capacitor type. The term $\sigma\left(\frac{\Delta C}{C}\right)$ is the standard deviation of the difference ΔC of identically designed capacitors, normalized to their absolute value C. The parameter W and L define the geometric size of the capacitor. The standard deviation $\sigma(C)$ of a single capacitor is by factor $\sqrt{2}$ smaller than the standard deviation of the difference of two capacitors and is given by

$$\sigma(C)=\frac{C\cdot A_C}{\sqrt{2\cdot WL}}=c_A WL\cdot\frac{A_C}{\sqrt{2\cdot WL}}=c_A A_C\sqrt{\frac{WL}{2}} \ . \tag{7}$$

The factor c_A is a technology specific value for the area capacitance.

Based on the matching of the capacitors and using Eq. 3 it is possible to obtain an analytical solution for the attainable resolution N of the ADC. We claim that in every switch position, V_{TP} never differs more than a half LSB from the ideal value without mismatch. This leads to the definition

$$\Delta(V_{TP})<\frac{1}{2}\mathrm{LSB}=\frac{V_{Ref}}{2^{(N+1)}} \ . \tag{8}$$

Mathematical analysis [12] and measurement results show, that the error voltage reaches a maximum at the half point of the entire digital output range, equal to the MSB transition point.

A worst case analysis is used in [11] to deduce a relation between the error range $\Delta(C)$ of a unit capacitor and the attainable resolution N of a SAR ADC. Where $\Delta(C)$ is a specific value of the maximum matching tolerance of any two capacitors in the array. Fig. 3 shows the comparison of this theoretical curve and some measurement results. A considerable discrepancy at high resolutions are obvious. Existing measurement results with a resolution higher than the predicted limit prove that the assumptions made in [11] and [8] lead to a very pessimistic estimation.

According to the sum of n independent random variables, the standard deviation of the parallel connection of n unit capacitors is defined by

$$\sigma\left(\sum_{i=1}^{n} C_i\right)=\sqrt{n}\cdot\sigma(C_0) \ . \tag{9}$$

In contrary the worst case analysis assumes a linear summation of the variations.

$$\Delta\left(\sum_{i=1}^{n} C_i\right)=n\cdot\Delta(C) \tag{10}$$

This leads to much higher variation, but with a very low occurrence probability.

A realistic conclusion is only possible considering the distribution of the random variables and their correlation. An analytic calculation of the random variable X_{V_TP} based on Eq. 3 and the distribution of the capacitor mismatch leads to the following equation

$$X_{V_{TP}}=V_{In}+V_{Ref}\frac{X_1}{X_1+X_2} \tag{11}$$

where X_1 and X_2 are normal distributed random variables. Their parameters depend on the switch position D[N-1:0]. At the critical point D[N-1:0]=2^{N-1}, X_1 and X_2 have equal parameter, because half of the capacitors are connected to ground and the other half is connected to the reference voltage. The expectation values equates to the sum of half of the capacitors

$$E(X_1)=E(X_2)=2^{(N-1)}\cdot C_0 \tag{12}$$

and according to Eq. 9 the standard deviations are given by

$$\sigma(X_1)=\sigma(X_2)=\sqrt{(2^{(N-1)})}\cdot\sigma(C_0) \ . \tag{13}$$

Due to the nonlinear relation, the variable X_{V_TP} is not corresponding to a normal distribution and no analytical solution of the quotient $\frac{X_1}{X_1+X_2}$ is available. Calculating the distribution of a quotient of two uncorrelated normal distributions leads to an equation comparable to the Gaussian integral. With the help of a numerical solution it is possible to calculate the standard deviation $\sigma(V_{TP})$ of X_{V_TP} in relation to $\sigma(C_0)$ and the resolution N. The condition

$$\Delta(V_{TP})<3\sigma(V_{TP}) \ , \tag{14}$$

the numerically calculated solution of Eq. 11, and Eq. 8 lead to a relation of the attainable resolution and $\sigma(C_0)$. Comparison of both curves in Fig. 3 shows that the distribution based approach leads to a more realistic estimation than the worst case analysis in [11].

Both approaches are only valid for conventional ADCs with a fully binary-weighted capacitor array. Architectures with a series-split capacitor array (see Fig. 7) and a reduced total number of capacitors do not correspond to these approaches. Their resolution depends on the partitioning of the array, see Tab. 2.

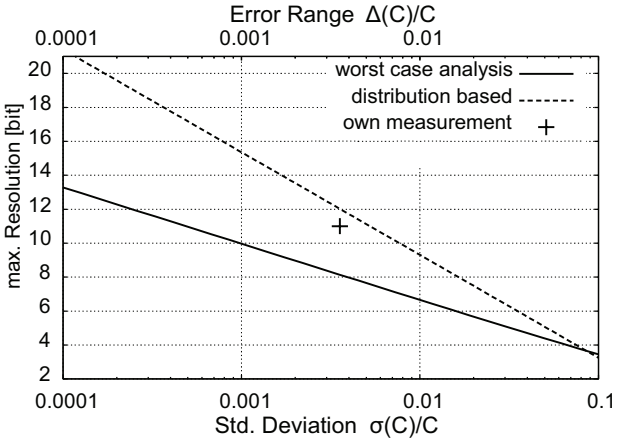

Figure 3. Maximum attainable resolution of a CR SAR ADC depending on the matching of an unity capacitor. Calculation with worst case method from [11], distribution based calculation and measurement results.

III. System Model Implementation

A. Combined Model and Testbench Structure

To calculate the error of all points of the ADC characteristic, we propose a Monte-Carlo analysis based on an analytical model of the circuit. No circuit simulator is required, instead an implementation of the model and the testbench with MATLAB or any other programming language is sufficient. Compared to a transient circuit simulation, the explicit calculation of the required voltages and the execution of the successive approximation requires only little computation time. This allows a thousand complete calculations of the whole ADC characteristic within only a few minutes. Fig. 4. shows the summarized sequence of the program.

To calculate the INL more accurately than 1 LSB it is not sufficient just to determine the digital output code of equidistant input voltages, but to rather calculate the precise transition point of each digital output code. This is implemented by iterating the input voltage at each transition point by applying the bisection method. This algorithm is demonstrated in Fig. 5. The initial voltage step is chosen slightly smaller than the expected size of an LSB. Thus, within only 6 iteration an accuracy of ⅛ LSB is achieved.

The model requires only a few technology specific inputs, such as size, standard deviation and voltage coefficients of the unit capacitor are part of the standard input. The architecture is given by the analytical description of the network. Descriptions of basic array structures are prepared and allow an easy construction of more complex architectures.

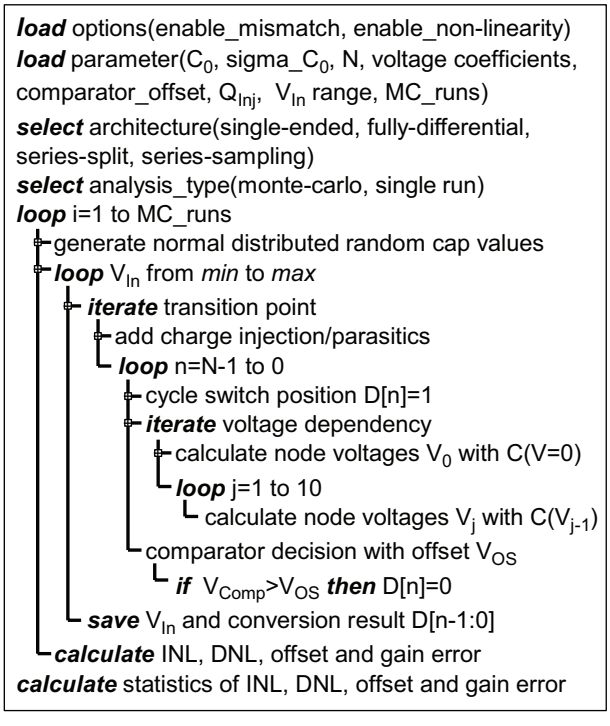

Figure 4. Program sequence of the model.

B. Capacitor Non-Linearity

Beside capacitor mismatch another major limitation of performance is the capacitor non-linearity. The capacitor non-linearity is usually modelled by the voltage dependency

$$C(V) = C_0 \cdot (c_2 \cdot (V - V_{nom})^2 + c_1 \cdot (V - V_{nom}) + 1) \quad . \tag{15}$$

where c_1 and c_2 are polynomial modelling coefficients. Typical characteristics are shown in Fig. 6a. The implementation in the presented model is achieved by iterative calculation. First the non-linearity is neglected while calculating the first iteration of the voltage V_{TP}. This provides an approximations of all node voltages and allows the calculation of the voltage dependency after a few iterations. The weak non-linearity guarantees convergence and an accurate result. This approach determines the bend of the ADC characteristic resulting from the capacitor non-linearity. This effect is important for resolutions higher than 12 bit and applies first of all to poly-silicon capacitors [1].

C. Additional Effects - Layout parasitics

Besides capacitor mismatch, the model covers all error sources and parasitic effects, that are to be emulated by the parameters capacitance, charge, and voltage. An additional charge Q_{Inj} in Eq. 1 represents the switching offset of S_{In} during acquisition. The offset voltage V_{OS} of the comparator can easily be considered while comparing V_{TP} and V_{Ref}. Enhancing the equation allows to include parasitic capacitance, e.g. C_{TP} from the top plate to ground. All this modifications lead to

$$V_{TP} = V_{In} + \frac{V_{Ref} \sum_{\text{to Ref}} C_i + Q_{Inj}}{\sum_{i=0}^{N} C_i + C_{TP}} + V_{OS} \quad . \tag{16}$$

The capacitance C_{TP} causes a constant gain error. A fully differential architecture eliminates this effect in case of equally sized parasitics in both parts of the array. The charge injection of S_{In} and the comparator offset voltage V_{OS} result in an offset error of the ADC characteristic. If the charge injection or the comparator offset is voltage dependent, than the resulting offset depends on input voltage or common-mode voltage and causes an INL error.

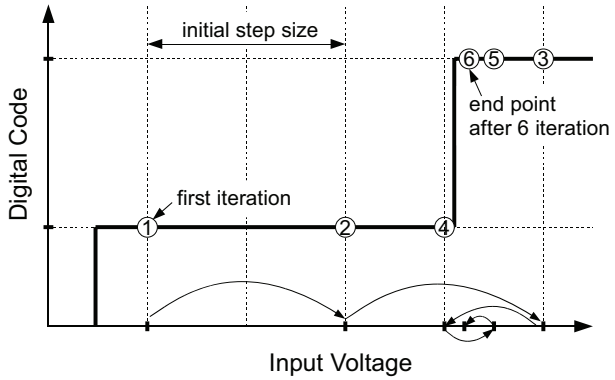

Figure 5. Algorithm for calculating the transition points of the digital output.

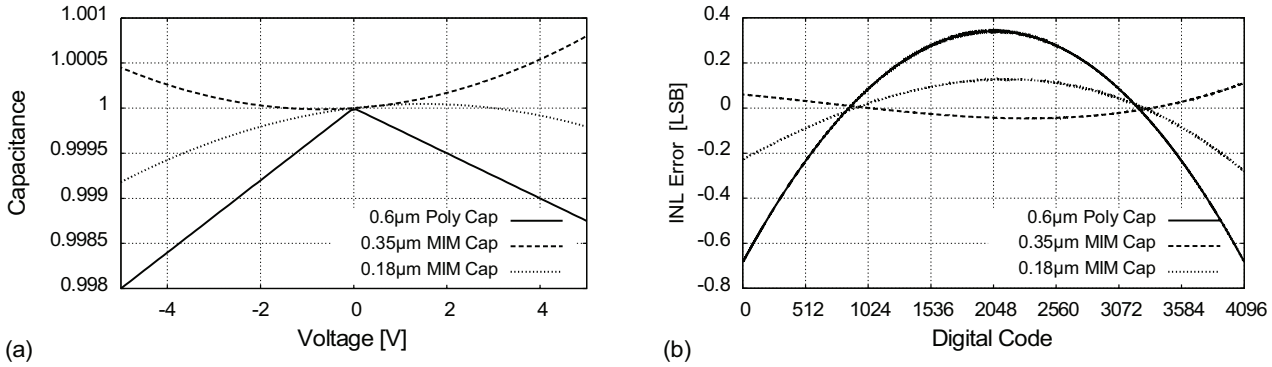

Figure 6. (a) Voltage dependency of capacitors in different technologies and (b) resulting INL error of a 12 bit differential ADC.

IV. Calculation and Measurement Results

Fig. 6a displays the voltage dependency of capacitors of 3 different technologies. The non-linearity is modelled by piecewise linear or quadratic functions. The different sign of the quadratic characteristic depends on the used dielectric material [12]. The resulting INL error of the same differential architecture is shown in Fig. 6b. The voltage dependency of the capacitors leads to a non-linear characteristic of the ADC, but not to DNL errors. The model enables analysis of capacitor non-linearity regarding different architectures. Improving the capacitor linearity is only possible by optimizing the technology parameters. The designer cannot influence the linearity by sizing the capacitors. Only circuit architecture, voltage ranges, and capacitor type provide some control.

Our approach allows comparing matching requirements of different architectures fast and easily. Tab. 2 shows results of different configurations of the fully differential 12 bit ADC with the series-split capacitor array from Fig 7. The standard deviation of the INL at the mid point of the characteristic (equal to the maximum INL error) is calculated with 1000 Monte-Carlo runs for different sizing and position of the series-split capacitor. Shifting the series-split capacitor towards the MSB capacitor at constant unit capacitor size increases the INL error but decreases the sampling capacitance.

TABLE I. Architecture Comparison

	series-split partitioning [MSB:LSB]	unit capacitor [fF]	$\sigma(C_0)$ [fF] / %	total number of capacitors	C_{Sample} [pF]	σ(INL)[a] [LSB]
equally sized	12:0	50	0.25 / 0.5	4096	204.8	0.23
	8:4	50	0.25 / 0.5	272	12.8	0.45
	6:6	50	0.25 / 0.5	128	3.2	0.90
	5:7	50	0.25 / 0.5	160	1.6	1.26
equal C_{Sample}	12:0	1.22	0.04 / 3.2	4096	5.0	0.71
	8:4	20	0.16 / 0.8	272	5.0	0.71
	6.6	78	0.31 / 0.4	128	5.0	0.71
	5:7	156	0.44 / 0.28	160	5.0	0.71

a. Max. standard deviation of the INL error calculated by 1000 MC runs of a 12bit ADC with different partitioning of the capacitor array using equal matching factor A_C=3.5% and c_0=1fF/µm².

Measured characteristics of a 12 bit differential ADC are plotted in Fig. 8. The analysis result is compared to the standard deviation of the INL error of 10 measured devices in Fig. 9. The attained resolution is within the predicted range and the standard deviation accords to the model in terms of characteristic and amplitude.

V. Limitation of the Model

The matching analysis assumes identically implemented devices without systematic variations. Conventional fully binary-weighted capacitor arrays fulfill this constraint because they consist only of unit capacitors. An attenuation/series-split capacitor for array partitioning has not the size or integer multiple of a unit capacitor. A uniform layout structure is usually not possible for series-split arrays, even with additional effort [8][9]. At this point, parasitic capacitance cause a systematic error and mismatch increases due to irregular size and layout structure. In addition to the mismatch of closely placed devices, variations or gradients of the process parameters occur especially at larger distances. To avoid systematic errors caused by gradients or marginal effects, an accurate common-centroid layout enclosed with dummy capacitors is essential. Mismatch caused by non-uniform layout structures is hard to predict, lacking an analytical definition. Although the prediction of these effects is not implemented in the model, but employing a manual inclusion of parasitic capacitance offers the possibility to analyze their effect.

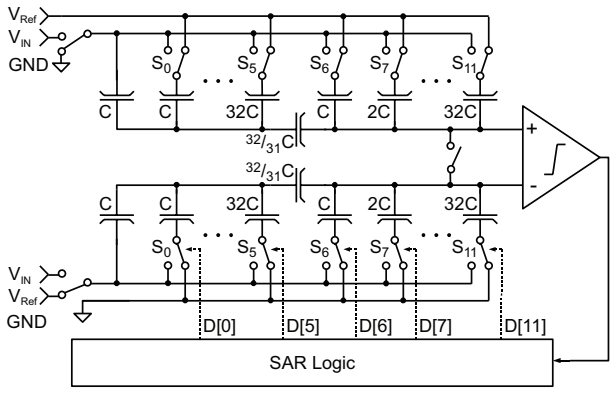

Figure 7. Fully differential ADC with series-split capacitor.

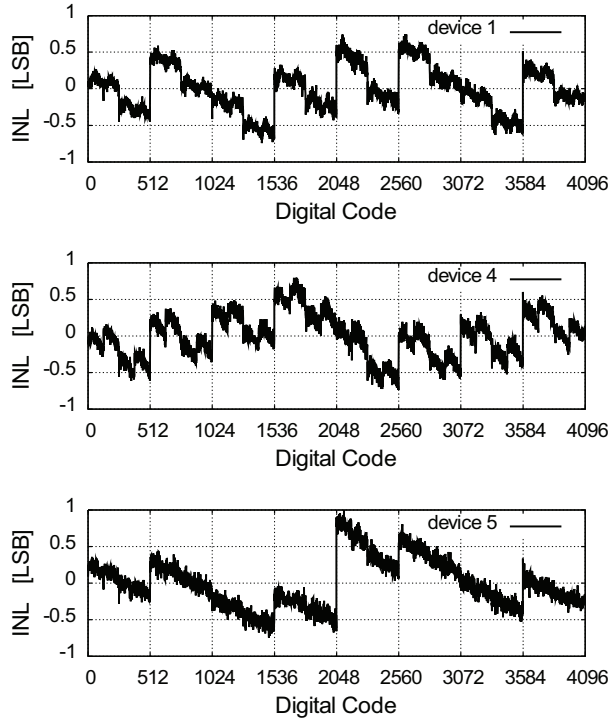

Figure 8. Measured INL Error of 3 typical ADC devices with 12bit resolution.

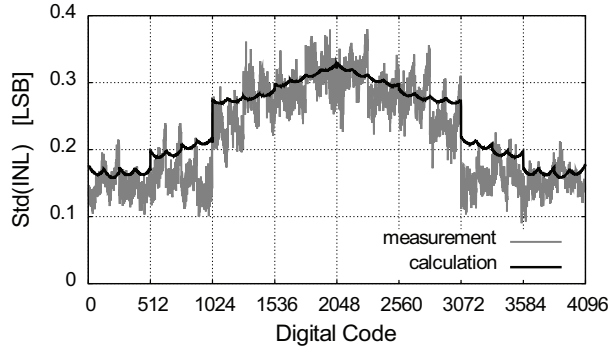

Figure 9. Standard deviation of the INL error extracted from the measured characteristic of 10 devices and the result of the system model after 20 000 Monte-Carlo runs.

VI. Conclusion

A system model for Monte-Carlo analysis based on an analytical solution has been presented. The model includes device mismatch, capacitor non-linearity, and additional effects e.g. charge injection and parasitic capacitance. This approach can be applied to different CR SAR ADC architectures. The analysis results are useful to evaluate the capabilities and limits of a technology, regarding especially capacitor non-linearity. We have shown that worst-case analysis is unsatisfying for high resolution ADC and leads to over-constraint designs. Compared to circuit simulation our method is fast enough to calculate several thousand Monte-Carlo runs and achieve statistic results with high confidence level. This is important for design optimization and offers an accurate prediction for necessary circuit calibration. The measurement results validate the proposed approach.

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