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A 8-bit 500-KS/s Low Power SAR ADC for Bio-Medical Applications

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***Abstract*—This paper presents a successive approximation register analog-to-digital converter (SAR ADC) design for bio-medical applications. An energy-saving switching sequence technique is proposed to achieve low power consumption. The average switching energy of the capacitor array can be reduced by 56% compared to a conventional switching method. The measured signal-to-noise-and-distortion ratios of the ADC is 46.92 dB at 500KS/s sampling rate with an ultra-low power consumption of only 7.75-μW from a 1-V supply voltage. The ADC is fabricated in a 0.18-μm CMOS technology.**

***Index Terms*—Successive approximation register analog-to-digital converter (SAR ADC), low power, bio-medical application.**

I. Introduction

Over the past years, many researches on successive-approximation-register analog-to-digital converters (SAR ADC) have been published [1]-[3] for applications which require low-power dissipation. The SAR ADC architecture is well suitable for large-scale wireless sensor networks and bio-medical applications due to its moderate speed, moderate resolution and very low-power consumption characteristics. The primary sources of power consumption in a SAR ADC are the comparator and charge/discharge of the capacitor array. The energy dissipation required to charge/discharge the capacitor array is dominated by the switching sequence. The conventional switching sequence is an inefficient procedure and much of energy is wasted on charging and discharging the capacitor array.

This paper proposes an energy-saving switching sequence technique to minimize the power consumption of the capacitor array and the details about circuit design are organized as followings: the ADC architecture and energy-saving switching sequence technique is discussed in Section 2 and the building block circuit designs are presented in Section 3. The measurement results are summarized in Section 4. Finally, summary of this design is offer in Section 5.

II. ADC Architectures

Figure 1 shows the SAR ADC architecture which consists of a binary-weighted capacitor array, a comparator, a SAR control unit and switches. Combining with the capacitor splitting technique proposed by [4], the MSB/2 capacitor is split into parallel binary-weighted sub capacitor array to save the energy required during a "down" transition. The operation of the ADC is based on the binary search algorithm which is accomplished by the capacitor array, the SAR control unit, and the comparator.

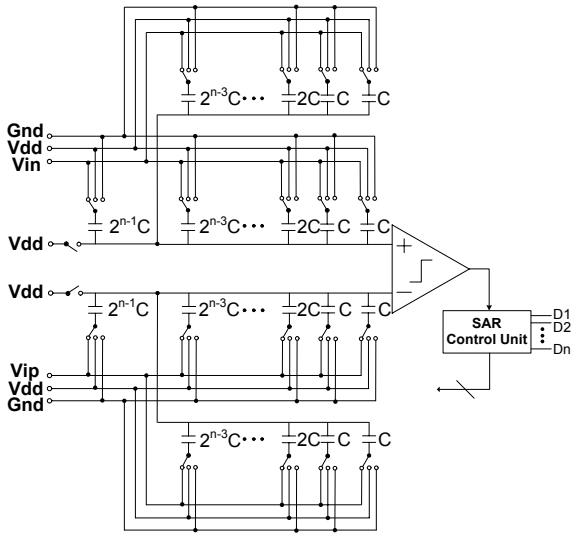

Fig. 1. Successive-approximation-register ADC architecture.

It is instructive to calculate the total energy drawn from V_{ref} when switching the capacitor array. For alleviating the computation, a 3-bit capacitor array is taken as an example. Fig. 2(a) shows all possible paths to convert an analog signal to digital signal in conventional SAR ADC and the energy consumption of each switching phase is calculated. If each path is equiprobable, it can be shown that the first switching phase consumes the most energy in a conversion period. Furthermore, even though the conventional switching sequence can charge the capacitor array efficiently during the down paths of each switching phase in Fig. 2(a), it is highly inefficient in the up paths. The average switching energy for an n-bit SAR ADC to convert an analog signal to digital signal can be derived as:

$$E_{total,n-bit} = \sum_{i=1}^{n} 2^{n+1-2i}(2^i - 1)CV_{ref}^2 \qquad (1)$$

In order to reduce the energy consumption, the proposed energy-saving switching sequence modifies the switching sequence as shown in Fig. 2(b). Compared to the conventional architecture consuming $4CV_{ref}^2$ Joules,

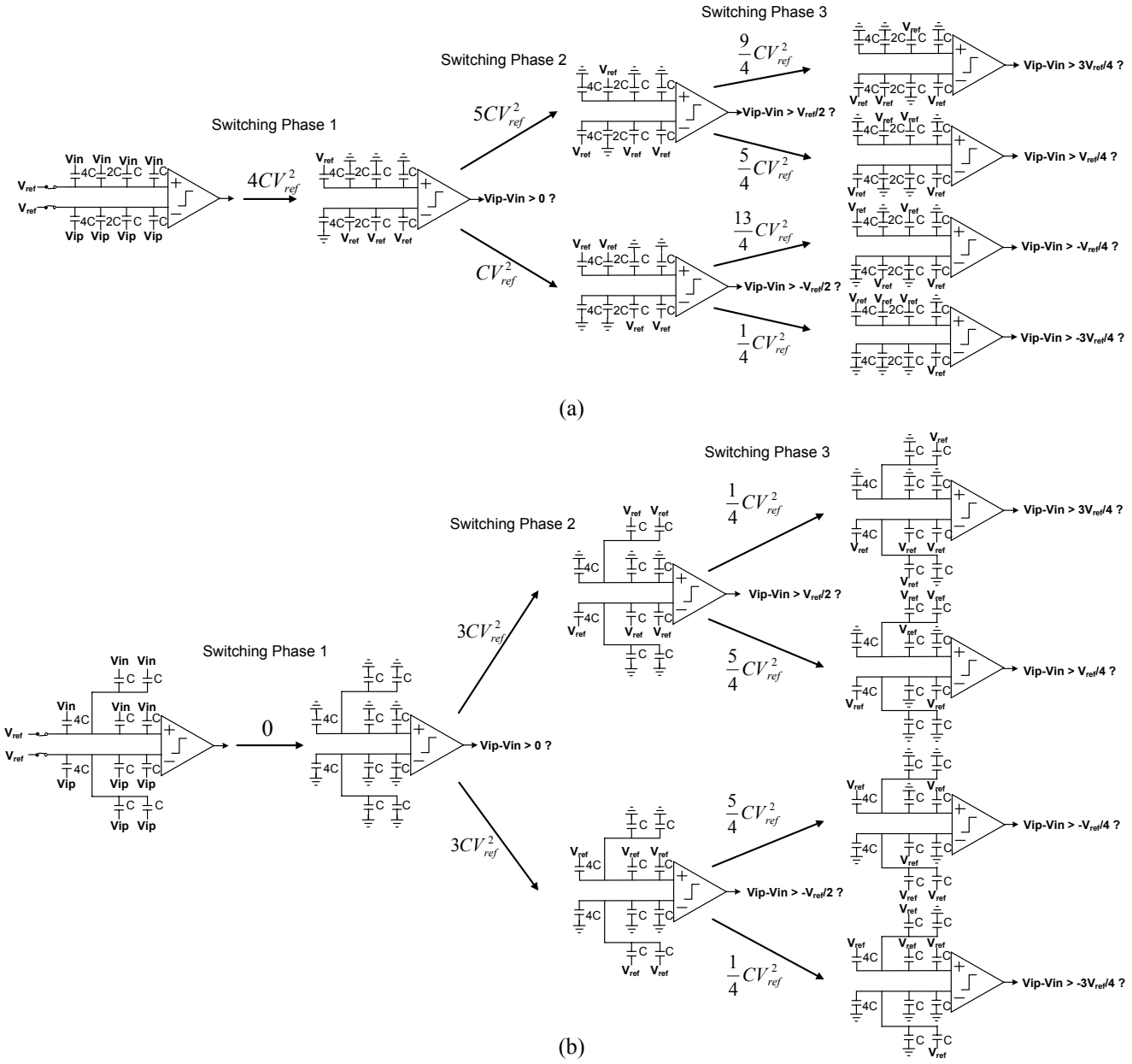

Fig. 2. (a) Conventional Switching Sequence. (b) Proposed energy-saving switching sequence.

the energy-saving switching sequence consumes no power in the first switching phase. Moreover, the energy-saving switching sequence combines capacitor splitting technique which splits MSB/2 capacitor into parallel binary-weighted sub capacitor array to efficiently reduce the energy required during the up paths of each switching phase in Fig. 2(a). The difference of two switching methodologies can be observed in detail in Fig. 2. The average switching energy for an n-bit SAR ADC using proposed energy-saving switching sequence can be derived as:

$$E_{total,n-bit} = 3 \cdot 2^{n-3} + \sum_{i=3}^{n} 2^{n+1-2i}(2^{i-1}-1)CV_{ref}^2 \quad (2)$$

The average switching energy, $E_{total,n\text{-}bit}$, of two switching sequences for an n-bit capacitor array is shown in Fig. 3. The energy-saving switching sequence is applicable to any bit of SAR ADC. For an 8-bit SAR ADC, it consumes $339CV_{ref}^2$ Joules using conventional switching sequence while the proposed energy-saving switching sequence only consumes $148CV_{ref}^2$ Joules which achieves 56% energy saving in switching the capacitor array compared to the conventional one. Fig. 4 shows the energy comparison of two switching sequences for every output code in a conversion period. The larger the output code, the more switching energy required for conventional sequence while the switching energy for each output code almost remains the same for energy-saving sequence.

III. CIRCUIT DESIGN

A. Capacitor Array

The linearity of the SAR ADC is dependent upon the

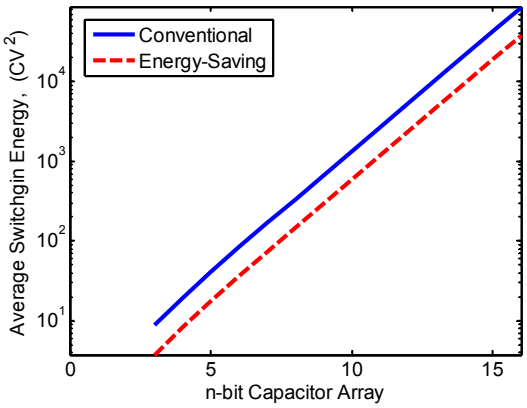

Fig. 3. The average switching energy of two sequences for an n-bit SAR ADC.

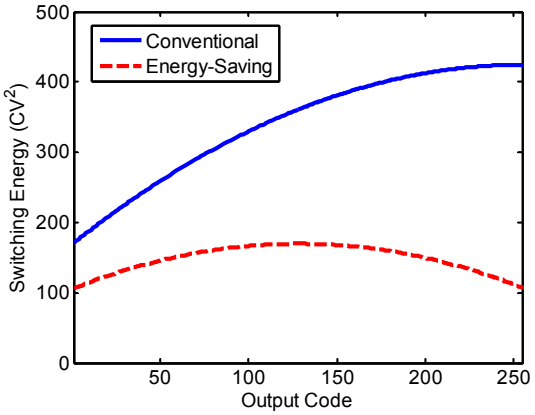

Fig. 4. The energy versus output code required for the switching of the capacitor array.

capacitor matching in the capacitor array. Each capacitor in the capacitor array consists of numbers of unit capacitors. A unit capacitance of 20fF metal-insulator-metal capacitor (MIMCAP of 4μm × 4μm) is chosen to guarantee the 8-bit linearity requirement. A layout floorplan of the capacitor array is depicted in Fig. 5. In order to improve linearity and tolerate process gradients, common-centroid layout technique is utilized. A dummy capacitor ring is also used on the edges of the capacitor array to ensure that all unit capacitors in the capacitor array have the same structure around them.

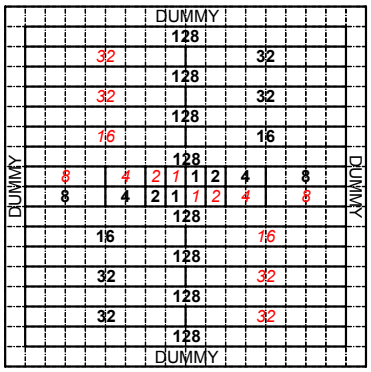

Fig. 5. The layout floorplan of the capacitor array.

B. Comparator

The comparator circuit is shown in Fig. 6.The operation principle is described below. When V_{clk} is low, the comparator is in precharge phase. Nodes V_{out}^+ and V_{out}^- are precharged to V_{dd} by transistors M_5 and M_6. Because M_9 is off at this time, no dc current flows from V_{dd} to ground. When V_{clk} is high, the comparator is in comparison phase. At this time, V_{out}^+ and V_{out}^- slew towards ground at unequal rates according to the differential input voltage V_{in}^+ and V_{in}^-. Once the voltages of V_{out}^+ and V_{out}^- are low enough, the PMOS positive feedback load formed by M_7 and M_8 latches the comparator. When the comparator is in steady-state, there is also no dc current flowing from V_{dd} to ground. Therefore, it is suitable for low power application due to no static current consumption.

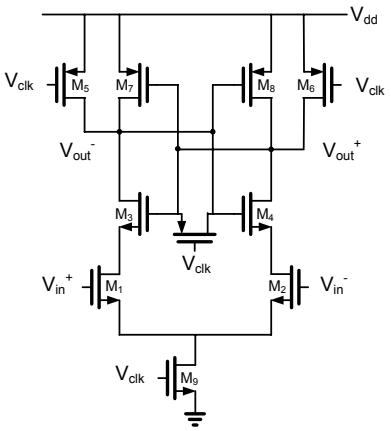

Fig. 6. Comparator circuit.

C. Successive Approximation Register

Figure 7 shows the SAR which provides control signals to the capacitor array to implement the energy-saving switching sequence.

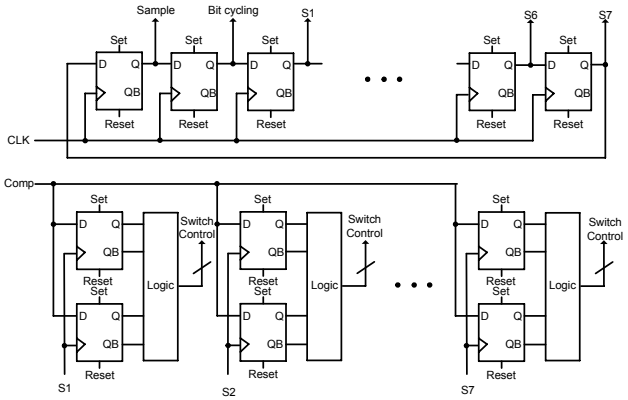

Fig. 7. SAR schematic.

IV. Measurement Results

The ADC is fabricated in a standard 0.18-µm CMOS process. A chip photograph is shown in Fig. 8. The total chip size occupies 1×1 mm^2 and the core size measures 250×320 µm^2.

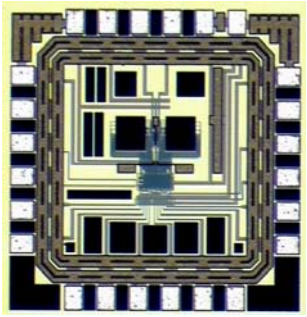

Fig. 8. Die photograph.

The static performance is characterized through differential nonlinearity (DNL) and integral nonlinearity (INL) measurement. The measured DNL and INL are +0.17/-0.24 LSB and +0.31/-0.28 LSB, respectively.

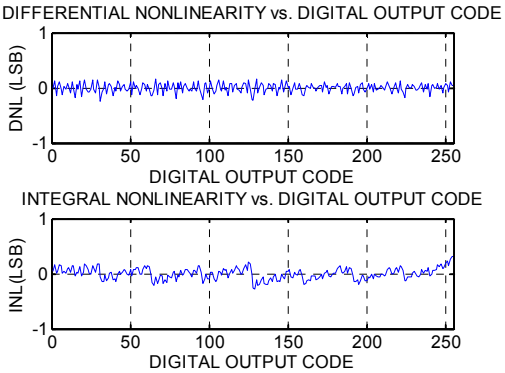

Fig. 9. Measured DNL and INL error..

The measured FFT spectrum at input frequency close to Nyquist rate is shown in Fig. 10. The measured SNDR is 46.92 dB which equals to ENOB of 7.5 bits and the SFDR is 62.69 dB. Fig. 11 plots the ENOB of the ADC as a function of input frequency. The total power dissipation of the ADC is 7.75-µW at 500-KS/s sampling rate and supply voltage of 1-V. The typical figure of merit (FOM) definition of the ADCs is defined as:

$$FOM = \frac{Power}{2^{ENOB} \cdot f_s} \qquad (3)$$

The FOM of this work corresponds to 86fJ/conversion-step and is better than previous publications [2][3].

V. Conclusions

A 1-V 8-bit 500-KS/s SAR ADC using proposed energy-saving switching sequence is realized in a standard 0.18-µm CMOS technology. The feature of low power dissipation makes it well-suited for bio-medical applications.

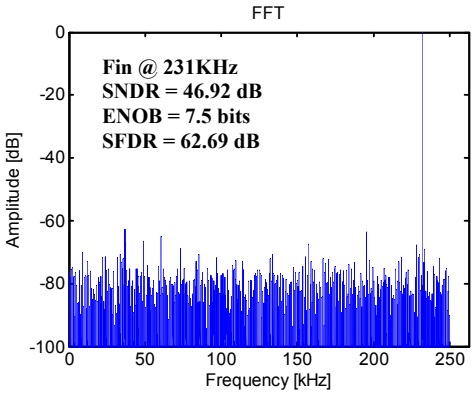

Fig. 10. Measured FFT spectrum at input frequency of 231-KHz.

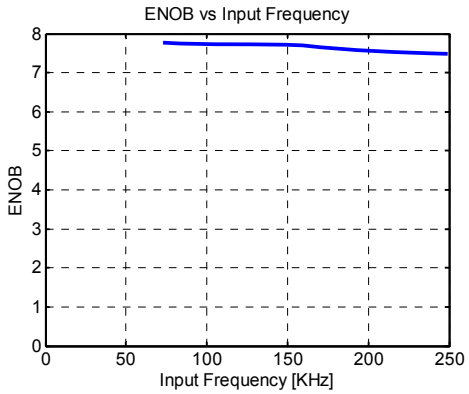

Fig. 11. ENOB versus input frequeny.

Acknowledgment

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References

[1] J. Sauerbrey, D. Schmitt-Landsiedel, and R. Thewes, "A 0.5-V 1-µW Successive Approximation ADC," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1261-1265, July 2003.

[2] M. Scott, B. Boser, and K. Pister, "An Ultra Low-Energy ADC for Smart Dust," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1123-1129, July 2003.

[3] N. Verma and A. Chandrakasan, "A 25µW 100kS/s 12b ADC for Wireless Micro-Sensor Applications," *ISSCC Dig. Tech. Papers*, pp. 222-223, Feb. 2006.

[4] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," in *Proc. IEEE Int. Symp. Circuits and Systems,*2005, vol. 1, pp. 184-187.