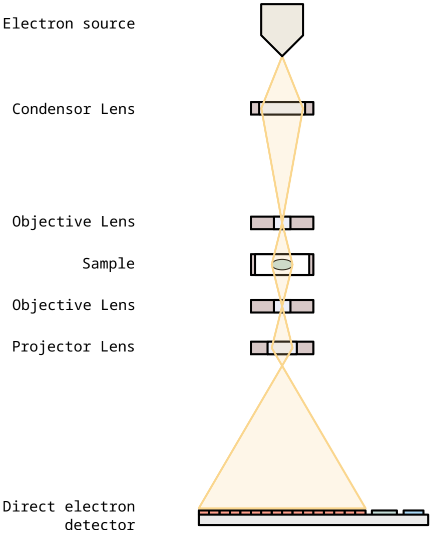
Modeling data converters for high frame rate imaging detectors

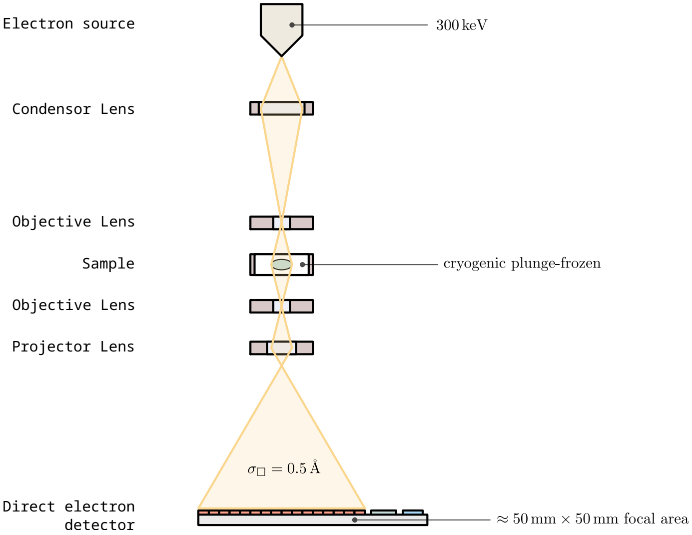
UNIVERSITÄT BONN

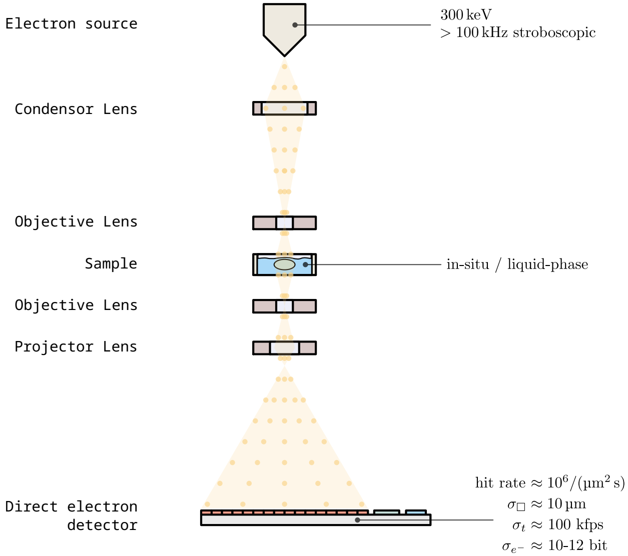
FTD

SI LAB Silizium Labor Bonn

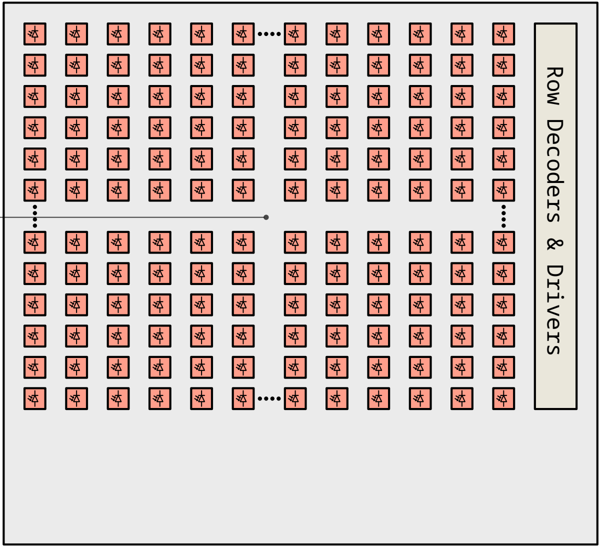
Bundesministerium für Bildung und Forschung


Electron source
Condensor Lens
Objective Lens
Sample
Objective Lens
Projector Lens
Direct electron
detector


Electron source
300 keV
Condensor Lens
Objective Lens
Sample
cryogenic plunge-frozen
Objective Lens
Projector Lens
$\sigma_\square = 0.5\,\text{Å}$
Direct electron detector
$\approx 50\,\text{mm} \times 50\,\text{mm}$ focal area


Electron source
300 keV
> 100 kHz stroboscopic
Condensor Lens
Objective Lens
Sample
in-situ / liquid-phase
Objective Lens
Projector Lens
Direct electron detector
hit rate $\approx 10^6/(\mu\mathrm{m}^2\,\mathrm{s})$
$\sigma_\square \approx 10\,\mu\mathrm{m}$
$\sigma_t \approx 100$ kfps
$\sigma_{e^-} \approx 10$-12 bit

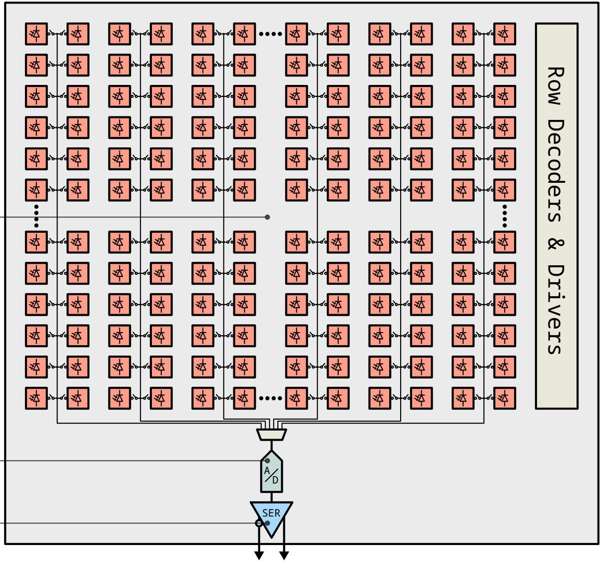
≈ 600 µm^2 reticle limit
≈ 15 µm pitch
≈ 1 Mpixel array
2-side buttable



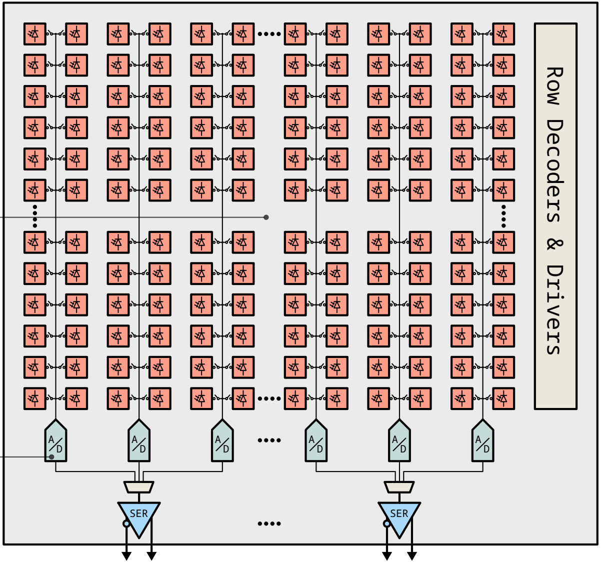
$\approx 600\,\mu m^2$ reticle limit
$\approx 15\,\mu m$ pitch
$\approx$ 1 Mpixel array
2-side buttable

$\approx 60\,mm^2$
$\approx 1\,W$
10-12 bit
$\approx$ 100 Gsps

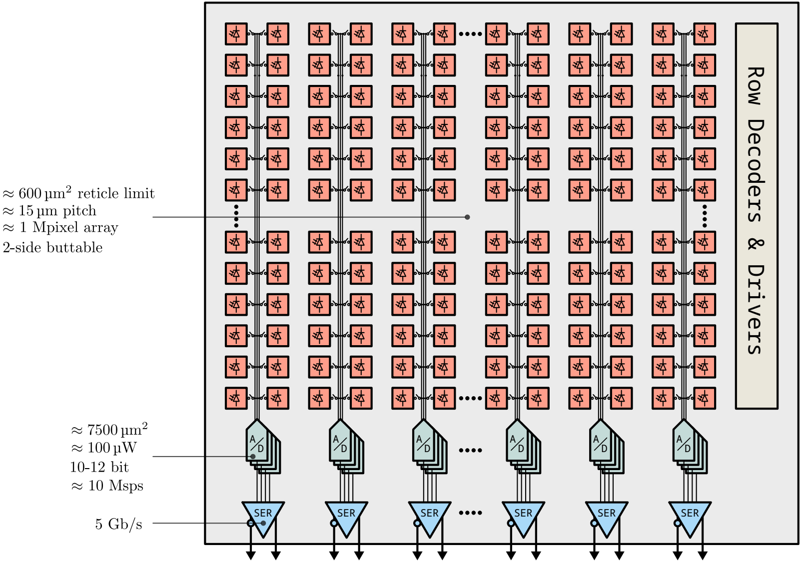
1 Tb/s

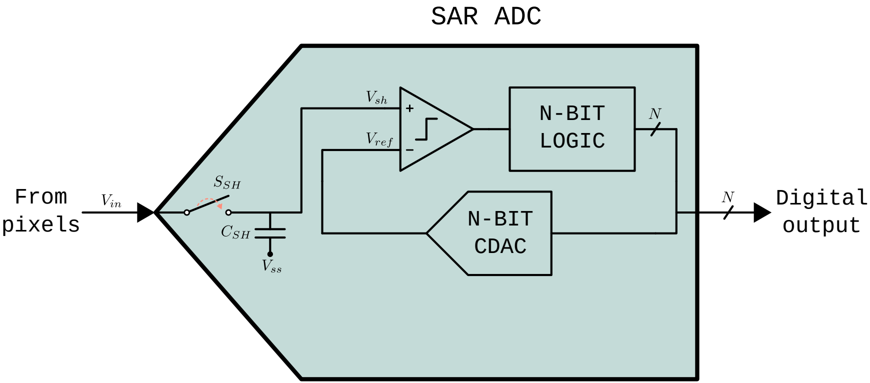


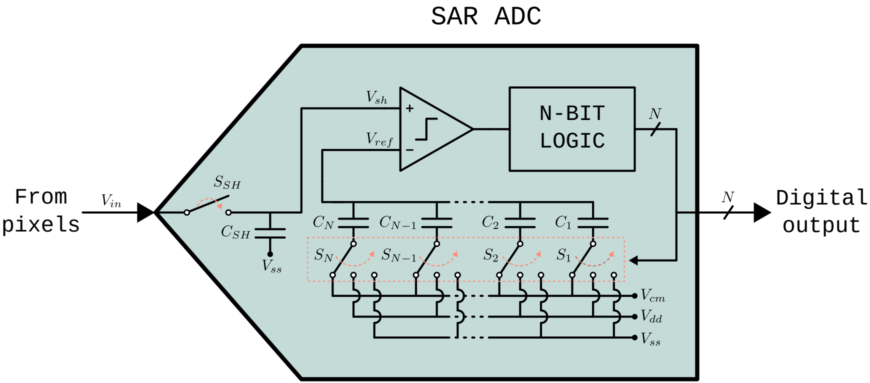
$\approx 600\,\mu m^2$ reticle limit
$\approx 15\,\mu m$ pitch
$\approx$ 1 Mpixel array
2-side buttable



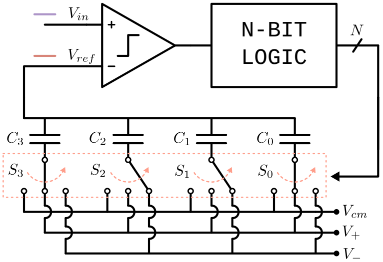
$\approx 120\,000\,\mu m^2$
$\approx 1\,mW$
10-12 bit
$\approx$ 200 Msps

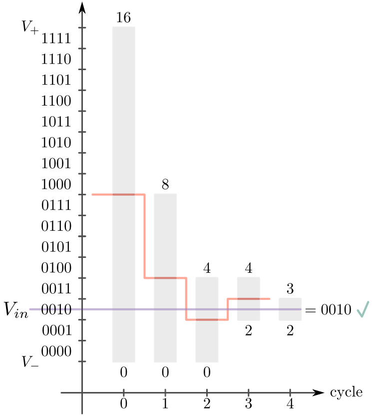

≈ 600 µm^2 reticle limit
≈ 15 µm pitch
≈ 1 Mpixel array
2-side buttable
≈ 7500 µm^2
≈ 100 µW
10-12 bit
≈ 10 Msps
5 Gb/s
Row Decoders & Drivers
A/D
SER


SAR ADC
From
pixels
V_{in}
S_{SH}
C_{SH}
V_{ss}
V_{sh}
V_{ref}
+
−
N-BIT
LOGIC
N-BIT
CDAC
N
N
Digital
output

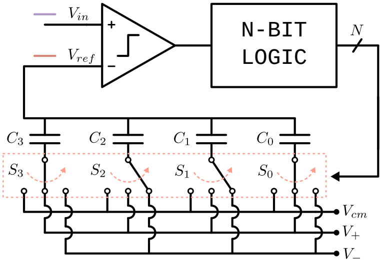

SAR ADC
From pixels
V_{in}
S_{SH}
C_{SH}
V_{ss}
V_{sh}
V_{ref}
+
−
N-BIT LOGIC
N
C_N
C_{N-1}
C_2
C_1
S_N
S_{N-1}
S_2
S_1
V_{cm}
V_{dd}
V_{ss}
N
Digital output

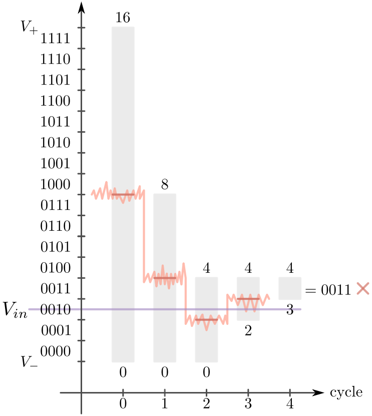
Basic ideal operation



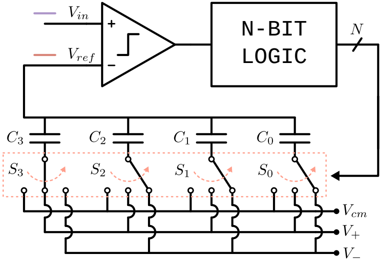


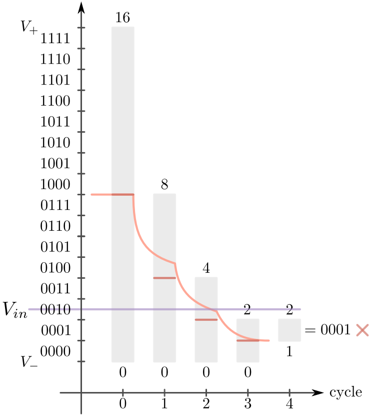
Threshold and reference noise (dynamic error)



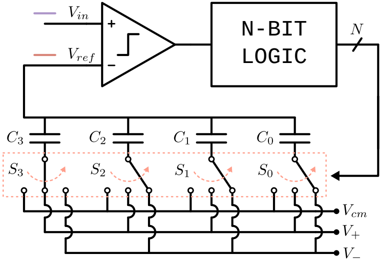


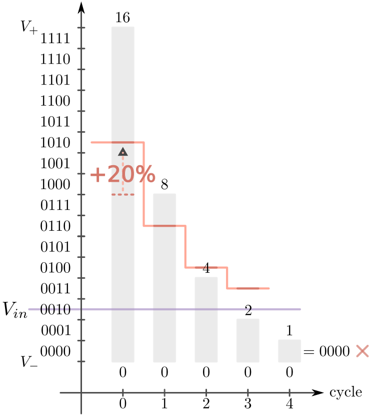
Settling error (dynamic error)





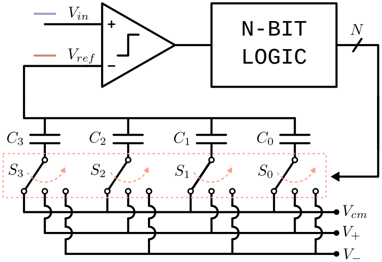
Mismatch errors (static error)





CDAC construction principles

For complete capacitor array. We'd like to be as close to min capacitance as possible, to the point that we'd have 125aF for unit caps in 10-bit design



$\downarrow \quad C_{total} \quad \uparrow$

MOM cap density $\approx 0.5\,\text{fF}/\mu\text{m}^2$

$E_{CDAC} \approx CV^2$

$\tau_{CDAC} \approx R_{switch} \times C_{total}$

$C_\sigma \approx \frac{1}{\sqrt{C_{total}}}$

$V_{rms} = \sqrt{\frac{k_B T}{C}}$

CDAC construction principles

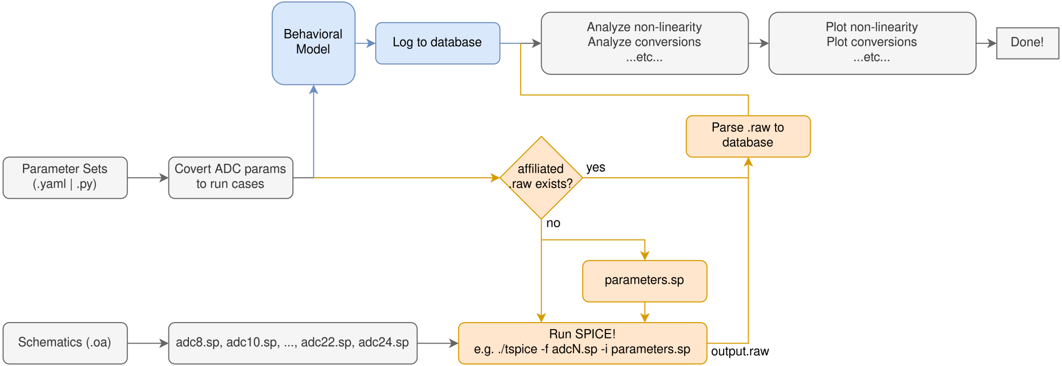
For individual capacitor weights

- Defining each bit weights as integers simplifies cap implementation; improves matching
- And defining each bit weight as sum of binary scaled values keeps DEC to just adders
- Finally, keeping sum total to binary scaled total prevents overflow

SAR modeling status

- Threshold noise and variation, reference noise, settling error, capacitor mismatch supported
- Arbitrary CDAC weights, with support for ”extended range bits”
- Monotonic and bidirectional-single-side switching supported (CRS, CAS, MCS to be added)
- Analyses for static and dynamic performance analyses ($ENOB@f_s$)
- Single test case requires 20 seconds
- Compatibility with T-Spice, AFS, and Spectre simulator (30hr run, 4hr with Spectre)

SAR modeling status



Ideal 10-bit operation

behavioral_10b_ideal_combine.pdf

Error tolerance strategies

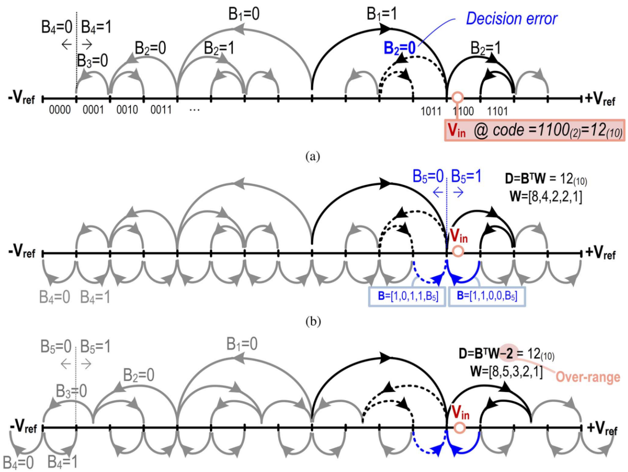
Sub-radix 2 steps

- Creates overlapping search voltages
- In D_{out} procesed as $W_i \times B_i$
- Can also satisfy calibratability requirements

Extended search steps

- In D_{out} procesed as $W_i \times (B_i - 0.5)$
- Decreases input amplitude swing to $V_{ref} \times \frac{C}{d}$
- Introduced by CC Liu 2010, where they were additional cap,

Error tolerance strategies

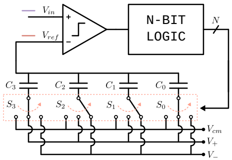


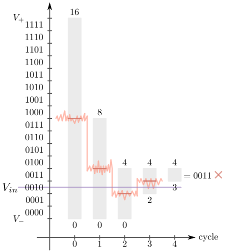
from HS Tsai 2015

Device and reference noise correction

- In most common case, only small LSBs errors will occur from thermal noise.
- Can be corrected by single post-bits, or more comparator power

$$\sigma_n^2 \leq LSB^2/2 \times 12$$

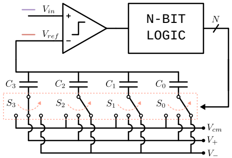


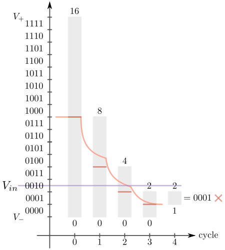


Settling error correction

Most pronounced in MSBs, recovery determined by remaining caps:

$$\text{Error tolerance } @B_i = \frac{\sum_{i+1}^{M} B_j - B_i}{\sum_{i}^{M} B_j} \times 100\%$$

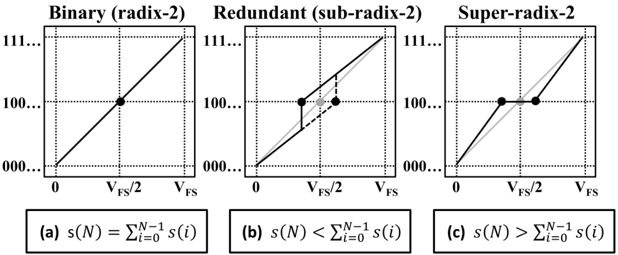




Mismatch static error & calibratability

- Redundancy can absorb static error, but what about mismatch?
- 1-bit comparator = inherintely linear, so CDAC dominates
- Assuming monotonic switching, without cap-reuse like CRS [Tsai 2015]

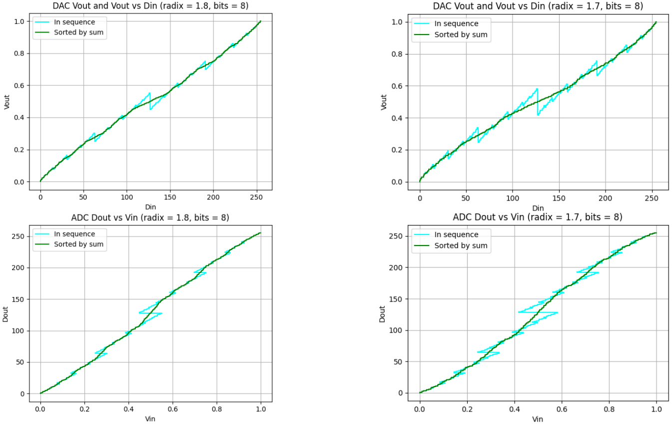
$$\sigma_{INL_{max}} \approx \frac{1}{2}(\sigma_{C_{unit}})\sqrt{2^N}$$



Visual from both A. Hsu 2013 and W. Liu 2010

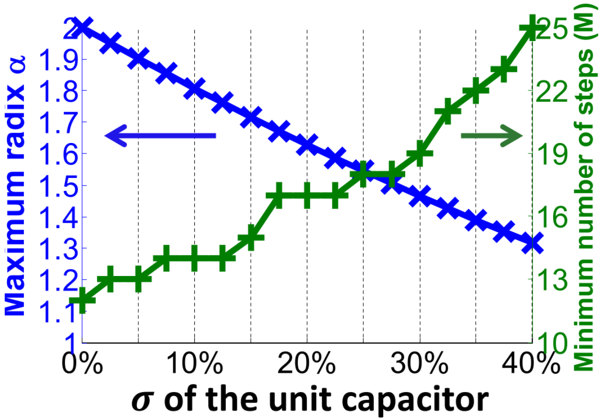
Mismatch static error & calibratability

Lower radixes create more overlap tolerance to prevent missing levels



Mismatch static error & calibratability

Radix β and min. steps vs unit cap mismatch $\sigma_{C_{unit}}$ (A. Hsu 2013)



10-bit w/ device noise

behavioral_10b_devnoise_combine.pdf

10-bit w/ reference noise

behavioral_10b_refnoise_combine.pdf

10-bit w/ device and reference noise

behavioral_10b_noisy_combine.pdf

10-bit w/ noise and postconversions

behavioral_10b_noisy_postconv_combine.pdf

10-bit w/ noise and split MSB

behavioral_10b_noisy_splitmsb_combine.pdf

10-bit w/ noise and radix 1.75

behavioral_10b_noisy_radix175_combine.pdf

10-bit w/ noise and radix 1.75 normalized

behavioral_10b_noisy_radix175norm_combine.pdf

10-bit w/ noise and binary compensation

behavioral_10b_noisy_bincomp_combine.pdf

10-bit w/ noise and binary recombination

behavioral_10b_noisy_binrecomb_combine.pdf

10-bit w/ noise and SC-ADEC

behavioral_10b_noisy_scadec_combine.pdf

10-bit w/ settling error

behavioral_10b_seterror_combine.pdf

10-bit w/ settling error and binary recombination

behavioral_10b_seterror_binrecomb_combine.pdf

10-bit w/ settling error and SC-ADEC

behavioral_10b_seterror_splitmsb_combine.pdf

10-bit w/ mismatch

behavioral_10b_mismatch_combine.pdf

10-bit w/ mismatch and binary recombination

behavioral_10b_mismatch_binrecomb_combine.pdf

10-bit w/ mismatch and radix 1.75 normalized

behavioral_10b_mismatch_radix175norm_combine.pdf