Data converters for high frame rate imaging detectors

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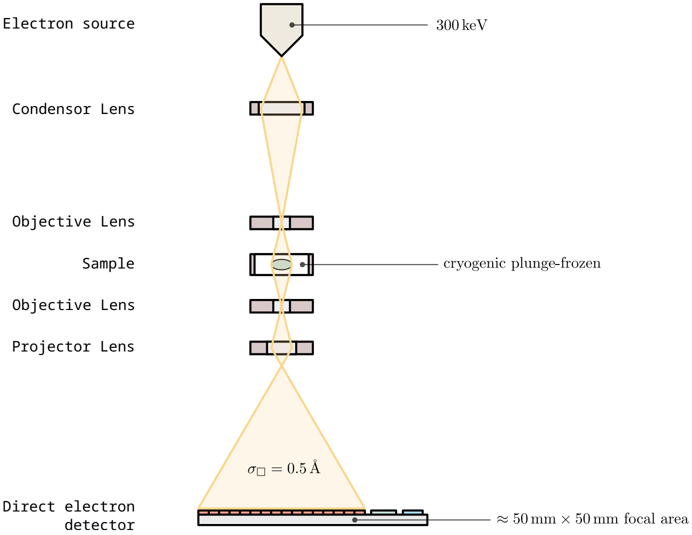
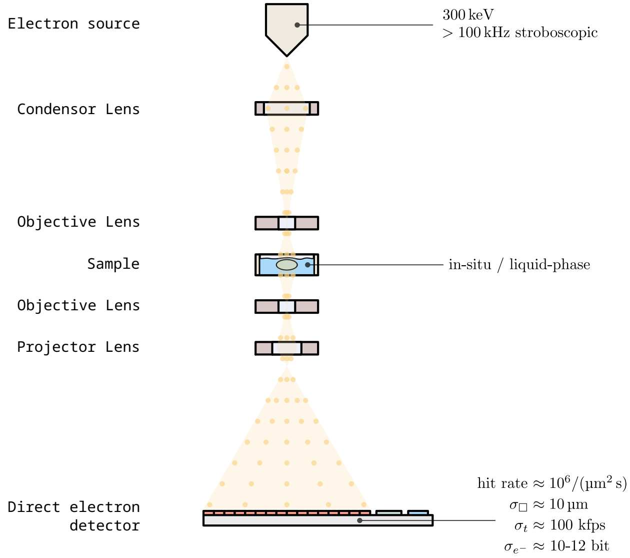
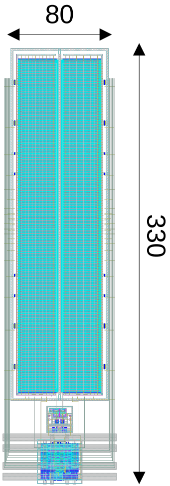

Electron source
300 keV
Condensor Lens
Objective Lens
Sample
cryogenic plunge-frozen
Objective Lens
Projector Lens
$\sigma_\square = 0.5$ Å
Direct electron detector
≈ 50 mm $\times$ 50 mm focal area

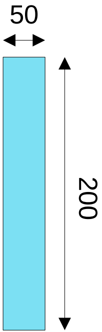


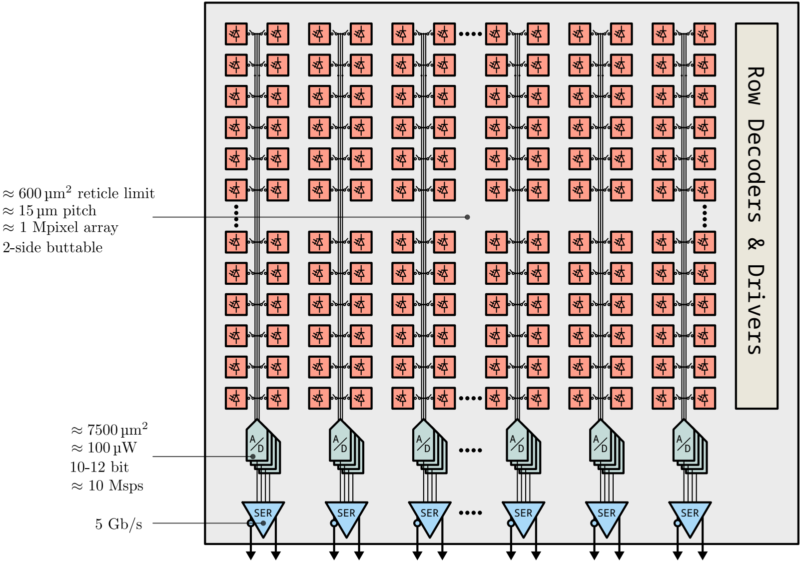
Electron source
300 keV
> 100 kHz stroboscopic
Condensor Lens
Objective Lens
Sample
in-situ / liquid-phase
Objective Lens
Projector Lens
Direct electron detector
hit rate ≈ $10^6/(\mu m^2\,s)$
$\sigma_\square \approx 10\,\mu m$
$\sigma_t \approx 100$ kfps
$\sigma_{e^-} \approx$ 10-12 bit



65nm → 28nm

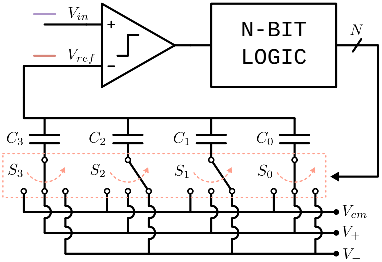
Design	CORDIA	FRIDA
ADC resolution	10-bit	10/12-bit
Conversion rate	2.5MHz	10 MHz
Area of one ADC	80x330 μm²	50x200 μm²
Power of one ADC	30 μW	100 μW
FOM_csa (conv/sec/area)	95 Hz/μm²	5000 Hz/μm²
FOM_epc (energy/conv)	12 pJ	10 pJ
FOM_ppa (power/area)	0.11 W/cm²	5.0 W/cm²
ADC qty Mpix @ 100 KHz	40000	10000
ADCs total pixel rate	100 Gpx/s	100 Gpx/s
ADCs total data rate	1 Tb/s	1 Tb/s
ADCs total area	10.5 cm²	0.2 cm²
ADCs total power	1.2 W	1.0 W

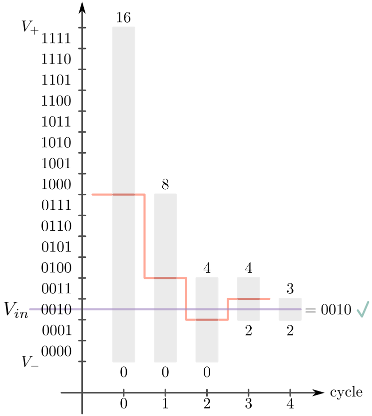




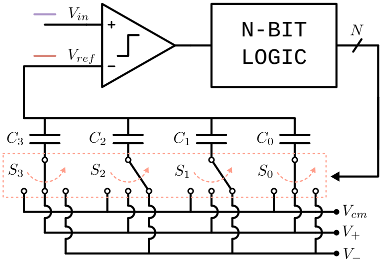
≈ 600 µm^2 reticle limit
≈ 15 µm pitch
≈ 1 Mpixel array
2-side buttable
≈ 7500 µm^2
≈ 100 µW
10-12 bit
≈ 10 Msps
5 Gb/s
A/D
SER
Row Decoders & Drivers

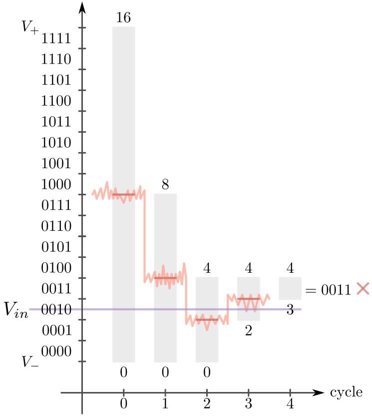
Basic ideal operation



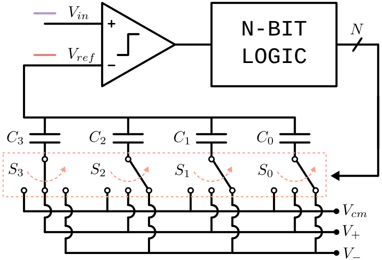


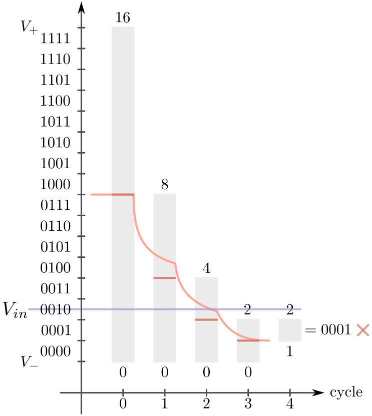
Threshold and reference noise (dynamic error)



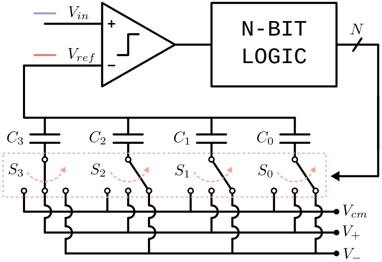


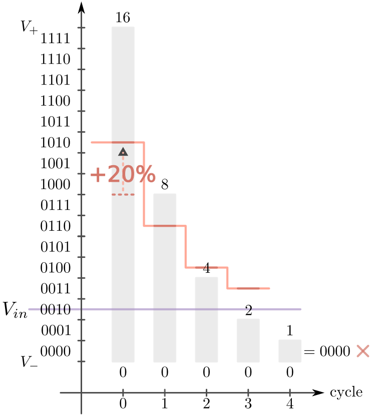
Settling error (dynamic error)





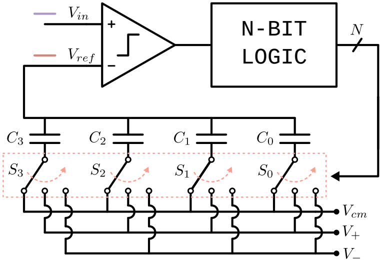
Mismatch errors (static error)





CDAC construction principles

For complete capacitor array. We'd like to be as close to min capacitance as possible, to the point that we'd have 125aF for unit caps in 10-bit design



$$C_{total}$$

MOM cap density $\approx 0.5\,\mathrm{fF}/\mu\mathrm{m}^2$

$$E_{CDAC} \approx CV^2$$

$$\tau_{CDAC} \approx R_{switch} \times C_{total}$$

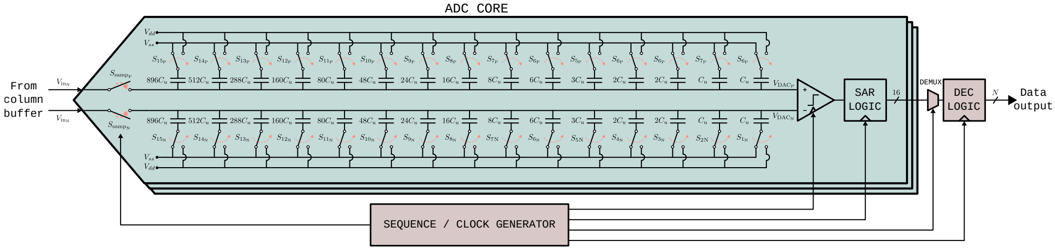
$$C_\sigma \approx \frac{1}{\sqrt{C_{total}}}$$

$$V_{rms} = \sqrt{\frac{k_B T}{C}}$$

CDAC construction principles

For individual capacitor weights

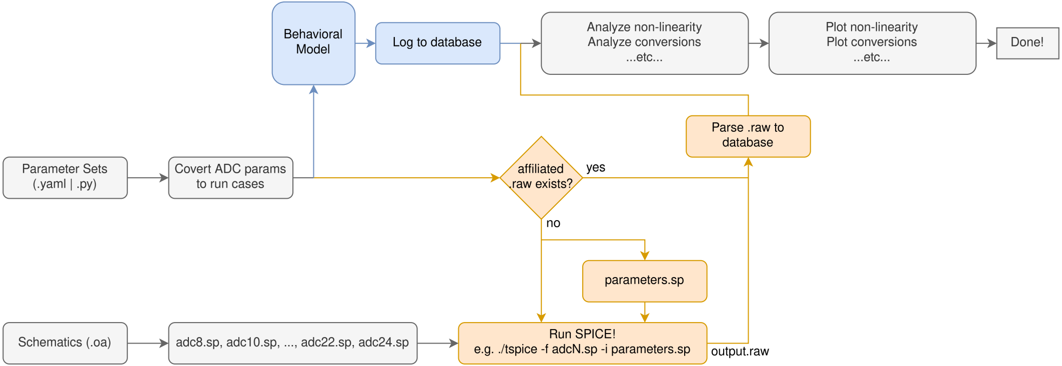
- Defining each bit weights as integers simplifies cap implementation; improves matching
- And defining each bit weight as sum of binary scaled values keeps DEC to just adders
- Finally, keeping sum total to binary scaled total prevents overflow


ADC CORE
From
column
buffer
V_inN
V_inN
S_sampP
S_sampN
Vdd
Vss
S15P S14P S13P S12P S11P S10P S9P S8P S7P S6P S5P S6P S6P S7P S6P
896Cu 512Cu 288Cu 160Cu 80Cu 48Cu 24Cu 16Cu 8Cu 6Cu 3Cu 2Cu 2Cu Cu Cu
V_DACP
V_DACN
S15N S14N S13N S12N S11N S10N S9N S8N S7N S6N S5N S4N S3N S2N S1N
SAR
LOGIC
16
DEMUX
DEC
LOGIC
N
Data
output
SEQUENCE / CLOCK GENERATOR

SAR modeling

- Threshold noise and variation, reference noise, settling error, capacitor mismatch supported
- Arbitrary CDAC weights, with support for ”extended range bits”
- Monotonic and bidirectional-single-side switching supported (CRS, CAS, MCS to be added)
- Analyses for static and dynamic performance analyses ($ENOB@f_s$)
- Single test case requires 20 seconds
- Compatibility with T-Spice, AFS, and Spectre simulator (30hr run, 4hr with Spectre)

SAR modeling status



Error tolerance strategies

Sub-radix 2 steps

- Creates overlapping search voltages
- In D_{out} procesed as $W_i \times B_i$
- Can also satisfy calibratability requirements

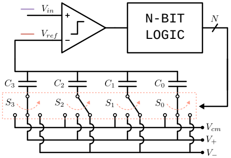
Extended search steps

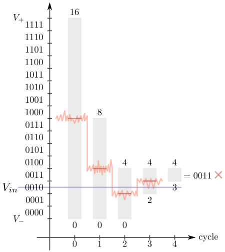
- In D_{out} procesed as $W_i \times (B_i - 0.5)$
- Decreases input amplitude swing to $V_{ref} \times \frac{C}{d}$
- Introduced by CC Liu 2010, where they were additional cap,

Device and reference noise correction

- In most common case, only small LSBs errors will occur from thermal noise.
- Can be corrected by single post-bits, or more comparator power

$$\sigma_n^2 \leq LSB^2/2 \times 12$$

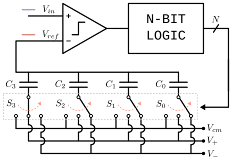


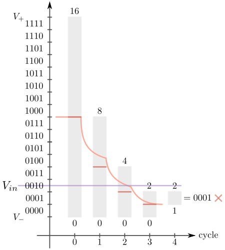


Settling error correction

Most pronounced in MSBs, recovery determined by remaining caps:

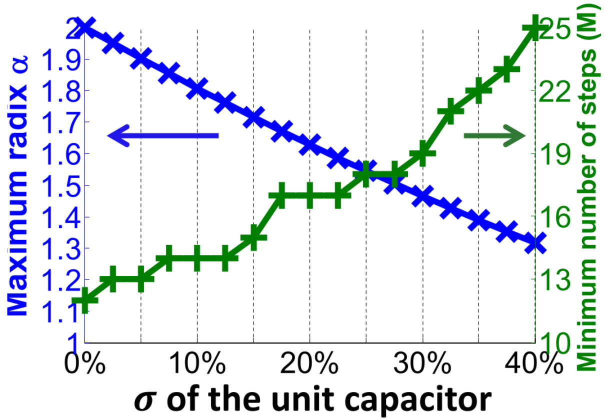
$$\text{Error tolerance } @B_i = \frac{\sum_{i+1}^{M} B_j - B_i}{\sum_{i}^{M} B_j} \times 100\%$$



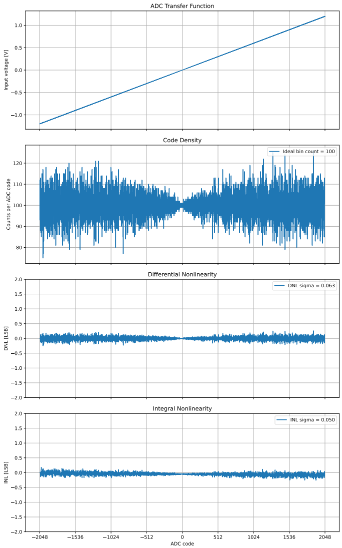


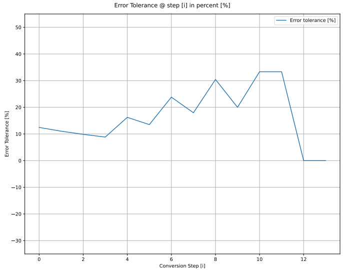
Mismatch static error & calibratability

Radix β and min. steps vs unit cap mismatch $\sigma_{C_{unit}}$ (A. Hsu 2013)

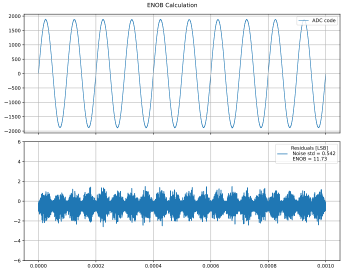


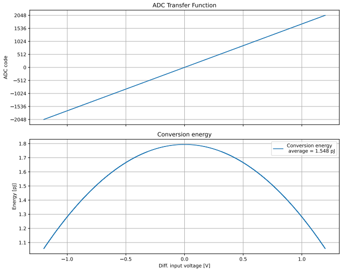
12-bit w/ device noise, mismatch, etc

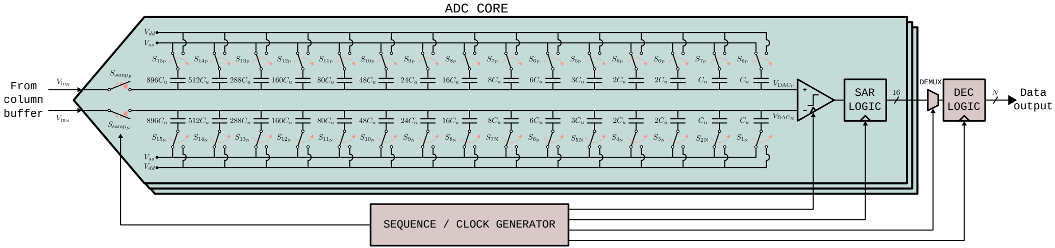




Parameter	Value	Unit
Resolution	12	bits
Sample frequency	10.000	Msps
LSB size	0.586	mV
DAC weights array	[896 512 288 160 80 48 24 16 8 6 3 2 2 1 1]	
DAC weights sum (+1)	2048	
DAC capacitor array size	15	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	2.048	pF
DAC settling error	0.00	%
Comparator noise	0.000	mV
Comparator offset	0.000	mV
Reference voltage noise	0.500	mV
DNL	0.06	LSB
INL	0.05	LSB
ENOB	11.73	bits
FOM (energy/conversion)	0.13	pJ






ADC CORE
From column buffer
SEQUENCE / CLOCK GENERATOR
SAR LOGIC
DEMUX
DEC LOGIC
Data output
16
N