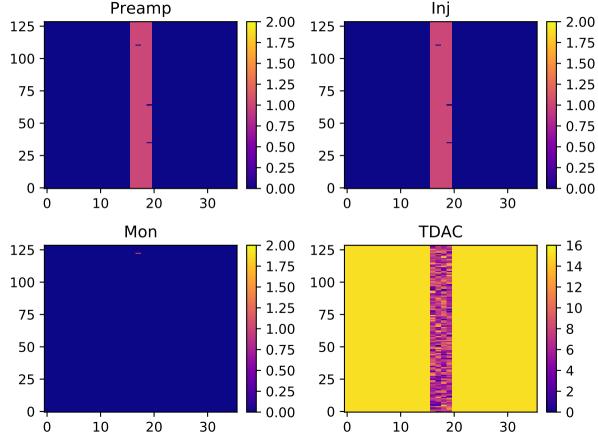
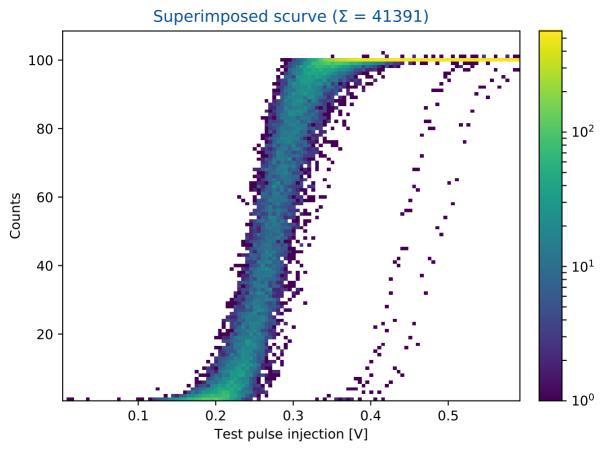
Chip configuration

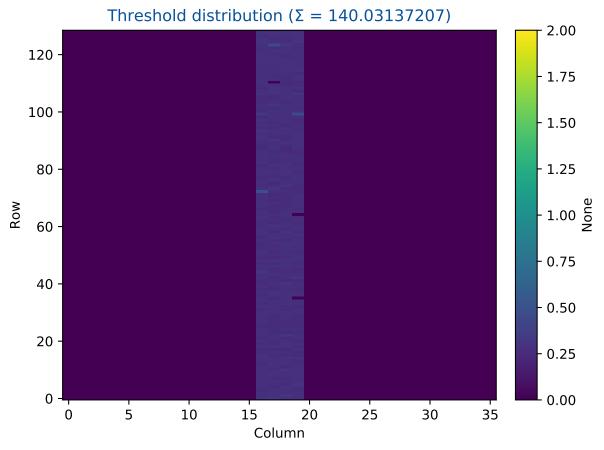
Param	Value	Param	Value	Param	Value
BLRes	32	VCascC[V]	0.80024316675	VPLoad	11
BL[V]	0.750341831166	VCascC[mA]	-0.0341521108066	Vbias_CS	32
BL[mA]	0.165990175419	VCascCset	0.8	Vfs	32
BLset	0.75	VCascN[V]	0.40083772064	Vsf_dis1	10
IBOTA	32	VCascN[mA]	-0.0374982734397	Vsf_dis2	20
lComp	32	VCascNset	0.4	Vsf_dis3	30
ILVDS	32	VDDA[V]	1.79289202196	inj_delay	5000
INJ_HIset	0.695	VDDA[mA]	5.616529772	inj_n	100
INJ_LOset	0.1	VDDAset	1.8	inj_width	5000
LSBdacL	45	VDDD[V]	1.795278124		
NTC[V]	0.043124243	VDDD[mA]	2.79704329735		
NTC[mA]	0.00468387075	VDDDset	1.8		
NTCset	5	VDD_BCID_BUFF[V]	1.69168245838		
PBias[V]	1.82314792706	VDD_BCID_BUFF[mA]	12.0438562526		
PBias[mA]	-0.00112305991013	VDD_BCID_BUFFset	1.7		
PBiasset	0.5	VPC[V]	1.49956992545		
TH[V]	0.766757103148	VPC[mA]	-6.03673399586e-08		
TH[mA]	0.00846572172922	VPCset	1.5		
THset	0.7655	VPFB	32		
VAmp	32	VPFoll	12		

Preamp

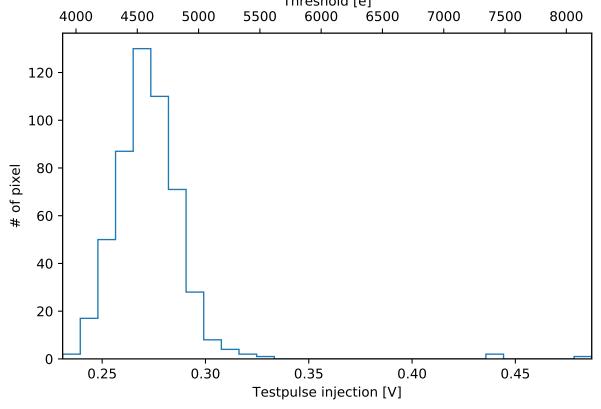


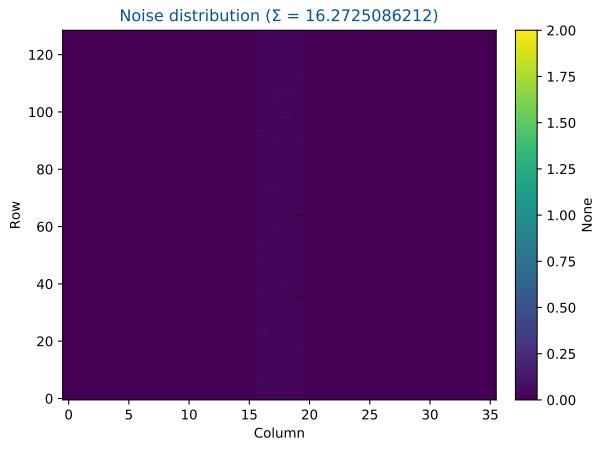
Pixel configuration





Threshold distribution Threshold [e]





Threshold distribution Noise [e]

