Capacitance Measurement of Silicon Hybrid Pixel Detectors

Evelyn Kimmerle

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1. Gutachter: Dr. Hans Krüger
2. Gutachter: Prof. Dr. Norbert Wermes

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CHAPTER 1

Introduction

In high energy physics the most fundamental constituents of particles and their interaction are studied. One of the biggest institutions dedicated to this research is CERN (European Organization for Nuclear Research). An elementary particle is characterized by its mass, charge and spin. In order to gather information about them, particle accelerators are used. One of them is the Large Hadron Collider (LHC) located at CERN. Two separate particle beams (protons or lead-ions) move in opposite directions close to the speed of light before they are brought to collision. Surrounding the interaction region, there are detectors which collect information about the colliding particles or their decay products. Each detector layer has a different task such as measuring momentum, energy or charge. From this, conclusions about the involved particles can be drawn.

The so called luminosity is a value describing the event rate of a collision. For the LHC, a luminosity upgrade from $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ up to $10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ (High-LHC) is planned for 2026 [1]. Increased luminosity also requires improvement of the innermost tracking layers since the pixel detectors are challenged by ten times higher hit rates and more radiation. They form the closest detector to the interaction point and provide information about particle tracks and vertices. Because of the new requirements given by the accelerator, the pixel detector of the ATLAS experiment at CERN will also be exchanged [2]. For this, advanced hybrid pixel sensor technologies are under development. Both the sensing and readout parts need to cope with data throughput and radiation damage what influences the performance of the detector in terms of degrading the signal-to-noise ratio and higher power consumption [3].

The pixel capacitance is a sensitive parameter when it comes to pixel sensors and signal processing so its precise knowledge is important. For this purpose, a dedicated integrated circuit – the PixCap65 chip – was developed.

This thesis is focussed on the capacitance measurement of hybrid pixel sensors with the PixCap65 chip. The second Chapter gives a brief overview of the basis pixel detector elements and the influence of the sensor capacitance on the readout electronics and the noise performance.

The third chapter introduces the capacitance measurement method and how its implemented in the PixCap65 chip.

In Chapter 4, operating parameters as well as parasitic contributions of the chip are determined. Afterwards the results of a hybrid pixel sensor measurement are presented.

The final Chapter summarises and prospects on further measurements.

CHAPTER 2

Influence of pixel capacitance in hybrid pixel detectors

2.1 Basic elements of a hybrid pixel detector

Hybrid pixel detectors are chosen for the first detector layer the particles pass after collision because of their precise spatial and time resolution. They are used in many experiments, e.g. ATLAS and CMS at CERN. They consist of a pixelated sensor and an electronic readout chip whose dimensions correspond exactly to the sensor pixel geometry. The two components are connected with solder bumps using a flip-chipping process [4] that enable the extraction of generated signals in the sensor [5].

The sensor operates with a negative bias voltage connected to the backplane in order to deplete the whole sensor bulk. In Fig. 2.1, an illustration of a hybrid planar sensor is shown.

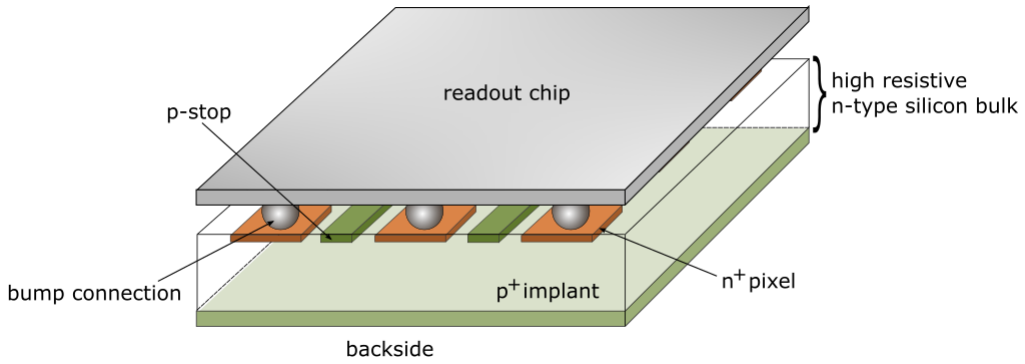


Figure 2.1: Schematic hybrid pixel detector setup. The pixels (n^+-implantations) are separated by p-stops (p^+-implantations). The readout chip is bump-bonded on the sensor.

When a pixel sensor is hit by a particle, the generated signal is processed by the readout chip. At first, the analogue hit information needs to be amplified, shaped and discriminated. Since the pixel capacitance has significant influence on signal processing and noise performance of the readout chip, these factors are discussed in more detail in the following two sections.

2.2 Time response of a charge sensitive amplifier

The charge sensitive amplifier (CSA) is a component of the readout chip consisting of an inverting amplifier with capacitive feedback C_F and amplification A_0 (see Fig. 2.2).

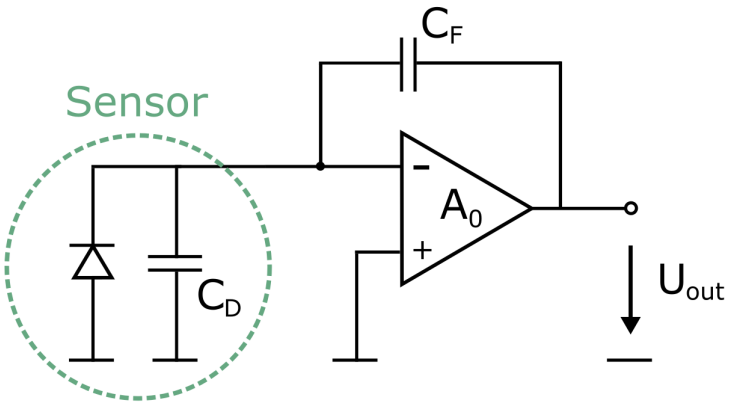


Figure 2.2: Principle configuration of a charge sensitive amplifier.

For the reason that in a real amplifier the gain is a function of the frequency f, the pulse at the output of the CSA has a non-zero rise time τ_{CSA} [6]:

$$U(t) = \frac{Q_{in}}{C_F}\left(1 - e^{-t/\tau_{CSA}}\right)$$

with the input charge Q_{in} and $\tau_{CSA} \propto C_D/g_m$. C_D is the pixel capacitance and g_m the transconductance of the input transistor. Accordingly, the rise time increases with C_D. In order to ensure fast rise of the signal, it is of interest to keep C_D as small as possible. Another option would be to adjust g_m which is related to the drain current I_D and the gate-source voltage V_{GS} of the transistor [6]:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \propto \sqrt{I_D}$$

Therefore, one could increase the drain current I_D, which, however, goes hand in hand with higher power consumption.

2.3 Equivalent noise charge

The electronic components of a detector-CSA system produce noise that degrades the accuracy of the signal. There are three dominant noise sources [6, 7]:

1) There is noise parallel to the input transistor due to detector leakage current which is caused by statistical fluctuations of electrical charge (shot noise) .

2) At the input transistor, there is serial voltage noise rising as $1/f$ (flicker noise) for low frequencies.

3) Thermal noise caused by velocity fluctuations leads to serial voltage noise at the input transistor.

A parameter which combines the contributions of the noise sources is the total equivalent noise charge (ENC). It is defined as the input charge for which the signal to noise ratio (S/N) is equal to 1 [6]:

$$\mathrm{ENC}^2 = a_{\mathrm{shot}}\tau_{\mathrm{sh}} + a_{1/\mathrm{f}}C_{\mathrm{D}}^2 + a_{\mathrm{therm}}C_{\mathrm{D}}^2$$

with the time constant τ_{sh} of the pulse shaper. The pre-factors a_i summarize the quantities that describe the noise sources. While the first term (current noise) is independent of the pixel capacitance the last two scale with C_{D}^2. Furthermore, a_{therm} is inversely proportional to g_{m} [6]. Consequently it is also important to keep C_{D} small or g_{m} high when it comes to noise.

The requirement of low noise performance, good time resolution and low power consumption can not be satisfied independently. For given detector parameters, a faster rise time and less noise is associated with higher power consumption. Instead of increasing the power consumption, the most promising approach is to improve the sensor design in the first place.

In order to determine the pixel capacitance of hybrid pixel detectors, a dedicated chip was developed. In the following chapter, an introduction to the measurement method as well as the characterization of the so called PixCap65 chip is given.

CHAPTER 3

PixCap65-Chip

3.1 Functional principle of pixel capacitance measurement

There are several ways to measure the capacitance of pixel sensors. It is straightforward to use a LCR meter (inductance-capacitance-resistance meter), which allows a measurement accuracy of 5 fF [8]. In addition, simulation tools give a good estimation about the pixel capacitance. Another, more precise approach that only requires a DC current meter is the Charge-Based Capacitance Measurement (CBCM) which is originally proposed in [9].

A schematic representation of this method is shown in Fig. 3.1. As switch 1 is closed, the capacitor charges up to a given voltage V_{in}. After that, switch 1 opens and switch 0 closes so C_{D} is discharged to ground. This cycle repeats periodically with a given frequency f. In order to make sure that the two switches are never closed at the same time, they are driven by non-overlapping signals. This avoids short circuit current from V to ground [9]. The average value of the charging current I_{avg} can be measured.

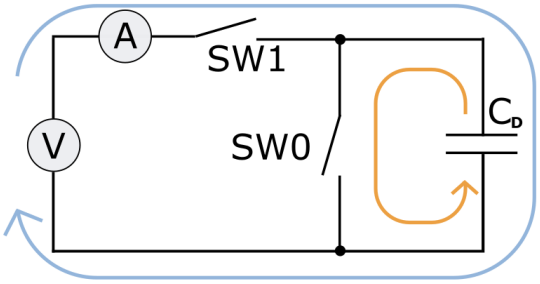


Figure 3.1: Equivalent circuit diagram describing the Charge-Based Capacitance Measurement method. Periodically switching of SW1 and SW0 generates a switching current charging and discharging C_{D}.

With a known switching frequency f and voltage V_{in} the capacitance of the sensor pixel is [10]:

$$C = \frac{Q}{V_{\text{in}}} = \frac{\int_0^T i(t)\,\mathrm{d}t}{V_{\text{in}}} = \frac{\frac{1}{T}\int_0^T i(t)\,\mathrm{d}t}{f \cdot V_{\text{in}}} = \frac{I_{\text{avg}}}{f \cdot V_{\text{in}}} \tag{3.1}$$

This formula provides the capacitance of one individual sensor pixel. In order to determine a statistically more representative value for this capacitance, a dedicated device that operates on the base of the CBCM method was developed. The so-called PixCap65 chip and the corresponding measurement setup is described in the following Section.

3.2 Specifications

The PixCap65 chip is a integrated circuit fabricated in a 65nm TSMC CMOS process [11]. A photograph can be seen in Fig. 3.2. The chip is designed for capacitance measurement of hybrid pixel sensors. In

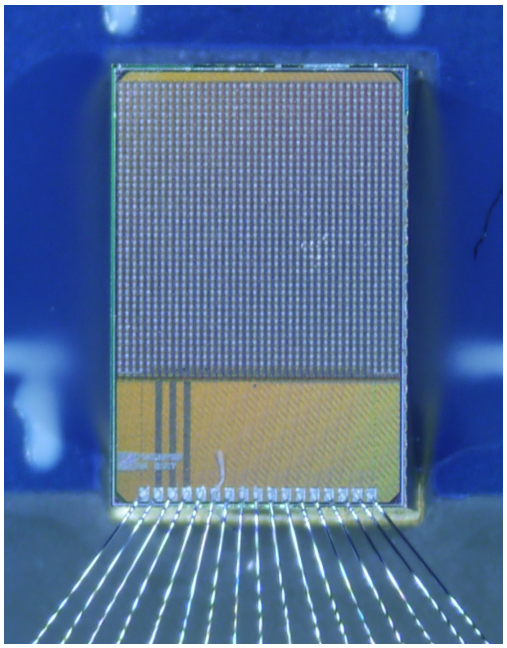


Figure 3.2: Bare PixCap65 chip assembly. Wire bonds are connecting the IO pads to the test PCB.

place of the readout chip, the PixCap65 is connected to the sensor with the same bump-bonding technique. It has a 40×40 pixel matrix with a $50 \times 50\,\mu m^2$ pitch. Next to the 40 rows, it has one extra pixel row with a few internal capacitors that can be used for testing or calibration. This row is outside of the matrix and will not be bump-bonded to the sensor. Since some of the pixels are not connected to the bump pads on top, the parasitic capacitance of the bare switch circuit can be extracted.

Each pixel has an extended switch logic based on the functional principle explained in Section 3.1. The pixel switches are implemented using two PMOS and two NMOS transistors. For the total pixel capacitance measurement one PMOS and NMOS transistor would be sufficient. However, for more advanced measurements like the inter-pixel measurement (see Section 5), two additional transistors are required. The switches are driven by four global clock nets (CLK0, CLK1, CLK2, CLK3) that can be individually programmed. A 6 bit pixel shift register enables the clock lines (CLK_EN[3:0]) and the static bias (SEL[1:0]). The corresponding block diagram is shown in Fig. 3.3.

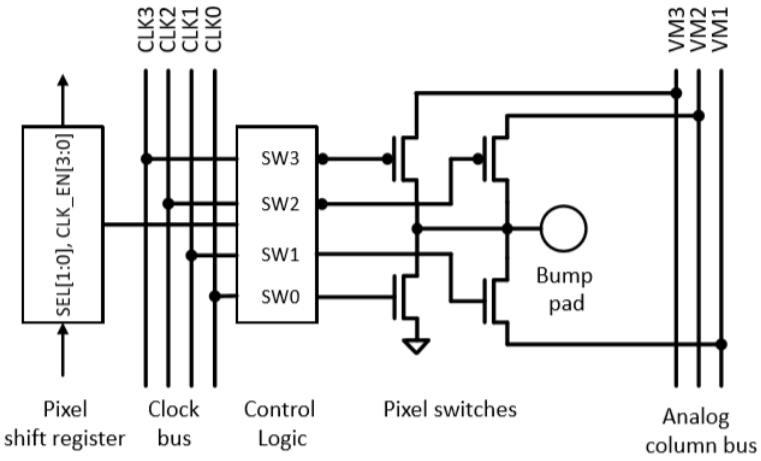


Figure 3.3: Pixel cell block diagram of the PixCap65 chip [12]. Each pixel cell is connected to a pixel cell on the sensor via a bump (pad).

3.3 Measurement setup

The PixCap65 chip is connected to a custom PCB to allow powering and data communication. In addition, the sensor is wire-bonded to the same test PCB in order to provide the biasing voltage. The measurement setup is shown in Fig. 3.4.

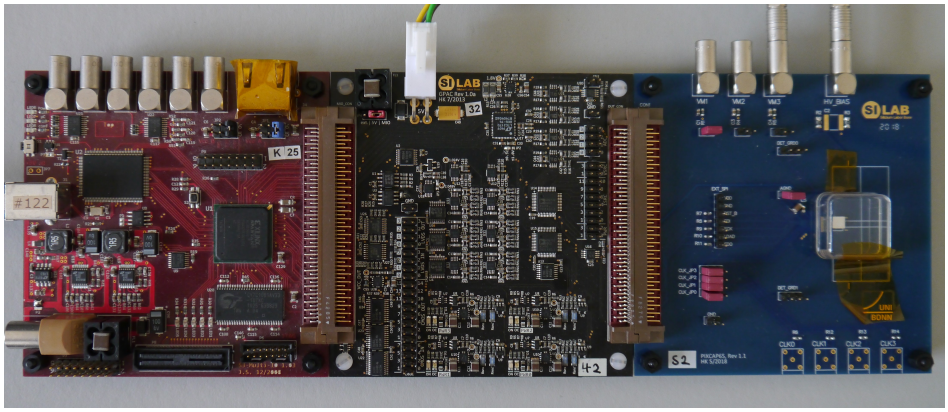


Figure 3.4: Setup for capacitance measurement including a FPGA Multi-IO board (left), GPAC board (middle) and the PixCap65 PCB (right).

Next to the PixCap65 PCB two additional circuit boards are needed. The FPGA Multi-IO board enables data exchange between computer and measuring chip and provides clock signals (see Fig. 3.5). The PixCap65 chip may be operated at a maximum voltage of 1.2 V. Since the Multi-IO operates at 3.3 V a GPAC board translates the voltage to the desired value of 1.2 V. Besides the level shifter, it includes several analogue help functions.

The measurements were performed with source measurement units (Keithley 2410) which are controlled by *Python* scripts based on the `basil` framework [13]. The host software for the PixCap65 chip is also available on [13]. The test script was individually adapted to the required measuring output.

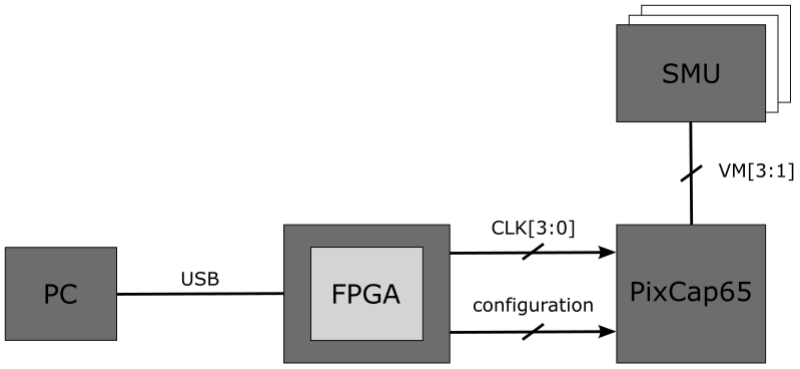


Figure 3.5: Schematic block diagram of the measurement setup. Up to three Source Measurement Units (SMU) can be connected.

Before capacitance measurements with sensors were performed, the operating parameters and systematic offsets such as parasitic capacitances were examined. The results of the measurements are discussed in Chapter 4.

CHAPTER 4

Capacitance measurement

4.1 Operating parameters

4.1.1 Switching frequency

As a first step, the influence of the switching frequency f on the capacitance measurement was evaluated. In order to do this, the average current I_{avg} of known test capacitors was measured for different switching frequencies. Fig. 4.1 shows the I/f-curves for three test capacitors with design values $C_7 = 60.14\,\text{fF}$, $C_8 = 119.39\,\text{fF}$ and $C_9 = 237.87\,\text{fF}$. The measurement shows that for C_7 and C_8 the average switching

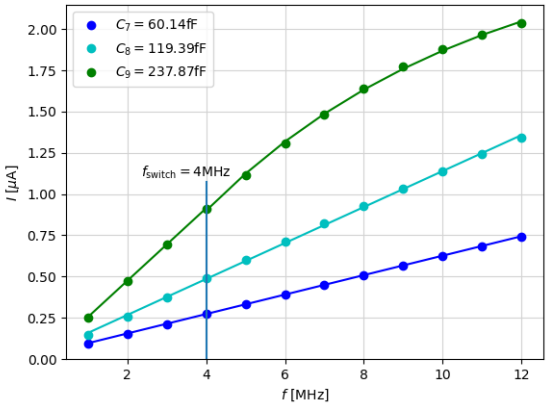


Figure 4.1: Frequency behaviour of test capacitors C_{7-9} in order to find the optimal switching frequency.

current increases linearly for frequencies up to $f = 12\,\text{MHz}$. For larger capacitors (C_9), however, a deviation from the linear behaviour can be detected around $f = 4\,\text{MHz}$. Because of the finite on-resistance of the switches, C_9 could not be fully charged before the discharging process starts. Although sensor pixel capacitances are expected to be smaller ($\sim 50\,\text{fF} - 100\,\text{fF}$) a frequency of $f = 4\,\text{MHz}$ is completely sufficient for further measurements.

4.1.2 Bias voltage of PixCap65 and sensor

In addition to the switching frequency, the formula for pixel capacitance calculation (3.1) requires a known input voltage V_{in} the capacitors are charged up to. For the sake of simplicity, PixCap65 was

operated at $V_{\text{in}} = 1\,\text{V}$ in the following measurements.

A pixel detector in the experiment is generally operated with a depleted sensor. As long as the sensor is not completely depleted, free charge carriers are present in the substrate. In order to ensure that only the switching current is measured, the capacitance behaviour of one pixel for different bias voltages V_{bias} was observed. The result can be seen in Fig. 4.2. The capacitance already drops significantly within a few volts. At this point, the sensor surface (i.e. the region between n^+ implantations and p^+ grid) is fully depleted. After that, it keeps slightly decreasing because the depletion zone grows further into the n^+- and the p^+-implantations. For an ideal parallel plate geometry, the pixel capacitance C scales with the width of the depletion region d with $C \propto 1/d$ and $d \propto \sqrt{V_{\text{bias}}}$ [6]. That means that $1/C^2$ increases linearly with higher bias voltages and remains constant as the depletion width has reached its maximum. Such a characteristic is shown in Fig. 4.3. The "surface" depletion voltage is about $(-8.22 \pm 0.02)\,\text{V}$. Since a real detector is operated with an over depleted sensor, for the following measurements the sensor is kept at $V_{\text{bias}} = -80\,\text{V}$.

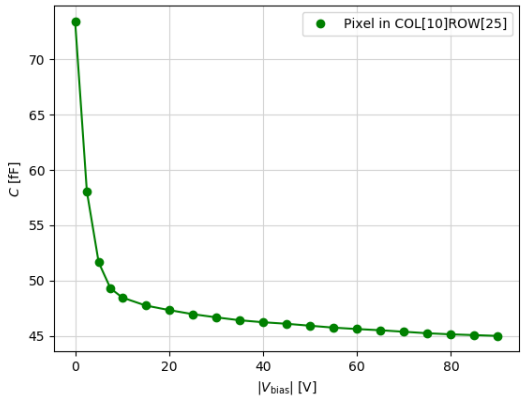


Figure 4.2: Total pixel capacitance as a function of the bias voltage of the sensor.

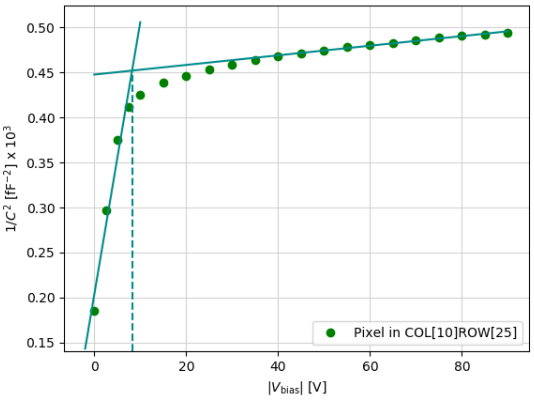


Figure 4.3: $1/C^2$ against the bias voltage of the sensor. The intersection point of the extrapolated linear fits provides the depletion voltage.

Even if the sensor is completely depleted leakage current caused by thermal generated electron and hole pairs is present. In general, this leakage current adds up to the switching current generated by the PixCap65 and the pixel capacitance could not be determined precisely. In order to avoid this problem, the capacitance was derived using the slope of a linear fit (see Fig. 4.1). In this way the leakage current which corresponds to the offset of the linear fit does not affect the capacitance calculation. Using the PixCap65 chip, this leakage current was measured for a bare chip sample and compared to the offset fit values, which showed that they coincide.

4.2 Parasitic capacitance

The PixCap65 chip itself is not free of parasitic capacitances. The measurement of the test rows of two chip assemblies provides detailed information about their contribution.

In column 27-34, there are pixel cells that have no connected bump pads on top. This allows the extraction of the bare switch logic capacitance. The average value of the corresponding test row pixels of two assemblies is:

$$C_{\text{switch}} = (4.43 \pm 0.01)\,\text{fF}$$

This value is worth knowing in connection with chip design but has no practical use in the proceeding analysis.

4.2.1 Bare chip

In order to determine the bare chip capacitance, a measurement without any bumps and connected sensor was performed. A 2D map of the pixel matrix and the corresponding histogram are shown in Fig. 4.4 and 4.5.

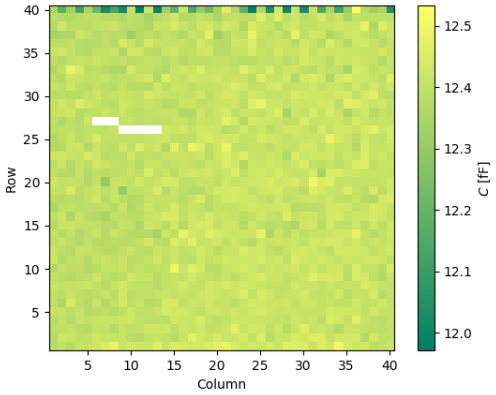


Figure 4.4: 2D map of the parasitic pixel capacitance of a bare PixCap65 sample 2. The values are evenly distributed over the hole chip.

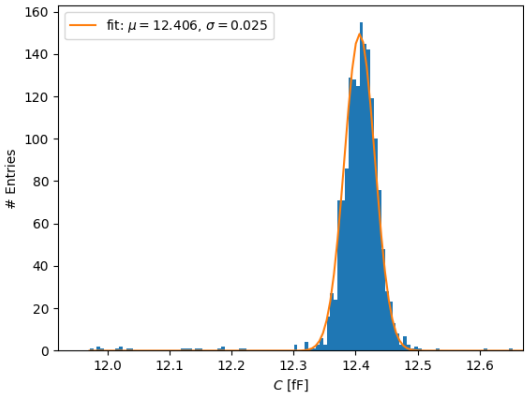


Figure 4.5: Pixel capacitance distribution of sample 2. The peak position is fitted with a Gaussian function.

A few pixels in this sample were non-functional so for the sake of clarity they were masked. In the top row, pixels with lower capacitance occur. This is caused by non-regular distribution of additional filling elements which are necessary for the manufacturing process of the chip. The capacitance of the remaining pixels is evenly distributed on the chip. A Gaussian fit [1] of the corresponding histogram yields a parasitic pixel capacitance of the bare chip of:

$$C_{\text{par}} = (12.406 \pm 0.025)\,\text{fF}$$

The error corresponds to the standard deviation of the Gaussian distribution. This value is composed of the bare switch logic and the connected bump pad capacitance, so that the latter can be extracted. Its contribution is (7.98 ± 0.03) fF.

With another sample of this configuration, a possible correlation of the chip layouts due to the manufacturing process was examined. Therefore, the capacitance of the second bare PixCap65 chip was measured and plotted against the capacitance of the other chip. The result can be seen in Fig. 4.6.

[1] The following fit function was used: $f(x\,|\,A,\mu,\sigma) = A \cdot \mathrm{e}^{-\frac{(x-\mu)^2}{2\sigma^2}}$. The fit parameters are the amplitude A, the average peak position μ and the standard deviation σ.

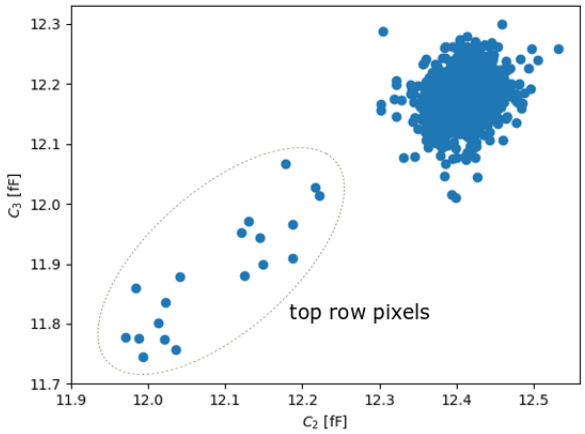


Figure 4.6: Correlation plot of pixel capacitances of two PixCap65 chip assemblies without bump connection.

For this plot, the non-functional pixels of both chips were not considered. Apart from the top row pixels, there is no correlation between the two layouts and the pixel capacitance is rather randomly distributed.

4.2.2 Chip with bumps

In addition to the parasitic capacitance of the bare chip, the bumps also make a contribution. In order to determine it more precisely, a measurement of two PixCap65 chip assemblies with bumps was performed. The result of sample 4 is shown in Fig. 4.7 and 4.8.

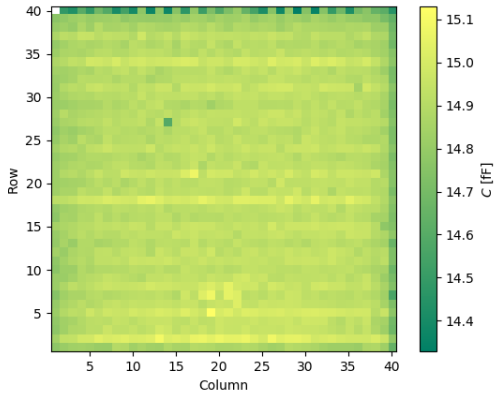


Figure 4.7: 2D map of the parasitic pixel capacitance of a PixCap65 sample 4 with bumps on top.

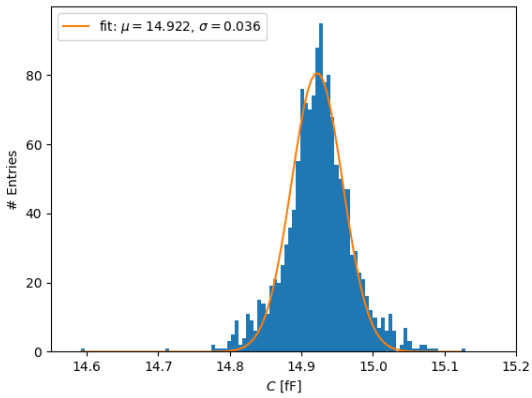


Figure 4.8: Pixel capacitance distribution of sample 4. The peak position is fitted with a Gaussian function. Top row and edge pixels are excluded from the fit.

As already seen in Fig. 4.4, the filling pattern around the top row are clearly noticeable in the capacitance. Besides to the top row pixels, the edges of the chip also have lower capacitance. A pixel located at the edge has less neighbours compared to a pixel inside the matrix. Hence, the capacitance of the corresponding pixels is smaller.

From a Gaussian fit a parasitic pixel capacitance of a bare chip with bumps of

$$C_{\text{par+bump}} = (14.922 \pm 0.036)\,\text{fF}$$

could be extracted. By subtracting the two measurements from each other, the bump capacitance yields to:

$$C_{\text{bump}} = C_{\text{par+bump}} - C_{\text{par}} = (2.52 \pm 0.04)\,\text{fF}$$

Furthermore, a second sample was measured to examine a possible correlation. The result is shown in Fig. 4.9. The top row and edge pixels are not included.

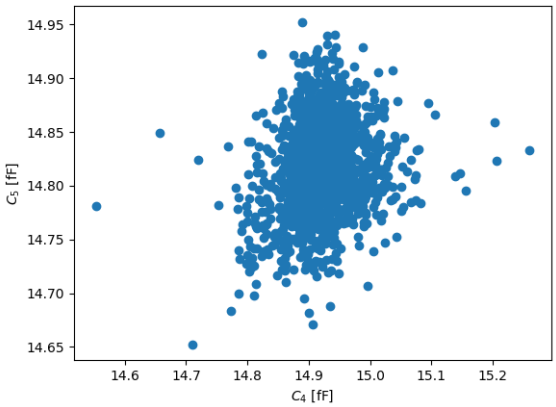


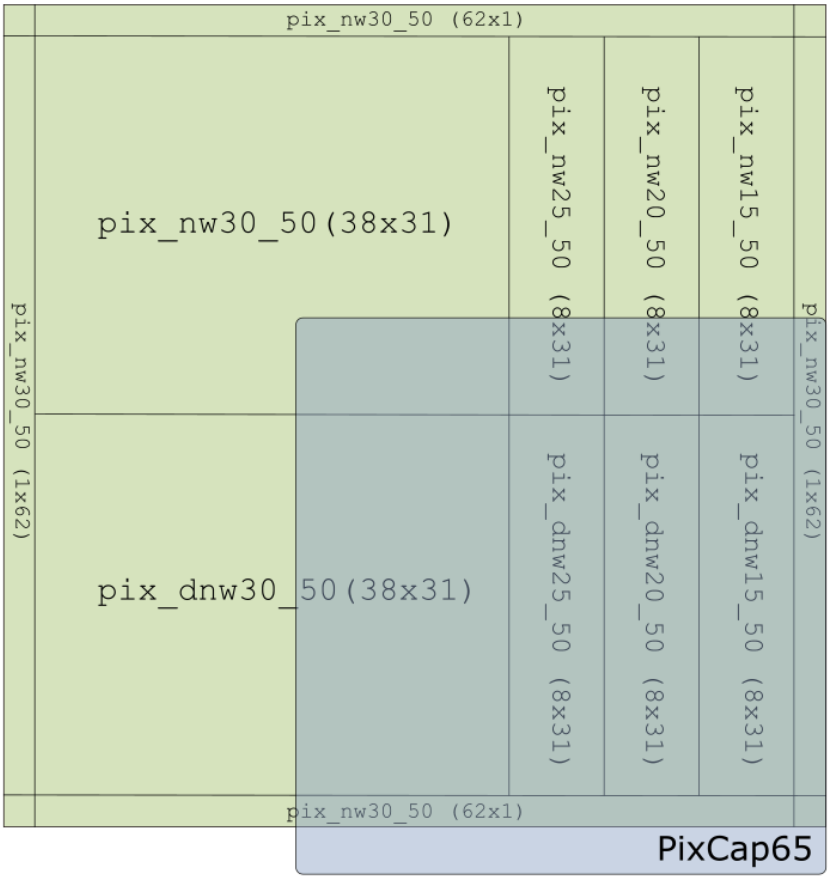
Figure 4.9: Correlation plot of pixel capacitances of two PixCap65 chip assemblies with bumps on top. The top row as well as the edge pixels are not considered.

A huge amount of the pixel values is concentrated in one area. According to the result from Subsection 4.2.1, one would not speak of a correlation here either.

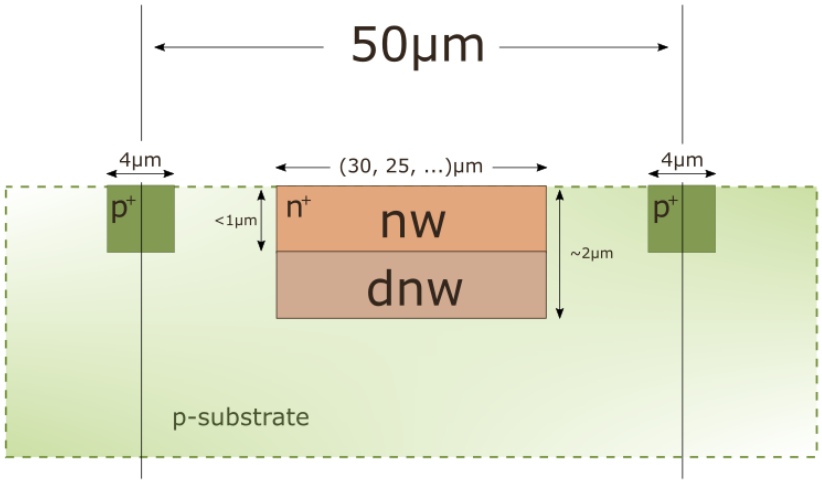
4.3 Capacitance of a silicon planar sensor

The parasitic contributions of the PixCap65 chip itself was determined so that a measurement of a biased sensor could be made. Therefore, the PixCap65 chip is connected to the sensor with the same bump-bonding technique as the front-end chip. PixCap65 and the sensor need to have the same pixel geometry (length and width).

For the measurements two sensor samples (S2 and S3) were under investigation. They are test samples (n^+ on n type) that have different implantation regions in order to get more extensive information on the capacitance behaviour of different pixel geometries. They have a 64×64 matrix with a $50\,\mu\text{m} \times 50\,\mu\text{m}$ pitch. The thickness of sample 2 is $100\,\mu\text{m}$ and for sample 3 $200\,\mu\text{m}$. The corresponding layout and a cross section of a sensor pixel can be seen in Fig. 4.10(a) and 4.10(b).



(a) Layout of the measured sensor. The PixCap65 chip is bump-bonded on the lower right corner.



(b) Cross section of the depleted sensor. Width and depth of the n^+-implantations are varied on the measured sensor.

Figure 4.10: The different implantation areas are denoted as e.g "`pix_nw30_50(38x31)`". "`nw`" refers to the implantation depth and "`30`" characterizes the width of the pixel. Additionally, the pitch parameters (50 µm × 50 µm pitch) and number of corresponding pixels (in brackets) are given.

The width of the pixels (n^+ type implantations) is varied between 15 µm and 30 µm. Additionally, there are different implantation depths included. The n-well (nw) implantations have a depth of less than 1 µm as the deep n-well (dnw) regions refer to a depth of about 2 µm. The n^+ regions are separated by p^+ implantations (p-stop) that shield the pixels from an ohmic short connection [6].
Since the chip is slightly smaller than the sensor, it was placed at the lower right corner of the sensor.

4.3.1 Total pixel capacitance

A 2D map of the uncorrected total pixel capacitance of sensor sample 2 is shown in Fig. 4.11.

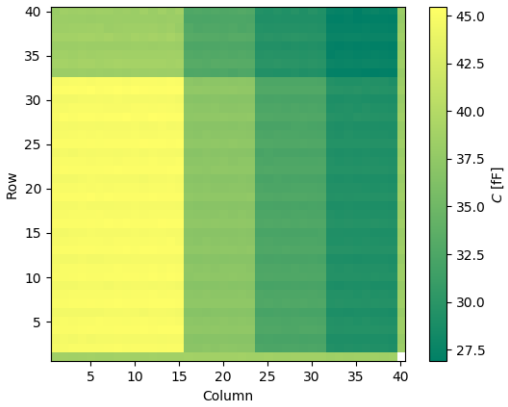


Figure 4.11: Uncorrected 2D map of the sensor pixel capacitance of sample 2. The pixel at the lower right corner is connected to a wire bond test pad and is masked.

The different implanted areas can be clearly distinguished from each other. Even the single row implantations are visible. The pixel in the lower right corner is connected to a wire bond test pad which leads to a much higher capacitance. For the following analysis this pixel was neglected.

The sharp transitions indicate that the capacitance is dominated by the n^+ to p^+-implants. If the pixel-to-pixel capacitance was the dominating one, the transitions would be more blurred. For example, having a closer look at the `dnw30_50` to `dnw25_50` boundary, the latter would contain more yellow shares and vice versa.

This is in good agreement with the result from Fig. 4.13. In this plot, the edge (to the `nw30_50` implantations) and inner pixels (see Fig. 4.12) of the `dnw15_50` implantation area are displayed separately. The capacitance of the edge pixels is not concentrated on one value but evenly distributed over the whole range.

Although these findings indicate no dependence on neighbouring implantation areas, analysis with a higher amount of edge pixels should be made.

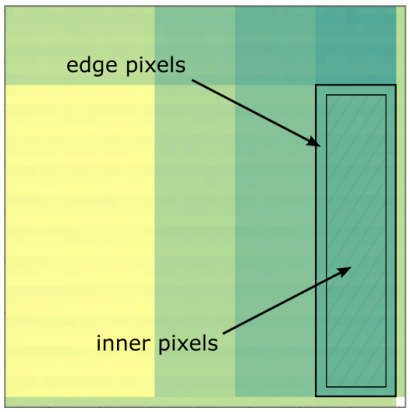


Figure 4.12: Inner and edge pixels of the dnw15_50 implantation region. Edge pixels are pixels that have neighbours with different implantation parameters.

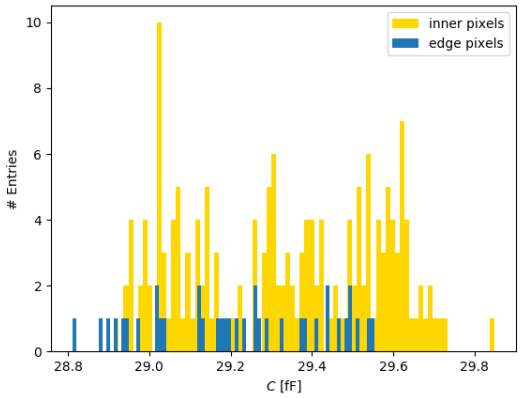


Figure 4.13: Pixel capacitance distribution of the dnw15_50 implantation area. The edge and inner pixels are displayed separately. Only the edge pixels to the nw30_50 implantation area are considered.

In the following, the individual implantation areas are described in detail. Starting with the dnw30_50 implanted area (column 1-15 and row 2-32), a separate 2D map is extracted (Fig. 4.14 and 4.15). In contrast to the continuous pixel capacitance distribution of the parasitic capacitance measurements (see e.g. Fig. 4.4), three distinct peaks separated by $\sim 0.3\,\mathrm{fF}$ can be seen. During the measurement the pixels were enabled horizontally which was considered to be a possible cause. However, vertical enable produced the same result. As a consequence, this effect is handled as a unknown systematic error most likely caused by the flip-chip process or the bump preparation of the sensor side.

In order to extract the total capacitance of this area the average value and the standard deviation was calculated. For the dnw30_50 area one finds $(44.94 \pm 0.22)\,\mathrm{fF}$. Since this result still contains the parasitic contributions of PixCap65 and bump, it needs to be corrected. By subtracting $C_{\mathrm{par+bumps}} = (14.922 \pm 0.036)\,\mathrm{fF}$ (see Subsection 4.2.2) a pixel capacitance of

$$C_{\mathtt{dnw30\_50}} = (30.018 \pm 0.223)\,\mathrm{fF}$$

can be obtained.

The same analysis was made for the remaining areas. Table 4.1 shows the resulting pixel capacitances of sample 2 and also of the additional sensor sample 3. For this table, the capacitances were rounded to the most significant decimal places.

Despite the alternating gradient in the pixel capacitance distribution, the findings do nevertheless represent the functionality of the method and the PixCap65 chip in a good way.

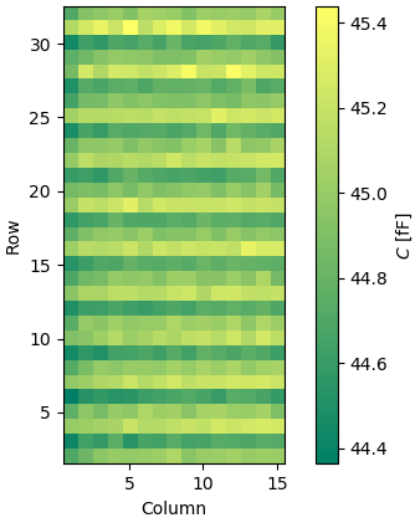


Figure 4.14: Extract of the `dnw30_50` implantation area. Three alternating capacitance bands are visible.

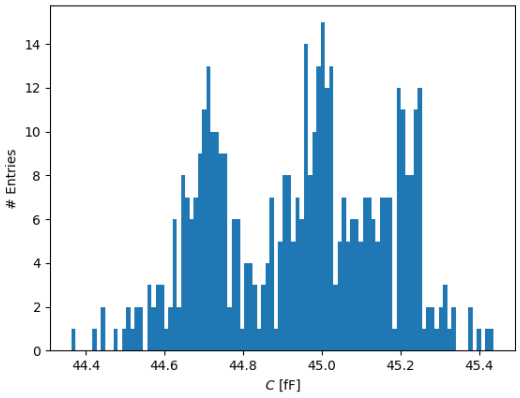


Figure 4.15: Pixel capacitance distribution of the `dnw30_50` area. The peaks correspond to the unknown pattern of the 2D map.

Table 4.1: Measured sensor pixel capacitance of different implantation types of two sensor samples. The right and lower edge were treated separately.

Implant	Column	Row	Sensor sample 2		Sensor sample 3	
			C_{avg} [fF]	C_{corr} [fF]	C_{avg} [fF]	C_{corr} [fF]
`nw15_50`	32-39	33-40	27.32 ± 0.26	12.40 ± 0.26	27.37 ± 0.21	12.45 ± 0.21
`nw20_50`	24-31	33-40	29.56 ± 0.26	14.64 ± 0.26	29.53 ± 0.20	14.61 ± 0.20
`nw25_50`	16-23	33-40	32.80 ± 0.27	17.88 ± 0.27	32.74 ± 0.20	17.82 ± 0.20
`nw30_50`	1-15	33-40	38.46 ± 0.27	23.54 ± 0.27	38.31 ± 0.20	23.39 ± 0.20
`dnw15_50`	32-39	2-32	29.32 ± 0.23	14.40 ± 0.23	29.35 ± 0.23	14.43 ± 0.23
`dnw20_50`	24-31	2-32	32.48 ± 0.22	17.56 ± 0.22	32.45 ± 0.23	17.53 ± 0.23
`dnw25_50`	16-23	2-32	37.07 ± 0.22	22.15 ± 0.22	37.01 ± 0.22	22.09 ± 0.22
`dnw30_50`	1-15	2-32	44.94 ± 0.22	30.02 ± 0.22	44.87 ± 0.22	29.95 ± 0.22
`nw30_50`	1-40	1	38.22 ± 0.20	23.30 ± 0.20	38.11 ± 0.20	23.19 ± 0.20
`nw30_50`	40	1-40	38.64 ± 0.07	23.72 ± 0.08	38.41 ± 0.05	23.49 ± 0.06

Taking into account the measurement errors, the results of the two sensor samples are in good agreement with each other. Since the error of the parasitic capacitance is rather small compared to the error of the uncorrected capacitances, the standard deviation of C_{avg} is the dominating error of the corrected values. There are also no significant differences between the larger `nw30_50` area and the single row values. These measurements revealed that the sensor pixel capacitance increases with the width and depth of the pixel implantation as expected. For identical dimensions, the deep n-well have higher capacitance compared to nw-implantations.

The precision achieved is superior to that obtained by other methods (see [8]). Using the PixCap65 chip, the pixel sensor capacitances of various implantation types were measured with sub-femtofarad precision.

Remarkable is that these findings also show that the sensor thickness has no effect on the sensor pixel capacitance. Although sample 3 is twice as thick as sample 2, there is no significant difference. This is because the contribution of the pixel to backplane capacitance is negligible since the sensor thickness is large compared to the lateral isolation distances between the implantations.

Analogous to the previous section, the correlation between the two sensor samples was tested. In Fig. 4.16, all of the implantation regions are considered.

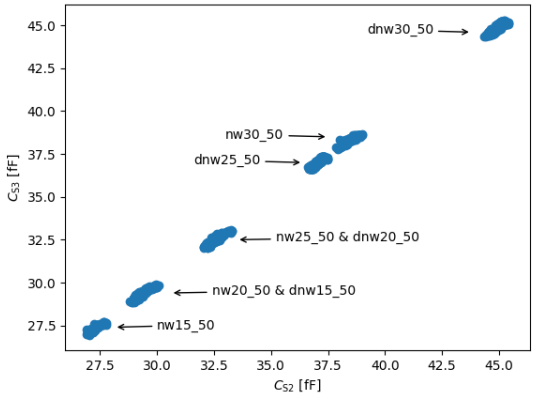


Figure 4.16: Correlation plot of the uncorrected pixel capacitance of two sensor samples. The different implantation areas are clearly differentiable.

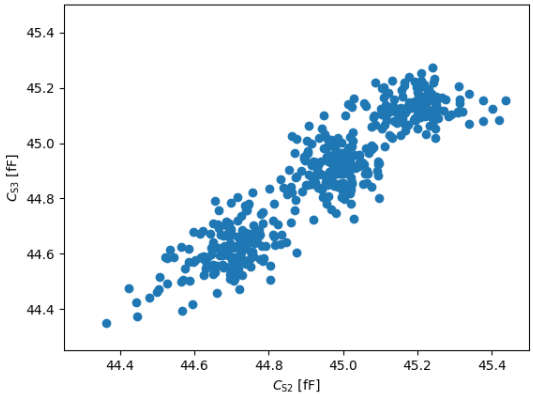


Figure 4.17: Extraction of the `dnw30_50` implantation pixels. Within one of the concentrated areas no correlation is observable.

The linearity within one of the implantation areas is due to the unknown alternating pattern which leads to three dominating capacitance values instead of one (see Fig. 4.15). Having a closer look at the `dnw30_50` implantation area (Fig. 4.17), especially at one of the "bands", no correlation is observed. However, without this effect only one big circle would be visible. Analysis of the other areas also confirmed that there is no significant correspondence between the sensor layouts.

CHAPTER 5

Summary and Outlook

In this thesis, the capacitance of silicon hybrid pixel detectors was under investigation. The pixel capacitance is in general not well known, but a significant parameter when it comes to design, noise performance, and signal processing of readout electronics. Hence, this work discussed the influence of pixel sensor capacitance on different readout components with regard to time resolution and electronic noise.

Motivated by the detector upgrade for the High-LHC [2], new sensor types are under development which need to be characterized. A method that allows the precise measurement of the pixel sensor capacitance, the Charge-Based Capacitance Measurement (CBCM), was presented. A dedicated device that operates on the basis of the CBCM method was designed. The so-called PixCap65 chip provides a powerful tool for pixel sensor capacitance measurement with unprecedented sub-femtofarad precision. Its characterization and the corresponding measurement setup was presented.

Main aspect of this thesis was the determination of the pixel sensor capacitance of two silicon sensor samples with different pixel implementations using the PixCap65 chip. Before that, operating parameters as the switching frequency and the sensor bias voltage were examined. Equally important was the determination of parasitic capacitances of the PixCap65 chip. In addition, possible layout correlations between chip samples due to the fabrication process were studied.

The measurement of the total pixel sensor capacitance of two identical sensor samples led to precise results with an absolute uncertainty in the range of 0.20 fF – 0.27 fF. As a consequence, comprehensive knowledge concerning different pixel implementations was obtained.

Taken together, a cutting-edge solution for the determination of silicon hybrid pixel capacitances was found. Both the functionality of the PixCap65 chip and the accuracy of the method were demonstrated.

The present study was only focussed on the total capacitance of a pixel sensor. However, the implementation of the PixCap65 chip allows the measurement of inter-pixel capacitances. Future work will concentrate on the inter-pixel capacitance measurement which will give insight into the contributions of the total pixel sensor capacitance.

The prospect of being able to measure capacitances in this order of magnitude serves as an impulse to extend the measurements on different sensor types such as diamond or 3D-sensors. Another interesting topic for future research is the influence of radiation on the pixel sensor capacitance.

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