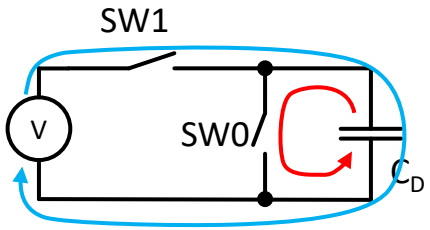
Pixel Sensor Capacitance Measurement Chip PixCap65

H. Krüger

Capacitance Measurement Method

- Charge based capacitance measurement

$$C_D = \frac{\overline{I_V}}{dV \cdot f_{SW}}$$

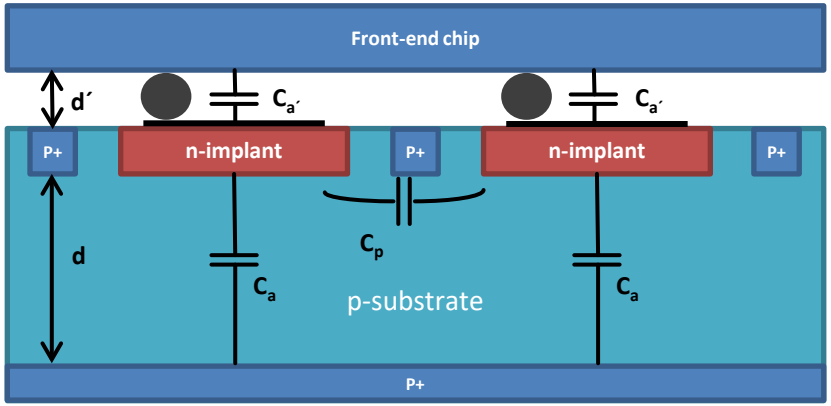


SW0 and SW1 driven with non-overlapping clocks

- Measurement principle originally proposed for precise measurement of on-chip parasitic capacitances (B. McGaughy, A Simple Method for On-Chip, Sub-Femto Farad Interconnect Capacitance Measurement, IEEE Electronic Device Letters, VOL. 18, NO. 1, Jan 1997)

Pixel Capacitance (Planar Sensor)

Total sensor capacitance $C_d = C_a + C_{a'} + \boldsymbol{C_p}$



- Capacitance to backplane $C_a \approx \varepsilon_r \frac{A}{d}$ (parallel plate capacitor)
- Capacitance to FE chip $C_{a'}$ (similar to C_a with different ε_r and d)
- **Capacitance to neighbor pixels $\boldsymbol{C_p}$ and/or p-stop implant** ($\propto$ perimeter length)
- Bump (to bump) capacitance

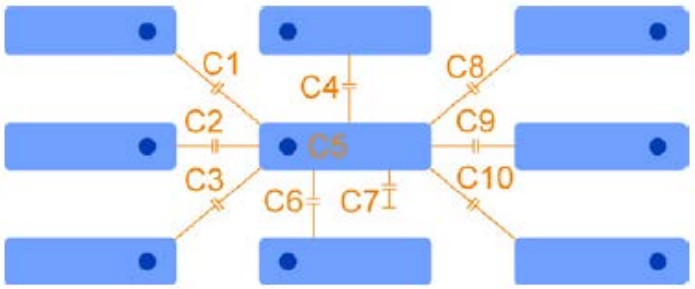
Recent Implementation

- Implementation for hybrid pixel sensor capacitance measurement
  - First “Pixcap” chip (2013), LF150nm CMOS technology, 250µm x 50µm pixel (FE-I4)

- Example: Measurement data for 250 x 50 µm^2 pixel total capacitance
  - Si planar sensor, 230µm thick: $C_d = (111.7 \pm 3.8) fF$
  - Diamond sensor, 750µm thick: $C_d = (21.4 \pm 0.1) fF$

- Measurement of inter-pixel capacitance:

Capacitance	C_{meas} (fF)	C_{sim} (fF)
C1	0.4	0.7
C2	0.9	1.1
C3	0.4	0.7
C4	5.1	7.1
C5	21.3	25.4
C6	5.1	7.1
C7	1.9	1.6
C8	0.3	0.7
C9	0.6	0.9
C10	0.3	0.5

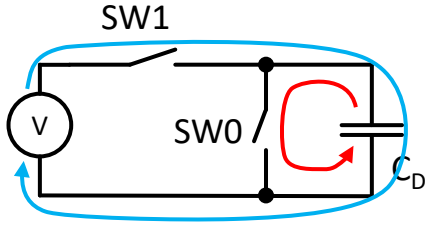


Measured capacitance values for a 250 x 50 µm^2 pixelated CVD Diamond sensor, 750µm thick

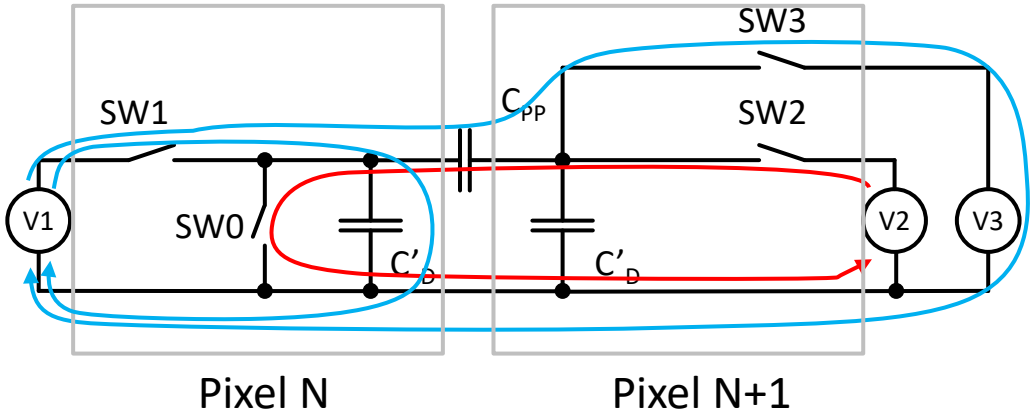
M. Havránek et al., Measurement of pixel sensor capacitances with sub-femtofarad precision, NIM A 714 (2013) 83-89

Pixel Switch Configuration

- Total pixel capacitance measurement (standard switch configuration)
  - Charge phase: SW1 closed, SW0 open
  - Discharge phase : SW1 open, SW0 closed
  - $\mathbf{I_V \rightarrow C_D}$

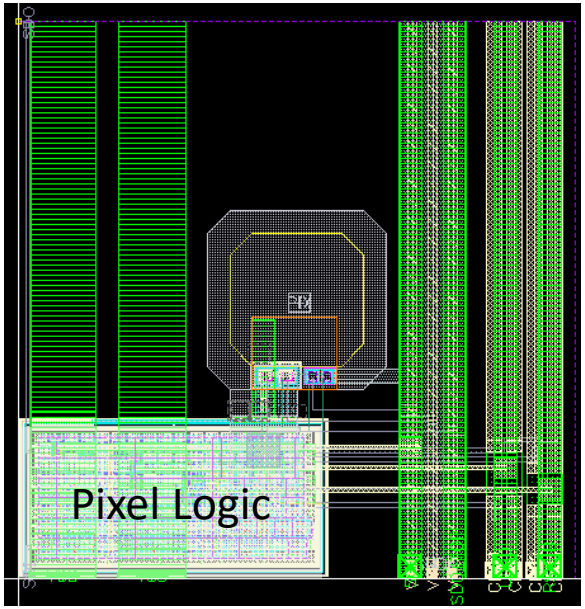


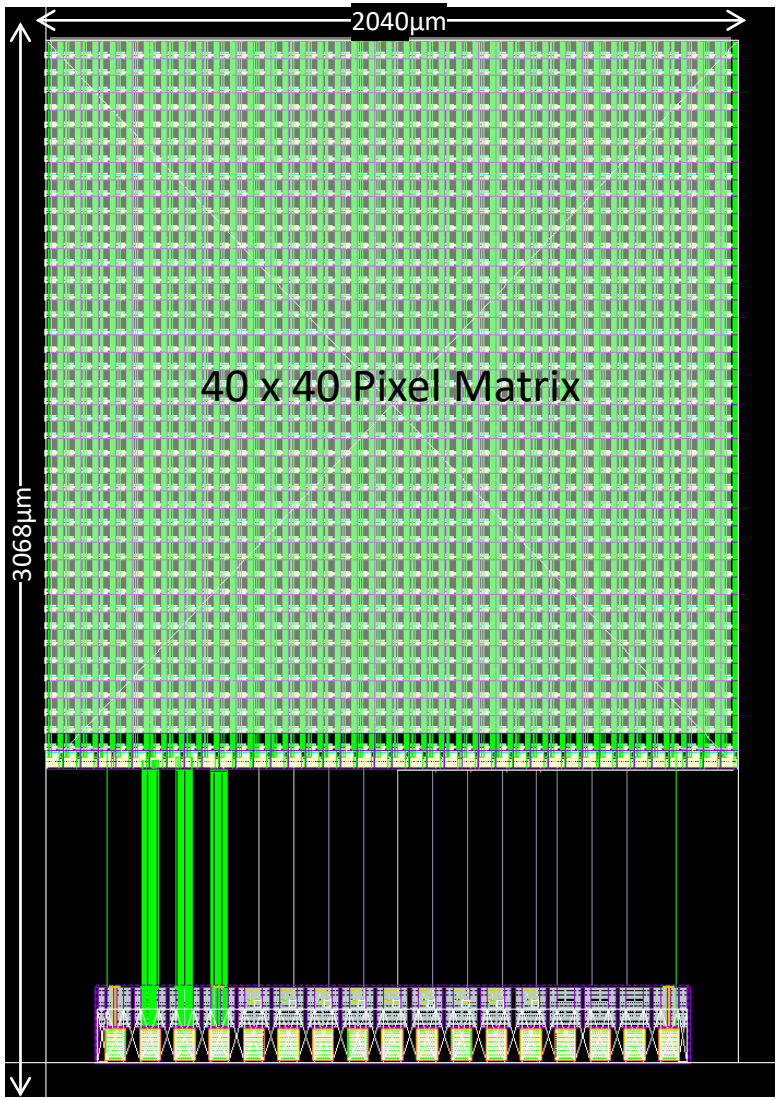
- Inter-pixel capacitance measurement (additional circuit)
  - V1 = V2 = V3
  - Charge phase: SW1 & SW3 closed, SW0 & SW2 open
  - Discharge phase: SW1 & SW3 open, SW0 & SW2 closed
  - $\mathbf{I_{V1} \rightarrow C'_D + C_{PP}}$
  - $\mathbf{I_{V2}, I_{V3} \rightarrow C_{PP}}$



PixCap65 Specifications

- 40 x 40 pixel matrix, 50µm pitch
- In-pixel + intra-pixel capacitance measurement
- Extra pixel row w/o bumps for test & calibration capacitors
- Column-wise enable for reduction of switch leakage





Pixel Cell Block Diagram

- Individual programmable clock and voltage routing per pixel:
  - Four switches per pixel: two PMOS plus two NMOS
  - Four global clock nets: CLK0, CLK1, CLK2, CLK3
  - Three global voltage lines: VM1, VM2, VM3 (VM0 = GND)
- Pixel configuration shift register
  - Enable clock lines CLK_EN[3:0]
  - Static bias SEL[1:0]

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SEL[1:0] Static bias
0 0          GND
0 1          VM1
1 0          VM2
1 1          VM3

CLK_EN[3:0]  Function
0 0 0 0      No clock enabled, static bias active
x x x 1      CLK0 enabled (NMOS to GND), static bias off
x x 1 x      CLK1 enabled (NMOS to VM1), static bias off
x 1 x x      CLK2 enabled (PMOS to VM2), static bias off
1 x x x      CLK3 enabled (PMOS to VM3), static bias off
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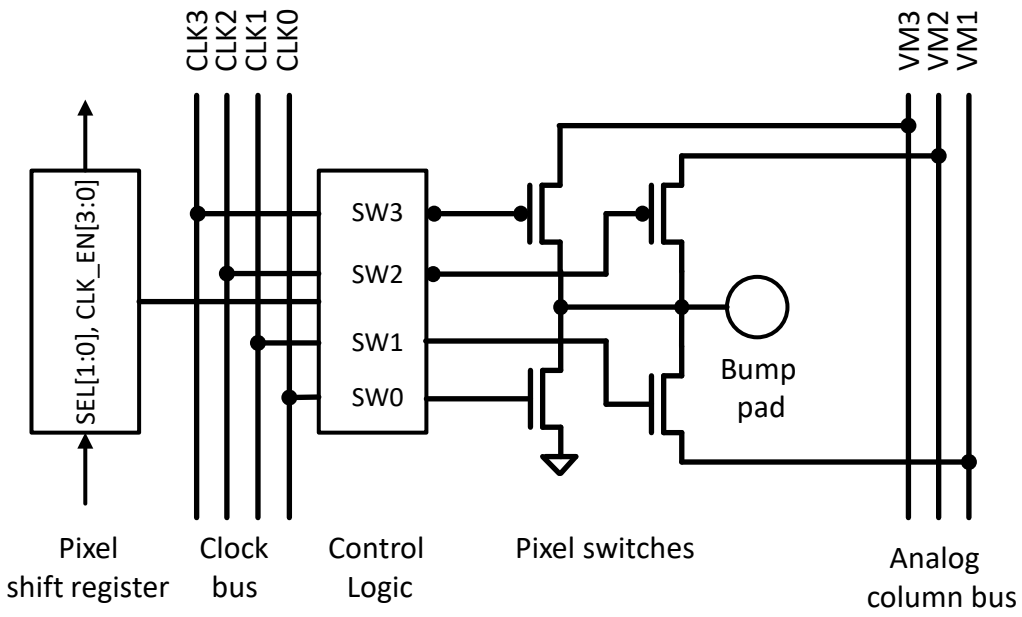
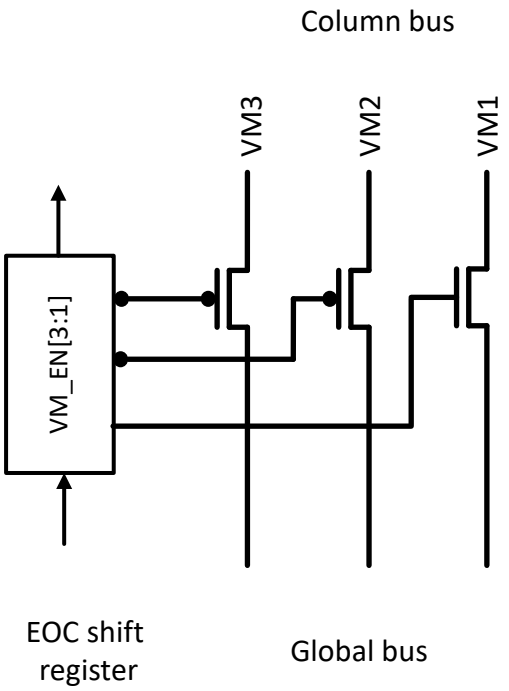


EOC Block Diagram

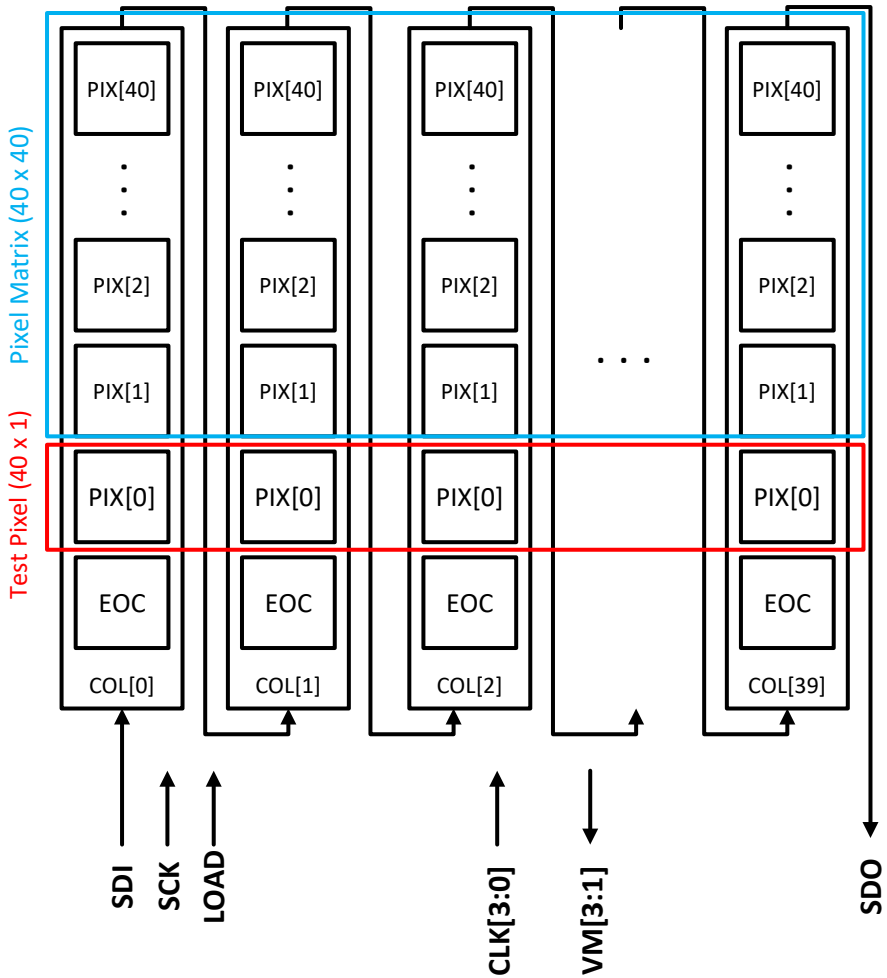
- Control of the column voltage lines: VM1, VM2, VM3
- Three switches per column to connect the VM lines to the corresponding global bus line
- Shift register configuration:
  - Enable lines VM_EN[3:1]



Chip Block Diagram

- Topology
  - 40 columns
    - EOC cell + 41 pixel cells
  - Four global clock lines
  - Three global bias lines

- Configuration via SPI
  - Chip shift register (9960 bit): COL[39:0]
    - Column shift register (249 bit): COL=(PIX[40:0], EOC)
      - Pixel shift register (6 bit): PIX=(SEL[1:0], CLK_EN[3:0])
      - EOC shift register (3 bit): EOC=VM_EN[3:1]
  - MSB shifts in first
    - (COL[0].VM_EN[1] ……..COL[39].PIX[40].SEL[1]) →



PixCap65 IO Pads

Nr.	Name	Type	Description
1	DET_GRD0	Passive	Connection to four bias bumps on the left-hand side (column 0-3)
2	VDD	Power	1.2V power supply for logic and NW/DNW bias
3	VSS	Ground	Ground rail for logic, local substrate bias
4	GNDA	Ground	Ground for NMOS switch 0, global substrate
5	RST_B	CMOS in	Reset for pixel configuration shift register
6	SDI	CMOS in	Serial data in
7	SCK	CMOS in	Shift clock
8	LOAD	CMOS in	Load strobe for pixel configuration
9	SDO	CMOS out	Serial data out
10	CLK0	CMOS in	Clock 0 input (→ NMOS switch to GNDA)
11	CLK1	CMOS in	Clock 1 input (→ NMOS switch to VM1)
12	CLK2	CMOS in	Clock 2 input (→ PMOS switch to VM2)
13	CLK3	CMOS in	Clock 3 input (→ PMOS switch to VM3)
14	VM1	Passive	VM1 line, return for NMOS switch
15	VM2	Passive	VM2 line, connection to PMOS switch
16	VM3	Passive	VM3 line, connection to PMOS switch
17	DET_GRD1	Passive	Connection to four bias bumps on the right-hand side (column 36-39)

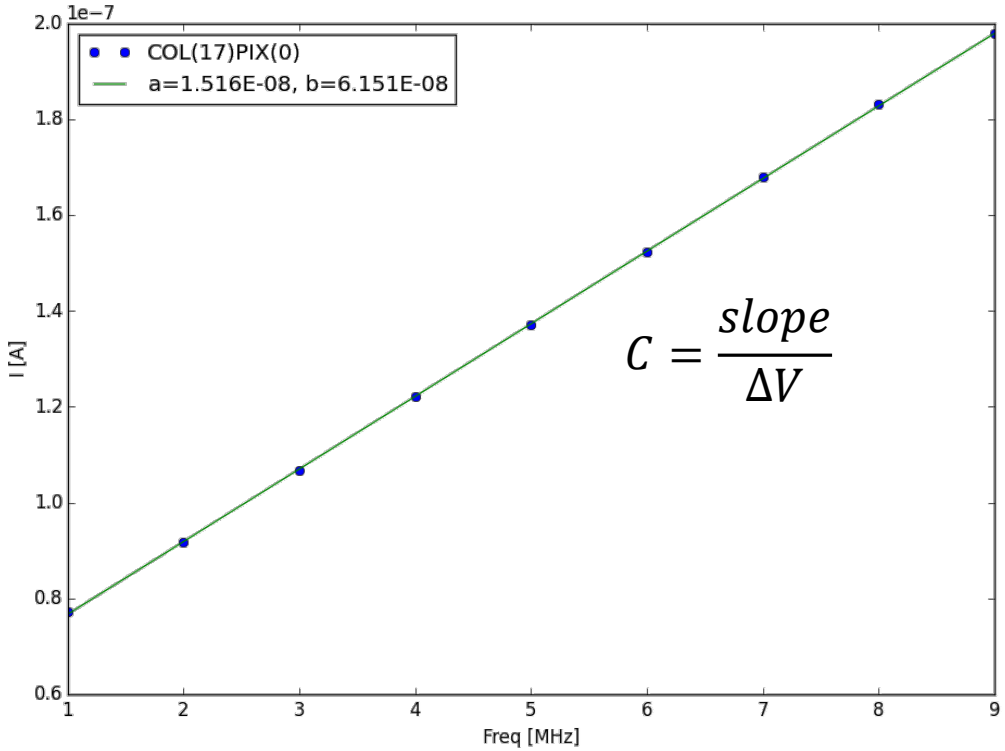
Internal Test Capacitors

- The bump bond matrix is connected to COL[39:0]PIX[40:1]
- A few cells COL[x]PIX[**0**] **outside** of the pixel matrix are connected to test capacitors:

COL	Capacitor	Design Value [fF]	Comment
5	“CRTMOM 1”	15.41	CRTMOM, M3-M5, nv=16, nh=16, w=100n, sp=100n
6	“CRTMOM 2”	30.33	CRTMOM, M3-M5, nv=32, nh=16, w=100n, sp=100n
7	“CRTMOM 4”	60.14	CRTMOM, M3-M5, nv=32, nh=32, w=100n, sp=100n
8	“CRTMOM 8”	119.39	CRTMOM, M3-M5, nv=64, nh=32, w=100n, sp=100n
9	“CRTMOM 16”	237.87	CRTMOM, M3-M5, nv=64, nh=64, w=100n, sp=100n
10	“CRTMOM 1 x 2”	30.82	Two “CRTMOM 1” parallel
11	“CRTMOM 1 x 4”	61.64	Four “CRTMOM 1” parallel
12	“CRTMOM 1 x 8”	123.28	Eight “CRTMOM 1” parallel
13	“CF AFE_TO_1”	2.51	Torino AFE Cf, large value
14	“CF AFE_TO_2”	1.63	Torino AFE Cf, small value (two 3.2fF cap. in series)
15	“CF AFE_BGPV”	5.51	Bergamo/Pavia AFE Cf
17 - 26	“CINJ”	8.53	Injection capacitor, CRTMOM, M2-M4, nv=22, nh=6
0 - 4 27 – 39	No connection	-	Not connected cells, to measure parasitic capacitance, 0-4 and 35-39 have not connected bump pads on top

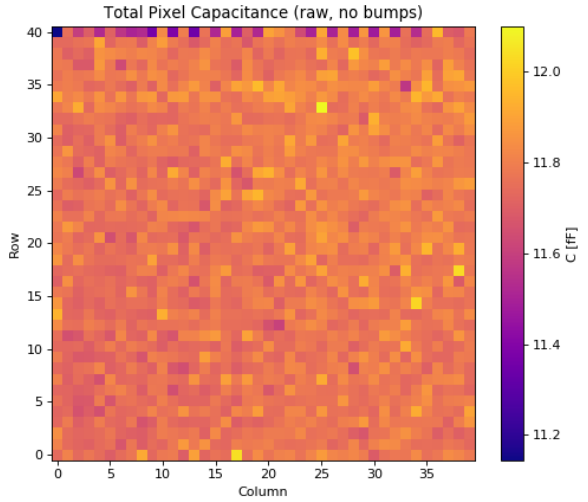
Example Measurement

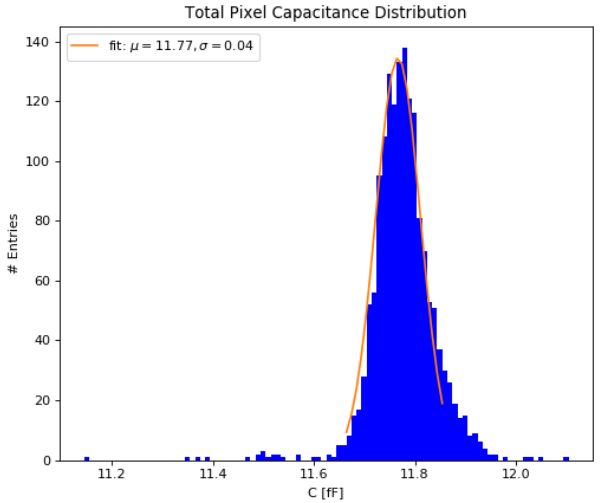
- Internal test capacitor: CINJ (RD53A injection capacitor)
- Design value: 8.533 fF (w/o parasitic extraction)
- Measured value: 8.318 fF



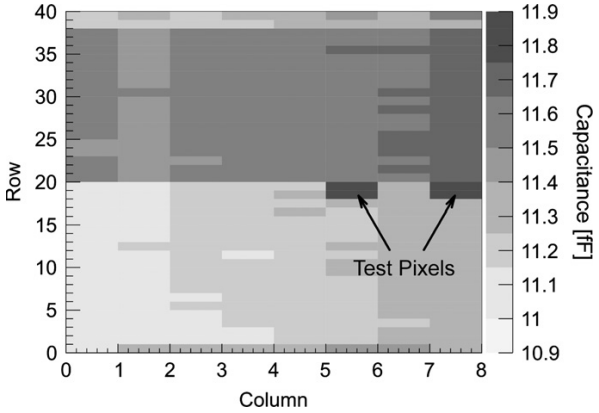
Bare Chip Pixel Capacitance

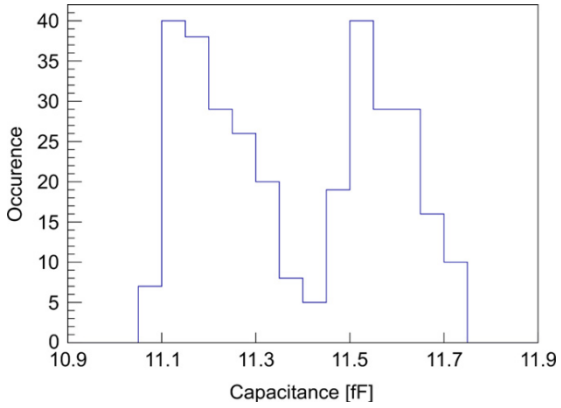
- Bump pad + parasitic capacitance of the pixel switches: ~11.77 fF





- Comparison to PixCap(FE-I4):





M. Havránek et al./NuclearInstrumentsandMethodsinPhysicsResearchA714(2013)83–89

PixCap65 Pixel Cell

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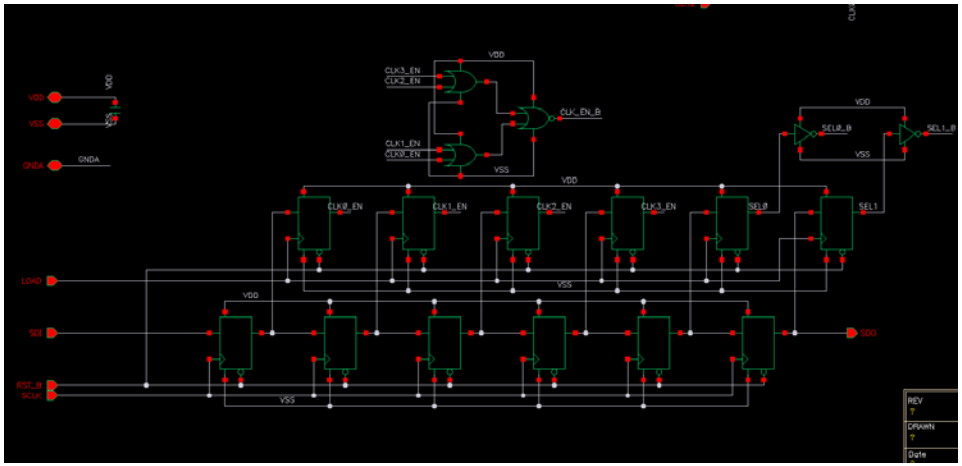
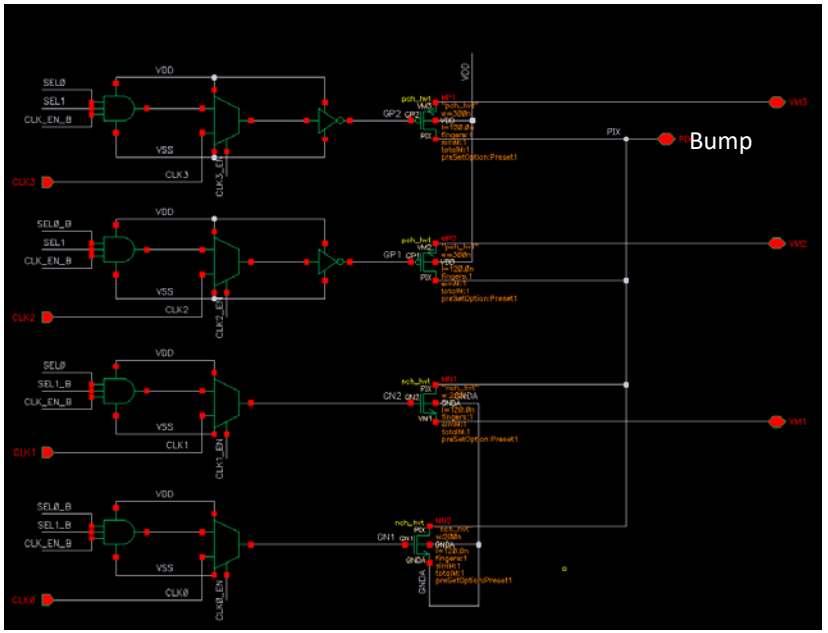


Pixel shift register



Pixel switches with control

PixCap65 EOC Cell

- Control of the three global voltage lines: VM1, VM2, VM3
- Three switches per column to connect the VM lines to the corresponding IO pads
- Shift register configuration:
  - Enable lines VM_EN[3:1]