

## Precision measurement of pixel sensor capacitance

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## Precision measurement of pixel sensor capacitance

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**ABSTRACT:** The capacitance of the charge collection node of a sensor system is an important parameter for the design of the analog front-end electronics. The analog front-end of high-granularity sensors like for example hybrid pixel detectors need to be optimized for timing resolution, power consumption, and electronics noise — parameters which all depend on the pixel capacitance. Current pixel detector developments for the HL-LHC upgrade typically use silicon sensors with a pixel size in the order of  $50 \times 50 \mu\text{m}^2$  which have a pixel capacitance of several tens of fF, depending on the sensor geometry. We have developed a dedicated integrated circuit to be bump-bonded to a pixel sensor, which enables a precise pixel capacitance measurement by using the charge-based capacitance measurement method. In this paper, we will describe the measurement method and the implementation of the capacitance measurement chip (Pixcap65) and show measurement results of a planar pixel sensor whose pixel capacitance is influenced by variations of the implant geometry.

**KEYWORDS:** Front-end electronics for detector readout; Hybrid detectors; Electronic detector readout concepts (solid-state); Analogue electronic circuits

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## Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
<b>2</b>	<b>Measurement method</b>	<b>3</b>
<b>3</b>	<b>Implementation of the Pixcap65 chip</b>	<b>3</b>
<b>4</b>	<b>Design of the test sensor device</b>	<b>5</b>
<b>5</b>	<b>Measurement results</b>	<b>7</b>
5.1	Measurement errors	7
5.2	Bare chip	9
5.3	Pixel sensor measurements	10
<b>6</b>	<b>Summary</b>	<b>12</b>

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## 1 Introduction

For the Large Hadron Collider (LHC) a luminosity upgrade from  $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  to  $10^{35} \text{ cm}^{-2} \text{ s}^{-1}$  (HL-LHC) is planned for 2026 [1]. This increase in luminosity requires an upgrade of the innermost pixel tracking layers since they will be exposed to ten times higher hit rates and radiation levels. To meet this challenge, a new generation of pixel sensors and read-out chips is being developed [2]. The increase in hit rate demands smaller pixels to cope with the high track densities. At the same time thermal and mechanical constraints limit the allowed power consumption for the pixel layers. Therefore on-chip analog and digital signal processing of the hit data has to be carefully optimized to meet all performance specifications, including the power budget. The sensor capacitance influences the performance of the analog front-end as follows.

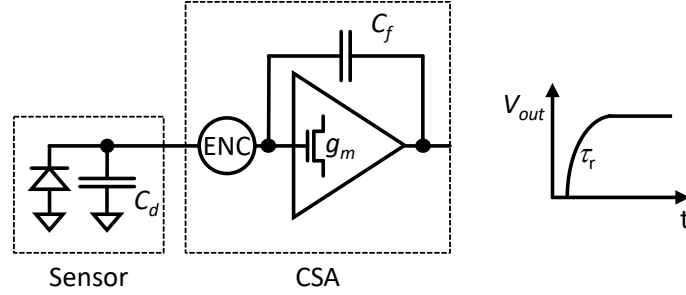
The circuit analysis of a typical charge sensitive amplifier (CSA, see figure 1) shows that the pixel capacitance  $C_d$ , which loads the input of the CSA, influences the analog performance of a detector system in terms of noise and timing behavior. Both the signal rise-time  $\tau_r$  and the series noise component  $ENC_{\text{ser}}$  (the equivalent input referred noise charge caused by the flicker noise and thermal noise of the input device [4]) are proportional to the capacitance  $C_d$ . Also the charge collection efficiency  $CCE$  depends on  $C_d$  [5]. These dependencies are expressed by the following relations:

$$\tau_r \propto \frac{C_d}{C_f \cdot g_m} \quad (1.1)$$

$$ENC_{\text{ser}} \propto \frac{C_d}{\sqrt{g_m}} \quad (1.2)$$

$$CCE \approx \frac{C_f}{\frac{C_d}{A_0} + C_f} \quad (1.3)$$

with the feedback capacitance  $C_f$ , the input device transconductance  $g_m$ , and the DC gain of the pre-amplifier  $A_0$ . Equations (1.1) and (1.2) show that for a given performance parameter a change of  $C_d$  can be compensated by adapting  $g_m$ , which is proportional to the square root of the drain current  $I_d$  of the input device when operating in weak inversion, which is typical for analog front-end designs in pixel detectors. As changing  $g_m$  has a direct impact on the power consumption of the pre-amplifier, it is necessary to have a precise knowledge of the input capacitance  $C_d$  to be able to design an analog front-end with optimum performance and power efficiency.



**Figure 1.** Simplified equivalent circuit of a charge sensitive amplifier (CSA) connected to the n-side of a charge collecting diode of the sensor. The parasitic capacitance  $C_d$  at the input of the CSA is typically dominated by the junction capacitance of the charge collection electrode. Also shown are the input referred (series) noise source ENC and the output waveform with finite rise-time  $\tau_r$  in response to an ideal charge signal. The transconductance  $g_m$  of the CSA input device plays a central role in optimizing the noise and timing performance in the presence of the input capacitance  $C_d$ .

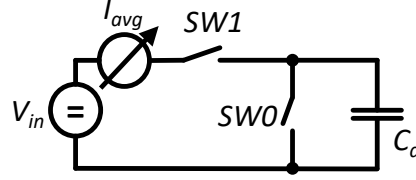
The capacitance of the sensor collection node depends on various parameters (implant geometry, isolation distances, doping density, etc.) which have to be optimized with respect to the charge collection efficiency — in particular after radiation damage — and the breakdown voltage which limits the maximum depletion bias. The discussion of these issues is beyond the scope of this publication. However, different collection node geometries will be briefly described in section 4.

A typical sensor pixel with the size of  $50 \times 50 \mu\text{m}^2$  has a capacitance in the order of a few tens of fF. Thus, a direct measurement, for example with an LCR meter, is challenging since the parasitic capacitance of the measurement connection usually an order of magnitude larger than the capacitance to be measured. Nevertheless, in [6] sensor pixel test structures have been characterized with a total measurement error of 5 fF using an LCR-meter, low parasitic capacitance probes, and a shielded probe station setup. However, one drawback of that approach is that such a setup requires dedicated sensor pixel test structures. In addition, only few pixels per structure (mostly only one) can be characterized that way. To overcome these limitations, we developed a dedicated integrated circuit (Pixcap65) that can be bump-bonded directly to any pixel sensor with a bump pitch of  $50 \times 50 \mu\text{m}^2$ . In particular, the pixel matrix can be of any size and its design does not need dedicated features to enable the capacitance measurement.

In section 2, we will introduce the measurement method and in section 3 we will explain how it is implemented in the Pixcap65 chip. The test sensor we used as a device under test is described in section 4 and finally the measurement results of the test pixel sensors bump-bonded to the Pixcap65 chip will be presented in section 5.

## 2 Measurement method

The pixel capacitance measurement implemented in the Pixcap65 chip makes use of the charge-based capacitance measurement method (CBCM) [3], which is schematically shown in figure 2.



**Figure 2.** Equivalent circuit diagram describing the charge-based capacitance measurement method. Periodic non-overlapping switching of SW1 and SW0 generates charge and discharge currents across the capacitance  $C_d$  while only the average charge current that flows from the voltage source  $V_{in}$  is measured. The relation between the average charge current, the switching frequency and the DC voltage facilitates the extraction of the capacitance value.

The basic measurement scheme consists of two switches SW0 and SW1, a constant voltage supply  $V$ , a DC current meter, and the capacitance to be measured. SW0 and SW1 are controlled by a non-overlapping clock sequence, which periodically charges the capacitance  $C_d$  to the voltage  $V_{in}$  (SW0 open, SW1 closed) and discharges to ground (SW0 closed, SW1 open). Since the charge and discharge currents have different paths, the average charge current  $I_{avg}$  can be measured separately with a DC current meter. With switching frequency  $f$  and voltage  $V_{in}$ , the capacitance value can be evaluated as:

$$C_d = \frac{Q}{V_{in}} = \frac{\int_0^T i(t) dt}{V_{in}} = \frac{\frac{1}{T} \int_0^T i(t) dt}{f \cdot V_{in}} = \frac{I_{avg}}{f \cdot V_{in}}. \quad (2.1)$$

Any additional parasitic current source (sensor leakage current, sub-threshold leakage of the switches) will cause an offset in the measurement. To avoid this systematic error, the capacitance is derived by measuring the current  $I_{avg}$  as a function of the switching frequency  $f$  and applying a linear fit to the measured data. The capacitance is then given by the slope of  $I_{avg}(f)$  divided by the applied voltage  $V_{in}$ :

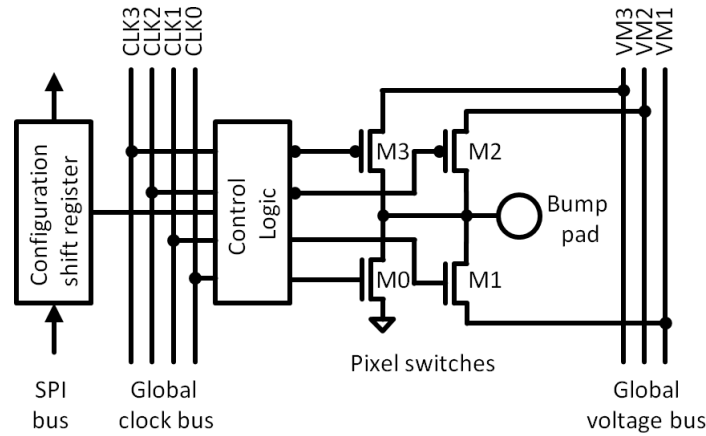
$$C_d = \frac{dI_{avg}(f)}{df} \cdot \frac{1}{V_{in}} \quad (2.2)$$

Other systematic errors could be introduced by the on-resistance  $R_{on}$  of the switches. Combined with the capacitance, the on-resistance introduces a first-order low-pass filter with a time constant  $\tau = R_{on} \cdot C_d$ , which leads to finite charge and discharge times. To minimize this error, the maximum switching frequency (i.e., the minimum pulse width of the non-overlapping clock) has to be limited to allow charge and discharge voltages across  $C_d$  to settle to the required precision. On the other hand, the switching frequency must not be too low in order to allow for a reasonable precision of the current measurement (see section 5 for a more detailed discussion of the systematic errors).

## 3 Implementation of the Pixcap65 chip

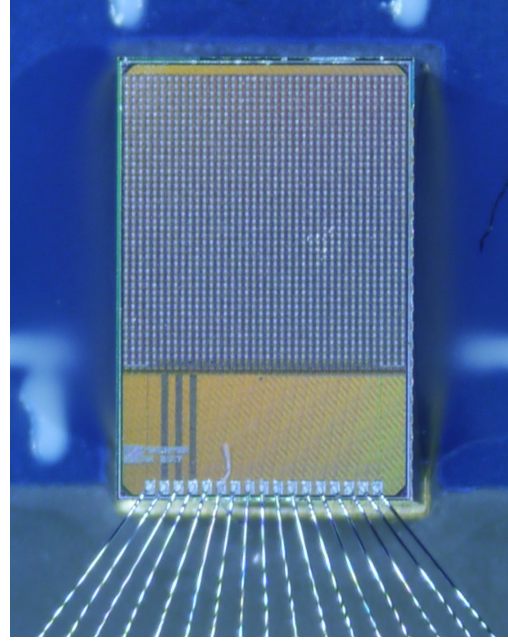
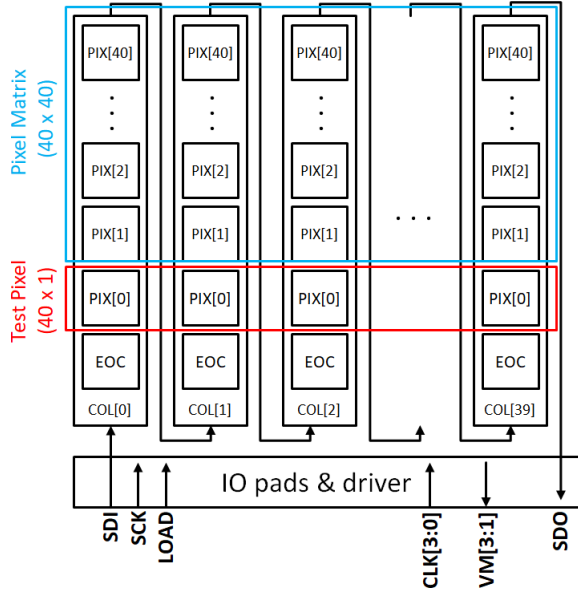
The Pixcap65 chip is an integrated circuit fabricated in a 65 nm CMOS technology. Its concept is similar to a previous chip implementation which was designed to be compatible with sensors with

a pixel size of  $50 \times 250 \mu\text{m}^2$  [8]. The Pixcap65 chip has a  $40 \times 40$  pixel matrix with a  $50 \times 50 \mu\text{m}^2$  pitch. This pitch makes the Pixcap65 chip compatible with planar and 3D sensors which are designed for the hybrid-pixel read-out chips of the HL-LHC upgrades of the ATLAS and CMS experiments at CERN. The pixel cell as shown in figure 3 consists of an array of switches, a control logic, and a bump pad to connect to a sensor pixel. The basic switch configuration to measure the total pixel capacitance only, as shown in figure 2, is realized by a PMOS transistor M3, which charges the capacitance under test via the global voltage line VM3 and an NMOS transistor M0 to discharge the capacitance to ground. The transistors are switched via the global clock lines CLK3 and CLK0 respectively. The Pixcap65 chip has two additional sets of clock lines, voltage lines, and switch transistors (CLK1, VM1, M1, and CLK2, VM2, and M2) which enable more advanced measurements. The pixel control logic, which is programmed via a shift register, configures the connection between clock lines and switches for each pixel. This allows each pixel to either be toggled by a selective connection of the switch transistors to their corresponding clock net or to have a permanent connection to one of the potentials VM3, VM2, VM1 or ground. By choosing an appropriate pixel configuration and clock sequence, not only the total pixel capacitance can be measured but also displacement currents and thus the coupling between pixels can be resolved.



**Figure 3.** Simplified circuit diagram of the Pixcap65 pixel cell. Each pixel has four MOS transistor switches which can be programmed to toggle the potential of the capacitance connected to the bump pad. The voltage levels are defined by the lines VM[3:1] and ground while the toggling sequence is controlled via the clock lines CLK[3:0].

Electrically the pixels are grouped in columns as shown in the chip organization sketch in figure 4. Each pixel column has an end-of-column block (EOC) which controls the connection of the column-level voltage lines to the global voltage lines VM[3:1]. These additional (static) switches reduce loading of the voltage lines with leakage current from pixels in columns that are not active in a current measurement. Apart from the bump-bondable  $40 \times 40$  pixel matrix, the chip has one additional pixel row at the bottom of the matrix. Its cells are connected to internal capacitors of various sizes which can be used for testing the chip without a sensor connected. A few of these extra pixels have an open output which facilitates an extraction of the parasitic capacitance of the bare switch circuit.



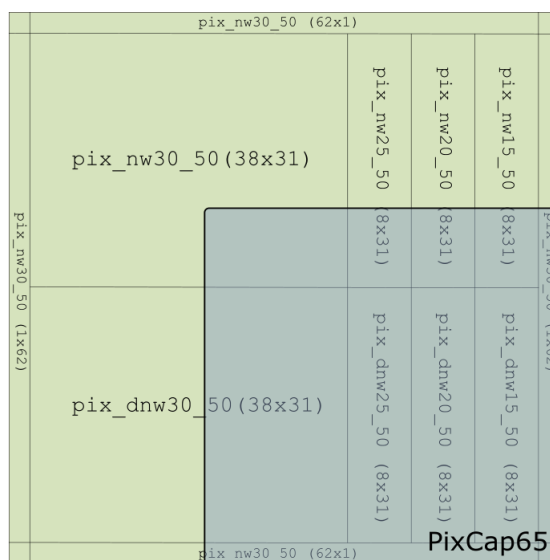
**Figure 4.** Organization of the Pixcap65 chip (left) and photograph of a bare chip mounted on a test PCB (right). The chip has a size of  $2040 \times 3068 \mu\text{m}^2$ . A matrix of  $40 \times 40$  pixels has bump pads to be connected to a sensor. An additional row of pixels without or with unconnected bump pads is located at the bottom of the matrix whose cells are used for testing and calibration. An SPI bus (SDI, SCK, LOAD, and SDO) is used for chip/pixel configuration. Up to four externally generated clock sequences can be transmitted over the global clock lines CLK[3:0] while the voltage lines VM[3:1] connect to external source monitoring units which generate the constant charge and discharge potentials and measure the resulting currents.

#### 4 Design of the test sensor device

To evaluate the performance of the Pixcap65 chip, we used a sensor prototype which was designed with variations in the sensor node geometry and thus varying pixel capacitances. This sensor is a planar  $n^+$ -on- $n$  type and has  $64 \times 64$  pixels with  $50 \times 50 \mu\text{m}^2$  pixel size and a  $p^+$ -implant grid (“p-stop”) for inter-pixels isolation. Two basic parameters of the collection electrodes have variations in the design: the width of the  $n$ -implant and its depth. The aim of this design is to study how much the pixel capacitance can be reduced without affecting the charge collection performance which has been analysed in [7]. Figure 5 shows the simplified cross section of a sensor pixel cell. The  $p$ -implants define the pixel border and provide isolation between neighboring  $n$ -type charge collection nodes. While the distance between these  $p$ -type boundaries, and thus the pixel size, is kept constant the size and the depth of the  $n$ -implant is parameterized: the size of the  $n$ -implant is varied from  $30 \times 30 \mu\text{m}^2$  to  $15 \times 15 \mu\text{m}^2$  in four steps. Also the  $n$ -implant depth has two variants: a standard  $n$ -implant (nw), and a deeper  $n$ -implant using an  $n$ -well extended by a deep  $n$ -well (dnw). All possible eight variants are implemented on the pixels sensor. Since the Pixcap65 chip has  $40 \times 40$  pixels it cannot cover the full sensor area of  $64 \times 64$  pixels. However, the relative placement is chosen such that the Pixcap65 chip is connected to sensor pixels of all eight variants (see figure 6).



This micrograph shows a large, square silicon die mounted on a carrier. The die is connected to the carrier's pads via a grid of gold wire bonds. The carrier has a series of gold pads at the bottom, which are connected to the die's pads via a series of gold wire bonds.



– 6 –



## 5 Measurement results

Measurements have been made with different assembly types: bare Pixcap65 chips with and without solder bumps, and chips assembled with the test sensor described in section 4. Before the measurement results are presented, the main error sources of the measurement will be discussed.

### 5.1 Measurement errors

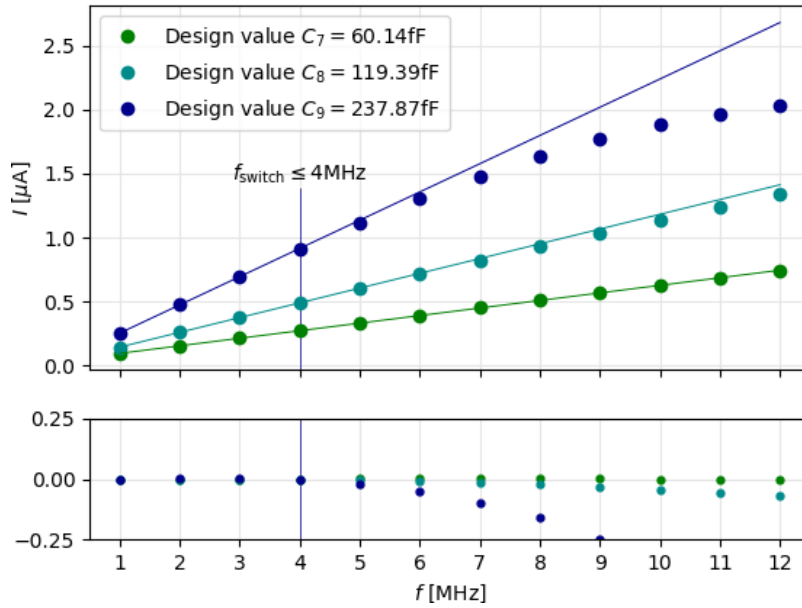
The accuracy of the sensor capacitance measurement is limited by two main contributions: the measurement error of the capacitance measurement and the dispersion of an offset correction. The first contribution depends on the error of the parameters of equation (2.1) (the voltage amplitude of the charge/discharge cycle, the current measurement, and the clock frequency), which define the error of the slope in relation (2.2) and thus the measurement error of the total capacitance (i.e. the sensor capacitance plus the parasitic capacitance of the switch circuit). The second and dominating error contribution (as will be shown below) comes from the offset correction, which is necessary to suppress the parasitic capacitance from the switching circuit and its wiring. Inherent process variations of the CMOS technology lead to a dispersion of this parasitic capacitance, thereby limiting the accuracy of the absolute pixel capacitance measurement.

**Clock frequency.** The clock oscillator which is used as a frequency reference has a precision of 150 ppm. The error on the frequency can therefore be neglected compared to the other sources.

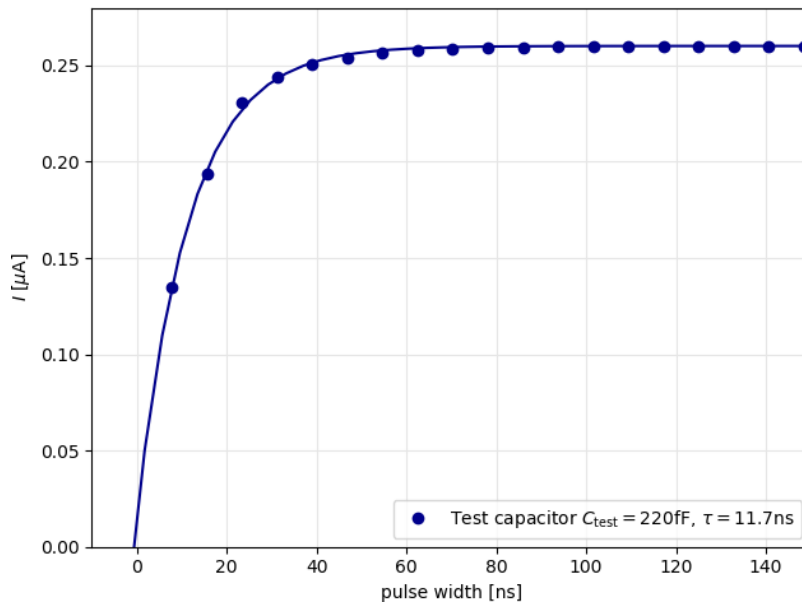
**Current measurement.** The measurement accuracy of the source-measurement-unit (Keithley 2410) is  $0.029\% + 300 \text{ pA}$  at the  $1 \text{ }\mu\text{A}$  range. This error is taken into account for the fit of a linear function to the current values measured as a function of the clock frequency.

**Voltage level.** The error of the voltage output of the source monitoring unit is  $0.02\% + 600 \text{ }\mu\text{V}$  at the  $2 \text{ V}$  output range, which is negligible. More important is the discussion of the systematic error resulting from the finite settling time  $\tau$  given by the on-resistance  $R_{\text{on}}$  of the switches and the total capacitance  $C_{\text{d}}$ . A too high clock frequency (i.e. a too narrow pulse width of the non-overlapping clocks) would reduce the voltage amplitude across the capacitance and thus underestimate the capacitance value (see figure 7). For example, to keep the contribution of the settling error below  $1\%$  ( $0.1\%$ ) the charge and discharge pulse width has to be larger than  $5\tau$  ( $7\tau$ ). To access the value of  $R_{\text{on}}$ , the charge current into one of the large test capacitors ( $C = 220 \text{ fF}$ ) has been measured as a function of the charge and discharge pulse width at a constant switching frequency of  $1 \text{ MHz}$  (figure 8). The resulting curve resembles the resistive charge-up of the capacitor and an exponential fit yields  $\tau = 11.7 \text{ ns}$  and thus  $R_{\text{on}} = 53 \text{ k}\Omega$ . With these numbers the settling error at a maximum switching frequency of  $4 \text{ MHz}$  is below  $1\%$  ( $0.1\%$ ) for capacitance values of up to  $250 \text{ fF}$  ( $170 \text{ fF}$ ).

**Process variations.** The systematic error introduced by the correction of the parasitic capacitance of the switch circuit is more difficult to access. The total capacitance measured with the described method is the sum of the capacitance under test (the sensor pixel capacitance) and the parasitic capacitance of the switch circuit itself. Process variations and finite matching of devices in CMOS processes lead to a dispersion of the circuit parameters that influence the parasitic capacitance. The result is a dispersion of the measurements across a pixel matrix as well as a dispersion of the pixel matrix average from chip to chip. Since the circuit parasitic capacitance can only be accessed with a



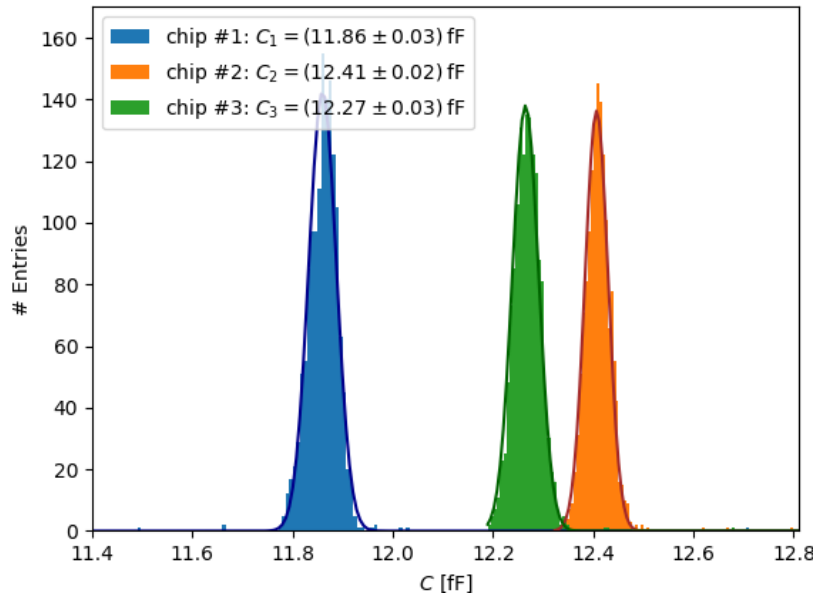
**Figure 7.** Measurement of the displacement current as a function of the clock frequency. For large capacitances and high frequencies the deviation from a linear behavior becomes apparent when charge and discharge times approach the RC time constant given by the on-resistance of the switches and the measured capacitance.



**Figure 8.** Measurement of a large test capacitor (220 fF) at a constant frequency of 1 MHz as a function of the charge and discharge pulse width. The resulting time constant of 11.7 ns yields  $R_{\text{on}} = 53\text{ k}\Omega$ .

Pixcap65 chip without sensor, a sensor measurement from a Pixcap65 chip with sensor suffers from a systematic error given by the dispersion of the parasitic capacitance. While the pixel-to-pixel dispersion within a chip is in the order of 0.05 fF and 0.03 fF for chips with and without bumps, respectively (see figure 9 and 10), the spread of the average from chip to chip is larger. Since only a small number of samples (8 chips in total) was available, we estimated the error due to chip-to-chip dispersion to be about 0.3 fF (see also table 1), which defines the calibration error of the parasitic switch capacitance (offset calibration) for the further sensor measurements.

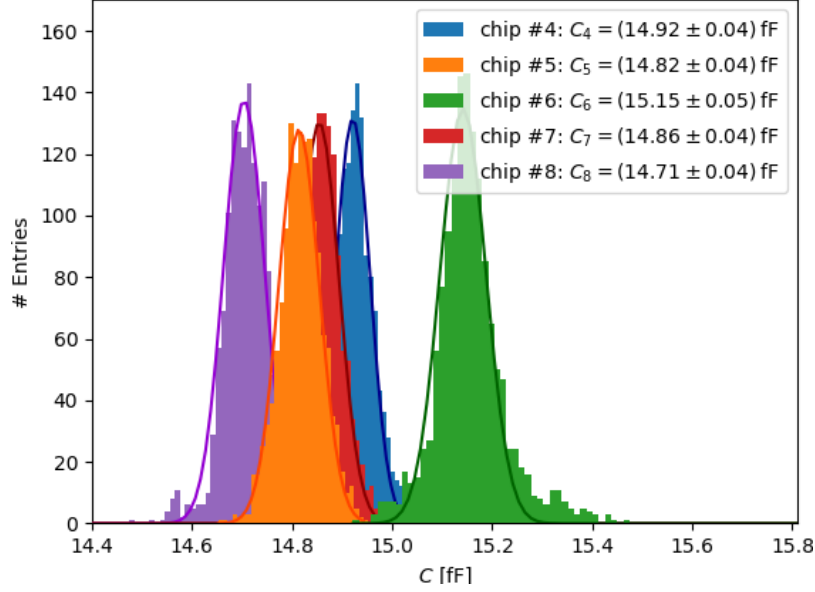
In summary, it can be concluded that the accuracy of the sensor pixel capacitance measurement — comparing all its contributions stated above — is dominated by the inherent process variations of the CMOS technology resulting in an uncertainty of the parasitic capacitance calibration of about  $\pm 0.3$  fF.



**Figure 9.** Distribution of the pixel capacitance of the bare chips without bumps.

## 5.2 Bare chip

Bare chips (with and without solder bumps) have been measured to evaluate the parasitic capacitance of the measurement circuit in the pixel which would overestimate the sensor capacitance in the measurement if not corrected for. This parasitic capacitance of the circuit is mainly caused by the gate-drain capacitance of the switches, the wiring between switches and bump pad, and the bump pad itself. Measurements of the capacitance of bare pixel circuits (without solder bumps) show an average capacitance of  $C_{\text{bare}} = 12.18(29)$  fF (average of all pixels, see figure 9 and table 1). The histogram in figure 10 shows the capacitance distributions of chips with attached solder bumps. The average capacitance of these samples is  $C_{\text{bare+bump}} = 14.89(17)$  fF. This common offset value is used for the correction of all following measurements of sensor assemblies.



**Figure 10.** Distribution of the pixel capacitance of the bare chips with bumps.

**Table 1.** Measured capacitance values of the Pixcap65 samples. The switch and test capacitances are measured for all available samples including four assemblies with sensors.

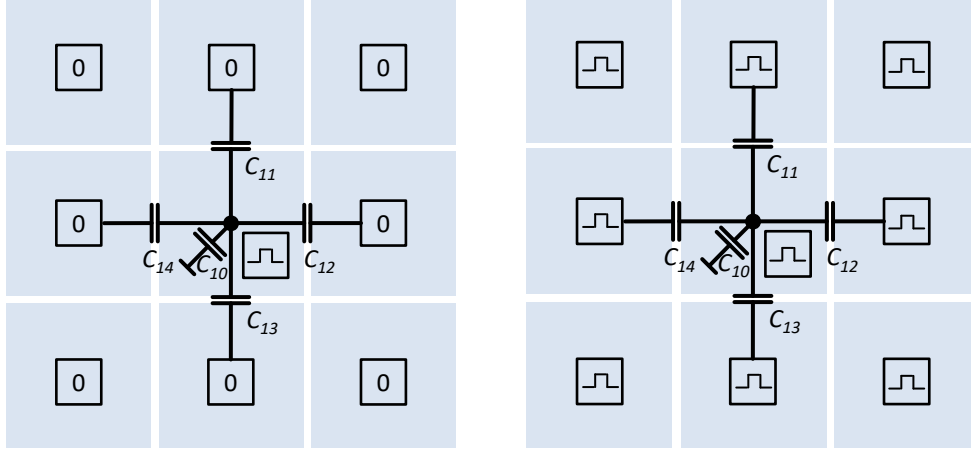
Capacitance type	No. samples	No. cells/sample	$C_{\text{avg}}$ [fF]	$C_{\text{sigma}}$ [%]
Switch only	11	9	4.45(3)	0.66
Switch + test capacitor	11	10	12.58(13)	1.01
Switch + pixel w/o bump	3	1600	12.18(29)	2.34
Switch + pixel w/ bump	5	1600	14.89(17)	1.11

### 5.3 Pixel sensor measurements

Four samples of Pixcap65 chips flip-chipped to the test sensor described in section 4 are used for pixel capacitance measurements. The only difference in the samples is the thickness of the sensor substrate, which is available in 100  $\mu\text{m}$  and 200  $\mu\text{m}$ . The applied bias voltage is  $V_{\text{bias}} = -80$  V to ensure that the sensor volume is fully depleted.

**Total pixel capacitance.** For the measurement of the total pixel capacitance — which is the sum of the contributions from coupling to the neighbor pixels, the backside and the p-stop implant — the matrix is scanned with one pixel toggled and its current measured at a time while all other pixels are held static (connected to ground). The configuration is shown as a simplified sketch in figure 11 on the left.

**Inter-pixel capacitance.** To access the inter-pixel capacitance, the additional switch resources of the pixel circuit (see figure 3) are used to toggle the neighbor pixels with the same timing and amplitude as the active pixel without their current added to the measured current. The configuration is shown in figure 11 on the right. Since this mode cancels the displacement current between the

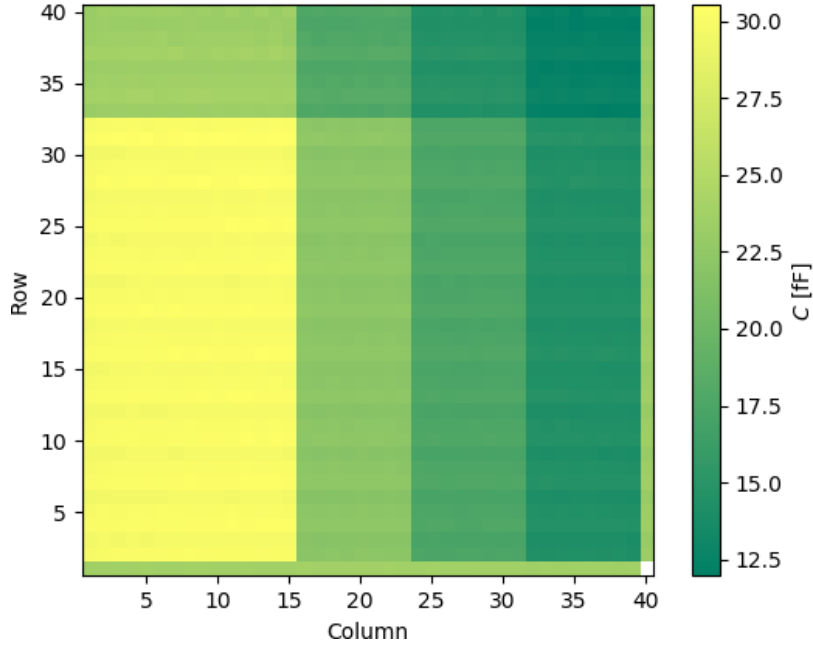


**Figure 11.** Configuration for pixel total capacitance measurement (left) and configuration for suppression of the neighbor pixel capacitance (right). For the total pixel capacitance measurement, the central pixel is toggled and the resulting current measured while all neighboring pixel are connected to ground. In order to suppress the coupling to the neighboring pixels, they are toggled simultaneously with the central pixel. Thus, only  $C_{10}$  contributes to the measured charge current of the central pixel. For better readability, the diagonal coupling capacitances have been omitted.

active pixel and its neighbors, their mutual capacitance ( $C_{11}$ ,  $C_{12}$ ,  $C_{13}$ , and  $C_{14}$ ) is suppressed in the measurement. Thus, the measured capacitance in this mode — summarized as  $C_{10}$  — is the difference of the total capacitance and the sum of the coupling capacitances to the neighboring pixels.

In figure 12 a 2D map of the measured total sensor pixel capacitances of sample 1 is shown. The different implantation areas can be clearly distinguished from each other. The pixel in the lower right corner is connected to a wire bond test pad, which leads to much higher capacitance. For the analysis this pixel was neglected. The sharp transitions indicate that the capacitance is dominated by the coupling between the  $n^+$ -implant of the pixel electrode and the  $p^+$ -implant of the isolation grid. If the pixel-to-pixel capacitance was the dominating contribution, the transitions between the differently implanted areas would be more blurred. The results of the total pixel capacitance and the inter-pixel capacitance measurements are summarized in table 2. The accuracy of the absolute capacitance values (total capacitance) is limited by the process variation discussed in section 5.1 (estimated to be 0.3 fF). The error on the absolute inter-pixel capacitance is much smaller since it is a relative measurement where the error contribution of the parasitic capacitance correction cancels out. The standard deviations in table 2 are calculated from the distribution of four analyzed sensor assemblies.

These measurements reveal that the sensor pixel capacitance increases with the width and depth of the pixel implantation, as expected. For identical implant dimensions, compared to the n-well implantation, the deep n-well flavour has a higher capacitance. No influence is seen due to the different thicknesses (100  $\mu\text{m}$  and 200  $\mu\text{m}$ ) of the four analyzed sensor assemblies. This shows that the contribution of the pixel-to-back-plane capacitance is negligible since the sensor thickness is large compared to the lateral isolation distances between the implantations. We also note that the coupling between neighboring pixel implants is very small. The ratio between  $C_{\text{pix-pix}}$  and  $C_{\text{total}}$  is between 0.016 and 0.026. This implies that the by far dominating contribution to the pixel capacitance comes from the coupling to the p-stop implant. Other sensor types might behave



**Figure 12.** 2D map of the sensor pixel capacitance of sample 1.

**Table 2.** Summary of the measured sensor pixel capacitances of different implantation types of the Pixcap65/test-sensor assemblies. Listed are the total pixel capacitance  $C_{\text{total}}$  and the capacitance between two neighboring pixels  $C_{\text{pix-pix}}$  (mean values from four measured assemblies).

Implant	Columns	Rows	$C_{\text{total}}$ [fF]	$C_{\text{pix-pix}}$ [fF]
nw15_50	32–39	33–40	12.42(15)	0.20(2)
nw20_50	24–31	33–40	14.62(14)	0.26(2)
nw25_50	16–23	33–40	17.84(13)	0.35(2)
nw30_50	1–15	33–40	23.46(13)	0.47(3)
dnw15_50	32–39	2–32	14.39(16)	0.27(2)
dnw20_50	24–31	2–32	17.51(14)	0.38(3)
dnw25_50	16–23	2–32	22.09(13)	0.54(3)
dnw30_50	1–15	2–32	29.98(13)	0.80(3)

differently, depending on the type of inter-pixel isolation, the use of a bias grid (the test sensor has no bias grid) and other layout details.

## 6 Summary

In this paper we describe a pixel chip (Pixcap65) implementing the Charge-Based Capacitance Measurement (CBCM) method to precisely measure the capacitance of a pixel sensor. The chip can be flip-chip mounted to any pixel sensor with  $50\,\mu\text{m} \times 50\,\mu\text{m}$  pitch and facilitates a measurement of the total pixel and inter-pixel capacitances with sub-femtofarad precision using a simple desktop test setup. As a test device, the pixel capacitance of a planar  $\text{n}^+$ -on-n sensor with variations in the implant

geometries was analyzed. It shows pixel capacitance values in the range of 12.42 fF to 29.08 fF. The accuracy of the pixel capacitance measurement is estimated to be 0.3 fF, limited by the dispersion of the parasitic capacitance due to the inherent process variations of the CMOS technology.

## Acknowledgments

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