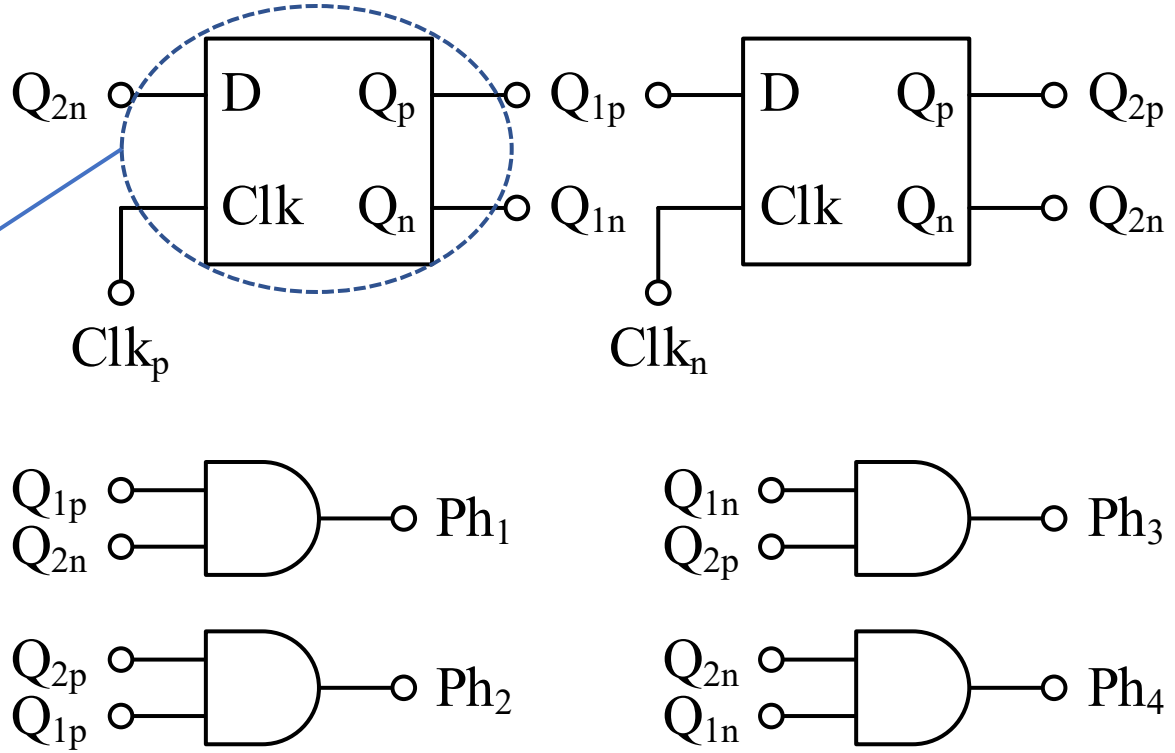
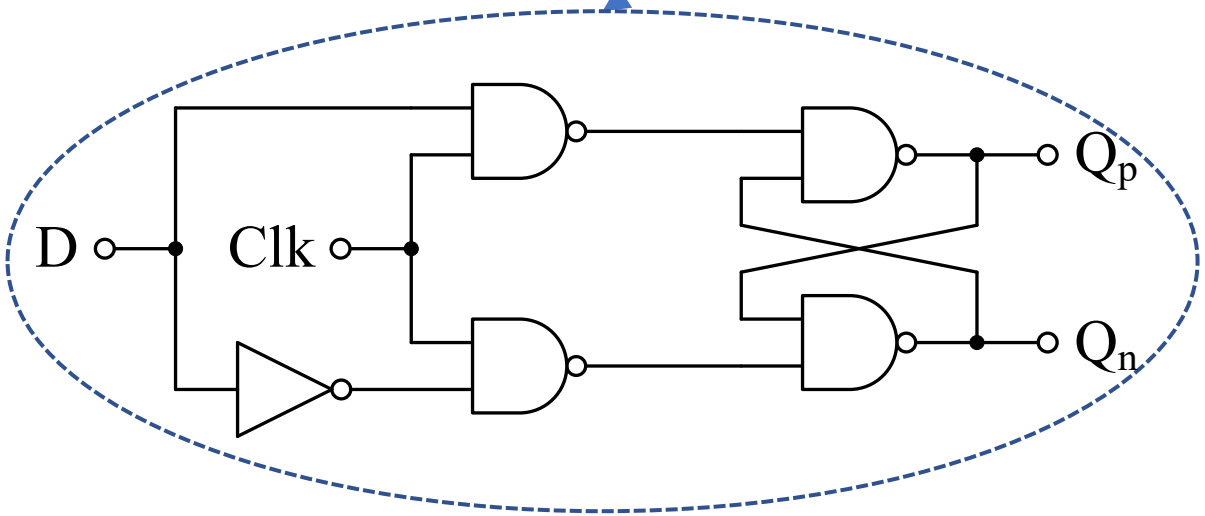
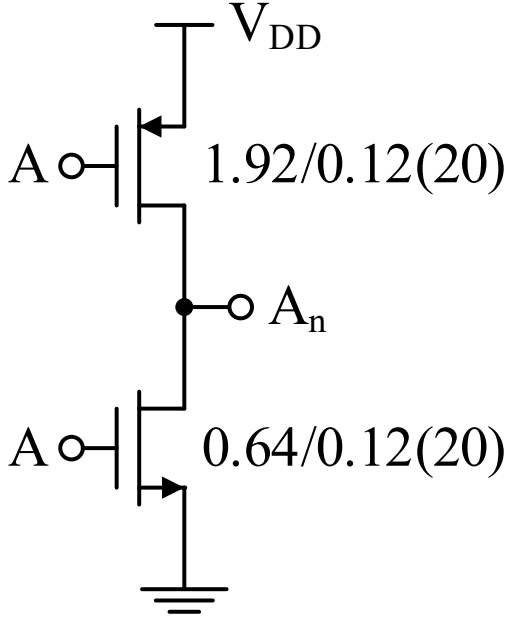
Phase generator

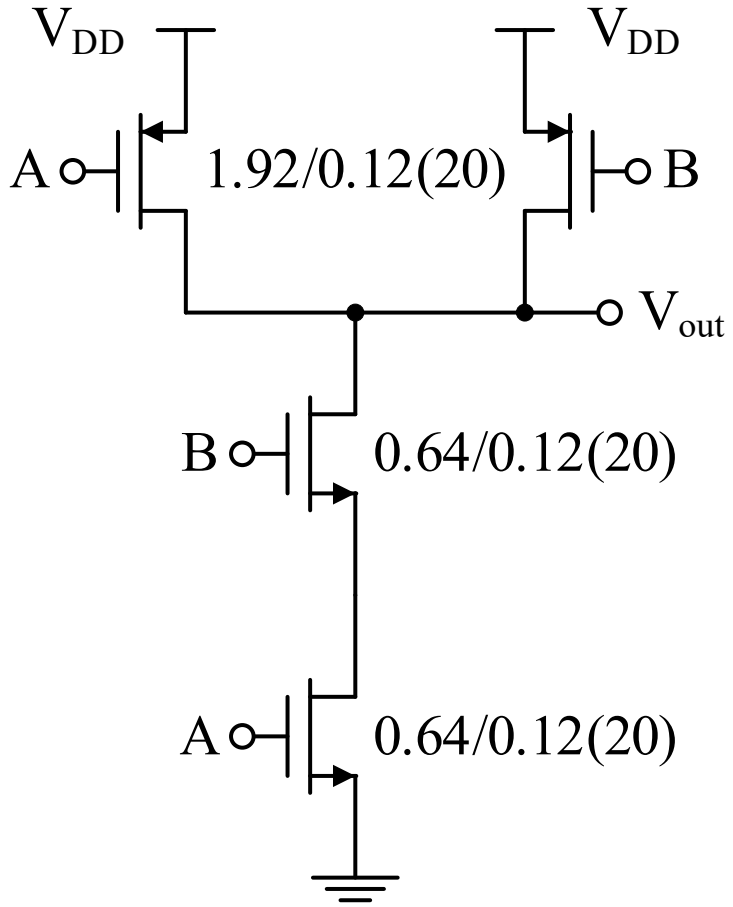
- Signal Clk_p and Clk_n need to have twice the desired frequency (F_{clk}) to obtain four phases with period $1/F_{clk}$



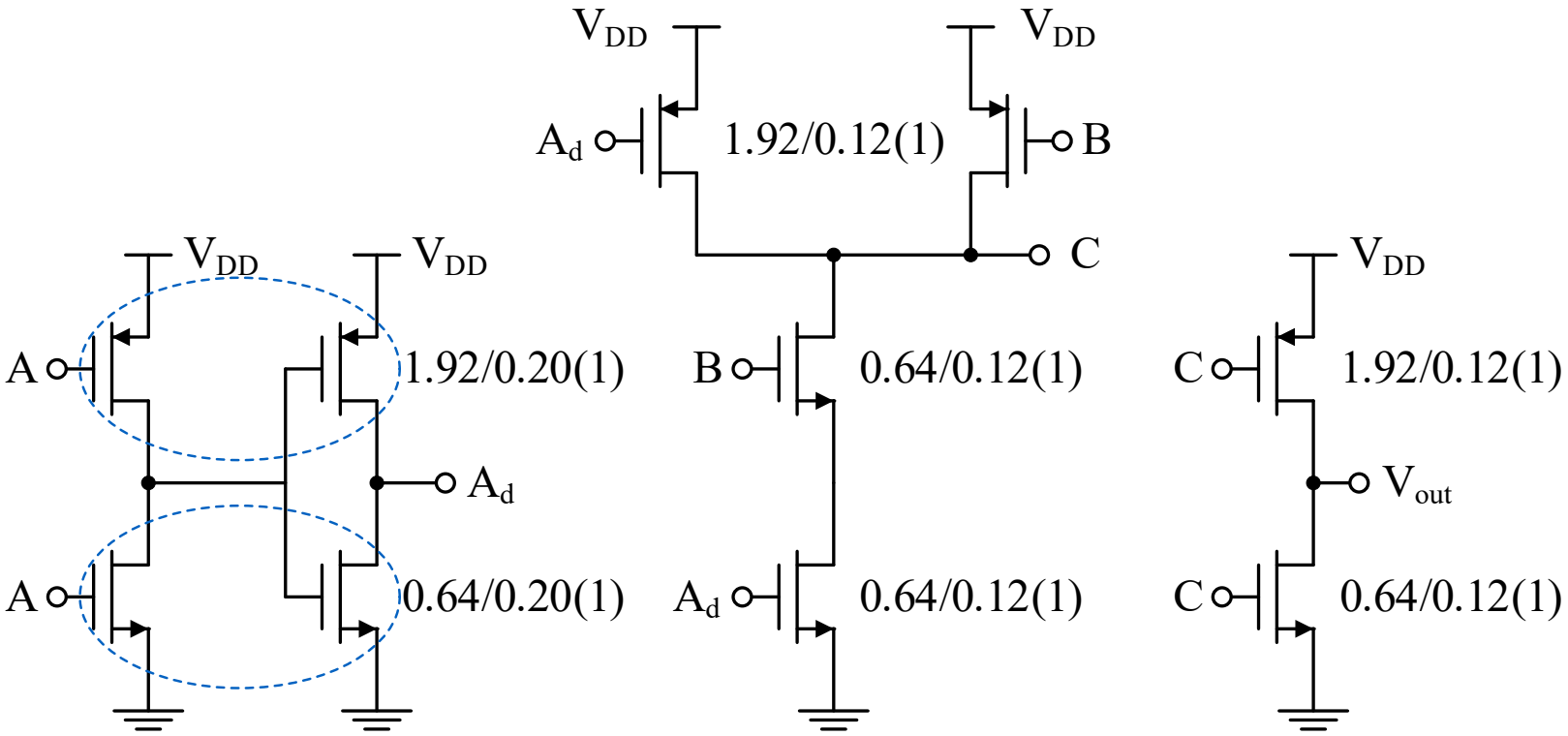




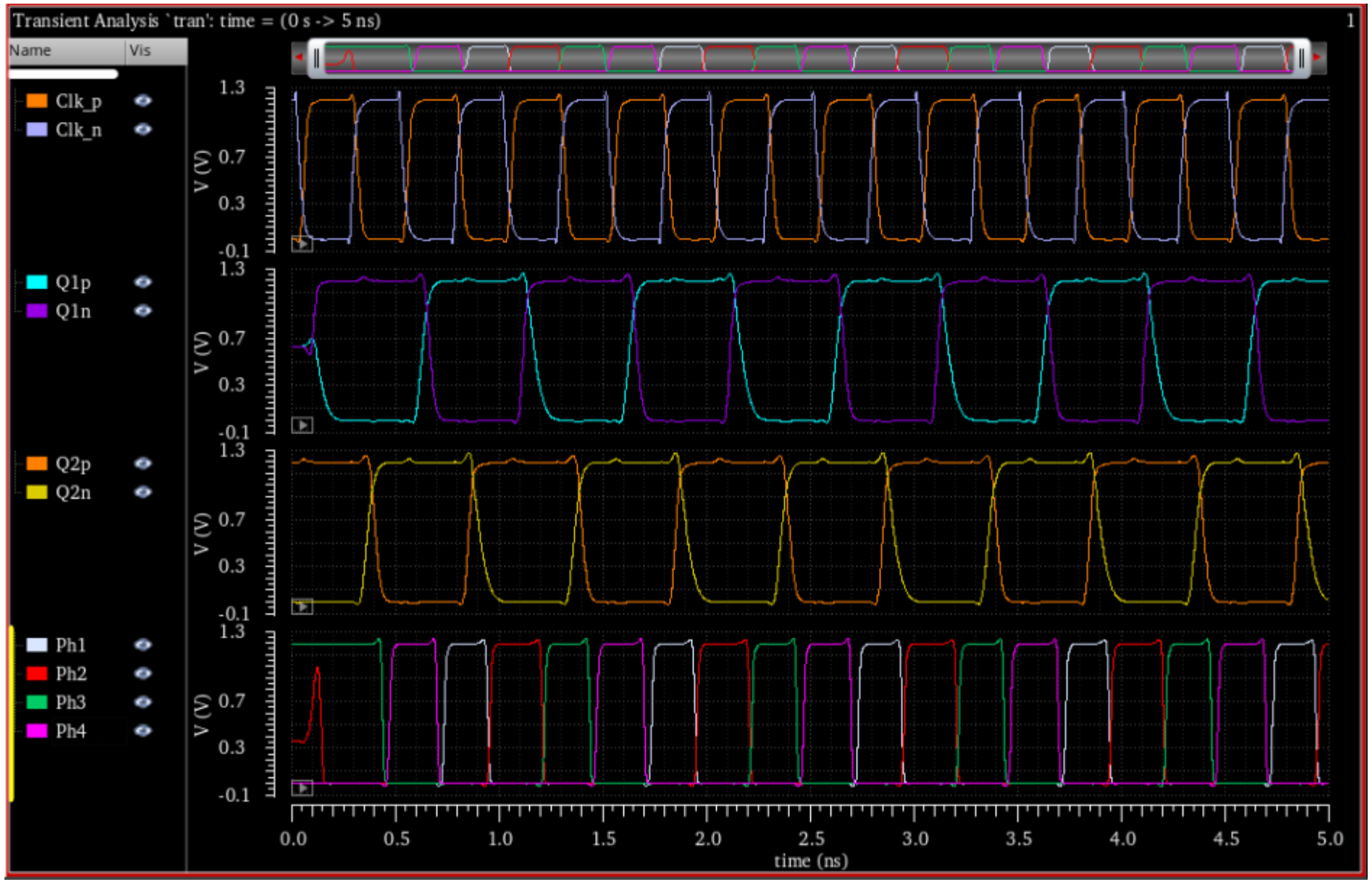
Inverter schematic and design



NAND schematic and design



AND schematic with delayed input A and its design


Transient Analysis `tran': time = (0 s -> 5 ns)
1
Name
Vis
Clk_p
Clk_n
Q1p
Q1n
Q2p
Q2n
Ph1
Ph2
Ph3
Ph4
1.3
0.7
0.3
-0.1
V (V)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
time (ns)