NOVA SCHOOL OF
SCIENCE & TECHNOLOGY

Master's in Electrical and Computer Engineering

Circuitos e Sistemas para Rádio-Frequência

Design of an RF-CMOS front-end for a Low Data Rate SDR.

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1 Introduction

The rapid growth of wireless communication systems and the increasing demand for flexible, low-power and highly integrated devices have driven the development of Software Defined Radio (SDR) architectures. In such systems, a significant portion of the signal processing is performed in the digital domain, which places stringent requirements on the analog front-end in terms of gain, noise, linearity and bandwidth to ensure proper signal digitization.

The radio-frequency front-end (RF Front-End – RFFE) plays a key role in the overall receiver performance, as it is responsible for the initial amplification of the weak signal captured by the antenna, the frequency translation to an intermediate frequency, and the conditioning of the signal to meet the input requirements of the analog-to-digital converter (ADC). In particular, the first active block of the receiver, typically a low-noise amplifier (LNA), has a dominant impact on the overall noise figure, while the subsequent stages largely determine the linearity, interference tolerance and dynamic range of the receiver.

In this project, an RF front-end for a low data-rate SDR receiver operating in the ISM band is studied, designed and simulated using a Low-IF architecture. This receiver topology represents a suitable compromise between the complexity of classical heterodyne receivers and the challenges associated with direct-conversion architectures, allowing the mitigation of DC offsets and low-frequency noise while maintaining a relatively simple and power-efficient implementation.

The adopted architecture consists of a 50 Ω input-matched LNA, followed by two quadrature mixers driven by local oscillator signals with a 90° phase difference, enabling the generation of the in-phase (I) and quadrature (Q) baseband components. After frequency downconversion, the signals are amplified and filtered at intermediate frequency (IF) before being applied to the ADCs, as illustrated in Fig. 1.

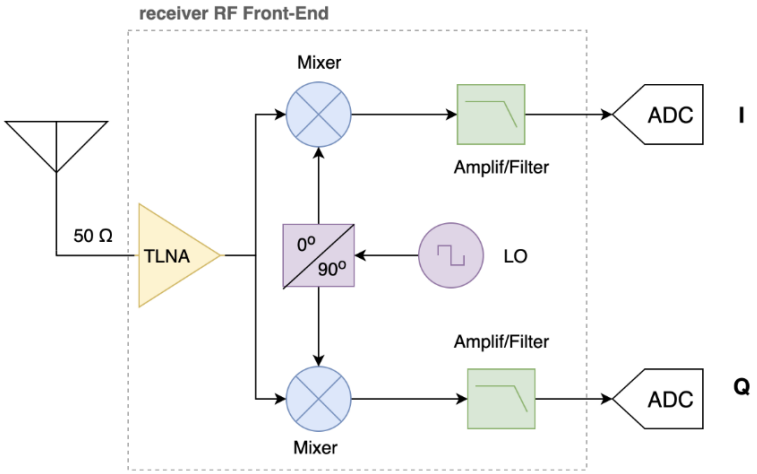

Figure 1: Simplified block diagram of the Low-IF SDR receiver RF front-end with I/Q paths.

The main objective of this work is to properly dimension each building block of the RF front-end in order to meet the system-level specifications, namely total gain, noise figure, linearity metrics (P1dB and IIP3), bandwidth and power consumption. To this end, an analytical design approach is first employed, followed by validation through circuit-level simulations us-

ing Cadence SpectreRF. The obtained simulation results are then compared with theoretical predictions, allowing a critical discussion of the main design trade-offs.

2 System Specifications

The RF front-end is designed according to the system-level requirements defined for a low data-rate SDR receiver operating in the ISM band. These specifications are derived from the application constraints and from the project statement provided in the course. They establish the performance targets that guide the design and dimensioning of each building block of the receiver.

Table 1 summarizes the main system specifications considered throughout this work. These requirements are used as reference values for the analytical calculations and circuit-level simulations presented in the following sections.

Table 1: System-level specifications for the SDR receiver front-end

Parameter	**Specification**
Operating band	ISM (915 MHz)
Receiver architecture	Low-IF
Modulation scheme	FSK / ASK
Data rate	40 kbps
Target BER	10^{-4}
TX EIRP	0 dBm
Maximum coverage range	100 m
Adjacent-channel blocker	-30 dBm @ $f_{\mathrm{IF}} + 300$ kHz
Allowed SNR degradation	≤ 2 dB
Minimum P1dB	> -10 dBm
Minimum IIP3	≥ -14 dBm
ADC input range	1 V_{pp}
ADC resolution	8 bits
ADC sampling frequency	10 MHz
CMOS technology	65 nm
Supply voltage	1.2 V

These specifications impose stringent requirements on the RF front-end, particularly in terms of noise figure, linearity and gain distribution. In the following sections, these constraints are translated into block-level requirements and used to guide the design of the LNA, mixers, IF amplifiers and local oscillator circuitry.

3 LNA Design

The low-noise amplifier (LNA) is the first active block of the receiver RF front-end and therefore has a dominant impact on the overall noise figure and sensitivity of the system. In addition to providing sufficient gain, the LNA must ensure proper impedance matching to the antenna while maintaining adequate linearity.

In this work, a common-source (CS) LNA with inductive source degeneration was adopted. Although a common-gate (CG) topology can also provide inherent input matching, the CS topology offers a more favorable trade-off between noise figure, gain and power consumption at the operating frequency of 915 MHz.

Inductive source degeneration enables simultaneous noise optimization and input impedance matching to 50 Ω without the use of resistive elements at the input. In this configuration, the real part of the input impedance is mainly determined by the transconductance of the input transistor, while the gate inductance is used to resonate out the input capacitance at the center frequency.

The operating region and biasing conditions of the LNA input transistor were carefully selected in order to satisfy the requirements of input matching, noise performance and linearity. For a common-source LNA with inductive source degeneration, the real part of the input impedance can be approximated by $1/g_m$. Therefore, achieving a proper match to a 50 Ω source requires a transconductance on the order of

$$g_m \approx \frac{1}{50\ \Omega} = 20\ \text{mS}.$$

This transconductance level strongly influences the choice of the transistor operating region. Although weak or moderate inversion operation can provide higher transconductance efficiency, strong inversion was selected in this design to ensure sufficient linearity and robustness against large input signals, which is particularly important in the presence of in-band and adjacent-channel interferers.

Once the target transconductance was defined, the bias current was selected accordingly. The input transistor was biased with a drain current of approximately 0.16 mA, resulting in a simulated transconductance close to the required 20 mS. This choice represents a compromise between power consumption and RF performance, while remaining compatible with the overall system specifications.

DC operating point simulations confirm that the input transistor operates in strong inversion and remains in saturation under nominal conditions. The simulated gate-to-source voltage, drain-to-source voltage and drain current provide sufficient voltage headroom to guarantee proper RF operation, avoiding triode-region operation across the expected signal swing. These biasing conditions ensure stable small-signal behavior and consistent large-signal performance.

The operating region and biasing conditions of the LNA input device were selected to meet the input matching, noise and linearity requirements at 915 MHz. For a common-source LNA with inductive source degeneration and a series gate inductor, the input impedance can be approximated by

$$Z_{in} \approx \frac{1}{j\omega C_{gs}} + j\omega(L_g + L_s) + \frac{g_m L_s}{C_{gs}}.$$

This expression shows that the real part is approximately frequency-independent and given by

$$\Re\{Z_{in}\} \approx \frac{g_m L_s}{C_{gs}}.$$

Therefore, imposing a 50 Ω input match at the design frequency leads to the matching condition

$$\frac{g_m L_s}{C_{gs}} \approx 50\ \Omega,$$

while the reactive component is canceled by choosing the total series inductance such that

$$\Im\{Z_{in}\} = 0 \ \Rightarrow\ L_g + L_s \approx \frac{1}{\omega_0^2 C_{gs}},$$

with $\omega_0 = 2\pi \cdot 915$ MHz.

In practice, at 915 MHz and in a 65 nm CMOS process, using an on-chip degeneration inductance on the order of 1 nH is realistic, but the corresponding matching condition depends strongly on the effective C_{gs} and on the ratio $g_m/C_{gs} \approx \omega_T$. For this reason, the input capacitance was shaped not only by the intrinsic transistor capacitances (set by device sizing) but also with an explicit capacitor C_{ex} connected at the input node. This approach effectively lowers the apparent ω_T seen at the input network and allows accurate matching with practical integrated inductor values.

The bias current was selected to obtain the required transconductance while keeping the power consumption low. DC operating point simulations yield a drain current of approximately $I_D \approx 0.16$ mA and a small-signal transconductance around $g_m \approx 20$ mS at the operating point. These values, together with the chosen L_s and the effective input capacitance, lead to an input impedance very close to the target: simulations show $\Re\{Z_{in}\} \approx 50.6\ \Omega$ and $\Im\{Z_{in}\} \approx 0$ at 915 MHz, confirming the validity of the matching design.

The transistor dimensions were implemented in Cadence using a combination of unit width (w_x), number of fingers, and multiplicity factors. In particular, the parameter `k` acts as a parallel multiplier (Cadence `m`-parameter), meaning that it replicates the transistor device `k` times in parallel, scaling the total effective width proportionally. For a device defined with unit width w_x and `fingers` equal to N_f, the effective total gate width becomes

$$W_{\text{tot}} = w_x \cdot N_f \cdot k.$$

This sizing approach is convenient in RF design because it allows sweeping the total width (and therefore g_m and parasitic capacitances) without modifying the unit device geometry, which is beneficial for layout regularity and for controlling gate resistance. In the implemented LNA, the main RF transistor width is therefore defined by `wx0`, `fingers_m0` and the multiplicity factor `k`, while auxiliary devices (cascode and bias transistors) are sized independently to ensure proper biasing and isolation.

[TO DO: INSERT HERE THE COMPLETE ANALYTICAL DIMENSIONING PROCEDURE OF THE LNA, INCLUDING THE DERIVATION OF g_m, DEVICE SIZING, INDUCTOR SELECTION AND NOISE OPTIMIZATION.]

The initial sizing of the LNA was performed using the design parameters summarized in Table 2. These values were provided as a reference starting point for the circuit dimensioning and were subsequently refined through analytical calculations and circuit-level simulations.

Table 2: LNA Design Parameters Used for Initial Dimensioning

Parameter	Value	Description
V_{DD}	1.2 V	Supply voltage
f_0	915 MHz	Target operating frequency
I_b	0.16 mA	Bias current
V_b	0.63 V	Bias voltage
L_g	54.4 nH	Gate inductance
L_s	1 nH	Source degeneration inductance
L_d	3 nH	Drain inductance
C_g	1 mF	Gate coupling capacitor
C_{ex}	0.50 pF	External input capacitance
C_L	10 pF	Load capacitance
w_{x0}	2.2 μm	Input transistor unit width
w_{x1}	2.2 μm	Cascode transistor unit width
w_{x2}	0.85 μm	Bias transistor unit width
$fingers_{m0}$	2	Input transistor fingers
$fingers_{m1}$	2	Cascode transistor fingers
$fingers_{m2}$	2	Bias transistor fingers
k	7	RF transistor multiplicity factor
k_2	1	Bias scaling factor

[TO DO: EXPLAIN HOW THE VALUES IN TABLE 2 WERE DERIVED, INCLUDING THE ROLE OF k AND THE EFFECTIVE TRANSISTOR WIDTH.]

The implemented LNA schematic, including the integrated spiral inductors used for input matching and load, is shown in Fig. 2.

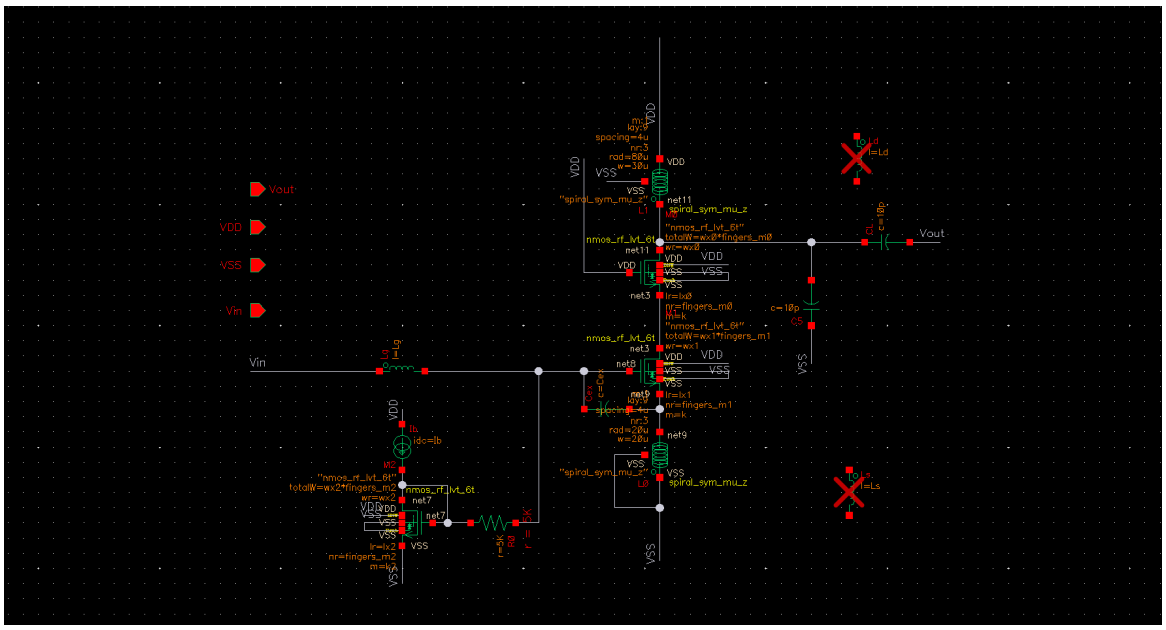

Figure 2: Schematic of the implemented common-source LNA with inductive source degeneration and on-chip spiral inductors.

The input matching and small-signal gain of the LNA were evaluated through S-parameter simulations. Figure 3 shows the simulated S_{11}, S_{21}, S_{12} and S_{22} parameters over frequency. At the operating frequency of 915 MHz, the input reflection coefficient S_{11} exhibits a deep minimum well below the -10 dB criterion, confirming accurate matching to 50 Ω. The forward gain S_{21} reaches approximately 13.3 dB at the same frequency. The reverse isolation S_{12} remains well below -50 dB, while S_{22} indicates acceptable output matching around the operating frequency.

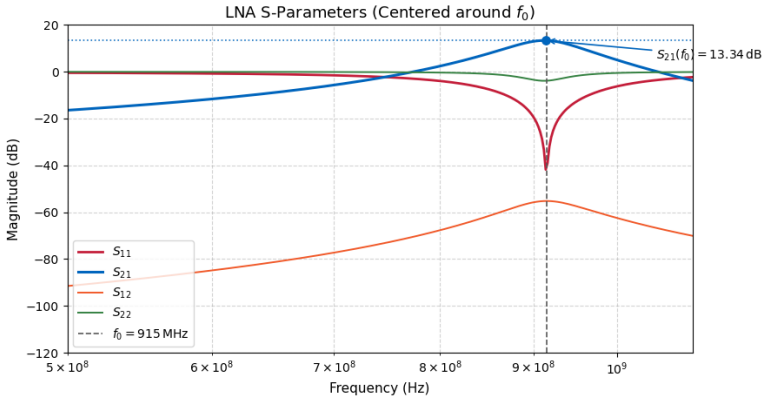

Figure 3: Simulated S-parameters of the LNA: S_{11}, S_{21}, S_{12} and S_{22}.

[TO DO: INSERT HERE THE NOISE FIGURE ANALYSIS AND DISCUSSION, INCLUDING THE CONTRIBUTION OF THE INPUT TRANSISTOR AND THE MATCHING NETWORK.]

The noise performance of the LNA was evaluated using periodic steady-state noise simulations. The resulting noise figure as a function of frequency is shown in Fig. **??**. At the operating frequency of 915 MHz, the simulated noise figure confirms that the LNA provides low-noise amplification, ensuring that the overall receiver noise performance is dominated by the first stage.

[TO DO: INSERT HERE THE ANALYTICAL EXPECTATION FOR THE 1 dB COMPRESSION POINT AND ITS RELATION TO BIAS CURRENT AND DEVICE SIZING.]

The large-signal linearity of the LNA was first evaluated through a swept-input power simulation in order to extract the 1 dB compression point. The corresponding output power characteristic is shown in Fig. **??**.

[TO DO: INSERT HERE THE THEORETICAL BACKGROUND ON THIRD-ORDER NONLINEARITY AND THE EXPECTED IIP3 FOR THE CHOSEN TOPOLOGY.]

Third-order nonlinearity was assessed using a two-tone input test. The intermodulation products and the extraction of the third-order input intercept point (IIP3) are illustrated in Fig. **??**.

[TO DO: INSERT HERE THE DC OPERATING POINT VALUES (VGS, VDS, ID) AND A DISCUSSION ON SATURATION MARGIN.]

The DC operating point of the LNA input transistor was verified through operating point simulations to ensure saturation and sufficient voltage headroom. The relevant bias voltages and currents are summarized in Fig. **??**.

4 OTA Design

This section will detail the operational transconductance amplifier (OTA) used in the receiver chain, covering biasing strategy, transconductance targets, and stability considerations. Content to be developed in the next iteration.

5 TIA Design

This section will present the transimpedance amplifier (TIA) that interfaces the mixer output with the subsequent filtering and conversion stages, including gain setting and noise analysis. Content to be developed in the next iteration.

6 Mixer Design

This section will describe the quadrature mixer architecture, LO drive requirements, conversion gain, and linearity considerations. Content to be developed in the next iteration.

7 Local Oscillator (LO)

This section will cover the local oscillator generation and quadrature phase splitting, addressing phase noise, startup margin, and buffering strategy. Content to be developed in the next iteration.

8 Low-Pass Filter

This section will explain the IF/baseband low-pass filter design, including pole placement, linearity trade-offs, and integration with the OTA/TIA stages. Content to be developed in the next iteration.

9 Conclusions

This section will summarize the RF front-end design outcomes, highlight key trade-offs, and outline future improvements. Content to be developed in the next iteration.

[?]

References