Circuits and Systems for Radio Frequency

Two-stage amplifier with Miller compensation

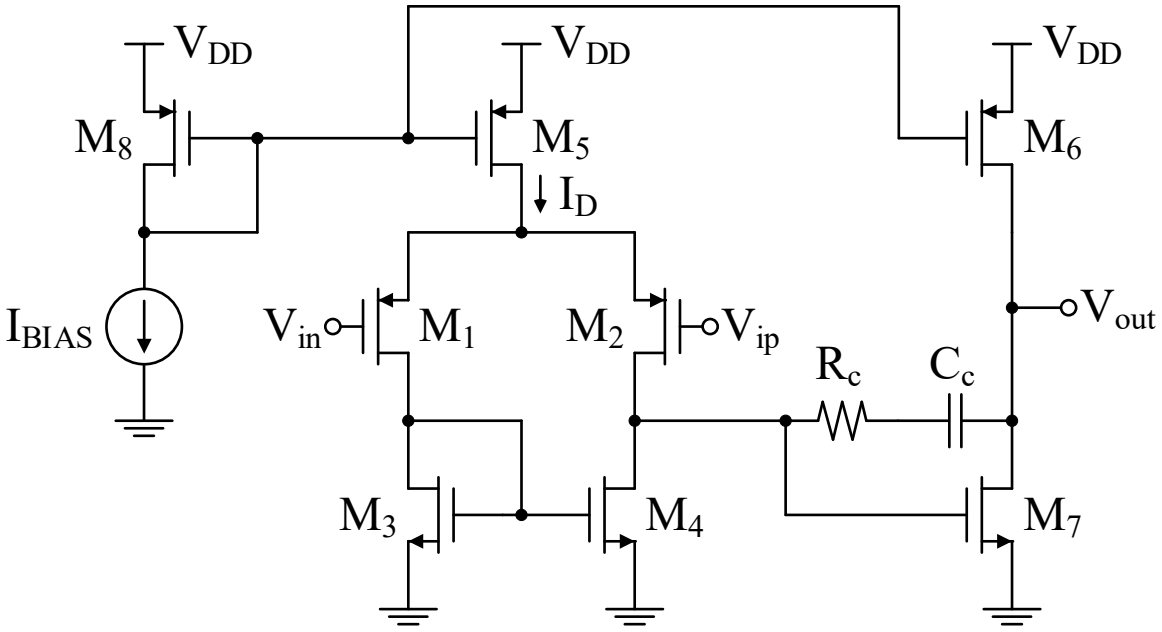
2025/2026

Two-stage amplifier with Miller compensation

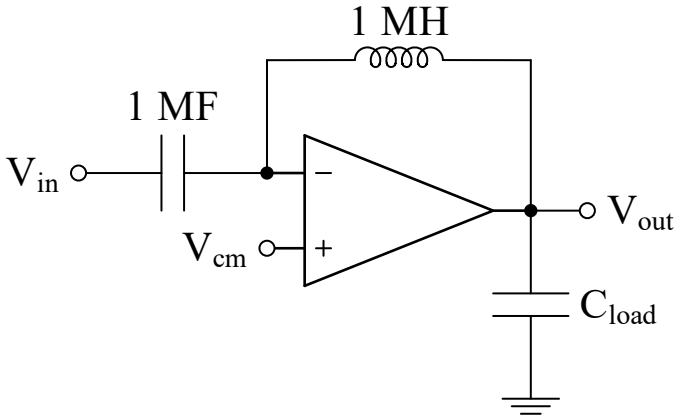
Read more about this circuit in the following book: Analog Integrated Circuit Design, T.C. Carusone

Design:

- nch_lvt
- V_{DD} = 1.2 V and V_{cm} = 0.6 V



Two-stage amplifier circuit

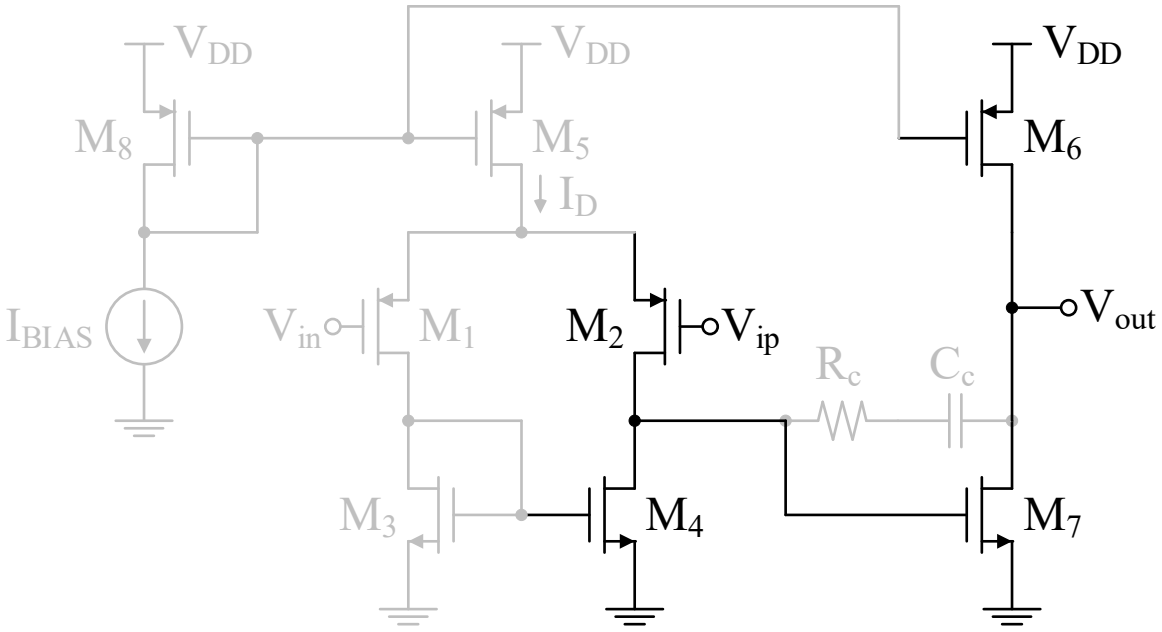


Testbench circuit to simulate amplifier

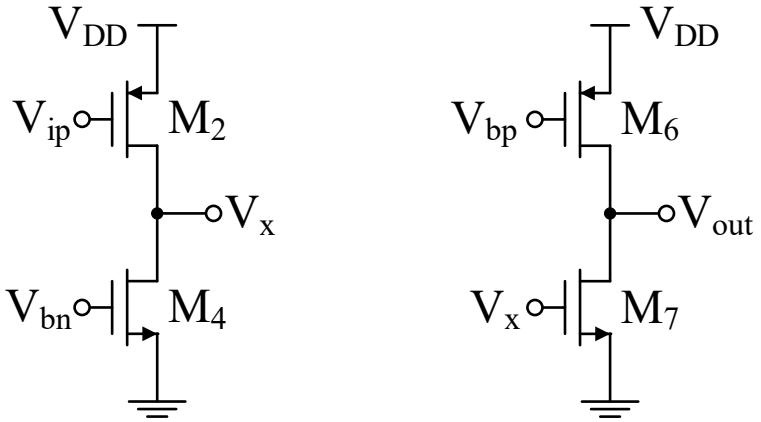
Two-stage amplifier with Miller compensation

For simplicity purposes only half of the circuit is analysed:

- Bias circuit is neglected since it does not affect AC
- Feedback elements (R_C and C_C) are also neglected



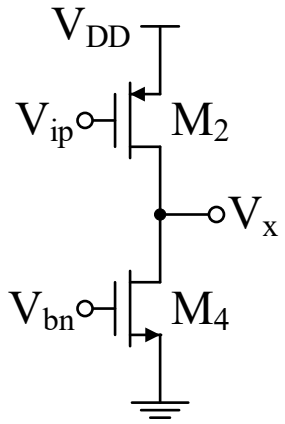
Half circuit

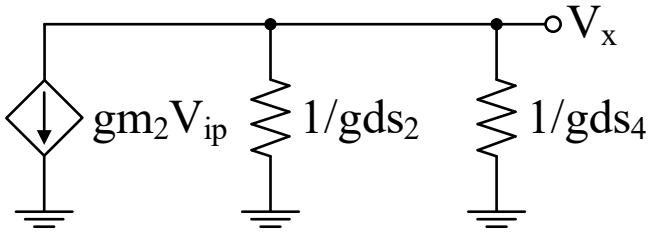


Circuits to be analysed

Two-stage amplifier with Miller compensation

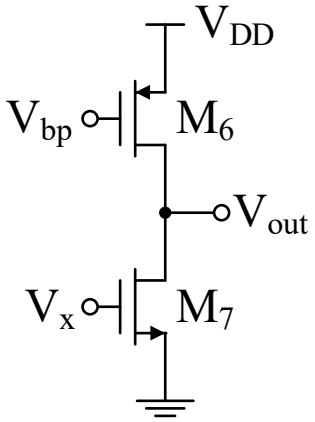
1st Stage:

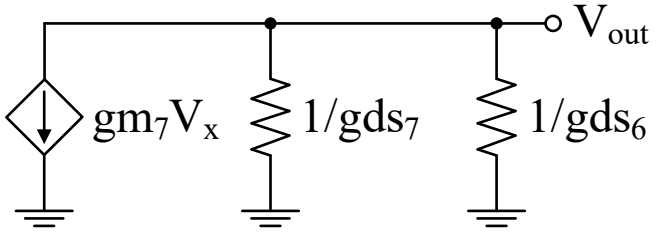




$$A_{v1} = \frac{V_x}{V_{ip}} = -\frac{gm_2}{gds_2 + gds_4}$$

2nd Stage:





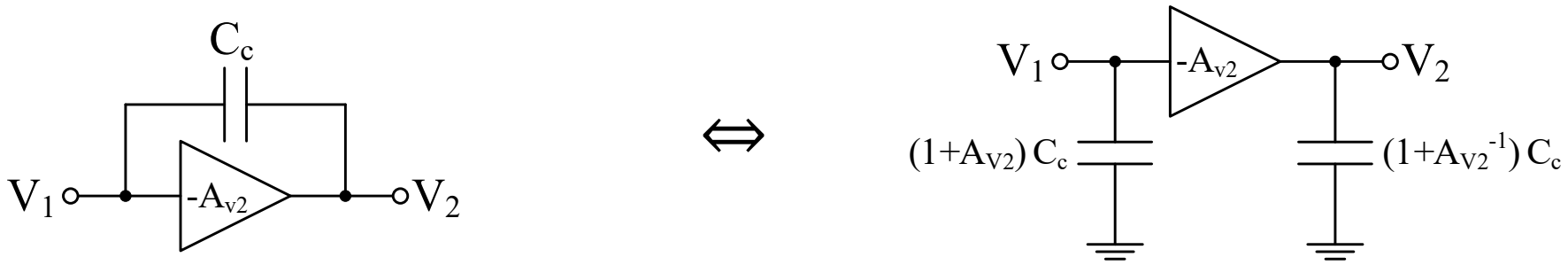
$$A_{v2} = \frac{V_{out}}{V_x} = -\frac{gm_7}{gds_6 + gds_7}$$

$$A_v = A_{v1}A_{v2} = \frac{gm_2 gm_7}{(gds_2 + gds_4) + (gds_6 + gds_7)}$$

$$gm = \frac{2\,I_D}{V_{GS} - V_T} = \sqrt{2\,\mu_n C_{ox}\left(\frac{W}{L}\right) I_D}$$

$$gds = \lambda \times I_D = \frac{I_D}{const \times L}$$

Miller Theorem

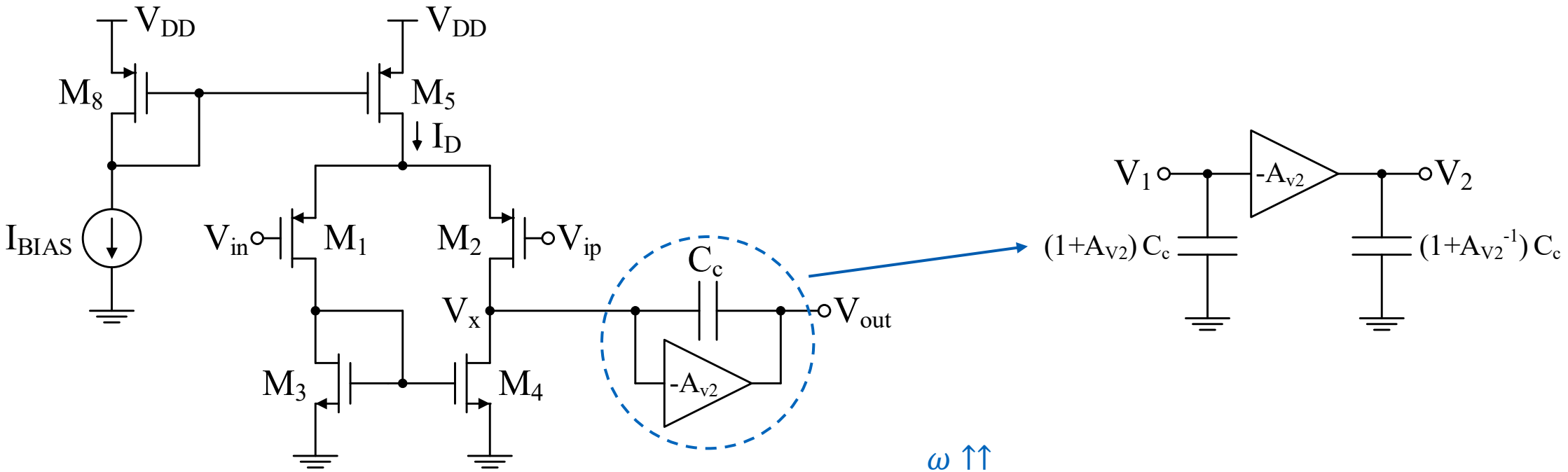


Simplified second stage **Equivalent circuit**

$$i_{C_c} = C_c \times \frac{dv}{dt} = j\omega(V_1 - V_2)C_c$$

$$\begin{cases} i_{C_c} = j\omega(V_1 - (-A_{v2})V_1)C_c \Rightarrow \dfrac{i_{C_c}}{V_1} = j\omega(1 + A_{v2})C_c \Rightarrow Z_{in} = \dfrac{1}{j\omega(1 + A_{v2})C_c} \\ i_{C_c} = j\omega\left(-\dfrac{V_2}{A_{v2}} - V_2\right)C_c \Rightarrow \dfrac{i_{C_c}}{V_2} = j\omega\left(1 + \dfrac{1}{A_{v2}}\right)C_c \Rightarrow Z_{out} = \dfrac{1}{j\omega(1 + A_{v2}^{-1})C_c} \end{cases}$$

Two-stage amplifier with Miller compensation



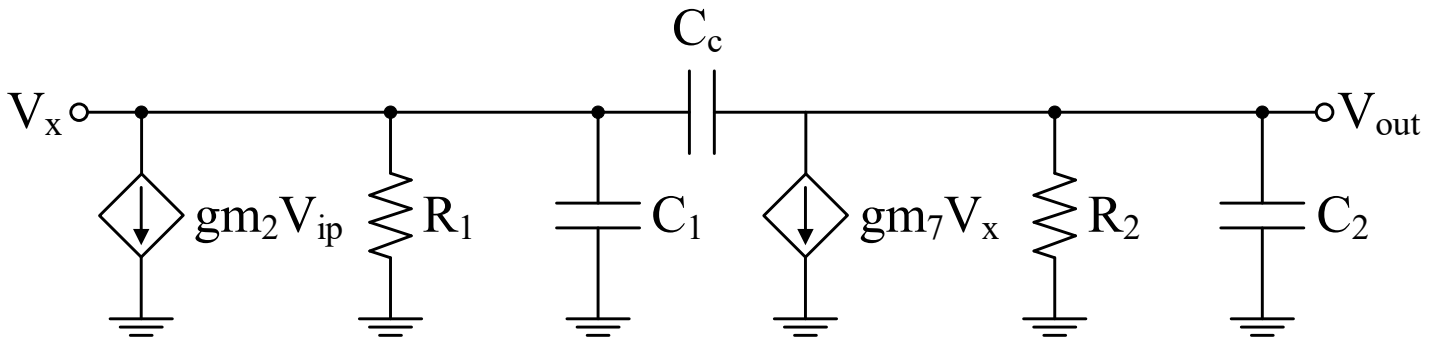
$$A_{v1}(s) = \frac{V_x}{V_{in}} = -gm_2\, Z_{out} \approx -gm_2 \left(\frac{1}{gds_2} // \frac{1}{gds_4} // \frac{1}{sC_c A_{v2}} \right) \approx \frac{gm_2}{sC_c A_{v2}}$$

$\omega \uparrow\uparrow$

$$A_v(s) = A_{v1}A_{v2} \approx \frac{gm_2}{sC_c A_{v2}} A_{v2} = \frac{gm_2}{sC_c}$$

$$1 = \frac{gm_2}{sC_c} \Rightarrow GBW\,[Hz] = \frac{gm_2}{2\pi\, C_c}$$

Two-stage amplifier with Miller compensation



$$A_v(s) = \frac{gm_2 R_1 R_2 \left(1 - \frac{s\,C_C}{gm_7}\right)}{1 + \left((C_1 + C_C)R_1 + (C_2 + C_C)R_2 + gm_7 C_C R_1 R_2\right)s + \left(R_1 R_2 (C_1 C_2 + C_1 C_C + C_2 C_C)\right)s^2}$$

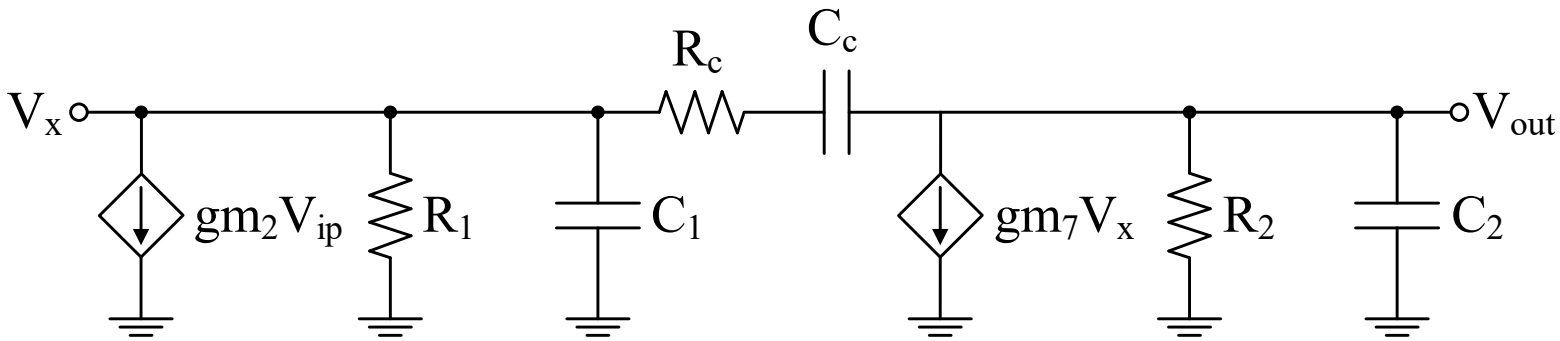
$$D(s) = \left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right) = 1 + \frac{s}{\omega_{p1}} + \frac{s}{\omega_{p2}} + \frac{s^2}{\omega_{p1}\omega_{p2}} \approx 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1}\omega_{p2}}$$

$$\omega_{p1} = \frac{1}{(C_1 + C_C)R_1 + (C_2 + C_C)R_2 + gm_7 C_C R_1 R_2} \approx \frac{1}{gm_7 C_C R_1 R_2},$$

$$\omega_{p2} = \frac{gm_7 C_C}{C_1 C_2 + C_1 C_C + C_2 C_C} \approx \frac{gm_7 C_C}{C_1 C_C + C_2 C_C} = \frac{gm_7}{C_1 + C_2}$$

$$\omega_z = -\frac{gm_7}{C_C}$$

Two-stage amplifier with Miller compensation

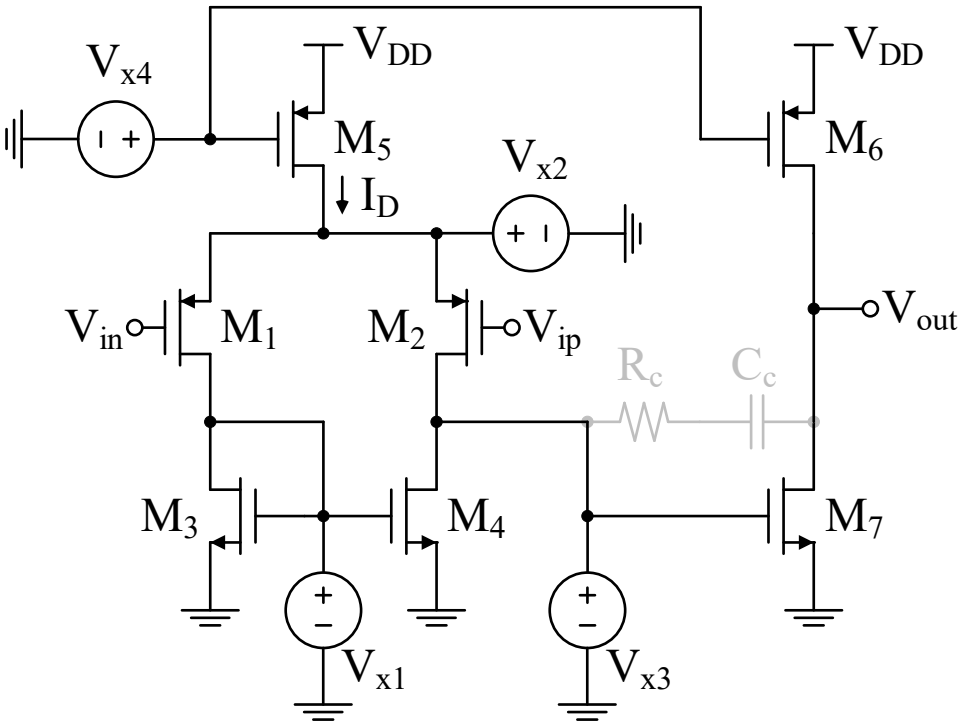


$$\omega_z = -\frac{1}{C_C\left(\frac{1}{gm_7} - R_C\right)}$$

Two-stage amplifier (Design through simulation)

- Define desired input and output common-mode voltages (V_{ip_vcm}, V_{in_vcm}, V_{out_vcm})
- To maximize gain, $V_{dsat1,2}$ need to be small to increase *gm* (i.e., $V_{dsat} \approx 50 - 75$ mV)
- Considering that V_{dsat} is related with $V_{GS} - V_T$ and $V_T \approx 300$ mV, then $V_{GS} \approx V_T + V_{dsat}$
- For transistors operating as current sources consider a V_{dsat} of $\approx 100 - 150$ mV
- Set the length of the transistors (use, at least, 3 times L_{min} to avoid pronounced short-channel effect)
- If V_T is high (e.g., > 300 mV) increase the length further, if moderate inversion is desired

- **<u>Example</u>:**
  - $V_{ip\_vcm} = V_{in\_vcm} = V_{out\_vcm} = 600$ mV $= V_{DD}/2$
  - $V_{x1} = V_{GS3,4} = V_T + 150$ mV $= 450$ mV
  - $V_{x2} = V_{ip\_vcm} + V_{GS1,2} = 950$ mV
  - $V_{X3} = V_{GS7} = V_T + 50$ mV $= 450$ mV
  - $V_{X4} = V_{GS5} = V_{DD} - V_T - 150$ mV $= 750$ mV



Two-stage amplifier (Design through simulation)

- Once the voltages are set, perform a DC simulation and check the transistors current
- Increase transistors width to achieve the desired current in each transistor (Ex. I_D = 100 µA)
- Once the desired currents are obtained remove/disable the auxiliary DC sources (V_{x1}, V_{x2}, V_{x3}), V_{x4} can stay if the bias network is not designed yet
- Perform an AC simulation and check the amplifier's DC gain and phase margin (amplifier will be unstable)
- Add C_c, remember that it needs to be larger than the parasitic capacitances (Ex. 1.5 pF).
- Add R_c, remember that R_c must be larger than $1/gm_7$ to move the zero to the left plane
- Can perform a sweep simulation varying R_c to find the point of maximum phase margin (> 60º)
- When designing the bias network, use a maximum mirroring factor of 10
- Scale bias current and the width of ALL transistors (multiplier) by an integer until desired GBW is obtained