NOVA NOVA SCHOOL OF SCIENCE & TECHNOLOGY

# Project

**Circuits and Systems for Radio-Frequency**

## Design of an RF-CMOS front-end for a Low Data Rate SDR

October 2025
Version 1.0

# 1- Introduction

Starting from the reference architecture associated with Software Defined Radio (SDR), the project has the objective to study, design and simulate a complete RF front-end (RFFE), depicted in Fig. 1, using a 65nm CMOS technology.

The design of the complete receiver is a complex task that should start by gathering all the required specifications ranging from application/system level up to electronic components and circuits.
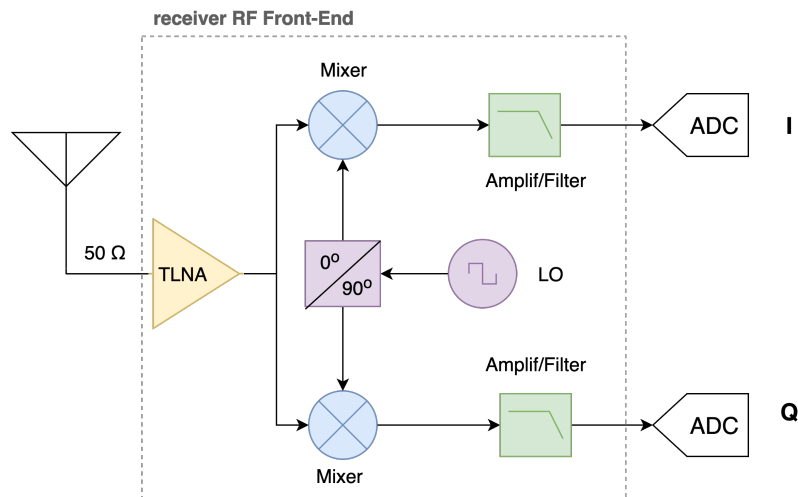


Figure 1- Simplified block diagram of a Receiver RF Front-End for a SDR.

Based on the collected specifications, the next step of the design is to select the architecture and topology. The requirements for each building block of the RF Front-End are determined to allow the sizing of each circuit, which should be selected previously.

The project of the RFFE involves the design of several building blocks, namely:

- **Low-noise amplifier**: the inductive degenerated common source topology can achieve very low noise figures;
- **Mixer**: use a current-driven passive mixer;
- **Low-IF low-pass filter**
- **Low-IF amplifier**
- **I/Q Local Oscillator (LO)**, including output drivers

## 2- Specifications / design requirements and constraints

- TX EIRP: 0 dBm
- Coverage range (distance): up to 100 m
- Modulation: FSK/ASK, 40kbps and BER=10e-4
- ISM band: 868MHz or 915MHz.
- Narrowband approach.
- Low-IF architecture
- P1dB > -10 dBm
- IIP3 >= -14 dBm
- Blocker spec (adjacent-channel): The receiver must tolerate a single-tone blocker at $f_{IF}$ + 300 kHz with –30 dBm at the antenna, when the wanted signal is at $P_{min}$ + 6 dB; SNR degradation ≤ 2 dB and no ADC clipping.
- ADC specs: input full scale range 1Vpp, 8 bits, sampling frequency of 10 MHz
- Technology: CMOS 65 nm
- VDD = from 0.7 to 1.2 V
- Inductors, resistors, and capacitors from the 65 nm design kit
  - Consider an approximate model of the on-chip inductor with parasitic capacitances; CP of 10 fF; also, consider an on-chip inductor quality factor of 7. You can fine-tune these values by checking the 65 nm design kit;
  - Due to area constraints, limit the total inductance;
  - On-chip capacitor with a bottom-plate parasitic capacitance of 4%.

If one or more specifications cannot be fully achieved during the design/simulation, provide a technical explanation and propose an updated value based on your analysis/results.

## 3- Design and Validation

### 65 nm CMOS technology Design and simulation process

The design process should include the determination of the circuit equations (or design tables) from which the device sizes are calculated (e.g., W, L, capacitance, inductance, resistance). The operation and performance achieved by the designed circuits should be confirmed through SpectreRF (Cadence) simulation using BSIM V4 transistor models. Also, the transistors that must process RF signals should be the ones with RF transistor layout (check 65nm component library).

The SpectreRF simulator from Cadence design framework includes the Periodic Steady State (PSS) analysis which is capable to simulate efficiently time-variants circuits. It is expected that the following simulation be performed:
- Distortion, non-linear
- noise simulation (e.g., through PNOISE option)
- PVT simulation for one or more building blocks.

Create a set of "testbenches" to simulate the behavior of your design under various conditions and input stimuli. A test bench serves as an environment or simulation setup in which you can verify the functionality and performance of your electronic designs.

The final report should address the analysis, design and the simulation of the RF Front-End. As a general indication, the report should include, clearly:

- Specifications and requirements for each building block, namely, in terms of Noise, Linearity, Sensitivity, Power consumption, and estimated chip area, among others;
- Theoretical analysis of the system and building blocks, including noise analysis, linearity analysis (1dB compression point, IIP3)
- If applicable, high-level simulations (Octave, scilab, Python, etc);
- Electrical simulations using realistic models of the components;
- Include a comparative analysis between theoretical and simulation results. Achievable specs.
- As general requirement, include one PVT simulation for one or more building blocks.

Besides the general indications given above, the following list of topics/information should be considered

## For the LNA

- Type of topology: A Common source (CS) is suggested but a common gate (CG) can also be chosen
- Region of operation of the transconductor: Weak, moderate or Strong Inversion
- Type of input: single ended or differential
- Type of output:
    o single ended or differential
    o voltage or current mode
- Noise figure
- Gain (which type is relevant when connected to the following mixer?)
    o Input matching: 50 Ω? Level of S11 (level of matching)
- Power consumption
- 1 dB compression point
- Linearity: IIP3
- Estimated area

## For Mixer (including the TIA)

- Type of topology/operation:
    o Passive: current-mode; (preferentially)
    o (if adequately justified, an active mixer can be selected)
- Conversion Gain;
- Linearity: IIP3;
- Noise analysis;
- For the TIA: Incorporate a first-order filter
- A clear indication should be given for the requirements of the buffers driving the mixer switches;
- Power consumption;
- Estimated area.

4

## For Local Oscillator

- Design the oscillator. Ring oscillator
- Design the output drivers
- Estimated area

## For IF amplifiers, filters, …

- Gain
- Bandwidth;
- Linearity analysis
- Noise analysis
- Gain programmability (optional);
- Operation region of the transistors: Weak, Moderate or Strong Inversion;
- Power consumption and estimated area;
- This stage can be implemented as a cascade structure;

## For the full front-end receiver

The full RF front-end should be simulated as a complete and unique system block (use an ideal LO when using PSS):

- Gain of the full RF front-end;
- Total noise figure and verify if it is compliant with the initial requirements;
- 1 dB compression point, P1dB;
- Linearity: IIP3;
- Verify Blocker effects;
- Total power consumption;
- Use an adequate input signal type and dynamic range to test the complete RF front-end.

The list items are a set of results that should be included in the report. However, additional characterization and analysis will be positively graded and strongly recommended.

# 4- LNA Layout (optional)

Proceed with the layout of the LNA, including real inductors available from the process design kit (PDK).

# 5- Evaluation

The complete RF Front-End should be analyzed, designed and simulated. The final technical report must not exceed **20 pages**, including figures, tables, and references. Appendices may contain raw simulation data, extended schematics, extended scripts code. The report should be delivered by the end of the semester (check dates on moodle). The project evaluation includes:

- Final report, calculation files (octave, excel, python, etc.) and design database
- Q&A session (individually)

## Classification options:

**Option A**: Up to 17.5: most of the receiver building blocks using a single-ended version

**Option B**: Up to 20: (fully) differential version of the receiver and (draft) LNA layout. Optimized for power consumption.